A/D module for injectors BPM systems

BI Technical board

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M.Bozzolan, O.Marqversen, A.Boccardi

Scope of the project

Consolidate and harmonize the DAQ of the following BPM systems

System	Type	DAQ rate [Msps]	ADC n. of bits	Responsible
L4 & PSB inj	TL	88	16	M.Bozzolan
LEIR injection	TL	100	12	M.Bozzolan
LEIR extraction	TL	100	12	M.Bozzolan
PSB extraction	TL	250	12	M.Bozzolan
PSB trajectory	Ring	125	14	M.Bozzolan
PS trajectory	Ring	125	14	M.Bozzolan
LEIR trajectory	Ring	125	16	O.Marqversen
AD trajectory	Ring	125	16	O.Marqversen
ELENA trajectory	Ring	125	16	O.Marqversen

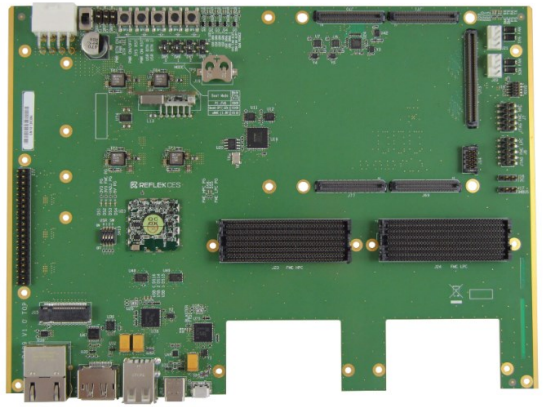
- ~ 250 pickups (~450 planes)
- 50Hz … 352MHz frequency range

250Msps/16bit/400MHz BW is a superset of the needs for all the systems

Possible (future) acquisition system

SoM based on Zynq Ultrascale SoC

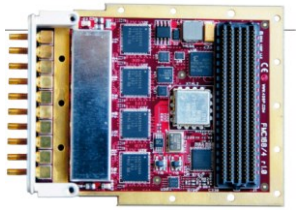
carrier board for SoM



The future DAQ board will be roughly two times the space of the current DAQs

We may acquire 4 pickups → 16 analog inputs per DAQ

2x 8 input



With standard mezzanine format 8 inputs needed (there is no space for 4 mezzanines)

With 8 inputs connectors are small and tight

Is “ADCs on the carrier” a better solution?

- **Disclaimer:** Images are commercial products for illustration purposes only

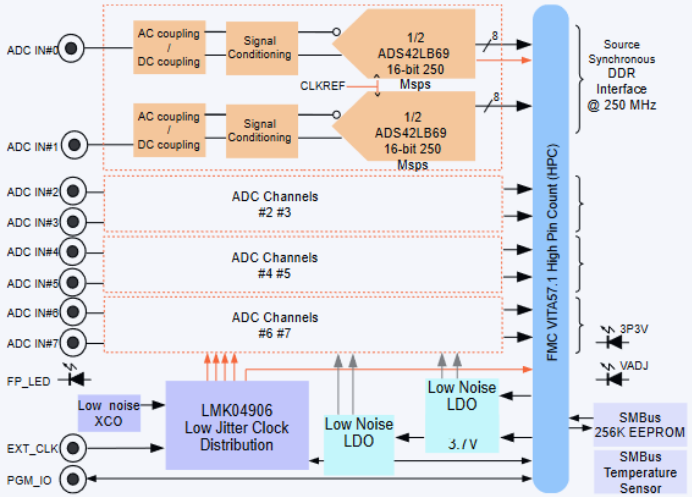
Industrial mezzanines

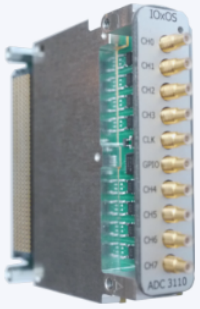
IOxOS TECHNOLOGIES
RELIABILITY BY DESIGN

ADC_3110/3111 – Eight Channel 16-bit ADC **Data Sheet**

FMC Mezzanine Board **ADC_3110_DS_A1**

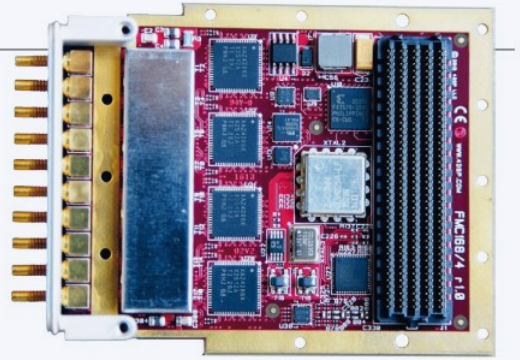
FMC





- **Swiss company**
- **250Msps / 16bit / 8ch**
- **Based on ADS42LB69**

DATASHEET



FMC168 low pin count FMC

8-channel 16-bit ADC - 250 Msps

The FMC168 is a digitizer FMC featuring eight ADC channels with 16-bit resolution and 250 Mega samples per second sampling rate per channel. With a flexible clock generation and distribution scheme, the FMC168/4 allows control on sampling frequency and analog input gain through serial communication with a carrier card.

The FMC168 design is based on the TI ADS42LB69 Dual Channel 16-Bit 250 MSPS A/D, is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions.

FEATURES:

- Eight channel 16-bit 250MSPS A/D conversion
- Available as air cooled and conduction cooled
- VITA 57.1-2010 compliant
- Based on TI ADS42LB69
- Coaxial front panel inputs on SSMC connectors
- Single ended AC- or DC-coupled

- **US company (ABACO)**
- **250Msps / 16bit / 8ch**
- **Based on ADS42LB69**

ADC device

TEXAS INSTRUMENTS

ADS42LB49, ADS42LB69

SLAS904F – OCTOBER 2012 – REVISED MAY 2016

ADS42LBx9 14- and 16-Bit, 250-MSPS, Analog-to-Digital Converters

1 Features

- Dual Channel
- 14- and 16-Bit Resolution
- Maximum Clock Rate: 250 MSPS
- Analog Input Buffer with High Impedance Input
- Flexible Input Clock Buffer with Divide-by-1, -2, and -4
- 2-V_{PP} and 2.5-V_{PP} Differential Full-Scale Input (SPI-Programmable)
- DDR or QDR LVDS Interface
- 64-Pin VQFN Package (9-mm × 9-mm)
- Power Dissipation: 820 mW/ch
- Aperture Jitter: 85 f_S
- Internal Dither
- Channel Isolation: 100 dB
- Performance at f_{IN} = 170 MHz at 2 V_{PP}, –1 dBFS
  - SNR: 73.2 dBFS
  - SFDR:
    - 87 dBc (HD2 and HD3)
    - 100 dBc (Non HD2 and HD3)
- Performance at f_{IN} = 170 MHz: 2.5 V_{PP}, –1 dBFS
  - SNR: 74.9 dBFS
  - SFDR:
    - 85 dBc (HD2 and HD3)
    - 97 dBc (Non HD2 and HD3)

2 Applications

- Communication and Cable Infrastructure
- Multi-Carrier, Multimode Cellular Receivers
- Radar and Smart Antenna Arrays
- Broadband Wireless
- Test and Measurement Systems
- Software-Defined and Diversity Radios
- Microwave and Dual-Channel I/Q Receivers
- Repeaters
- Power Amplifier Linearization

3 Description

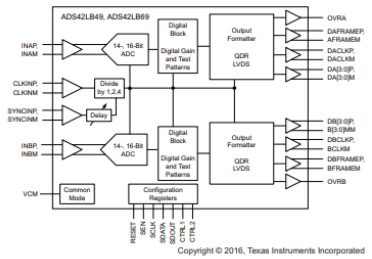
The ADS42LB49 and ADS42LB69 are a family of high-linearity, dual-channel, 14- and 16-bit, 250-MSPS, analog-to-digital converters (ADCs) supporting DDR and QDR LVDS output interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS42LBx9 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with low-power consumption.

Device Information(1)

PART NUMBER	PACKAGE	INTERFACE OPTION
ADS42LB49	VQFN (64)	14-bit DDR or QDR LVDS
		14-bit JESD204B
ADS42LB69	VQFN (64)	16-bit DDR or QDR LVDS
		16-bit JESD204B

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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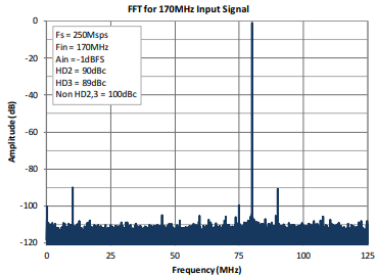

Features:

- Cost ~200euros (100euros/channel)
- Bandwidth > 500MHz
- Channels 2
- Interface DDR/QDR LVDS output

- Already adopted in industry
- On the paper it exceed the performances of the systems in operation
- 2 (or more) channels in the same chip is a desiderata because common drifts self-compensates

IOXIS board (member state)

Three input versions:

1. DC with OPAMP stage (DC … 150MHz)
2. AC (10MHz … 1GHz)
3. AC (200kHz … 300MHz)

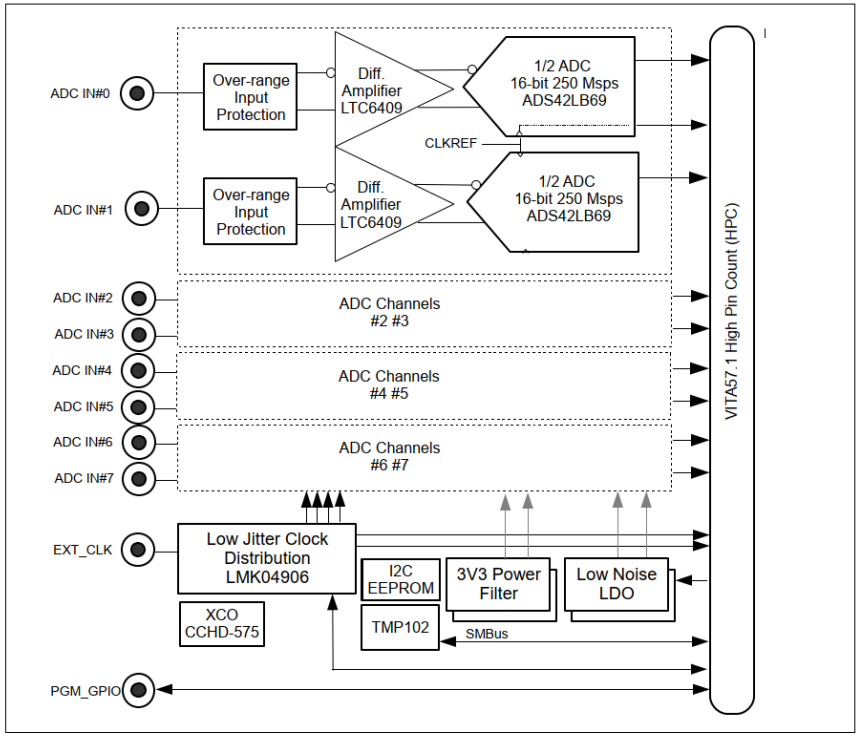

Illustration 9 : ADC_3111A Block Diagram

Prices not negociated:

1 à 9 unités : CHF 5'700
10 à 24 unités : CHF 5'415
25 à 49 unités : CHF 5'250
50 unités ou plus : CHF 5'130

- DC coupled version is OK for most of the applications
- For LINAC4, using the AC coupled version, direct sampling @ 352MHz is feasibile
- Under NDA the full project will be shared
- 8 channels (2 PUs) x mezzanine

Cost estimation & conclusions

Solution	ADC board (CHF)	Carrier & SoM (CHF)	#PUs	Price/PU (CHF)
2x 8ch mezzanine	10000	~3000	4	3250
2x 4ch mezzanine	6000(?)	~3000	2	4500
RF-SoC Gen2/3 (16 ch)	-	~30000	4	>7000

1. RF-SoC very expensive but DAQ ready in case we need system bandwidth > ~80MHz (may it happens?)

2. 2 mezzanines x 8 channels is a good solution also cost-wise

- **Mezzanines based on ADS42LB69 ADC are good candidates (to be confirmed with lab tests)**
- **If ADS… is OK, with "ADC on the carrier" cost reduction may be not negligible**
- **RF-SoC is an overkill (and anyway electrical performances have to be checked)**