TCAD simulation V

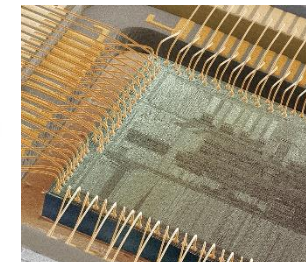
E. Giulio Villani

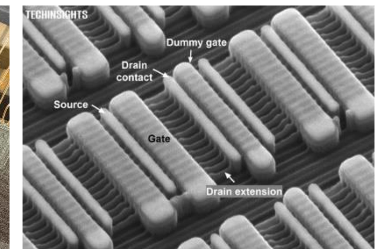
Overview

- **Semiconductor fabrication process**
  - *Fabrication process flow*
  - *Silicon epitaxial growth*
  - *Oxidation*
  - *Resist deposition*
  - *Photolithography/etching*
  - *Implantation*
  - *Thermal annealing/Activation*
  - *Metalization*
- **Process simulation in TCAD**
  - 2D process simulation of PN junction
- **Addendum: Fabrication process details**

Semiconductor fabrication process

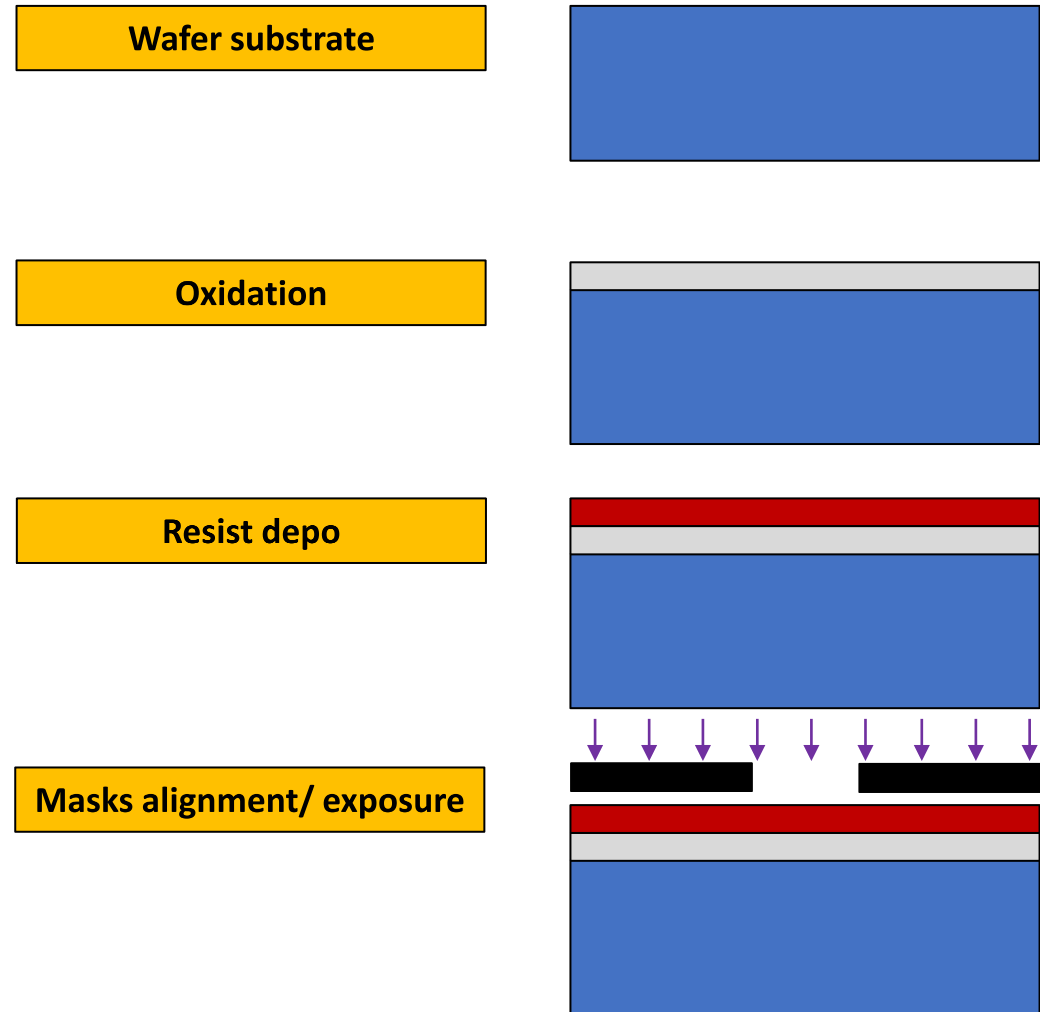
- The fabrication of semiconductor devices is a rather complex process
- Many intermediate steps and manufacturing precision at atomic level
- It starts with the growth of high purity Si crystals





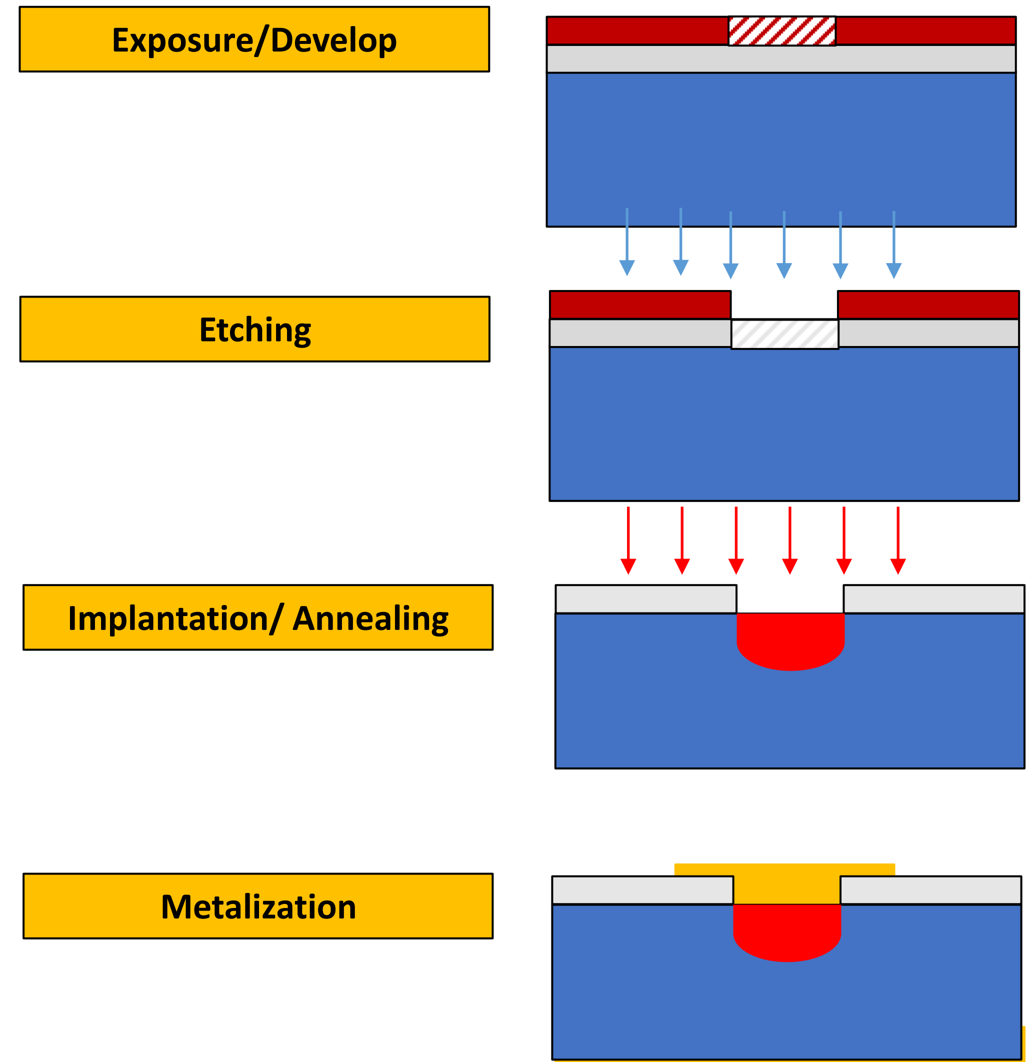
Silicon process fabrication example

- Start with Si wafer cleaned and polished
- The wafer top is covered by insulating layer, SiO_2
- Light-sensitive layer (photoresist) deposited
- A photomask with the desired pattern is aligned with the wafer



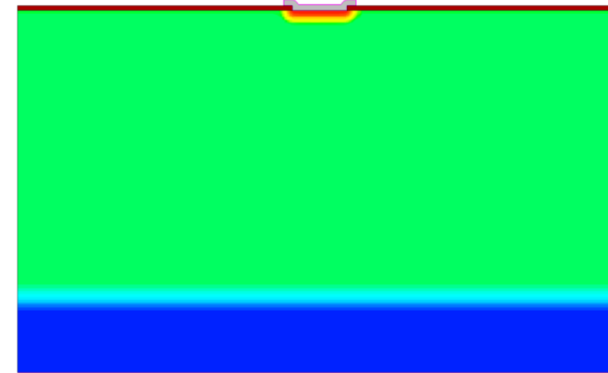
Silicon process fabrication example

- Exposure to UV light makes the photoresist not covered by masks easily removable
- Once the developed resist is removed, the unprotected SiO_2 is etched away, using chemical process. Remaining resist is stripped off
- The exposed areas of Silicon are then doped, e.g. to obtain PN junctions
- Metallization followed by a similar photolithographic process to obtain a final device



Silicon process fabrication example

- Additional layers of conducting or insulating materials can be added, to obtain multilayers structures
- 10s of layers in modern submicron CMOS process



PN junction cross section example – 1 layer

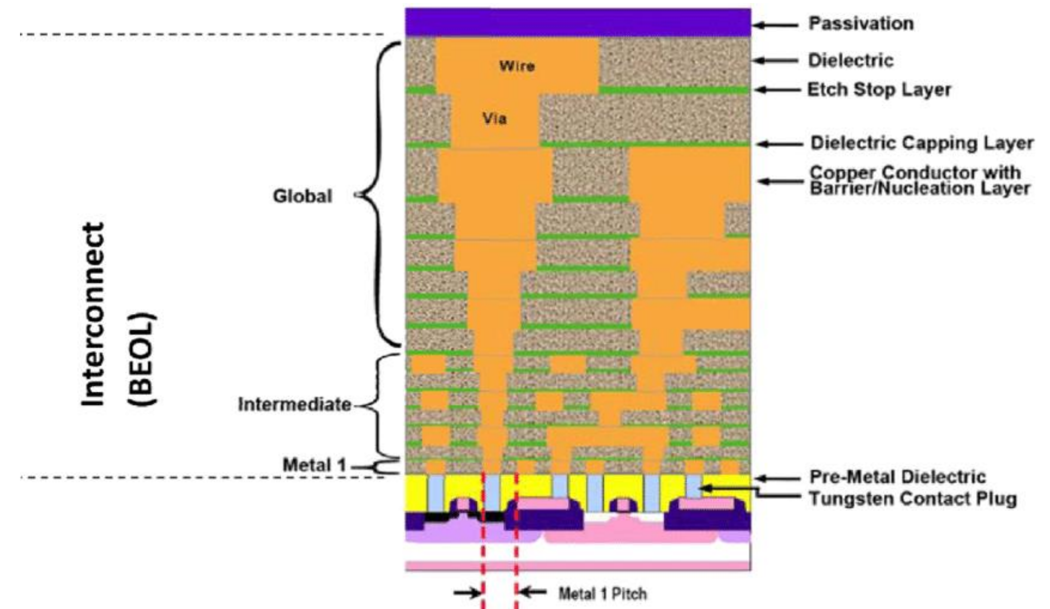


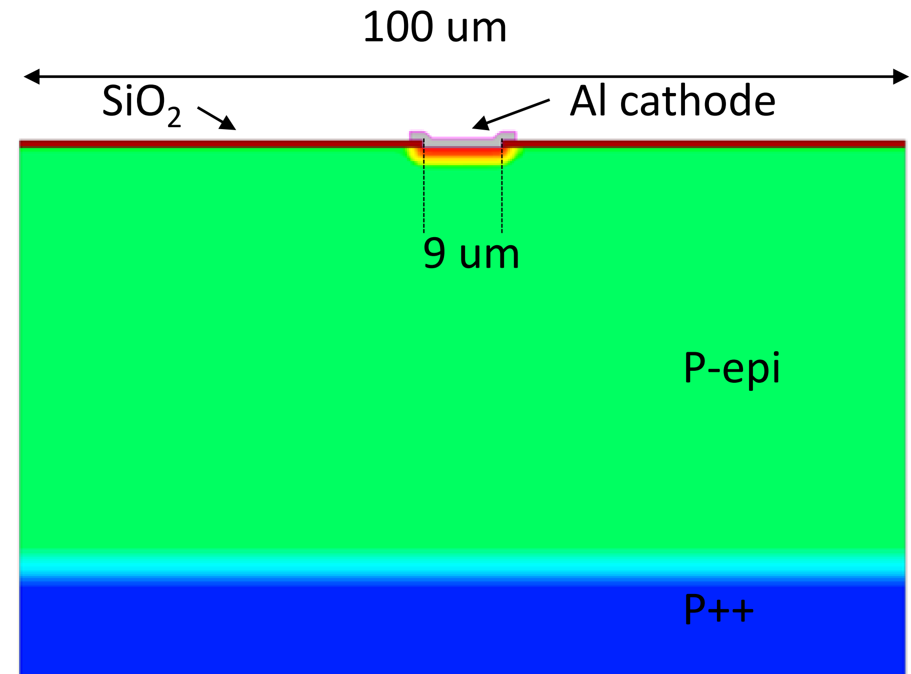
Diagram of a cross-section of a VLSI circuit
from ITRS 2005, http://www.itrs.net/Links/2005itrs/ home2005.htm. 58

Process simulation in TCAD

E. Giulio Villani

Silicon process fabrication example in TCAD

- Simulate the fabrication process of a PN junction
- Epitaxial layer thickness and doping can be modified by the user
- Thermal silicon oxide growth, implantation, etching, diffusion and metal cathode deposition



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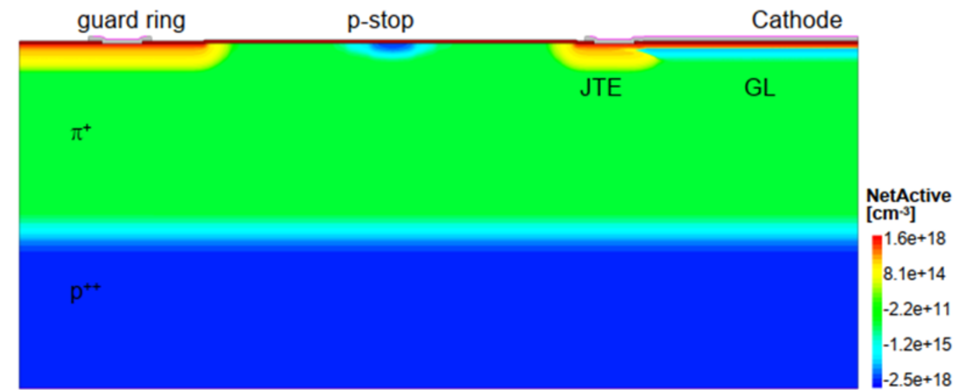
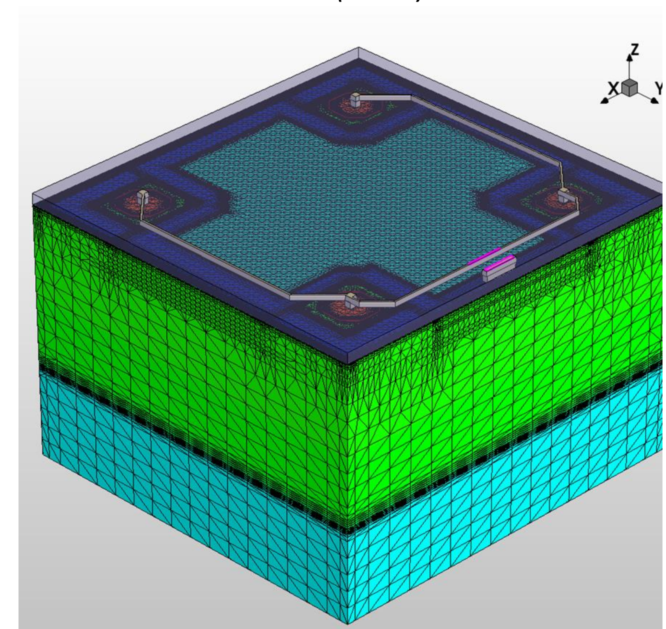
Silicon process fabrication example in TCAD

- The Synopsys tool **SPROCESS** can simulate the fabrication process of semiconductor device, 1/2/3D
- Simulated steps include epitaxial growth, implantation, etching, thermal annealing, metal deposition
- Analytical and MC simulation possible for realistic results
- Simulation of crystal damage following implantation

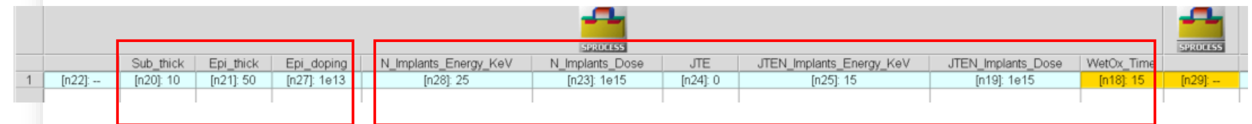


Cross section of 2D simulated Low Gain Avalanche Detector (LGAD)



A 3D simulated OVERMOS sensor

Silicon process fabrication example in TCAD



		Sub_thick	Epi_thick	Epi_doping	N_Implants_Energy_KeV	N_Implants_Dose	JTE	JTEN_Implants_Energy_KeV	JTEN_Implants_Dose	WetOx_Time	
1	[n22]: --	[n20]: 10	[n21]: 50	[n27]: 1e13	[n28]: 25	[n23]: 1e15	[n24]: 0	[n25]: 15	[n19]: 1e15	[n18]: 15	[n29]: --

Device parameters

Fabrication parameters

- Script in SPROCESS to simulate the fabrication of a PN junction on a epitaxial layer
  - Doping and thickness of the epi layer can be modified (device parameters)
  - Fabrication parameters can be modified (energy/dose of the implant, presence of oxide/JTE and oxidation time)

- The obtained mesh will then be simulated for IV, CV and Charge collection

Silicon process fabrication example in TCAD

- Substrate and mask definition: parameters taken from the main workbench window
- Additional SPROCESS parameters configuration

```
##### SPROCESS DEFINITIONS: SUBSTRATE

line x location= @<@Epi_thick@>@<um> spacing= 0.1<um> tag= SubTop
line x location=  @<@Epi_thick@+0.2*@Sub_thick@>@<um> spacing= 0.2<um>
line x location=  @<@Epi_thick@+@Sub_thick@>@<um> spacing= 0.7<um> tag= SubBottom


line y location= -50<um> spacing= 8.00<um> tag= SubLeft
line y location= 0.0<um> spacing= 1.00<um>

line y location=    50<um> spacing= 1.00<um> tag= SubRight

###################################

### JTE mask if needed
###
mask name= JTEGR  segments= { -5.5 -4.5 4.5 5.5 }

### ACTIVE REGION
###
mask name= Active  segments= { -4.5 4.5 }

### SHALLOW N WELL
###
mask name= SHN  segments= { -5 5 }

### CS MASK FOR OXIDE
###
mask name= CS  segments= { -4.5 4.5  }


### only up to front end line here, i.e. up to CS (contacts aded in the next SPROCESS steps)
```

Silicon process fabrication example in TCAD

- Substrate deposition and Epitaxial layer growth
- Saves the structure

```
### Substrate (P+) definition and initialization #
### DEPOSITS THE SUBSTRATE ###

region Silicon xlo= SubTop xhi= SubBottom ylo= SubLeft yhi= SubRight  name = substrate
init Silicon field= Boron concentration= 5e18 DelayFullD  wafer.orient= 100


#####################
pdbSet Oxide Grid perp.add.dist 1e-7
layers
####################


# Global Mesh settings for automatic meshing in newly generated layers
grid set.normal.growth.ratio.2d= 1.1 set.min.normal.size= 20<nm>

if {$SaveAllSteps} { set PlotNum 0; struct FullD tdr=2D_PROC_${PlotNum}_SUB }

### GROWS THE EPI LAYER ###

#if 1
deposit material= Silicon type= isotropic rate= 1.0<um/min> time=  @Epi_thick@<min> \
species= Boron concentration= @<@Epi_doping@>@<cm-3>
diffuse temperature= 1000<C> time= @<600/60>@<min>
#endif

#if 0
###Grows thermal Epi layer ###
temp_ramp name= ramp_topSi temperature= 550 t.final= 1000 time=1<min>
temp_ramp name= ramp_topSi t.final= 1000 time= 600<s> Epi thick= @Epi_thick@<um> \
epi.doping = { boron= @Epi_doping@ } epi.model= 1
diffuse temp.ramp= ramp_topSi

#endif

### saves the doping profile of substrate/epitaxial

if {$SaveAllSteps} { set PlotNum 0; struct FullD tdr=2D_PROC_${PlotNum}_Epi@Epi_doping@ }
```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Silicon process fabrication example in TCAD

- Thermal oxide growth 300 nm
- Oxide thickness extraction
- Saves the structure

```
### WET THERMAL OXIDE GROWTH
### ramp up
temp_ramp name= temperatureRamp temp= 700<C>  t.final= 900<C>   time= 20<min>     flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp= 900<C>   t.final= 1000<C>  time= 12.5<min>  flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp=1000<C>   t.final= 1080<C>  time= 16<min>    flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp= 1080<C> t.final= 1100<C>  time= 5<min>      flows= {N2=4.0   O2=0.1}

### hold for anneal

temp_ramp name= temperatureRamp temp= 1100<C>  t.final= 1100<C> time= @WetOx_Time@<min>  flows= {H2=7.0  O2=4}


###ramp down
temp_ramp name= temperatureRamp temp= 1100<C>  t.final=700<C>   time= 67<min>


diffuse temp_ramp= temperatureRamp
temp_ramp clear
gas_flow  clear

}
### Simple Oxide deposition
###deposit Oxide type= isotropic thickness= 300.0<nm>

if {$SaveAllSteps} { set PlotNum 1; struct FullD tdr= 2D_PNjnct_${PlotNum}_ThOx_BulkEpi@Epi_doping@ }

##  Oxide thickness extraction
set int_si_o2 [interface Silicon /Oxide y= 0 z= 0]
set int_o2_gas [interface Oxide /Gas y= 0 z= 0]
set tox_thickness [expr $int_si_o2 - $int_o2_gas]
puts "OX_Thickness [format %3.1f [expr $tox_thickness*1.0e3]]"
## End of  oxide thickness extraction
```

Silicon process fabrication example in TCAD

- Optional JTE
- Etching of Active area and growth of sacrificial oxide
- Saves the structure

```
# ========================================================================
# 4 -- etching active area
# ========================================================================

photo mask=Active thickness=1000<nm>


etch oxide  anisotropic thickness=0.400


strip resist

if {$SaveAllSteps} { set PlotNum 4;
 struct FullD tdr= 2D_PNjnct_${PlotNum}_Active_Etch_JTENACT_JTENimp@JTE@_@JTEN_Implants_Energy_KeV@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@}



# ========================================================================
# 5 --  ReOxide Growth - 40nm -
# ========================================================================
### WET THERMAL OXIDE GROWTH
### ramp up
temp_ramp name= temperatureRamp temp= 700<C>  t.final= 900<C>   time= 20<min>       flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp= 900<C>   t.final= 1000<C>  time= 12.5<min>    flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp=1000<C>   t.final= 1080<C>  time= 16<min>      flows= {N2=4.0   O2=0.1}

temp_ramp name= temperatureRamp temp= 1080<C> t.final= 1100<C>  time= 5<min>        flows= {N2=4.0   O2=0.1}

### hold for anneal

temp_ramp name= temperatureRamp temp= 1100<C>  t.final= 1100<C> time=0.7<min>  flows= {H2=7.0   O2=4}


###ramp down
temp_ramp name= temperatureRamp temp= 1100<C>  t.final=700<C>   time= 67<min>



diffuse temp_ramp= temperatureRamp
temp_ramp clear
gas_flow  clear


if {$SaveAllSteps} { set PlotNum 5;
struct FullD tdr= 2D_PNjnct_${PlotNum}_ReOxide_JTENimp@JTE@_@JTEN_Implants_Energy_KeV@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@ }

## SAC oxide thickness extraction
```


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Silicon process fabrication example in TCAD

- Implantation of N well: beam tilting to suppress channeling effect
- Low Temperature Oxide (LTO) deposition
- Saves the structure

```
# ======================================================================
# 6 --  implant shallow n  ---
# ======================================================================

photo mask=SHN thickness=1000<nm>

implant Phosphorus dose= @<@N_Implants_Dose@>@<cm-2> energy= @N_Implants_Energy_KeV@<keV> tilt= 7<degree> rotation= 27

strip resist


if {$SaveAllSteps} { set PlotNum 6;
 struct FullD tdr= 2D_PNjnct_${PlotNum}_ShalN_@N_Implants_Energy_KeV@_@N_Implants_Dose@_ReOxide_JTENimp@JTE@_@JTEN_Implants_Energy_Ke
V@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@ }


# ======================================================================
# 7 -- LTO deposit 500 nm
# ======================================================================

deposit material= {Oxide} type= isotropic time= 5 rate= {0.1}


if {$SaveAllSteps} { set PlotNum 7;
 struct FullD tdr= 2D_PNjnct_${PlotNum}_LTO_ShalN_@N_Implants_Energy_KeV@_@N_Implants_Dose@_ReOxide_JTENimp@JTE@_@JTEN_Implants_Energ
y_KeV@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@ }
```

Silicon process fabrication example in TCAD

- Activation of implanted ions and LTO densification
- Etching of SiO2 for contact placement
- Saves the structure

```
# ======================================================================
# 8 --  activation implants ,beside densification LTO 30 mins at 950 C
# ======================================================================

### Thermal annealing after Shallow N  implants

temp_ramp name= temperatureRamp temp= 600<C>  t.final= 900<C>   time= 30<min>     flows= {N2=8.0   O2=0.0}
temp_ramp name= temperatureRamp temp= 900<C>  t.final= 1000<C>  time= 12.5<min>     flows= {N2=8.0   O2=0.0}
temp_ramp name= temperatureRamp temp= 1000<C>  t.final= 1080<C> time= 16<min>     flows= {N2=8.0   O2=0.0}
temp_ramp name= temperatureRamp temp= 1080<C>  t.final= 1100<C> time= 5<min>     flows= {N2=8.0   O2=0.0}

### Hold
temp_ramp name= temperatureRamp temp= 1100<C>  t.final= 1100<C> time= 60<min>     flows= {N2=8.0   O2=0.0}


### Ramp down

temp_ramp name= temperatureRamp temp= 1100<C>  t.final= 600<C> time= 84<min>     flows= {N2=8.0   O2=0.0}


diffuse temp_ramp= temperatureRamp
temp_ramp clear
gas_flow  clear


if {$SaveAllSteps} { set PlotNum 8;  struct FullD tdr= 2D_PNjnct_${PlotNum}_ACT_LTO_ShalN_@N_Implants_Energy_KeV@_@N_Implants_Dose@_R
eOxide_JTENimp@JTE@_@JTEN_Implants_Energy_KeV@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@ }

# ======================================================================
# 9: etching for metal depo / contacts deposition
# ======================================================================
### etching of SiO2 for contacts


photo mask=CS thickness=1000<nm>

etch oxide  anisotropic thickness=1


strip resist
```

Silicon process fabrication example in TCAD

- The second SPROCESS re-meshes for device simulation
- Contact mask definition
- Metal deposition for contact and etching
- Saves the structure

```
### NOMINAL CONTACT MASK
mask name= contacts_mask segments= { -6 6 }

### DOPING BASED REFINEMENT
pdbSet Grid Adaptive 1

### reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0

### Set high quality delaunay meshes
pdbSet Grid sMesh 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh CoplanarityAngle 179
pdbSet Grid SnMesh MaxPoints 5000000
pdbSet Grid SnMesh MaxNeighborRatio 1e6

### Set the interface spacing
pdbSet Grid SnMesh min.normal.size 0.01
pdbSet Grid SnMesh normal.growth.ratio.2d 4.0
pdbSet Grid SnMesh max.box.angle.2d 179


###Set which interfaces will have interface refinement
refinebox interface.materials= "Silicon"
### Al DEPOSITION 1 UM FOR CATHODE CONTACT

deposit material= {Aluminum} type= isotropic time= 10 rate= {0.1}

etch material= {Aluminum} type= anisotropic time= 10 rate= {0.12} \
     mask= contacts_mask

### Cathode contact
contact box Aluminum xlo= -2 ylo= -6 xhi= 0.5 yhi= 6 name= Cathode


### Substrate contact
contact name = Substrate bottom

### saves the entire structure with contatcs and mesh for SDEVICE
###grid remesh
grid remesh info = 1


 set PlotNum 10

struct FullD tdr= 2D_PNjnct_${PlotNum}_ShalN_@N_Implants_Energy_KeV@_@N_Implants_Dose@_JTENimp@JTE@_@JTEN_Implants_
Energy_KeV@_@JTEN_Implants_Dose@_BulkEpi@Epi_doping@  !Gas
```

Silicon process fabrication example in TCAD

- Substrate and mask definition
- Epitaxial layer growth
- Thermal oxide growth 300 nm

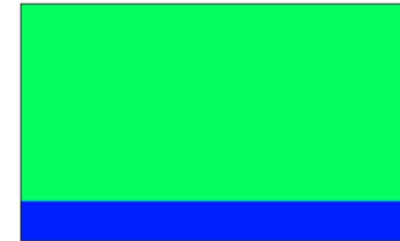
SPROCESS

TwoDsprocess

	Sub_thick	Epi_thick	Epi_doping	N_Implants_Energy_KeV	N_Implants_Dose	JTE	JTEN_Implants_Energy_KeV	JTEN_Implants_Dose	Oxidation	WetOx_Time
--	10	50	1e13	25	1e15	0	15	1e15	1	15

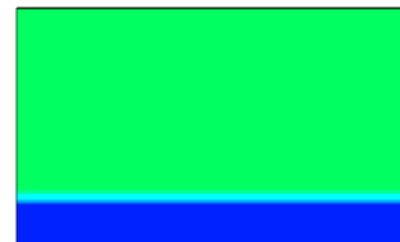
Substrate

Substrate + Epi



ThOx

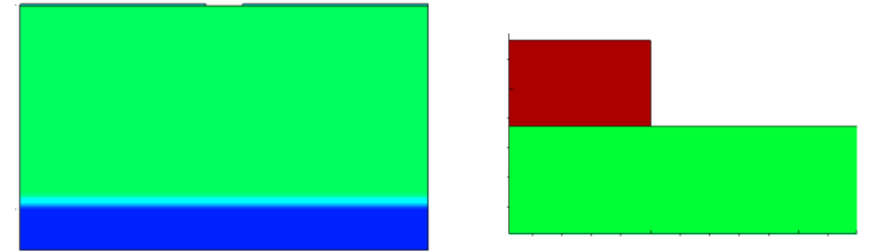
Substrate + Epi



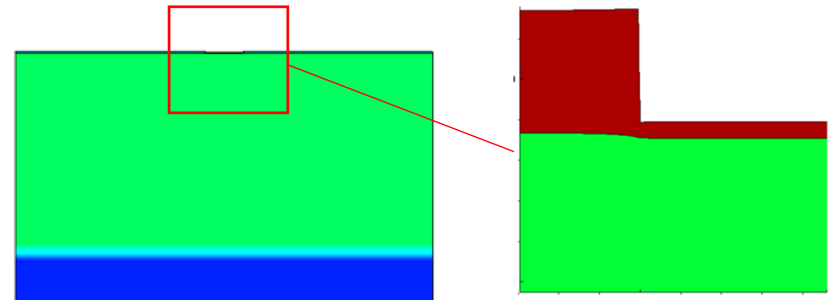
Silicon process fabrication example in TCAD

- SiO2 etching
- Sacrificial SiO2 growth
- Implant N well

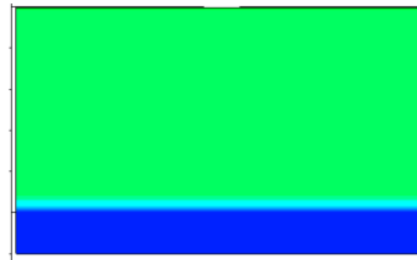
SiO2 etching



SiO2 growth



Implant



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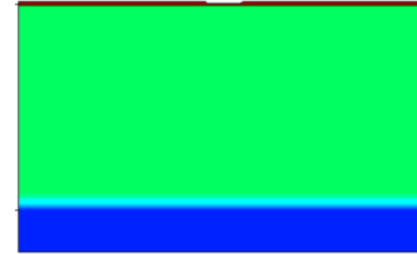
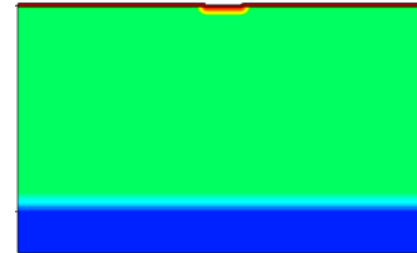
Silicon process fabrication example in TCAD

- LTO (Low Temp Oxide) deposition
- Activation / annealing
- Etching cathode contact

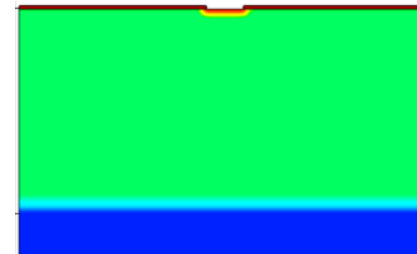
LTO



Activation



Etching



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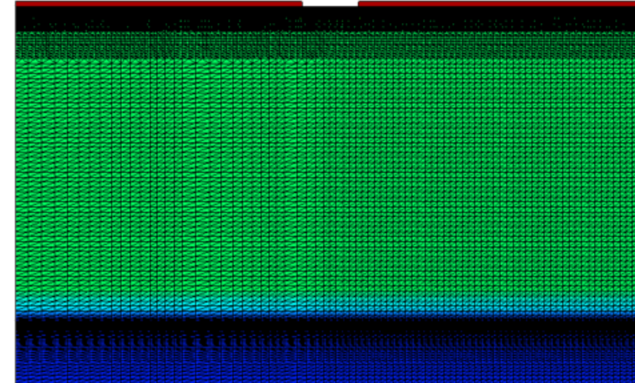
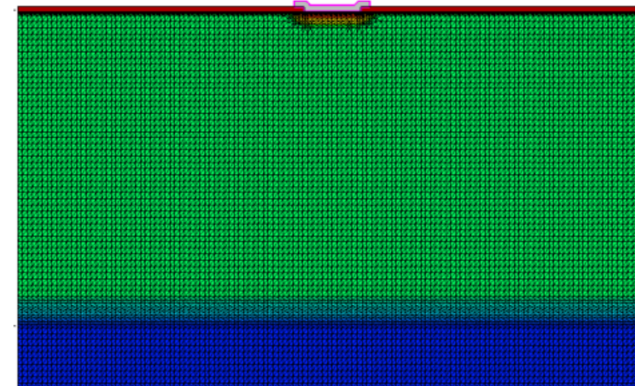
Silicon process fabrication example in TCAD

- Metal contact deposition and etching
- Remeshing for device simulation:
  - Delaunay meshing
  - Specify refinement in region of electrical simulation interest, i.e. near the junction, at the interface

Meshing 1



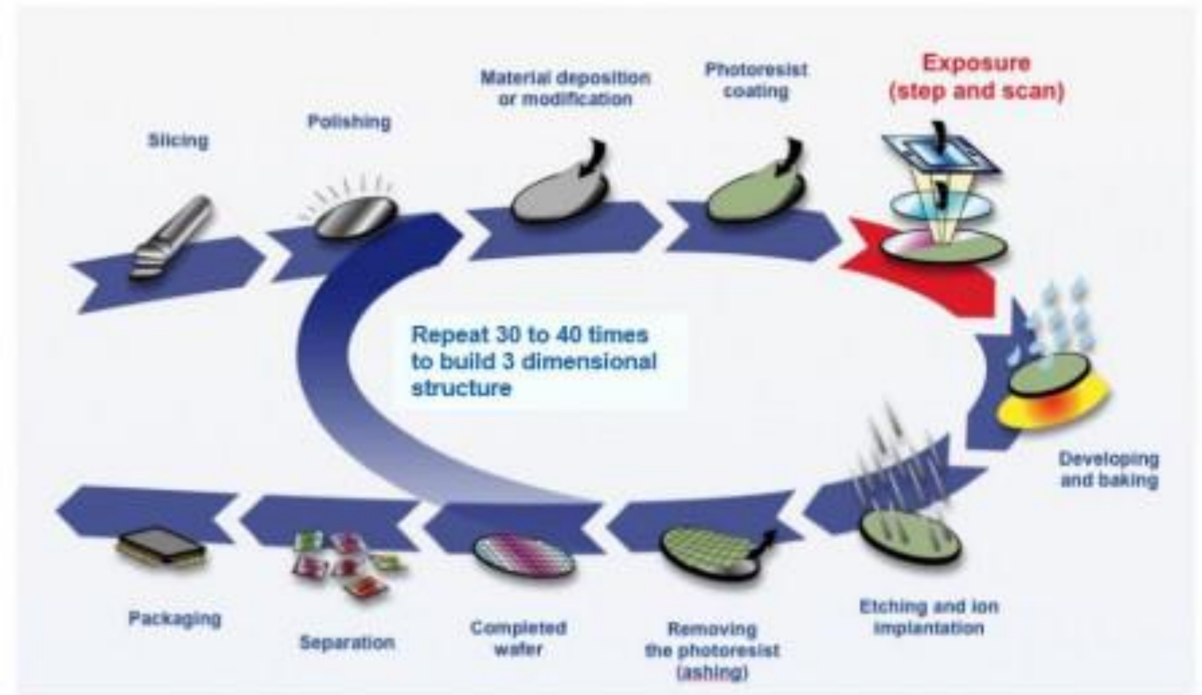
Re- Meshing +Al deposition + etching

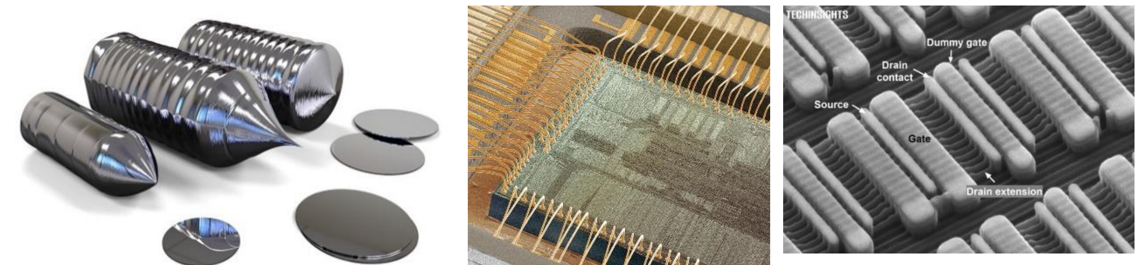


Addendum: More details on fabrication process

Silicon process fabrication details

- The fabrication of semiconductor devices is a rather complex process
- Many intermediate steps and manufacturing precision at atomic level
- Some details of the manufacturing steps are provided in the next slides





Silicon crystal growth Czochralski

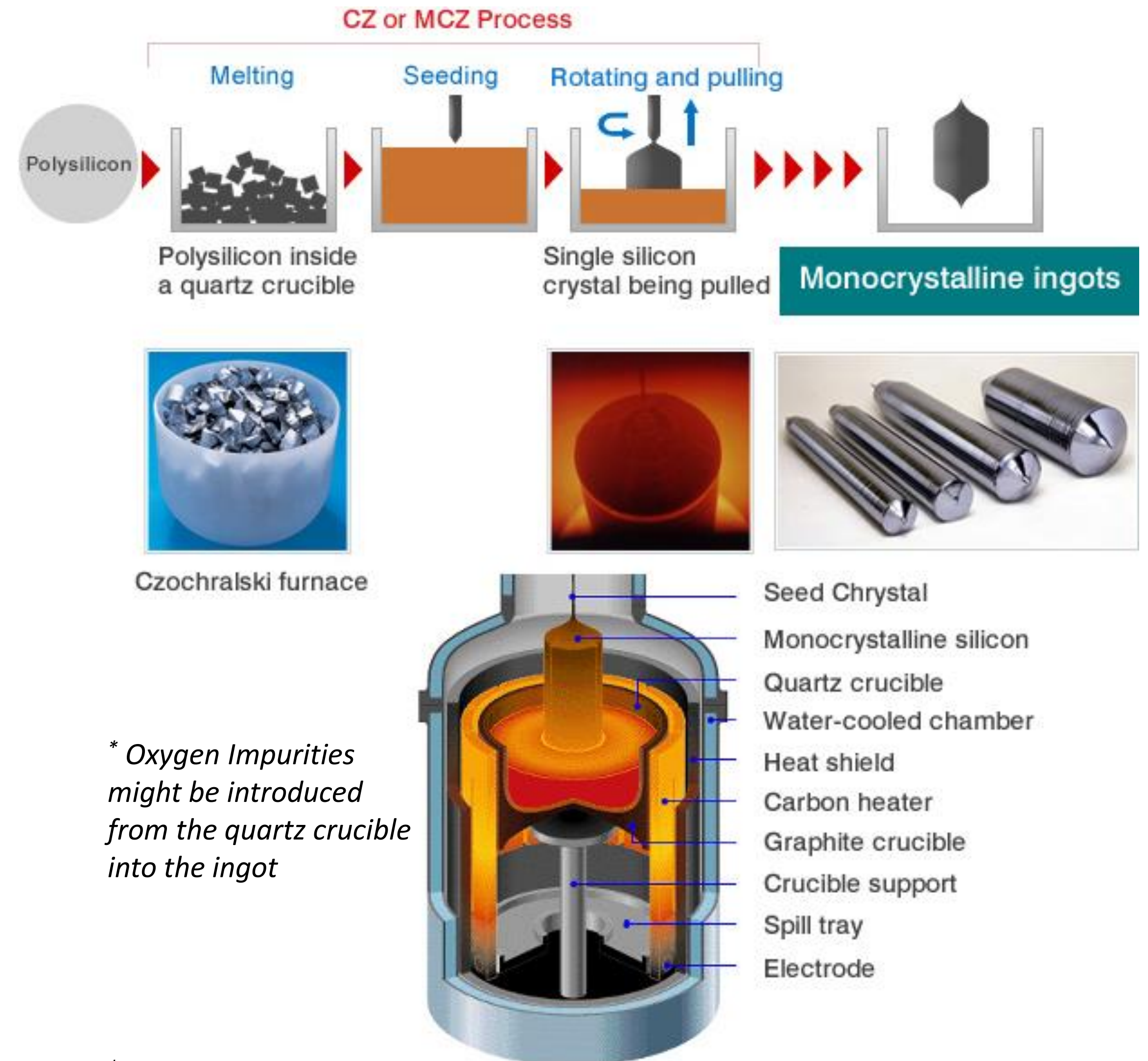
- The majority of ICs are made on single-crystal Si wafers grown in large ingots using **CZ** (Czochralski, 1915 [1]) method

  1. High purity polysilicon (99.9999999% or 9N) crushed into powder, put into a quartz crucible and heated until it melts

  2. A seed crystal is dipped into liquid silicon. As the stick is rotated and slowly pulled up, an ingot of monocrystalline silicon is formed that has the same atomic arrangement as the seed crystal

- For detector grade Si, the smallest concentration of contaminants is required. The Floating- Zone (FZ [2]) process is usually employed for this

[1] Development of Crystal Growth Technique of Silicon by the Czochralski Method, Vol. 124 ACTA PHYSICA POLONICA, 2013
[2] T.F. Ciszek, T.H. Wang, Silicon defect and impurity studies using float-zone crystal growth as a tool, Journal of Crystal Growth, 237, p. 1685-1691, 2002



* *Oxygen Impurities might be introduced from the quartz crucible into the ingot*

* *Czochralski discovered this by accident: instead of dipping his pen into his inkwell, he dipped it in molten tin, and drew a tin filament, which later proved to be a single crystal*

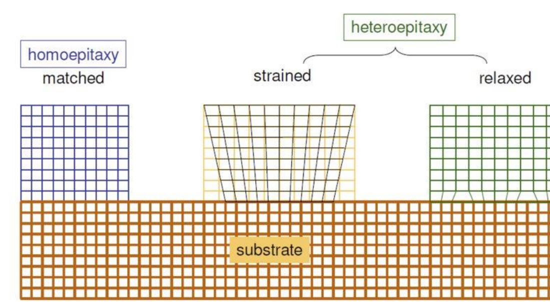
Silicon crystal growth
Epitaxy

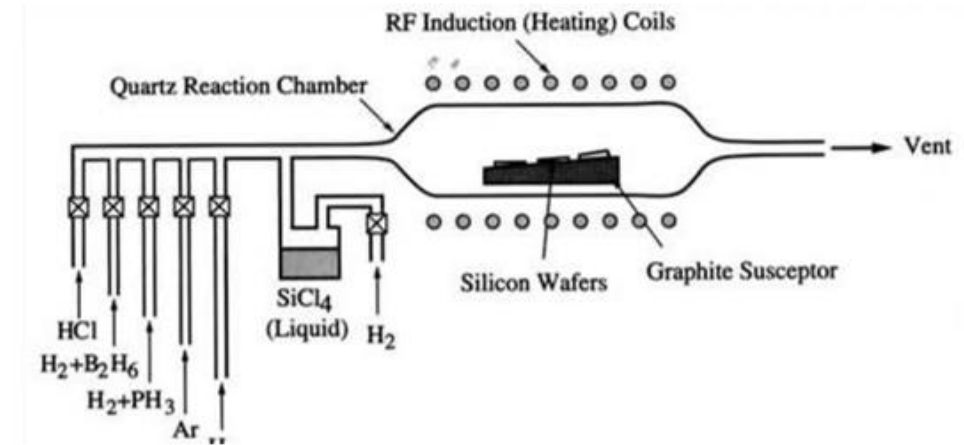
- Arrangement of atoms over existing planes of crystalline substrate, to form an extended crystal

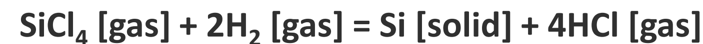
- The deposited layer can have very different doping of the substrate, allowing doping profiles unattainable with implantation.

- Different materials can be grown (heteroepitaxy)

- The epitaxially grown layer can be oxygen free







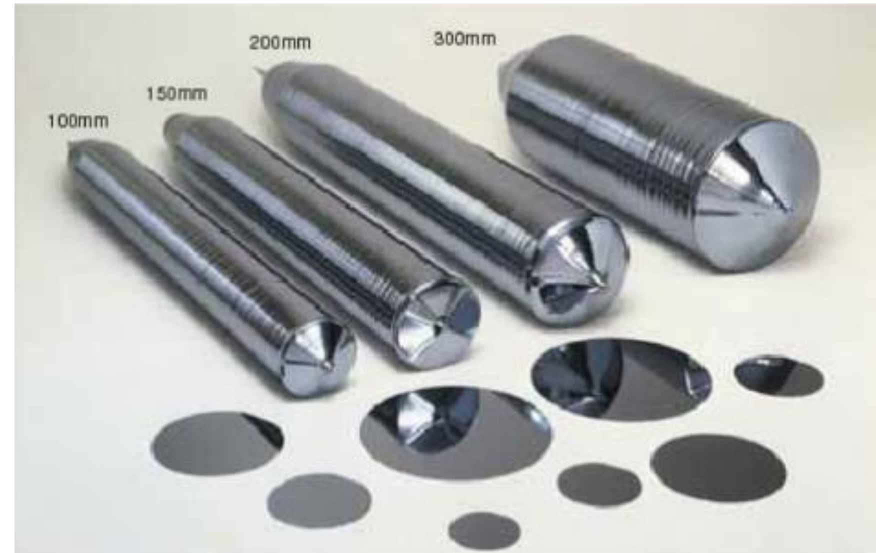
$SiCl_4$ [gas] + $2H_2$ [gas] = Si [solid] + 4HCl [gas]

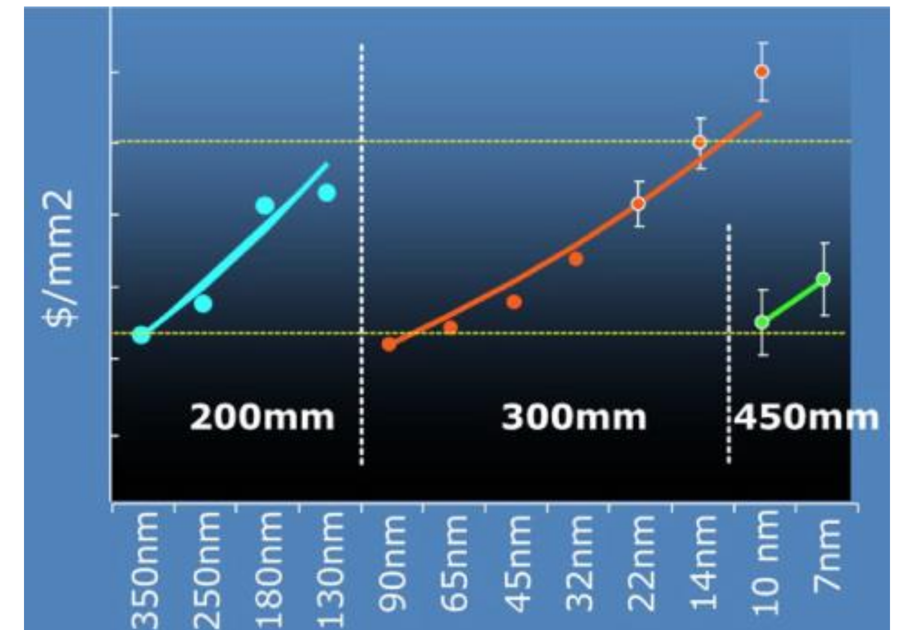
Chemical Vapour Deposition (CVD) is the formation of solid films on a substrate by exploiting a chemical reaction of reactants in vapour phase.

Reactants introduced in reaction chamber decompose and react with the heated surface to form the film

Silicon crystal

- The cylindrical ingot is sliced into thin circular wafers, polished, etched, and cleaned until their surface is almost roughness free (<< 1 nm)
- The diameter of Si ingots grew over the years: currently 300 mm diameter, driven by keeping the cost/area constant
- As per 2022, worldwide Si wafer area around 10e6 m^2 , for an approximate 1.15×10^{12} semiconductor chips produced





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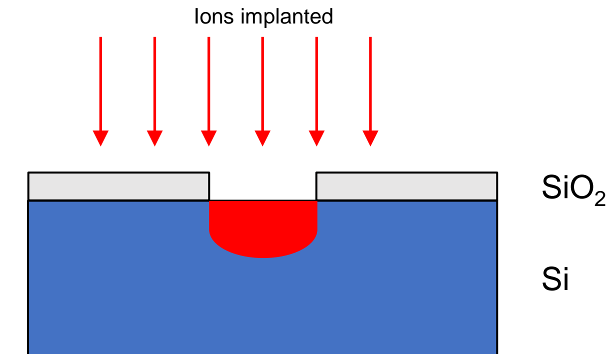
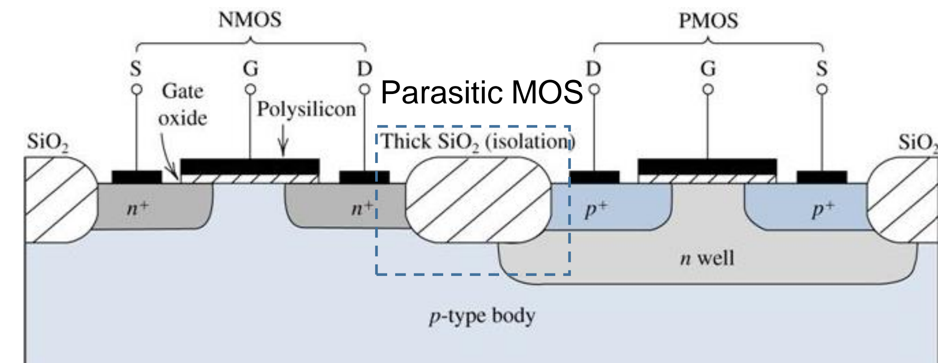
Oxidation process

- The purpose of oxidation is essentially to provide **isolation**:

- Barrier against dopants diffusion/implantation

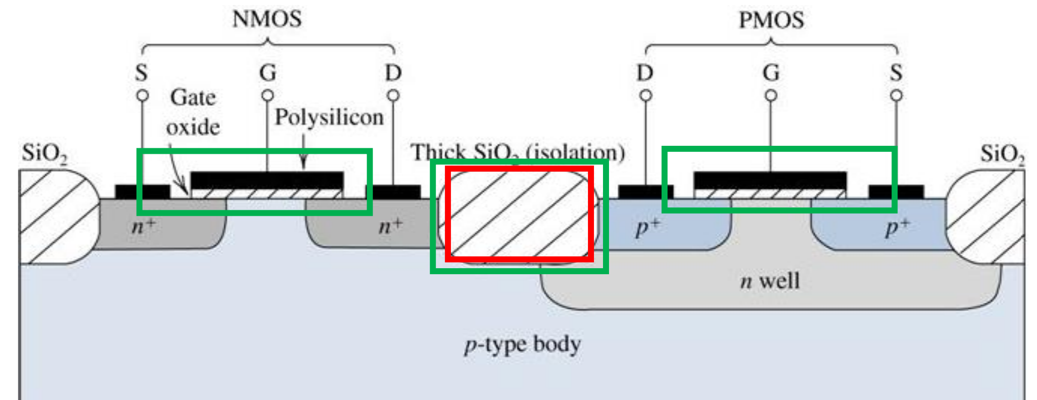
- Electrical insulator between devices (critical field ~ 10^7 V/cm)

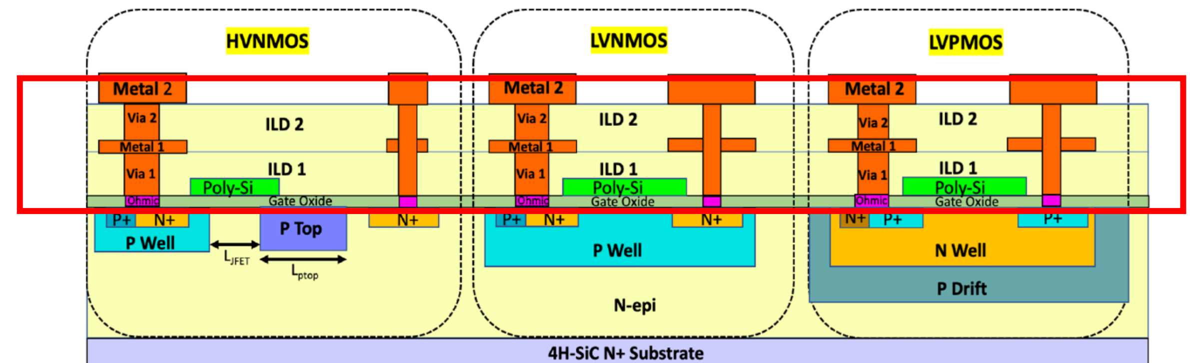




Oxidation process

- Two deposition methods:
  - **Thermal growth**
    - Dry: best quality, slow growth rate: used for gate oxide
    - Wet: lower quality, faster growth rate: used for field oxide (isolation)
  - **Chemical vapor deposition** [3] (lower quality, fast)
    - Used when no Si is available for oxidation (Interlayer Layer Dielectric, ILD)



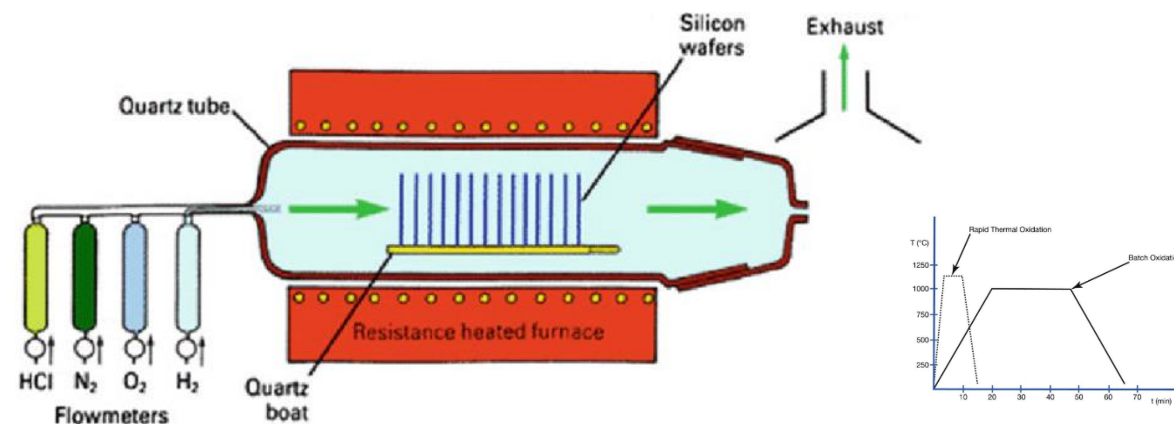


[3] J. K. Wang, D. R. Denison, Advanced techniques for interlayer dielectric deposition and planarization, Proc. SPIE 2090, https://doi.org/10.1117/12.156535, 1993.

Oxidation process tools

- **Thermal oxidation:**
  oxide is grown at high temperature (~ 1000° C) by supplying oxygen that reacts with silicon wafer to form SiO_2 at the surface

- Wafers inserted on a suspended boat into a tubular reactor of quartz, heated by resistance



$$Si + O_2 \rightarrow SiO_2.$$

Dry oxidation: best quality, slow (10 nm/hr)

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2.$$

Wet oxidation: lower quality, faster (>x10)

Wet oxidation is faster because H_2O molecules smaller than O_2 leading to faster diffusion through SiO_2

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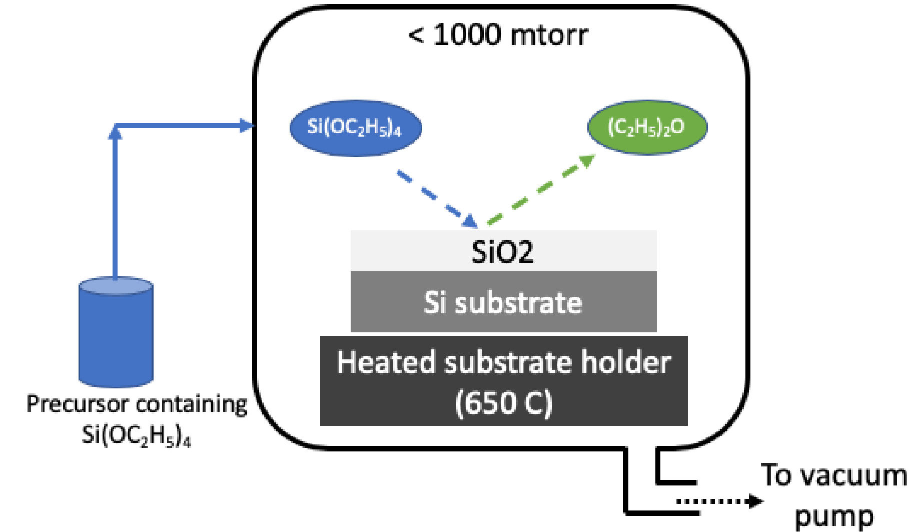
Oxidation process tools

- **Chemical Vapor Deposition (CVD) :** reaction of vapor phase chemicals containing the material to deposit form the solid film on substrate. Reactant gases decompose and form the film.
  - SiO_2 growth rate >x10 compared to thermal oxide, but lower quality
  - CVD is also used for growing dielectric materials of different electrical permittivity (high k/low k material)



Chemical reactions	Techniques
$SiH_4 + O_2 \xrightarrow{430\ °C,\ 1\ bar} SiO_2 + 2H_2$	Silane oxide CVD
$SiH_4 + O_2 \xrightarrow{430\ °C,\ 40\ bar} SiO_2 + 2H_2$	LTO CVD
$SiH_2Cl_2 + 2N_2O \xrightarrow{900\ °C,\ 40\ Pa} SiO_2 + Gas$	HTO CVD
$Si(OC_2H_5)_4 \xrightarrow{700\ °C,\ 40\ bar} SiO_2 + Gas$	TEOS CVD
$Si(OC_2H_5)_4 + O_2 \xrightarrow{400\ °C,\ 0.5\ bar} SiO_2 + Gas$	ACVD
$SiH_4 + 4N_2O \xrightarrow{350\ °C,\ Plasma\ 40\ Pa} SiO_2 + Gas$	PECVD

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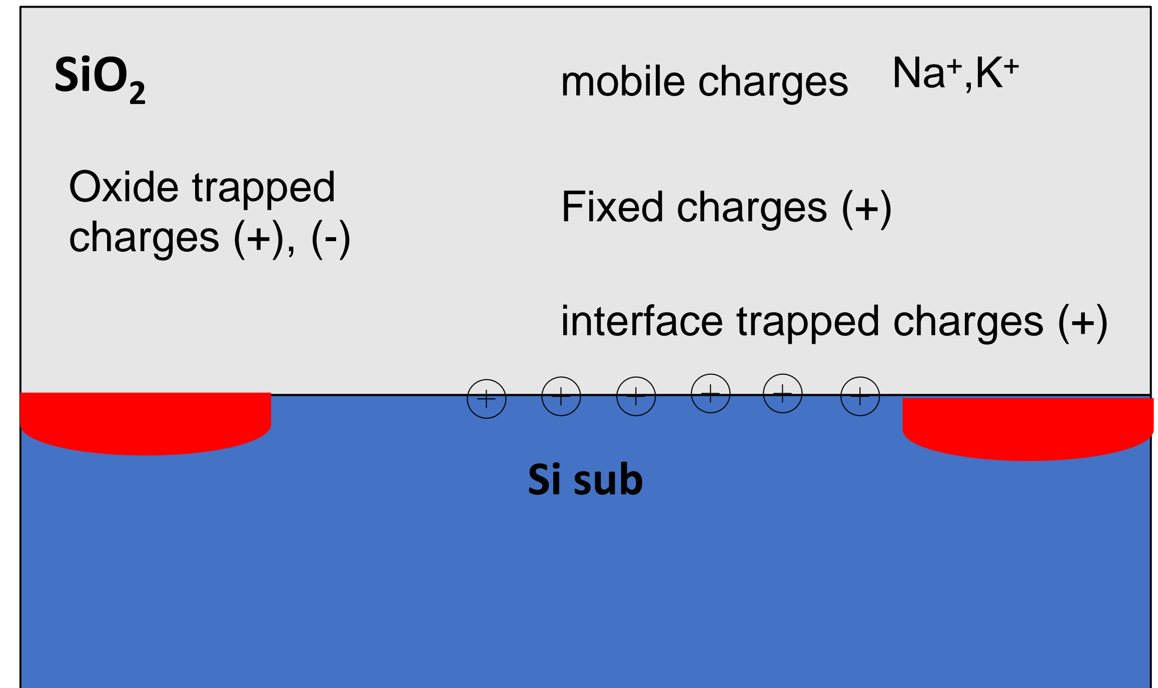
Oxide quality

- Mobile charges (contamination - make insulator conductive)
- Fixed charges (incompletely oxidized Si - create an extra electric field affecting the devices in Si)
- Oxide trapped charge (broken Si-O bonds, due to radiation)
- Interface trapped charges (dangling bonds – affect mobility and increase noise)



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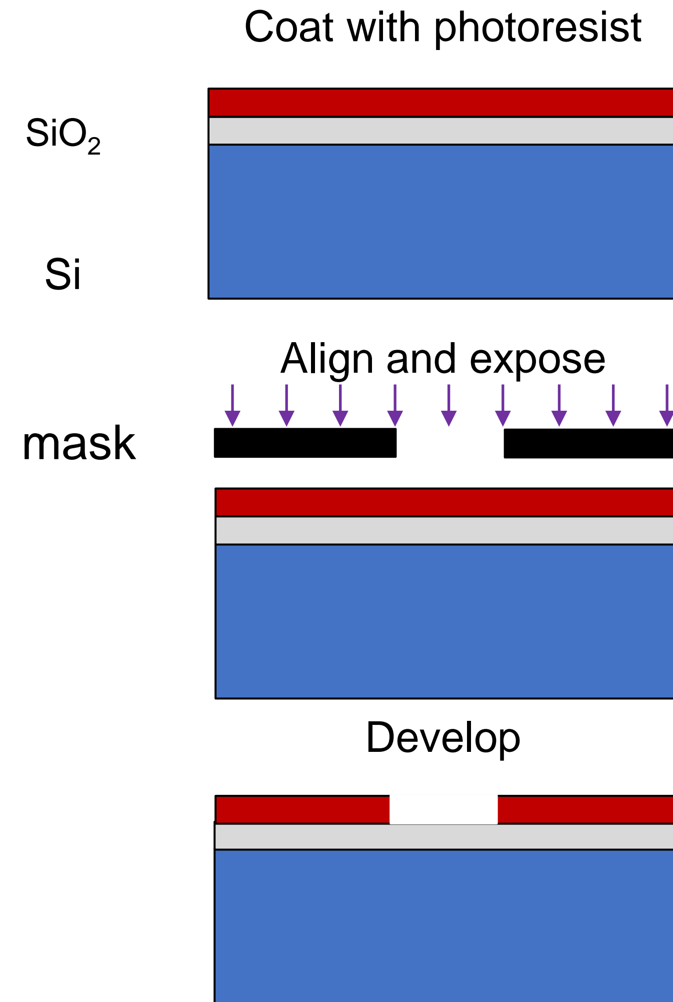
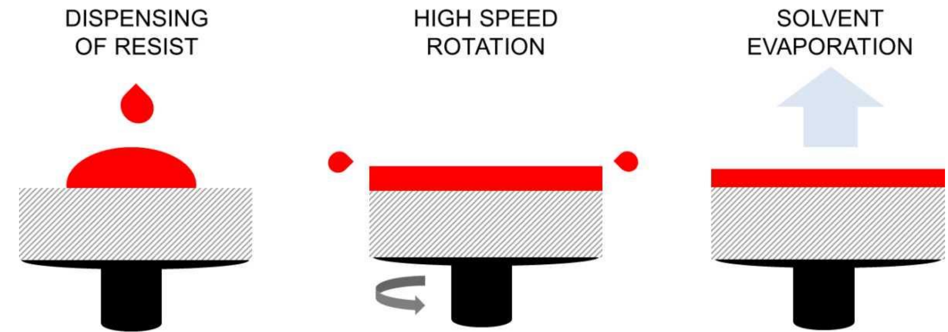
Resist deposition

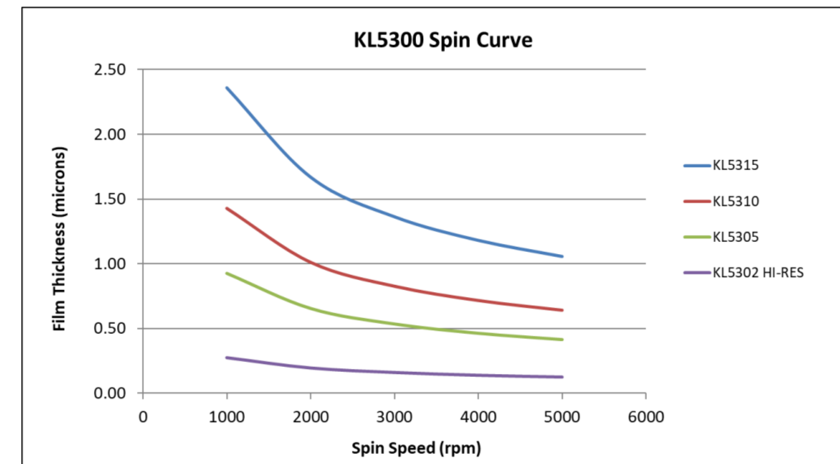
- The purpose of photoresist deposition is to prepare the wafer for the next step of lithography
- The pattern needs to be reproduced on the photoresist, using a special camera that projects the image of the photomask onto the photoresist
- Photoresist must allow to form a high-res image of the pattern (photo) and be able to stop etching (resist) to transfer the pattern onto the wafer



Resist deposition

- A small amount (~ml) of photoresist, with its solvent, is poured onto the wafer surface
- The wafer is spun at high speeds, the resist spreads out. The air flow increases the viscosity of the photoresists, by evaporating the solvent, which leads to a very uniform photoresist layer spread over the surface
- A post-apply bake is usually performed to further stabilize the film before lithography
- The obtained uniformity is of the order of < 1nm over the entire wafer surface





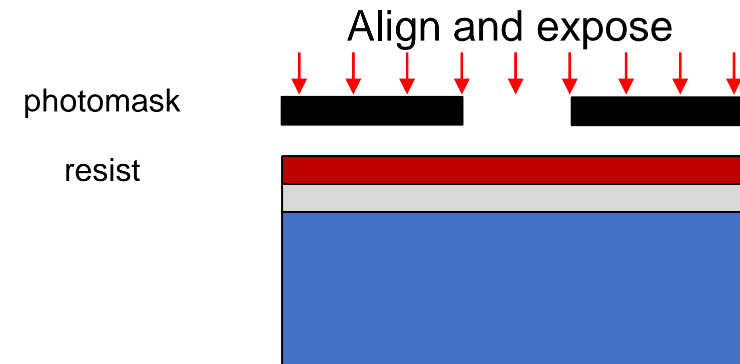
From KemLab website, https://www.kemlab.com/

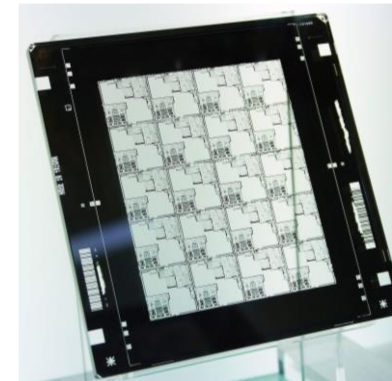
Resist thickness $\sim \frac{1}{\sqrt{\omega}}$

Mask/photolithography

- The photomask, usually made of chrome on quartz substrate, around 5 mm thick, includes the pattern to be reproduced onto the wafer. It can be put in direct contact (contact litho), kept at small distance (proximity litho) or projected onto the wafer (projection litho)

- The photomask is typically bigger (x4-x5) than the wafer pattern



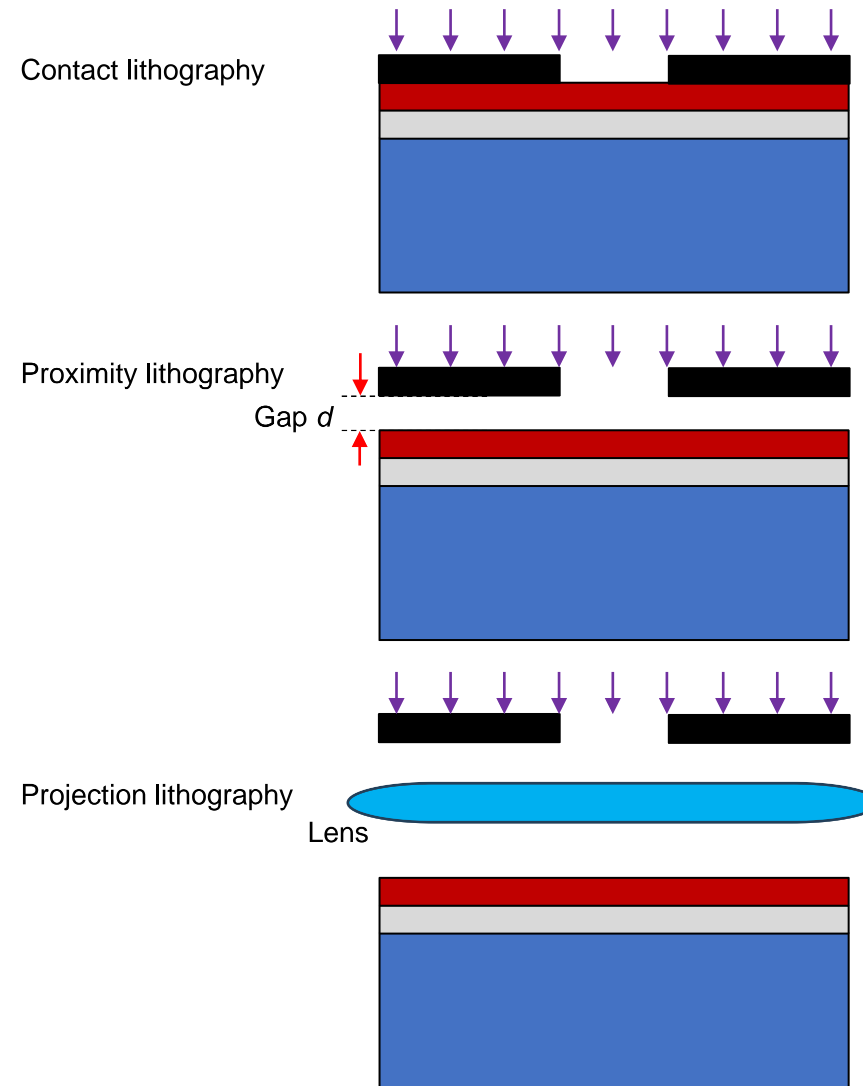


From Wikipedia

The photomask itself is an example of high-resolution photolithography, usually obtained by electron beams to expose a photoresist

Mask/photolithography

- Contact printing provides a resolution near the wavelength λ of light used, but every contact damages the mask, that can be used only for a number of times
- Proximity printing keeps mask and wafer separated, around 10 um to avoid cumulative defectiveness, but resolution is about $\sqrt{\lambda d}$
- The modern lithography process makes use of projection printing, where the mask is illuminated by UV light and the image is projected on the wafer



Mask/photolithography

- The cost of lithography process is around 30 % - 50 % of the entire fabrication process and bound to increase for the most modern technology nodes
- Lithography is a gating technology, which leads the advancement in semiconductor industry

From Nikon website

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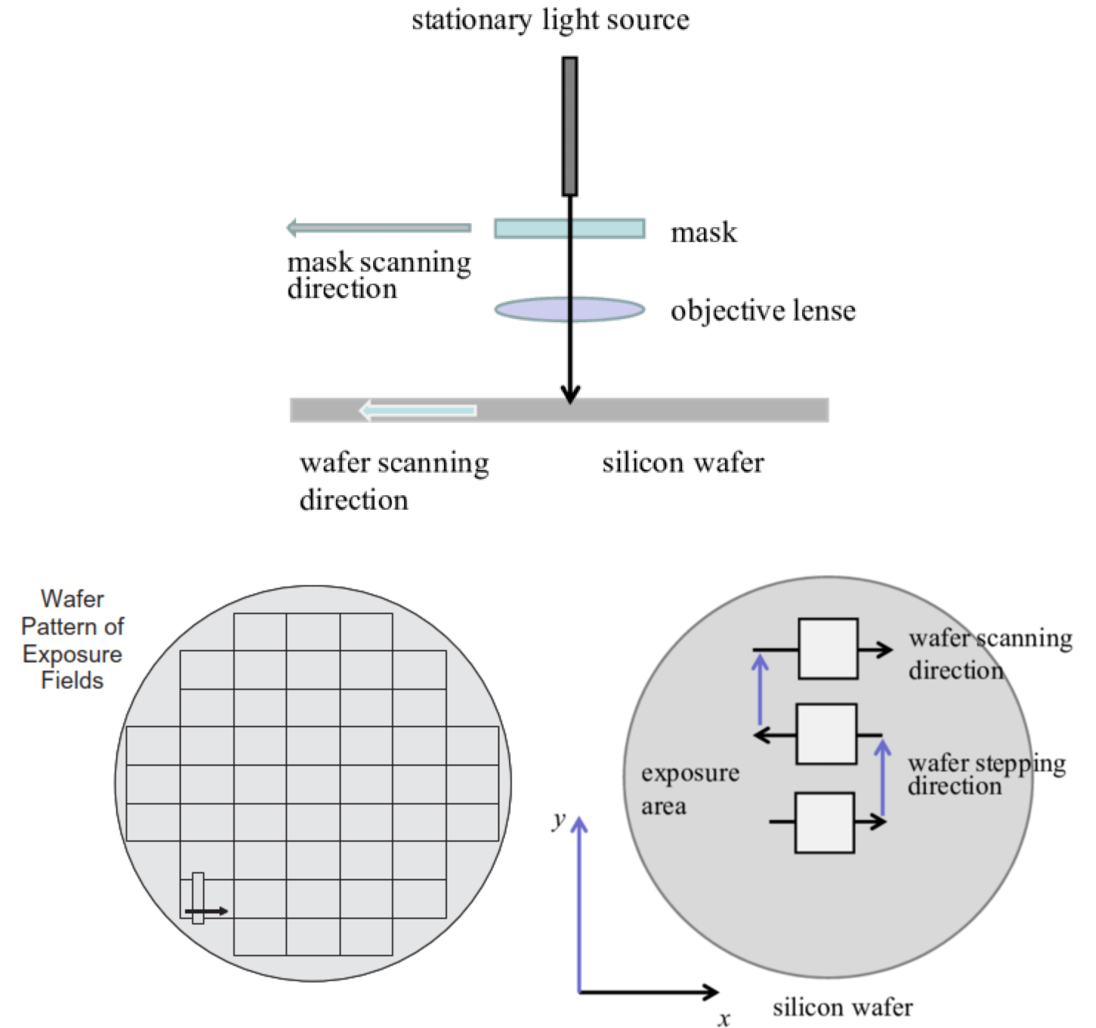
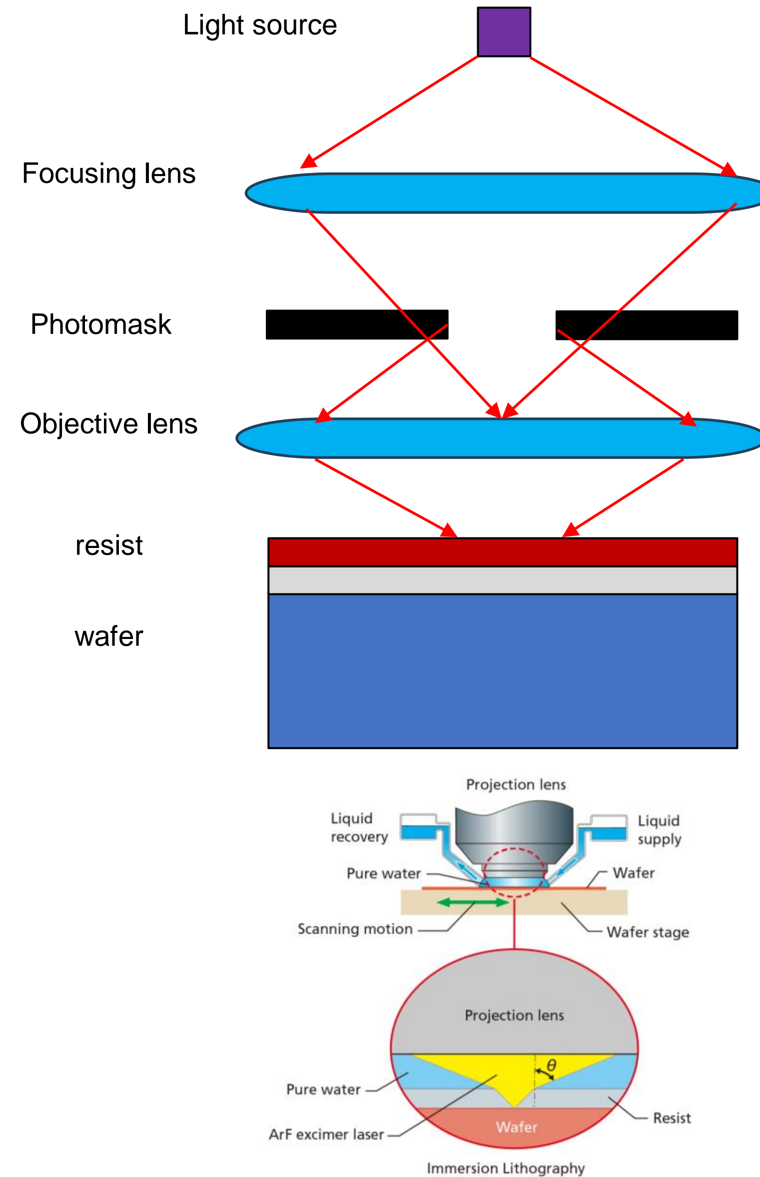
Mask/photolithography

- The patterning of the image is done using a step and scan procedure
- The light goes through a slit and the mask and wafer are scanned across the length of a field (mask pattern)
- Once a field is scanned, the wafer/mask are stepped along the orthogonal direction and the scanning is repeated
- Field size typically 26 x 33 mm^2, slit 25 x 8 mm^2



Mask/photolithography

- The projection method used by modern processes consist of a light source and a lens system
- Currently state-of-the-art photolithography [4] uses Deep Ultraviolet (DUV) light λ = 193 nm from an ArF excimer Laser
- The printing of nanometers feature size is possible using immersion lithography, where a media of higher refractive index (DI) is used between the lens and the wafer surface



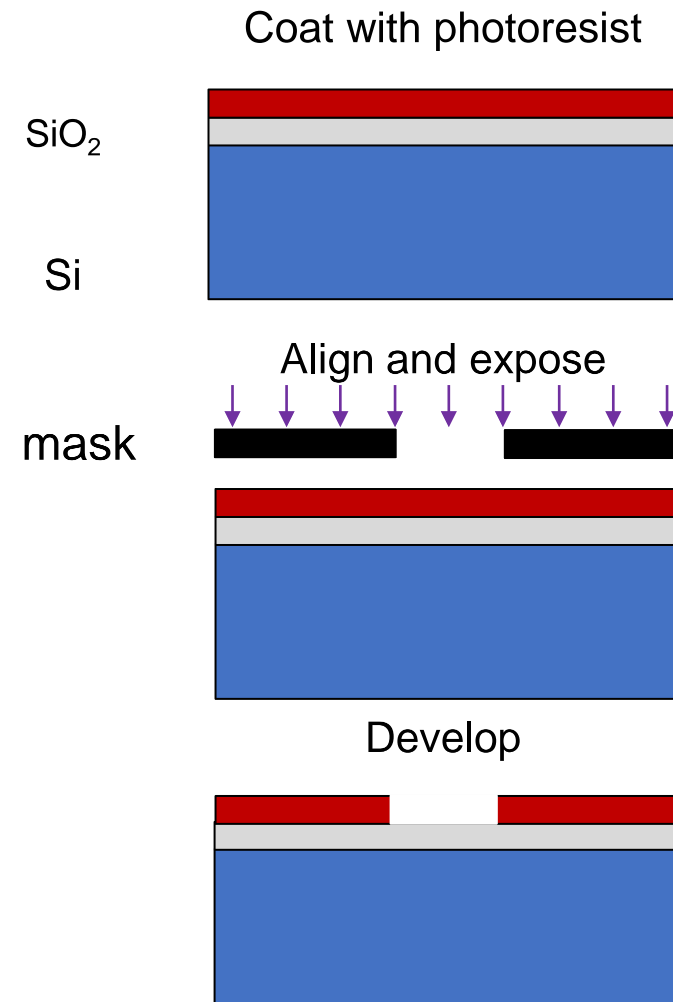
[4] B. Lin, *Optical lithography—present and future challenges*, C. R. Physique 7 (2006) 858–874

Resist development

- After photoresist deposition the mask is aligned and the process of exposure takes place

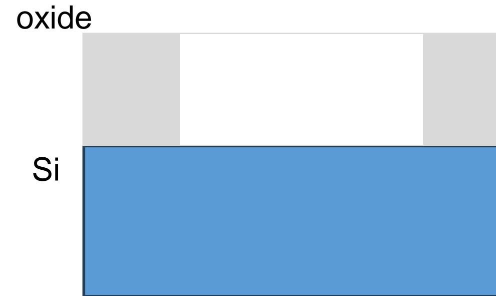
- Currently state-of-the-art photolithography uses Deep Ultraviolet (DUV) light λ = 193 nm ArF excimer Laser

- After the exposure, a post-bake to stabilize the film is performed , before the development

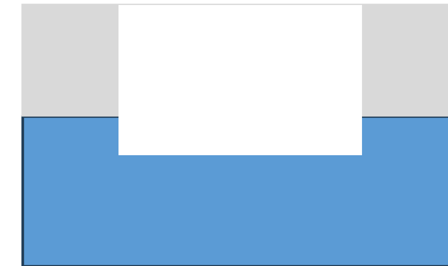


Etching

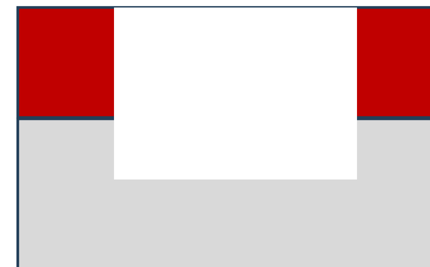
- After lithography, the process of etching usually follows
- Its purpose is to transfer a pattern onto the wafer, by removing material from some areas
- Either ‘wet’ or ‘dry’ etching is used
- **Selectivity**: etch rate ratio,e.g. $s=etch_{SiO2}/etch_{res}$ (>= 4-5)
- **Anisotropy**: A= $1 - e_h/e_v$
- Also high etch rates is required, 1 – 10 nm/s



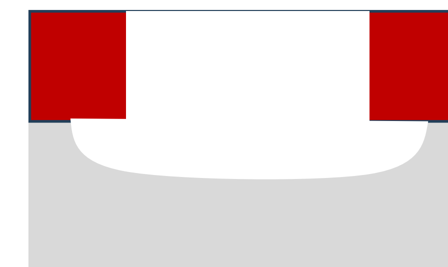
Good selectivity: only the material to be etched is removed



Poor selectivity: the material to be etched and the material below are etched



Good anisotropy: vertical sidewalls

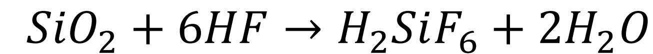


Poor anisotropy: round sidewalls

Etching

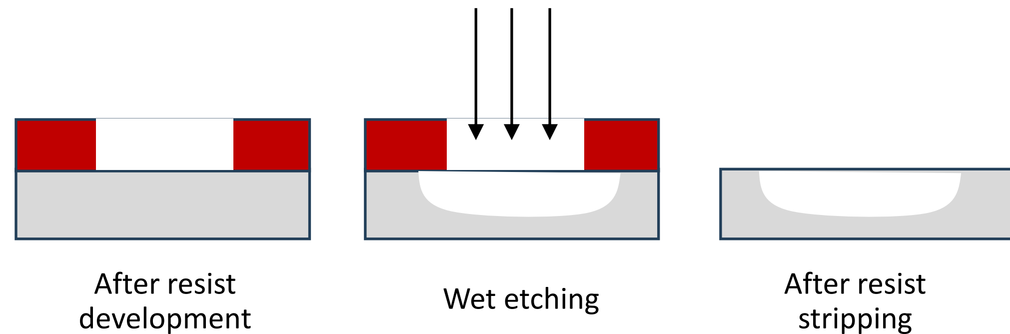
- Wet etching uses chemistry and might provide very high selectivity
- Plasma etching also uses reactive free radicals that chemically reacts with the material
- Usually poor anisotropy $A = 1 - e_h/e_v$
- Cheap and good selectivity but not suitable for precision etching, i.e. nanostructures

Wet etching example: Buffered HF etching of SiO_2



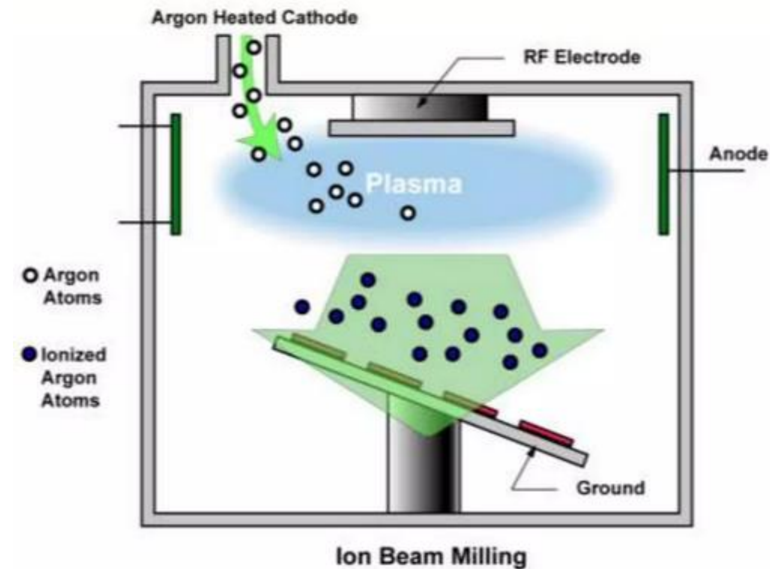
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

F displaces O atoms and dissolves oxide, no effect on Si: very high selectivity



Etching

- Sputter etching is a purely ‘physical’ process, i.e. no chemical reaction involved
- Anisotropy very high but poor selectivity
- The wafer is bombarded with chemically inert ions e.g. Ar^+
- Possible damage to the crystal (similar to ion implantation)



Plasma generates ion beam (Ar+) which are extracted and accelerated towards the sample

The ions sputter off atoms of the target

Low pressure (1e-4 Torr) to increase mean free path and provide line of sight travel to increase anisotropy

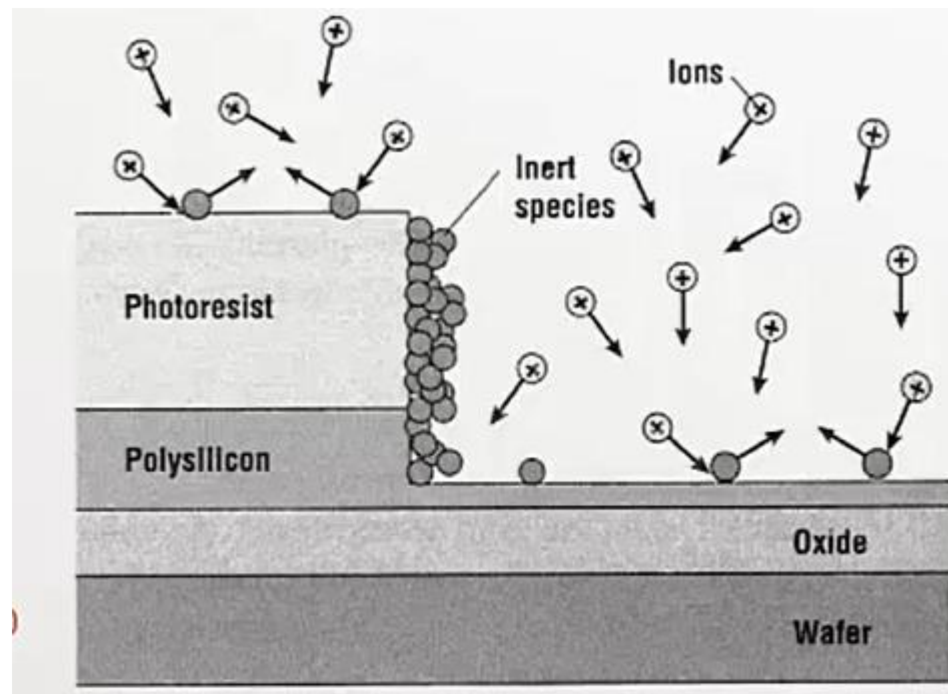
Etching

- Ideally one wants to combine **selectivity** using chemical reactions (like in wet etching) and **anisotropy** (like in sputter etching)
- Using Reactive Ion Etching (RIE) it is possible to achieve both high selectivity and anisotropy
- RIE uses ions bombardment to enhance the chemical process
- Chemical etching happens where the ions strike, leading to high selectivity and anisotropy

	High selectivity	**Low selectivity**
High anisotropy	Reactive Ion etch (RIE)	Sputter etch
Low anisotropy	Wet/plasma etch	

Etching

- Reactive-ion etching (RIE) uses chemistry and ions to simultaneously provide high selectivity and anisotropy
- The wafer is negatively biased
- Positive ions are accelerated towards its surface
- A plasma creates reactive species which diffuse towards the wafer
- The exposed parts of the wafer react and are etched
- Etch byproducts may deposit onto the surface and provide sidewall passivation as they do not react with the reactive species
- Unique RIE recipe for a specific etching process



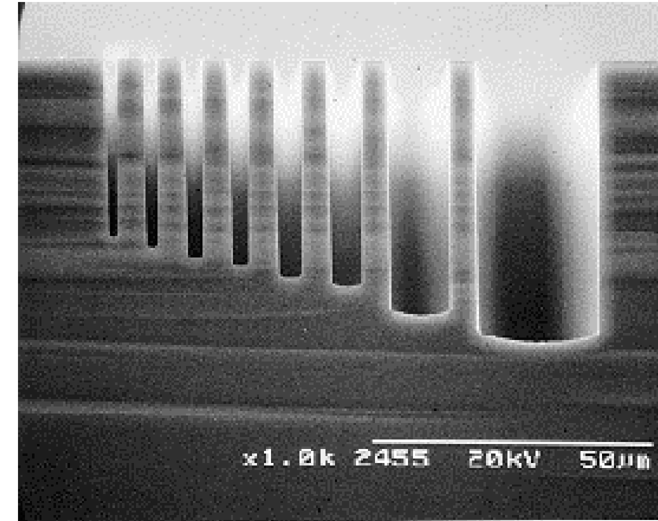
Polysilicon
CF_4/O_2

SiO2
CF_4/H_2

Resist
O_2

Etching

- Issues with RIE etching:
  - Ion damage to wafer
  - Etch loading (the etch rate changes depending on the mask pattern, i.e. Si with bigger aperture or narrow trenches etch more slowly)

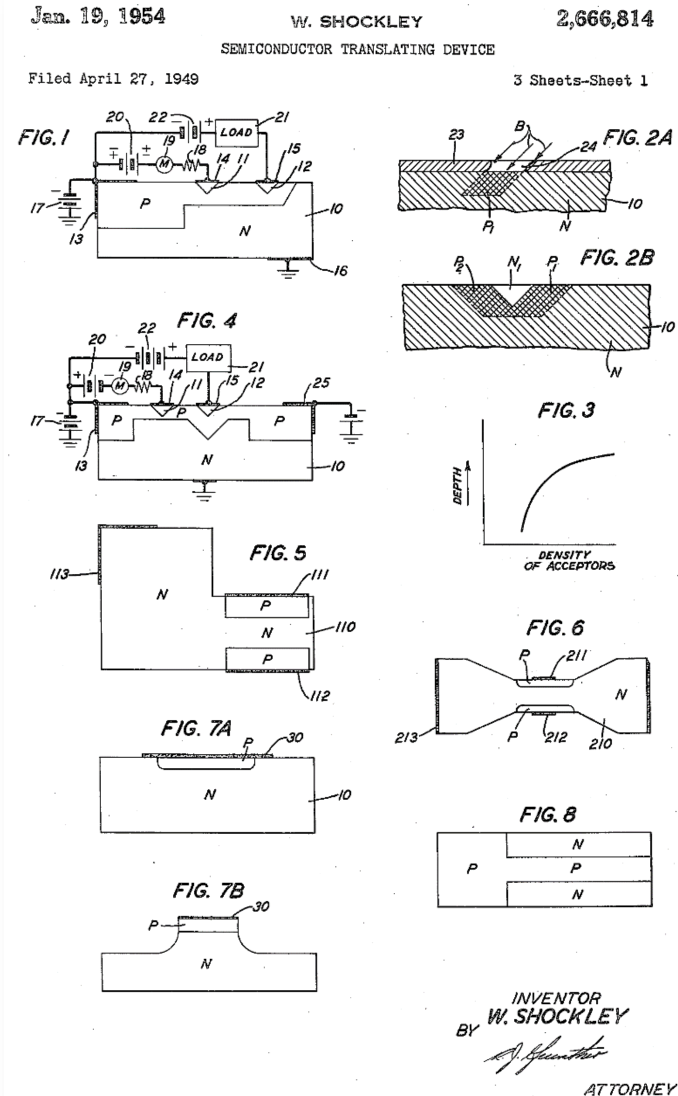


A wide trench allows fluorine radicals to reach the bottom more easily, hence fast etch rate compared to the narrow trench

Source: https://www.samcointl.com/opto/

Ion Implantation

- Technique to introduce atoms of dopants into a semiconductor material and create regions of different electrical characteristics
- Historically proposed by Shockley in 1949, became common in the 70's
- Ionized gas ions are accelerated by strong electric field and injected into a target wafer (a few nm to a few µm depth). Ion implanters spin-off from particle accelerator technology



...the layer is formed by bombardment of one face of the N-type body with nuclear particles and the N-type zones in the layer are produced by masking the surface areas of the layer from the bombarding particles.

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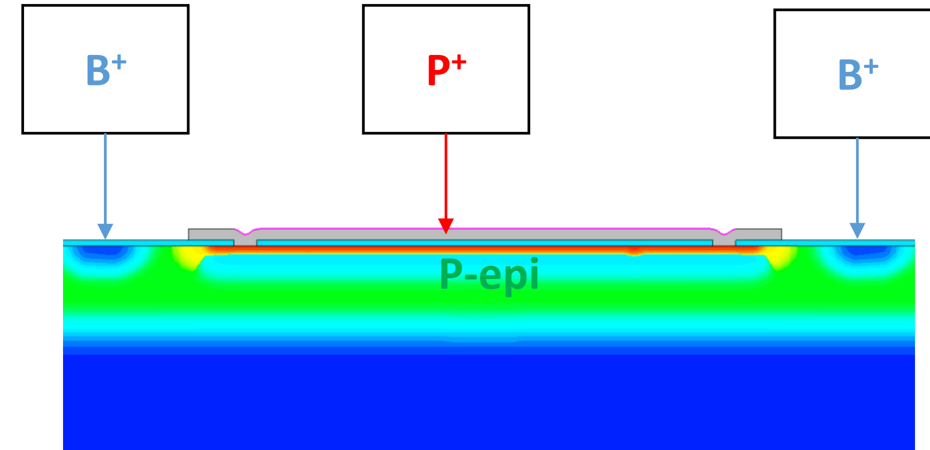
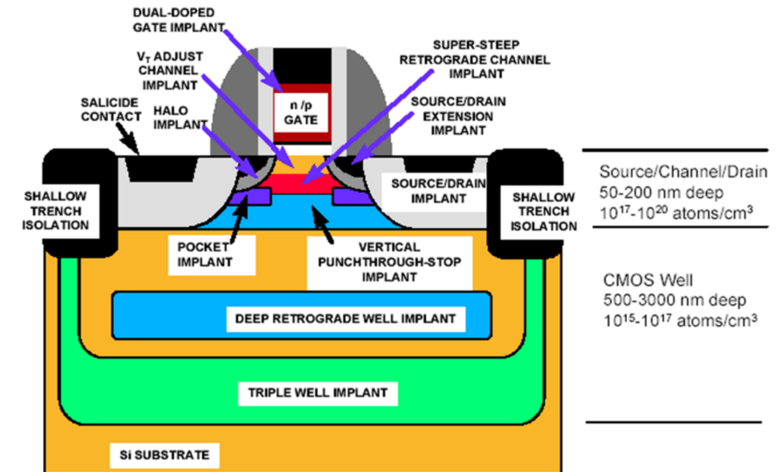
Ion Implantation

Pros

- Precise control of dose and depth profile, complex profiles
- RT process (can use photoresist as mask)
- Wide selection of masking materials e.g. photoresist, oxide, poly-Si, metal
- Excellent dose uniformity across wafers
- Little lateral dopant diffusion, important for small devices



4 implantations process, 1 metal layer

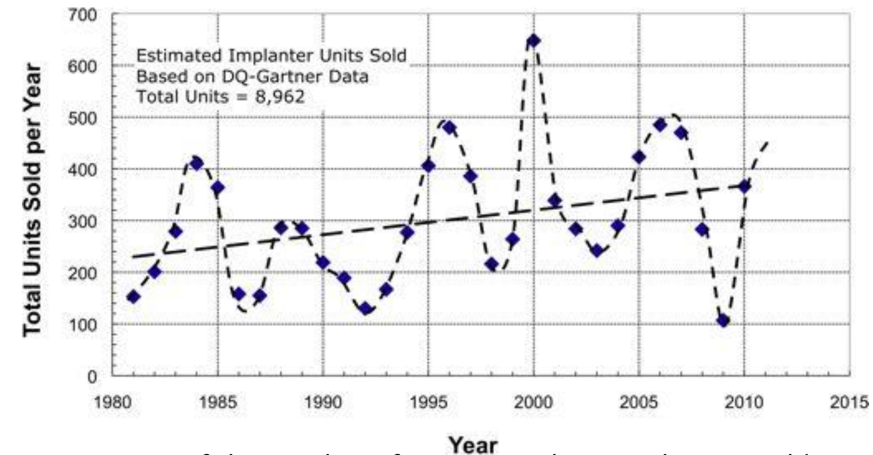


>10 implantations process

Ion Implantation

Cons

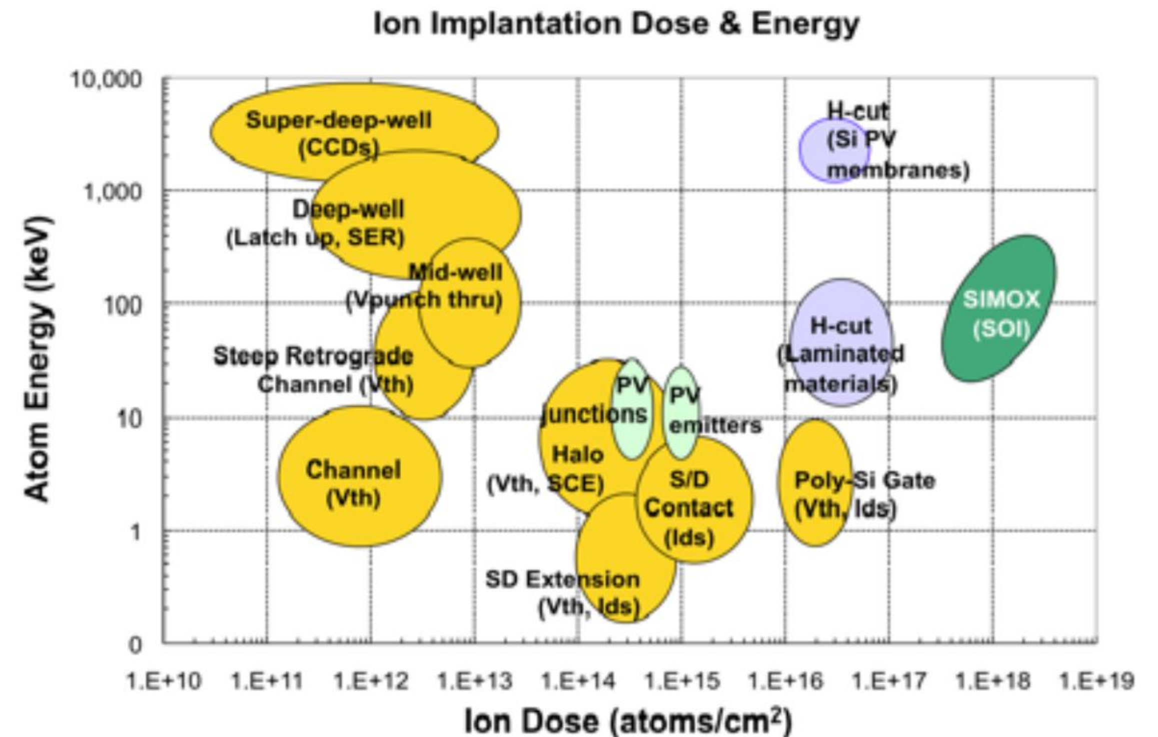
- Equipment big and expensive (> 1M$)
- Radiation damage: reticle damage due to implantation not always possible to correct
- Difficult to obtain very shallow and very deep doping
- Masks material can be scattered into the wafer, creating impurities and defects



Estimates of the number of commercial ion implanters sold per year, mainly for IC fabrication, showing the '5 year cycle'

Ion Implantation

- Ions used: As, B, P, In, O, Ar
- Energy: 1 - ~1000's keV
- Flux: $10^{12} – 10^{14}$ cm^{-2} s^{-1}
- Dose: $10^{11} – 10^{18}$ cm^{-2}
- Uniformity: ± 1% across 12'' wafers
- Absolute dose accuracy: ± 10 -15 %
- Temperature: RT



Dose and atom energy regions for CMOS transistor doping (gold), high dose hydrogen implants for Si layer splitting (lavender), and direct implantation of oxygen to form Silicon-on-Insulator (SOI) wafers (green).

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Ion Implantation tools

Typical ion implanter for semiconductor process consists of several elements

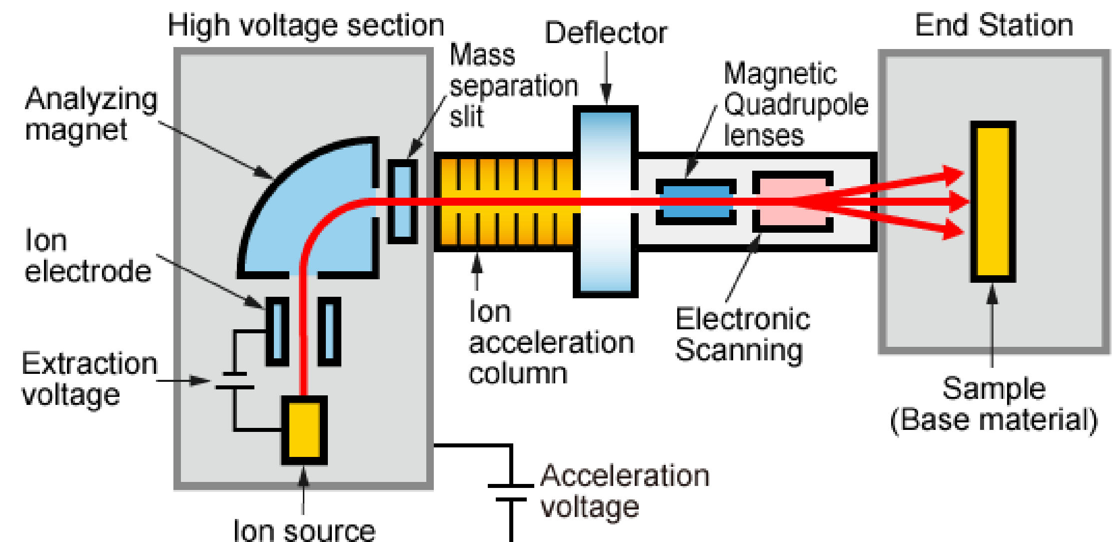
1: Ion source

2: Analyzing Magnetic

3: Ion Accelerator

4: Beam manipulating system

5: End station



Ion Implantation doping profile

- **Adiabatic approximation** : Scattering of ions with target is described using two separate collision processes:

- S_n collisions with nuclei (energy loss and geometry of trajectory)

- S_e collisions with electrons (energy loss only).

$$S = \left(-\frac{dE}{dx}\right)_{nuclear} + \left(-\frac{dE}{dx}\right)_{electronic} = S_n + S_e$$

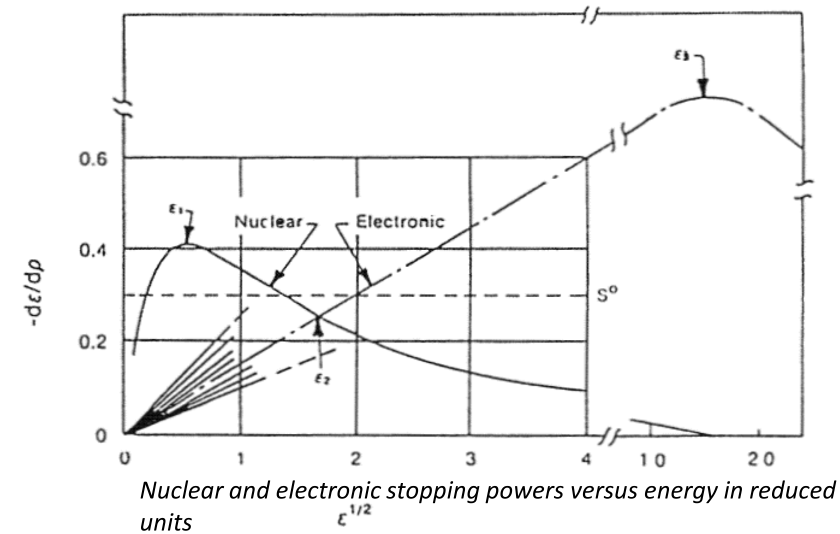
S_n screened potential classical two-body scattering Binary Collision Approximation BCA)

S_e interactions of ion with target electrons (Lindhard's Bethe-Bloch)

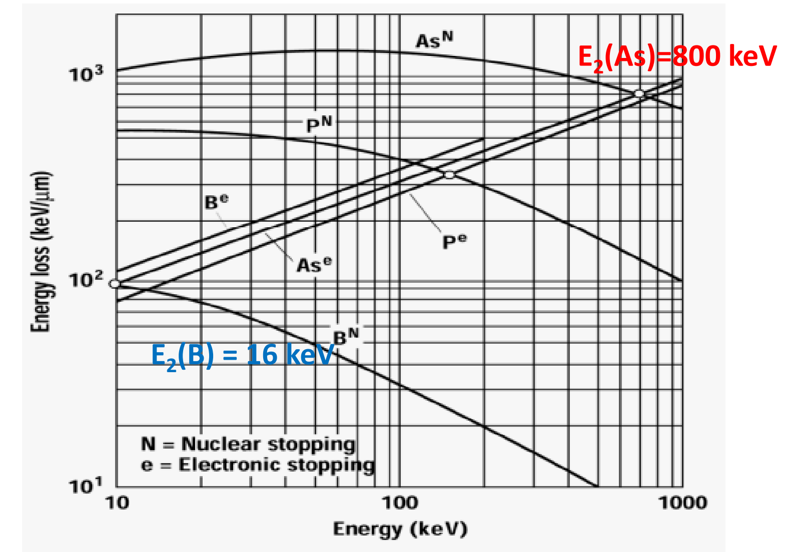
Ion Implantation doping profile

- At **low energy,** nuclear collisions dominate: at the end of its range the ion has low energy, S_n dominates leading to more crystalline damage

- At **high energy**, electronic collisions dominate, from scattering of electrons ~ Ohm's law



Nuclear and electronic stopping powers versus energy in reduced units $\varepsilon^{1/2}$



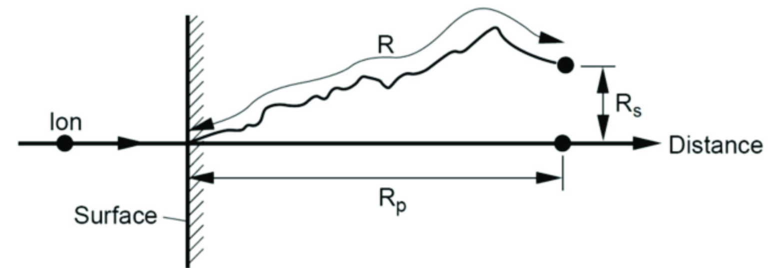
Ion Implantation doping profile

- From $\frac{dE}{dx}$,the total energy stopping power, one can estimate the average ion range

R: range

R_p: projected range along axes of incident ion, with straggle ΔR_p

R_s perpendicular distance



$$\frac{dE}{dx} = \left(\frac{dE}{dx}\right)_n + \left(\frac{dE}{dx}\right)_e$$

$$R = \int_0^E \frac{dE}{-\frac{dE}{dx}}$$

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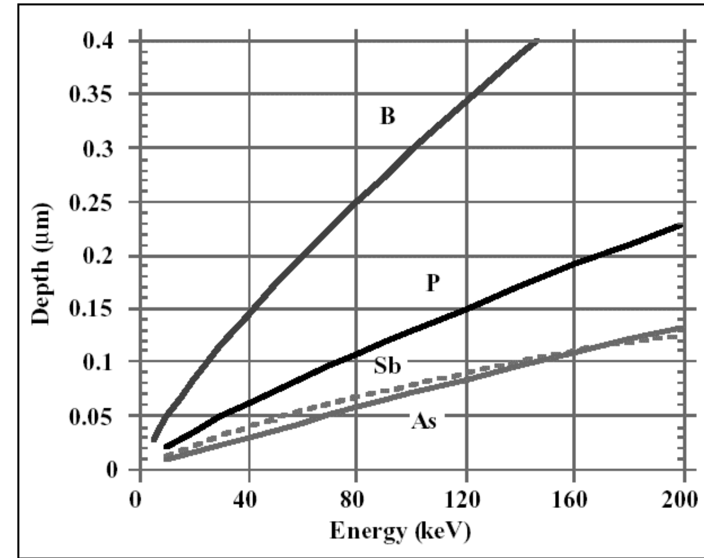
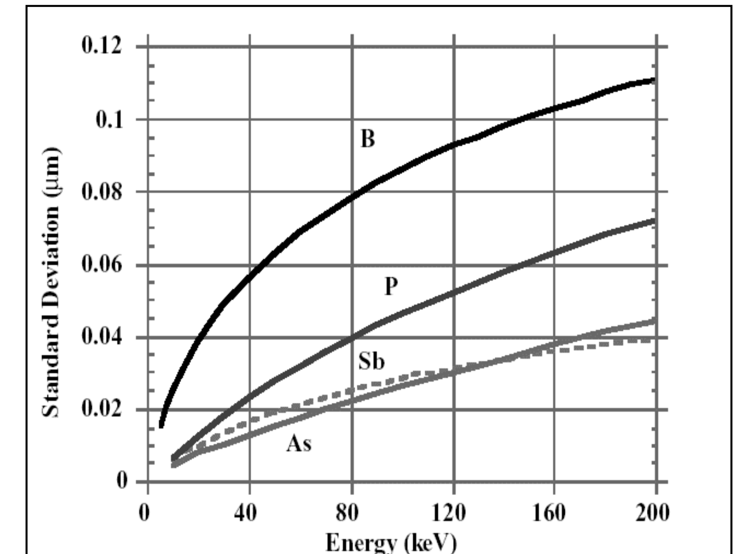
Ion Implantation doping profile

- Projected range Rp and Straggle ΔRp for common dopants
- Transverse spread increases with R_p ($R = (1 + M_2/3M_1)Rp$
- limiting factor on lower limit of mask opening, which affects maximum device density



Projected range R_p

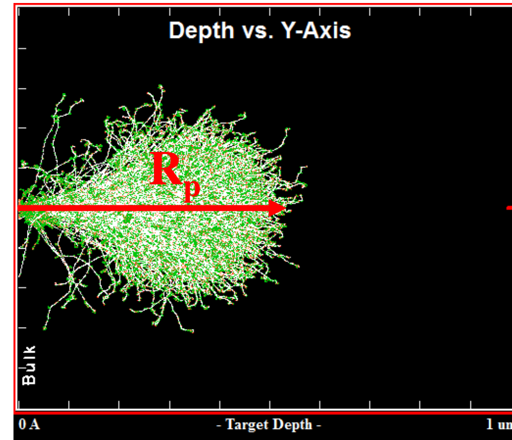


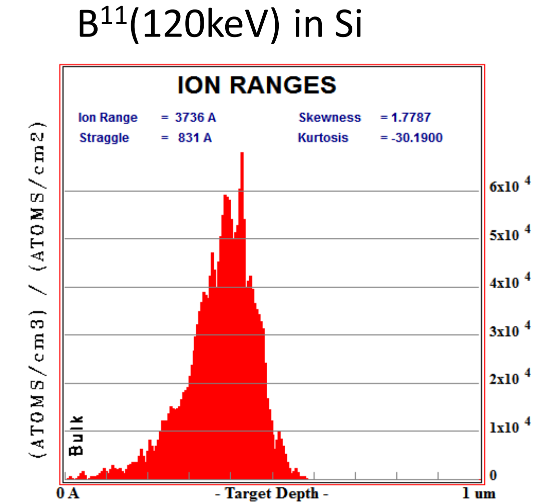
Straggle ΔR_p

Ion Implantation doping profile

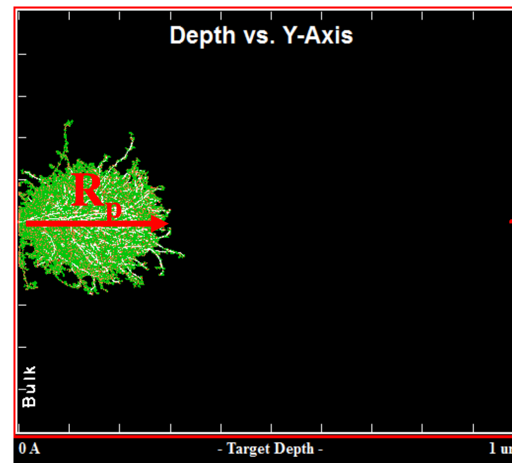
- Example of MC (>5000 runs) ion range simulations (SRIM*) of B^{11} and P^{31} implanted in amorphous Si
- No annealing, i.e. no dopants activation, no thermal diffusion

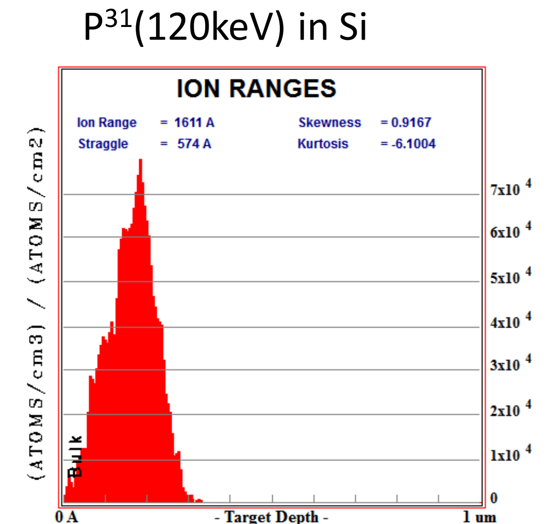
B^{11}(120keV) in Si





P^{31}(120keV) in Si

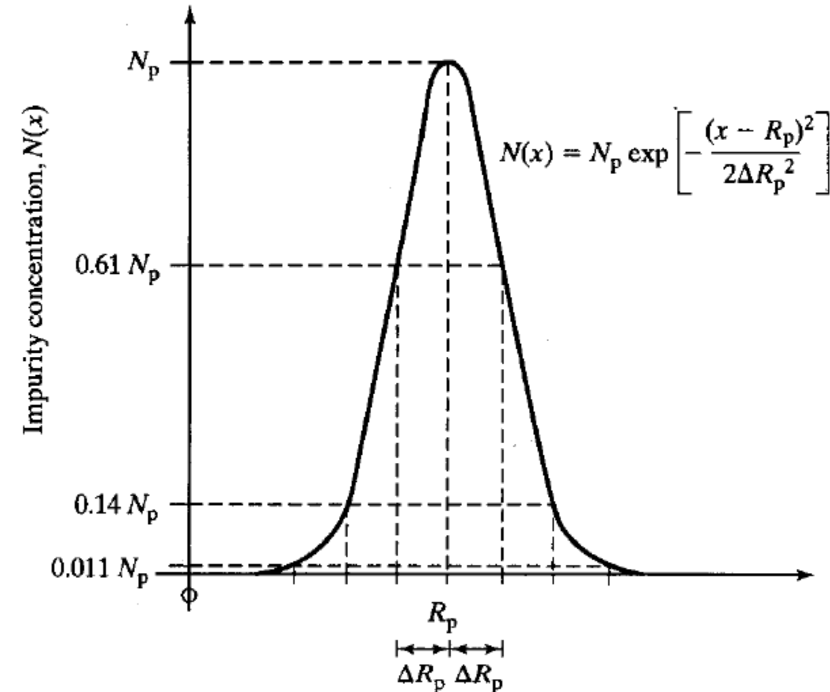




* http://srim.org/

Ion Implantation doping profile

- The range distribution of implanted impurities is described, as a first approximation, by a **symmetrical Gaussian distribution** (2 moments: R_p : projected range, ΔR_p : straggle)



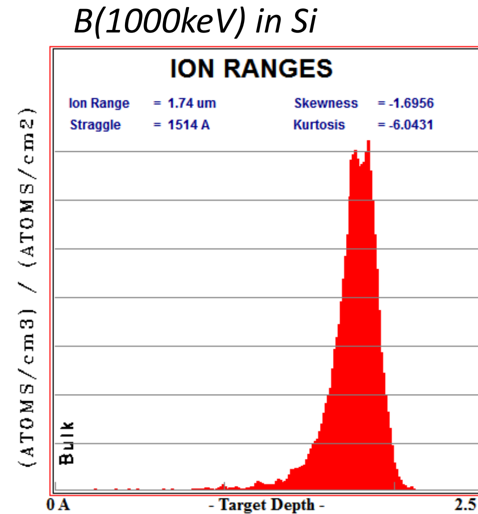
$$N(x) = N_{pk} e^{-\frac{(x-R_p)^2}{2(\Delta R_p)^2}} = \frac{Q}{\sqrt{2\pi}\Delta R_p} e^{-\frac{(x-R_p)^2}{2(\Delta R_p)^2}}$$

$$Dose = \int_0^L N(x) = Q = \sqrt{2\pi}\Delta R_p N_{pk} [atoms \cdot cm^{-2}]$$

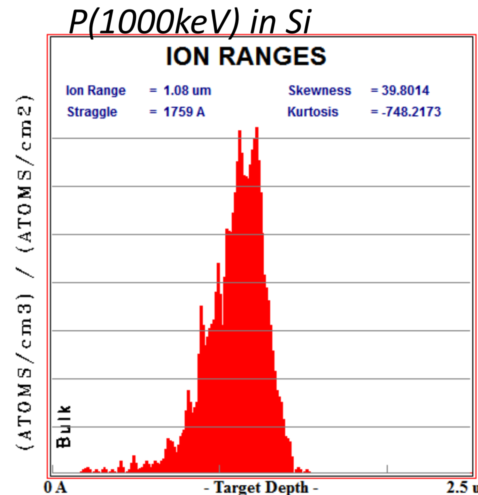
Ion Implantation doping profile

- Higher moments are needed to describe realistic profiles:
  - **skewness** (γ), describing asymmetry of distribution
  - **kurtosis** (β), describing peak sharpness of the profile

B(1000keV) in Si



P(1000keV) in Si



$$Q = m_0 = \int_{-\infty}^{+\infty} N(x)dx$$

$$R_p = m_1 = \int_{-\infty}^{+\infty} xN(x)dx$$

$$\Delta R_p = m_2 = \int_{-\infty}^{+\infty} (x - R_p)^2 N(x)dx$$

$$\gamma = m_3 = \frac{1}{\Delta R_p{}^3} \int_{-\infty}^{+\infty} (x - R_p)^3 N(x)dx$$

$$\beta = m_4 = \frac{1}{\Delta R_p{}^4} \int_{-\infty}^{+\infty} (x - R_p)^4 N(x)dx$$

Ion Implantation doping profile

- Analytical description of doping profiles can be obtained from Pearson distribution
- Coefficients of Pearson's equation are related to the four moments
- Explicit formula for the implanted profile can be obtained

$$\frac{df}{dx} = \frac{(x-a)f}{b_0 + b_1 x + b_2 x^2}$$

Pearson distribution function defined as DE solution

$$a = b_1 = -\frac{\gamma \Delta R_p^2 (\beta + 3)}{10\beta - 12\gamma^2 - 18}$$

$$b_0 = -\frac{\Delta R_p^4 (3\gamma^2 - 4\beta)}{10\beta - 12\gamma^2 - 18}$$

$$b_2 = -\frac{6 + 3\gamma^2 - 2\beta}{10\beta - 12\gamma^2 - 18}$$

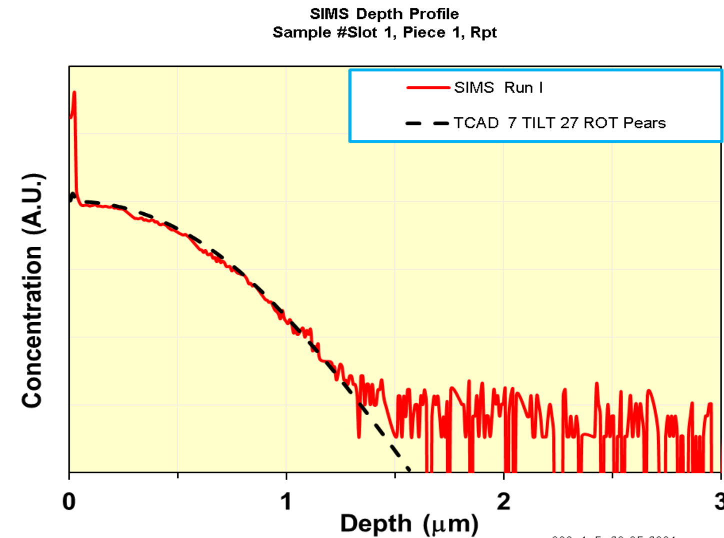
$$C(x) = C_o \exp\left\{\frac{1}{2b_2}\ln(b_2 x^2 + b_1 x + b_0) - \frac{2b_2 a + b_1}{b_2\sqrt{4b_2 b_0 - b_1^2}} \arctan\left(\frac{2b_2 x + b_1}{\sqrt{4b_2 b_0 - b_1^2}}\right)\right\}$$

Generic profile formula from Pearson distribution

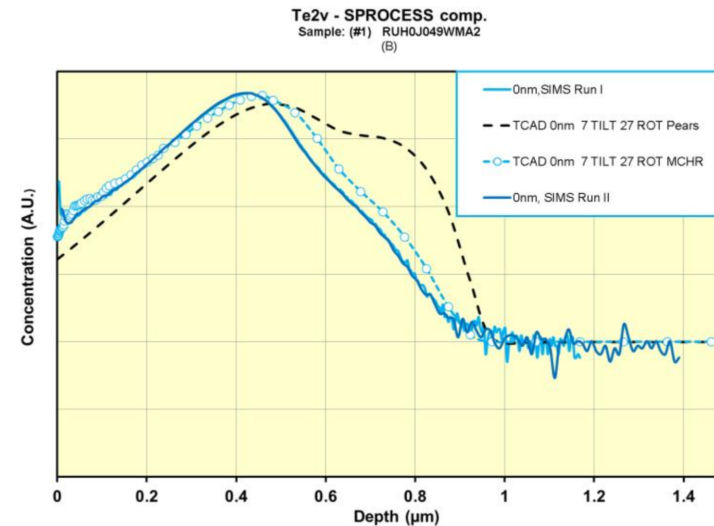
A. F. Tasch et al., "An Improved Approach to Accurately Model Shallow B and BF 2 Implants in Silicon," Journal of the Electrochemical Society, vol. 136, no. 3, pp. 810–814, 1989,

Ion Implantation doping profile

- Analytical doping profiles description reasonably accurate for heavy ions
- Lighter ions more accurately described using MC (crystal orientation depending)



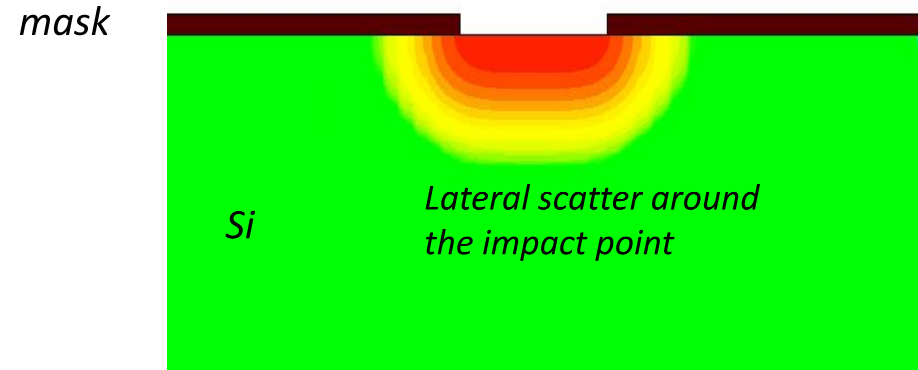
SIMS and Pearson IV distribution – 31P



SIMS, Pearson IV distribution and MC run – 11B

Ion Implantation masking

- Purpose of the mask is to Implant only in certain parts of the wafer, using a suitably thick mask (i.e. that its R_p lies within the mask material)
- The thickness of the mask should be large enough that the tail of the implant profile in the silicon should not significantly alter the doping concentration (C_B)



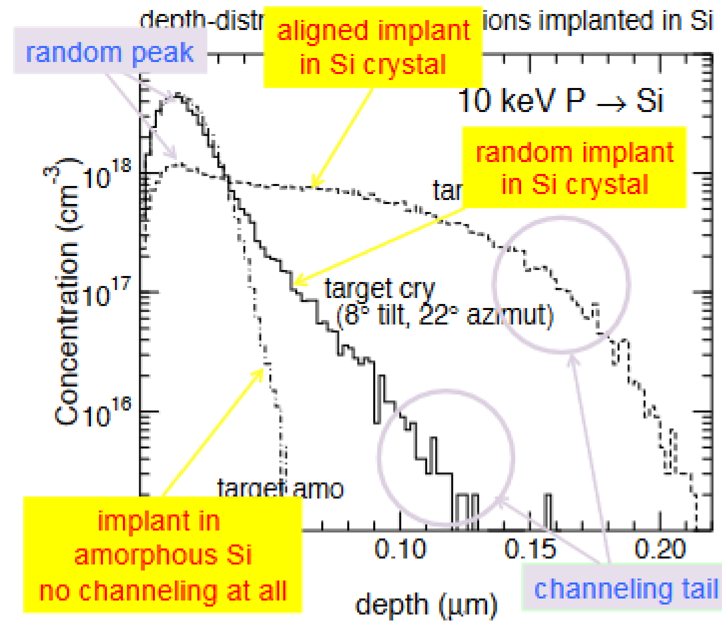
MATERIAL THICKNESS NEEDED TO MASK

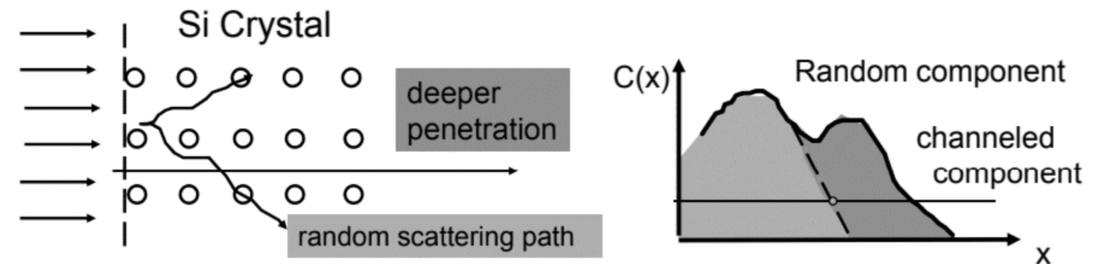
At 200 KeV	Poly	SiO2	Si3N4	Al	Resist
Boron	0.9µm	1.0µm	0.61µm	0.9µm	1.0µm
Phosphorous	0.7µm	0.6µm	0.42µm	0.55µm	0.8µm
Arsenic	0.3µm	0.3µm	0.18µm	0.28µm	0.35µm
Antimony	0.2µm	0.2µm	0.16µm	0.18µm	0.25µm
At 100 KeV	**Poly**	**SiO2**	**Si3N4**	**Al**	**Resist**
Boron	0.65µm	0.7µm	0.42µm	0.7µm	0.7µm
Phosphorous	0.4µm	0.36µm	0.25µm	0.3µm	0.45µm
Arsenic	0.18µm	0.16µm	0.1µm	0.16µm	0.20µm
Antimony	0.12µm	0.11µm	0.07µm	0.10µm	0.14µm

FOR 0.0001% TRANSMISSION

Ion Implantation channeling

- During ions implantation in a periodic structure, directional effects due to nuclear scattering might confine the ions into regions minimizing interactions along the path.
- Channelling: Average penetration depth is larger, affecting the final doping profile





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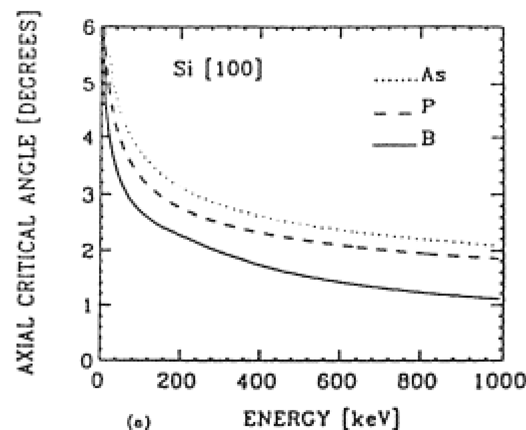
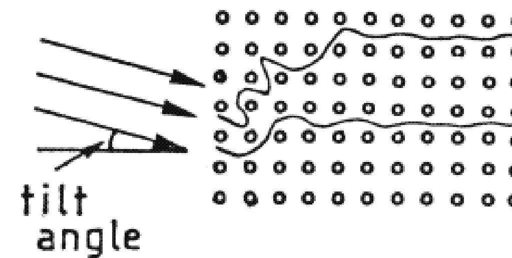
Ion Implantation channeling

To minimize channelling:

- **pre-amorphization** of the wafer via implantation

- the wafer is **tilted** by some degrees with respect to ion beam: the value of the critical angle below which there is channelling depends on crystal orientation and energy of the ion. In practice a tilting angle of **7** degrees is used

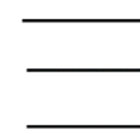


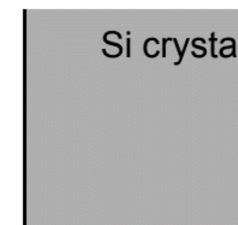


Step 1
High dose Si+ implantation to covert surface layer into amorphous Si

Si^+

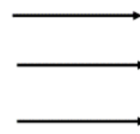
1 E15/cm^2

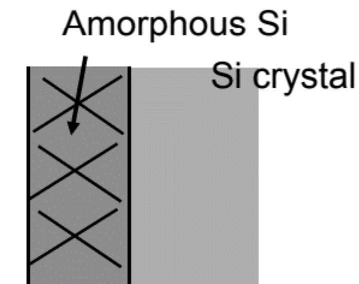




Step 2
Implantation of desired dopant into amorphous surface layer

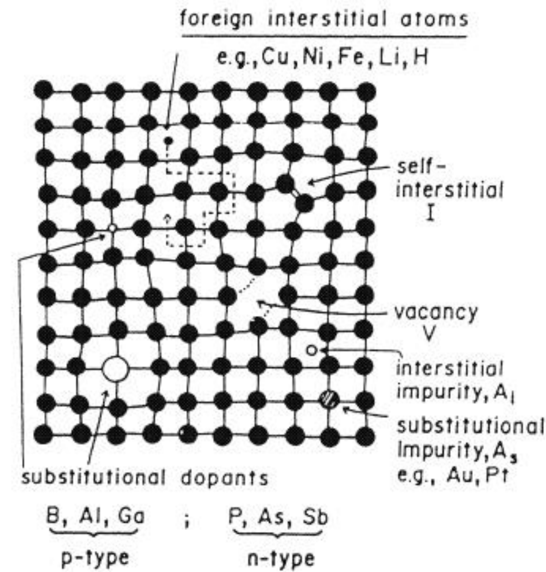
B^+

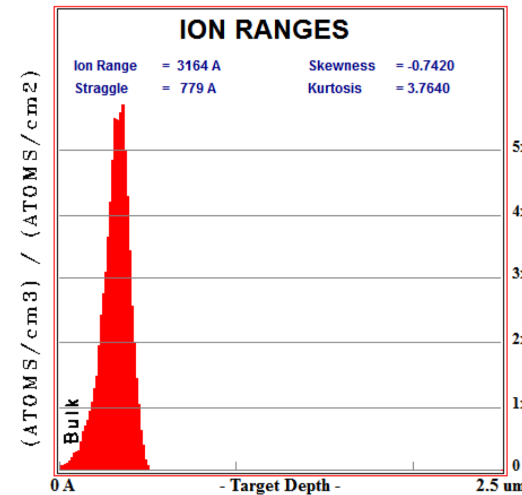


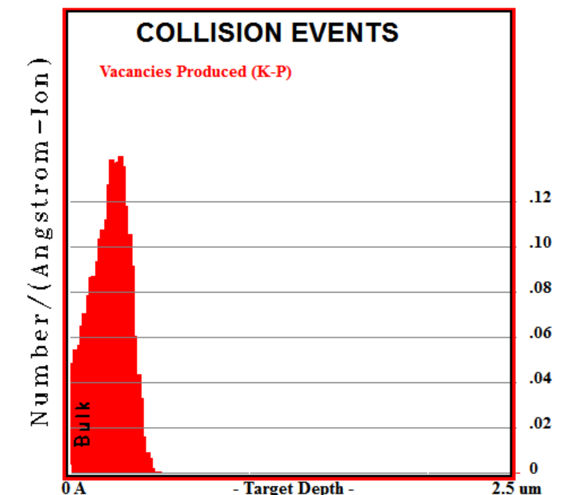


Ion Implantation damage and annealing

- Ion implantation creates defects in the target crystal, by displacing atoms from their regular lattice sites (see **radiation damage lectures**)
- The elementary radiation defect consists of Frenkel defect, i.e. displaced atom (interstitial) plus the related vacancy.
- More complex defects form as a result of accumulation and clustering of interstitials and vacancies (divacancies V-V, vacancy impurities, like V-O, As-I…)

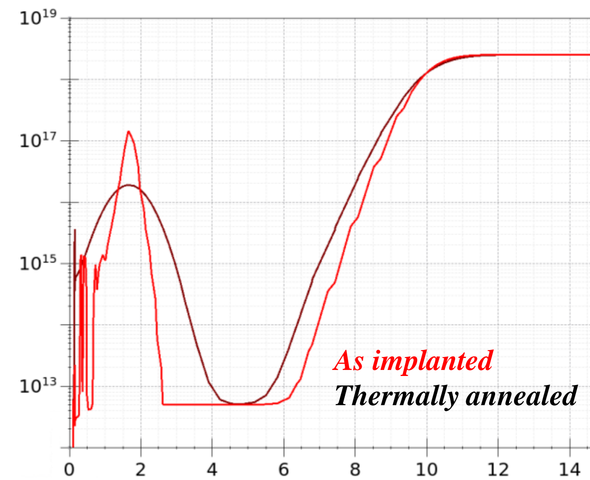




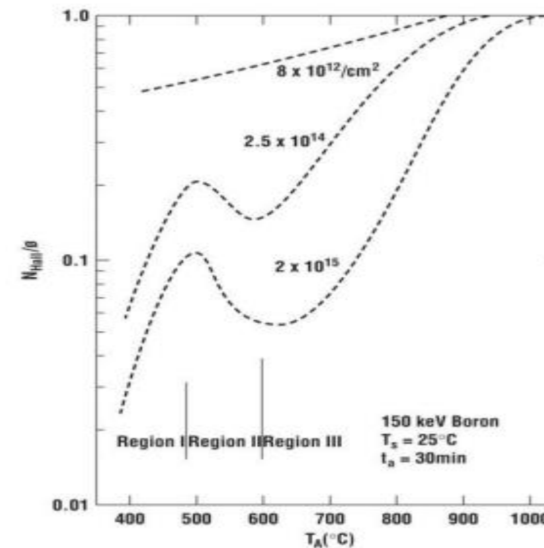


Ion Implantation damage and annealing

- After the implantation process, a thermal treatment is required to electrically activate the dopant (i.e. to have them moved to substitutional positions) and to restore the crystalline order of the semiconductor
- Annealing at high temperature (~1000°C) could result in perfect crystal, but leads to dopant diffusion. Particularly serious issue in modern technologies, where very shallow junctions are used



An example of doping profile from ^{11}B implantation in <100> Si, as implanted and after thermal annealing



Isochronal annealing of boron. The ratio of the free-carrier to dose (fraction of boron atoms located in substitutional lattice points) is plotted versus the anneal temperature for three doses of boron.

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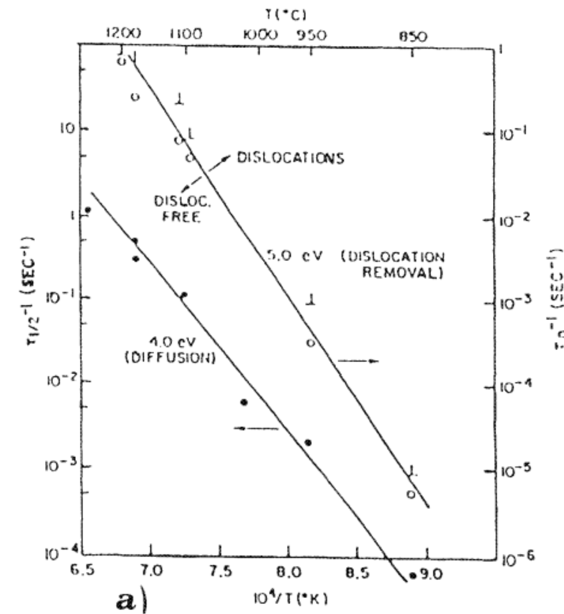
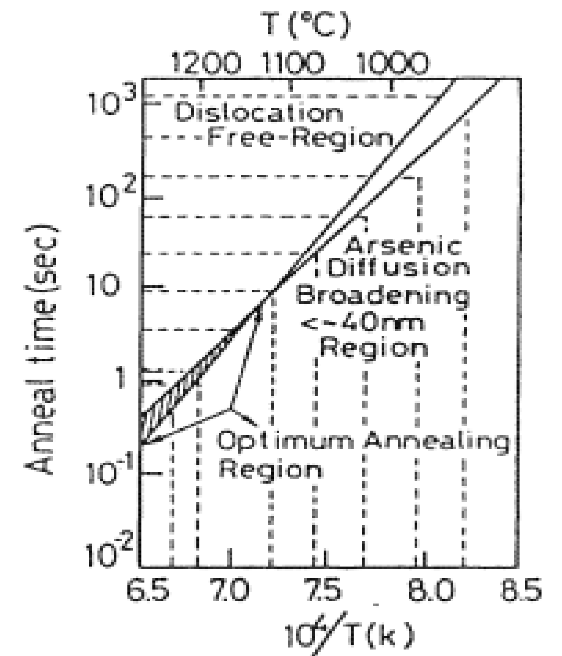
Ion Implantation damage and annealing

- Activation energy for removal of point defects (V and I) usually higher than that of impurity diffusion.

- Different slopes in Arrhenius plots allow to use high temperature to enhance annealing and depress diffusivity: Rapid Thermal Annealing (**RTA**)

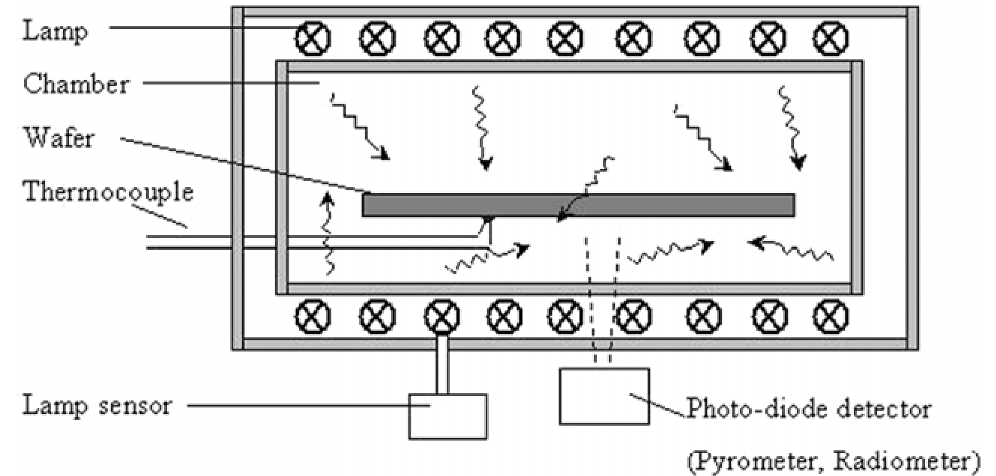


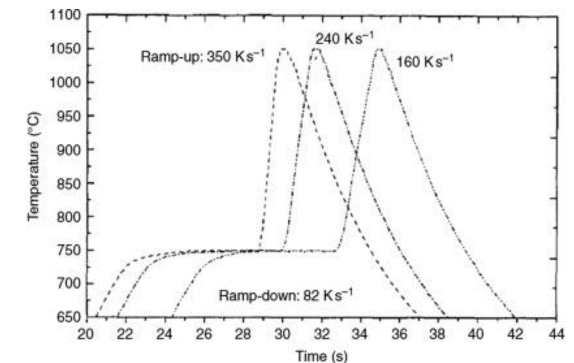
Dislocation removal rate in As implanted Si and As diffusivity vs. 1/T



Ion Implantation damage and annealing

- Rapid thermal annealing of wafers (**RTA**) optimizes the defects suppression, whilst minimizing dopants diffusion
- Wafers are rapidly heated by lamps (10's kW) to 1000 C for 1 – 20 secs max
- Various methods to measure the wafer temperature (optical, acoustic)



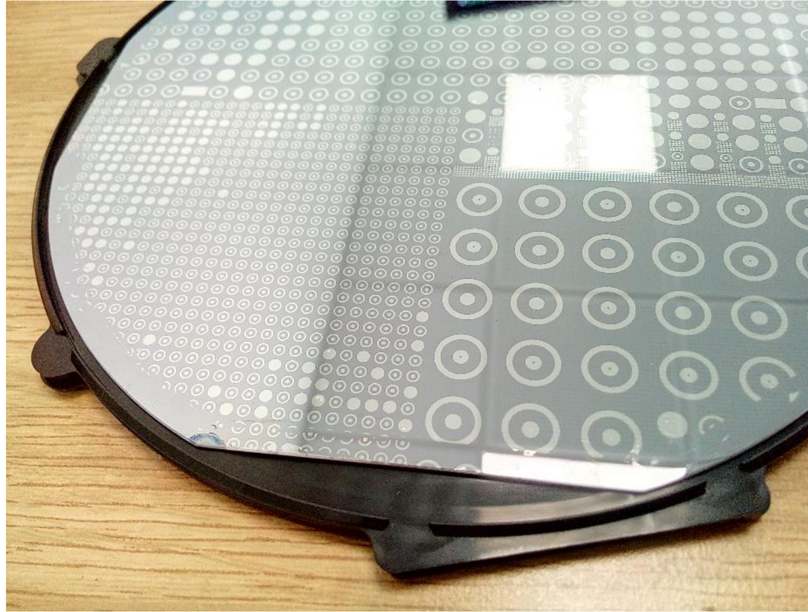


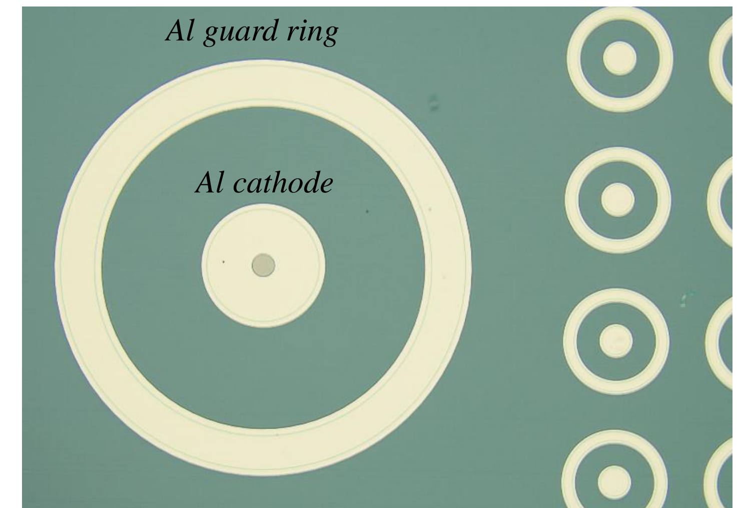
https://photonexport.com/rapid-thermal-processing/

Metallization

- Once devices have been fabricated in the wafer (Front End of Line), metal layers are deposited to form the conductive connections
- Modern technologies moved from Al to Cu to reduce resistivity in interconnect in Back End of Line (BEOL). This is a more complex process (Dual Damascene process) than sputtering

Schottky diode on P-type Si wafer

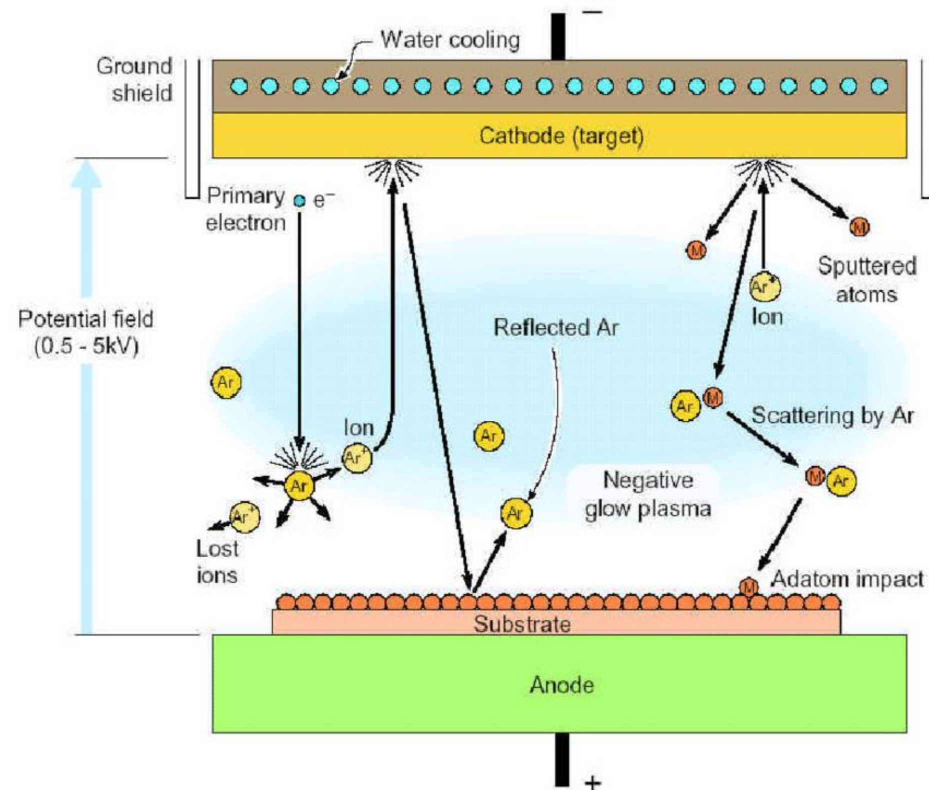




Metallization

- Sputtering (**PVD**, Physical Vapor Deposition) is one of the most common method to deposit thin film of metal

- Good step coverage obtained by reducing the mean free path of sputtered atoms (increasing Ar ions, magnetron sputtering)
  Sputtering also used to clean wafer before deposition, by Ar^+ etching



Cathode (target -) is the material to deposit, generally cooled

An inert gas (Ar) is ionized, accelerated and collides with the target. Ejected atoms have energies ~ 10's eV

Some atoms sputters off and, after scattered paths, land and deposit onto the wafer (+)

Appendix :The Deal-Grove oxidation model

- The Deal Grove Model is a simple kinetic model for oxide thermal growth, wet and dry
- Developed by Andy Grove (Intel's CEO) and Bruce Deal in the 60's

JOURNAL OF APPLIED PHYSICS VOLUME 36, NUMBER 12 DECEMBER 1965

General Relationship for the Thermal Oxidation of Silicon

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(Received 10 May 1965; in final form 9 September 1965)

The thermal-oxidation kinetics of silicon are examined in detail. Based on a simple model of oxidation which takes into account the reactions occurring at the two boundaries of the oxide layer as well as the diffusion process, the general relationship $x_0^2+Ax_0=B(t+\tau)$ is derived. This relationship is shown to be in excellent agreement with oxidation data obtained over a wide range of temperature (700°–1300°C), partial pressure (0.1–1.0 atm) and oxide thickness (300–20 000 Å) for both oxygen and water oxidants. The parameters A, B, and τ are shown to be related to the physico-chemical constants of the oxidation reaction in the predicted manner. Such detailed analysis also leads to further information regarding the nature of the transported species as well as space-charge effects on the initial phase of oxidation.

1. INTRODUCTION

OWING to its great importance in planar silicon-device technology, the formation of silicon dioxide layers by thermal oxidation of single-crystal silicon has been studied very extensively in the past several years.[1–15] Now, with the availability of large amounts of experimental data, it appears that there is much contradiction and many peculiarities in the store of knowledge of silicon oxidation. For instance, reported activation energies of rate constants vary between 27 and 100 kcal/mole for oxidation in dry oxygen; pressure dependence of rate constants has been reported as linear as well as logarithmic. While most of the data on silicon oxidation have been evaluated using the parabolic rate law, certain authors have taken recourse to using empirical power-law dependence,[14] $x_0^n=kt$, where both n and k were complex functions of temperature, pressure, and oxide thickness.

The problems associated with the latter approach can be illustrated by considering Figs 1 and 2. These figures contain a summary of data obtained in these laboratories which are in good general agreement with the corresponding data of Fuller and Strieter[14] and of Evitts, Cooper, and Flaschen.[13] (The experimental methods are dealt with in detail later.) The plots are logarithm of oxide thickness vs the logarithm of oxidation time for dry and wet oxygen (95°C H_2O) at various temperatures. The slope of the lines corresponds to the exponent n in the above power law. These values are indicated at the limiting position of some of the curves. In the case of wet oxygen (Fig. 1), n ranges from 2 for thicker oxides at 1200°C to 1 for the thinner oxide region of the 920°C data. However, for dry oxygen (Fig. 2), the value of n at 1200° approaches 2 as the oxide thickness increases above 1.0 μ; but at lower temperatures and oxide thicknesses the value of n decreases only to about 1.5 and then appears to increase again. Obviously the data cannot be represented by a simple power law.

Most of the previous theoretical treatments of the kinetics of the oxidation of metals emphasize only two limiting types of oxidation mechanisms.[16] In one, the

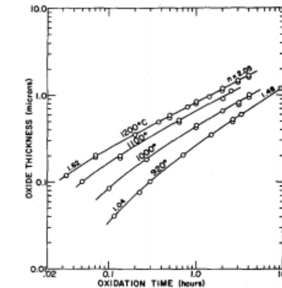
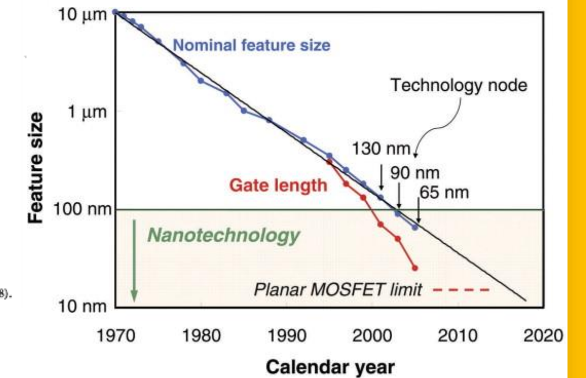


FIG. 1. Oxidation of silicon in wet oxygen (95°C H_2O).

[1] J. T. Law, J. Phys. Chem. **61**, 1200 (1957).
[2] M. M. Atalla, *Properties of Elemental and Compound Semiconductors*, edited by H. Gatos (Interscience Publishers, Inc., New York, 1960), Vol. 5, pp. 163–181.
[3] J. R. Ligenza and W. G. Spitzer, J. Phys. Chem. Solids **14**, 131 (1960).
[4] J. R. Ligenza, J. Phys. Chem. **65**, 2011 (1961).
[5] W. G. Spitzer and J. R. Ligenza, J. Phys. Chem. Solids **17**, 196 (1961).
[6] M. O. Thurston, J. C. C. Tsai, and K. D. Kang, "Diffusion of Impurities into Silicon Through an Oxide Layer," Report 896-Final, Ohio State University, Research Foundation, U. S. Army Signal Supply Agency Contract DA-36-039-SC-83874, March 1961.
[7] P. S. Flint, "The Rates of Oxidation of Silicon," Paper presented at the Spring Meeting of The Electrochemical Society, Abstract No. 94, Los Angeles, 6–10 May 1962.
[8] P. J. Jorgensen, J. Chem. Phys. **37**, 874 (1962).
[9] J. R. Ligenza, J. Electrochem. Soc. **109**, 73 (1962).
[10] B. E. Deal, J. Electrochem. Soc. **110**, 527 (1963).
[11] H. Edagawa, Y. Morita, S. Maekawa, and Y. Inuishi, J. Appl. Phys. (Japan) **2**, 765 (1963).
[12] N. Karube, K. Yamamoto, and M. Kamiyama, J. Appl. Phys. (Japan) **2**, 11 (1963).
[13] H. C. Evitts, H. W. Cooper, and S. S. Flaschen, J. Electrochem. Soc. **111**, 688 (1964).
[14] C. R. Fuller and F. J. Strieter, "Silicon Oxidation," Paper presented at the Spring Meeting of The Electrochemical Society Abstract No. 74, Toronto, 3–7 May 1964.
[15] B. E. Deal and M. Sklar, J. Electrochem. Soc. **112**, 430 (1965).
[16] N. Cabrera and N. F. Mott, Rept. Progr. Phys. **12**, 163 (1948).



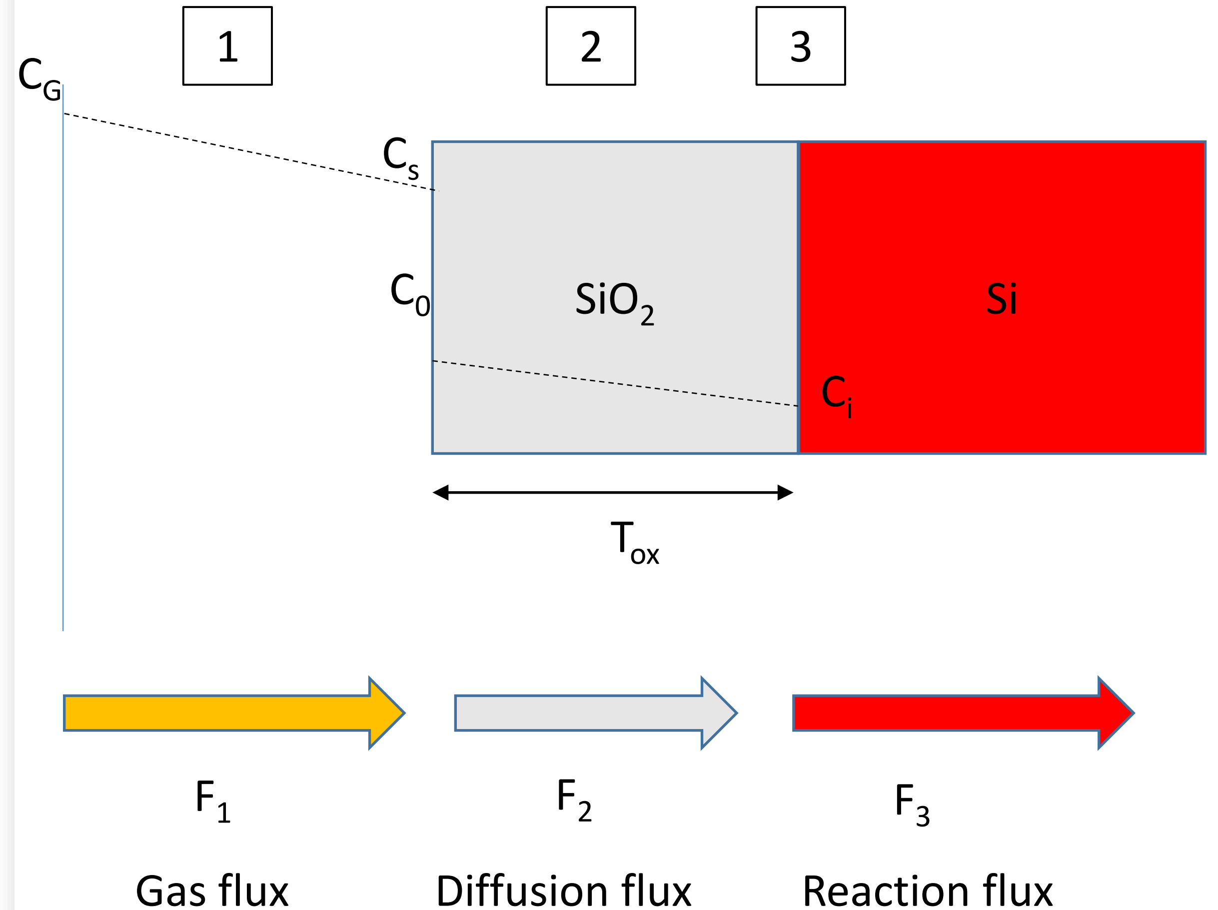
B. E. DEAL AND A. S. GROVE General Relationship for the Thermal Oxidation of Silicon, JOURNAL OF APPLIED PHYSICS VOLUME 36. NUMBER 12 DECEMBER 1965

The Deal-Grove oxidation model

1: Oxygen diffuses from bulk (C_G)to wafer surface (C_S)

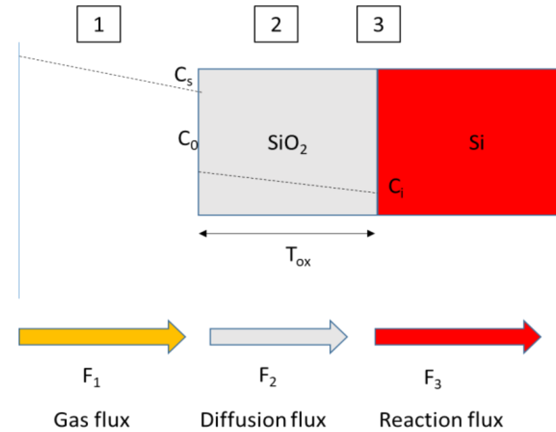
2: Oxygen diffuses from wafer surface (C_O) to Si surface (C_i)

3: Oxygen reacts with Si at interface to form SiO_2



The Deal-Grove oxidation model

- Oxygen diffusion through gas: Fick's 1st Law approximated as linear equation
- Adsorbed concentration C_o on surface ∝ partial pressure (Henry's Law)
- Oxygen diffusion through SiO_2 Fick's 1st Law approximated as linear equation
- 1st order reaction at Si interface



F1 Gas flux | F2 Diffusion flux | F3 Reaction flux

$$\mathbf{1}:\ F_1 = D\frac{dC}{dx} \approx \frac{D_g}{\delta}(C_g - C_s) = h_g(C_g - C_s)$$

$$C_o = HP_s = HC_s kT$$

$$\mathbf{2}:\ F_2 = D\frac{dC}{dx} \approx \frac{D_{ox}}{t_{ox}}(C_o - C_i)$$

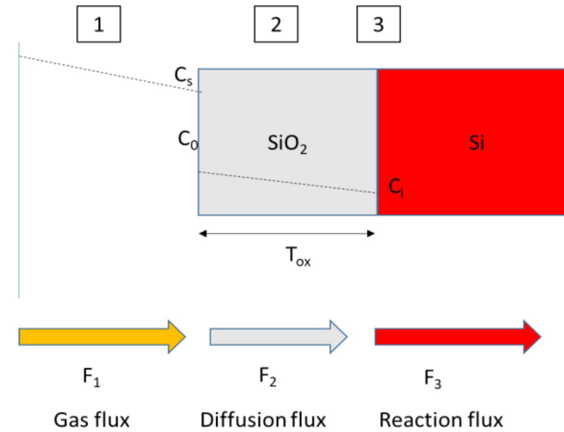
$$\mathbf{3}:\ F_3 = k_s C_i$$

$C_g = \frac{P_g}{kT}$	Reactant concentration
H	Henry's gas law coefficient
t_{ox}	SiO2 thickness
D_{ox}	Oxygen diffusivity in SiO2
h_g	Mass transfer coefficient

The Deal-Grove oxidation model

- Steady state: all fluxes are equal (Si interface reaction is the rate-limiting step)

- Oxygen flux F_{OX} = $v_{ox} N_{ox}$



$$F_1 = F_2 = F_3 = F_{OX}$$

$$F_{OX} = \frac{Hk_sP_g}{1+\frac{k_s}{h}+\frac{k_st_{ox}}{D_{ox}}} = \frac{dt_{ox}}{dt} N_{ox}$$

; h= $\frac{h_g}{HkT}$

$$\frac{dt_{ox}}{dt} = \frac{Hk_sP_g}{1+\frac{k_s}{h}+\frac{k_st_{ox}}{D_{ox}}} \frac{1}{N_{ox}}$$

The Deal-Grove oxidation model

- Integrating over t gives the expression for oxide thickness t_{ox} vs. time t
- The model requires coefficients adjustments for different crystal orientations

$$t_{ox}^2 + At_{ox} = B(t + \tau)$$

$$A = 2D_{ox}\left(\frac{1}{h} + \frac{1}{k_s}\right)$$

$$B = \left(\frac{2D_{ox}HP_g}{N_{ox}}\right)$$

$$\tau = \left(\frac{t_0^2 + At_0}{B}\right)$$

Table 4.1 Oxidation coefficients for silicon

Temperature (°C)	Dry A (μm)	Dry B (μm²/hr)	Dry τ (hr)	Wet (640 torr) A (μm)	Wet (640 torr) B (μm²/hr)
800	0.370	0.0011	9	—	—
920	0.235	0.0049	1.4	0.50	0.203
1000	0.165	0.0117	0.37	0.226	0.287
1100	0.090	0.027	0.076	0.11	0.510
1200	0.040	0.045	0.027	0.05	0.720

The τ parameter is used to compensate for the rapid growth regime for thin oxides. *(After Deal and Grove.)*

<111> Si

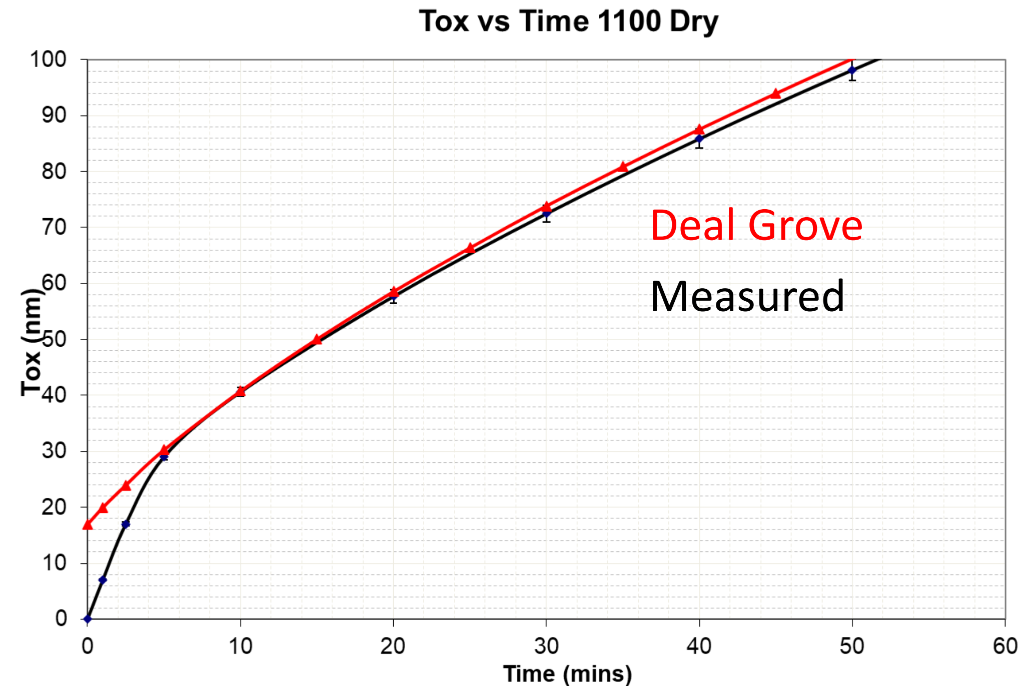
The Deal-Grove oxidation model

- Comparison of Deal-Grove model with measured oxide thickness (Dry oxide)

- With the correct coefficients (P,T, crystal) the Deal-Grove model works nicely for single crystal silicon (~%’s accuracy). Model extensions to 3D exist

- Additional tweaking needed for high Si doping

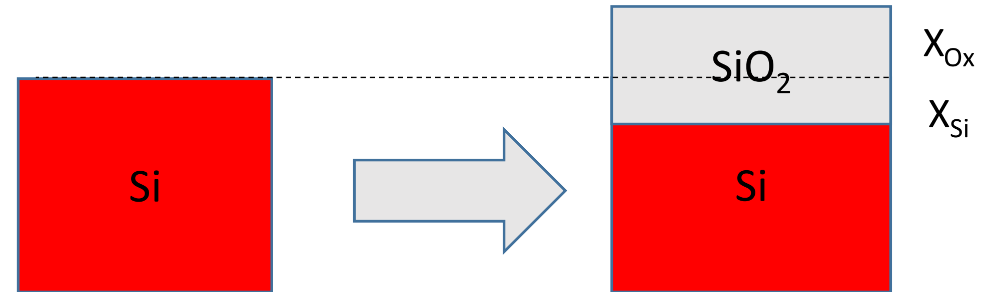
- The model fails for Polysilicon



* Self-limiting growth of native oxide saturates at around 2-3 nm
‘**Growth of native oxide on a silicon surface’** Journal of Applied Physics, Volume 68, Issue 3, August 1, 1990, pp.1272-1281

The Deal-Grove oxidation model

- The oxide grows at the expense of Silicon: during oxidation around half of Silicon is consumed



$$X_{Si}\, N_{Si} = X_{Ox}\, N_{Ox} \rightarrow X_{Si} = \frac{X_{Ox}\, N_{Ox}}{N_{Si}} \equiv X_{Ox} \frac{2.3\; 10^{22}}{5\; 10^{22}} = X_{Ox}\, 0.46$$

$N_{Ox} = molecular\ density\ SiO_2$
$N_{Si} = atomic\ density\ Si$

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