Silicon Zoology

Daniel Hynds

Outline

- Electronic structure of solids
- Semiconductor junctions

- Transistor anatomy
- Detector anatomy

- Signal formation
- Charge carrier generation
- Radiation damage

- Semiconductor fabrication
- Silicon pixel detectors
- Non-silicon pixel detectors

Practical zoology

When I was a young boy and I didn't understand how something worked, I just made stuff up in my head.

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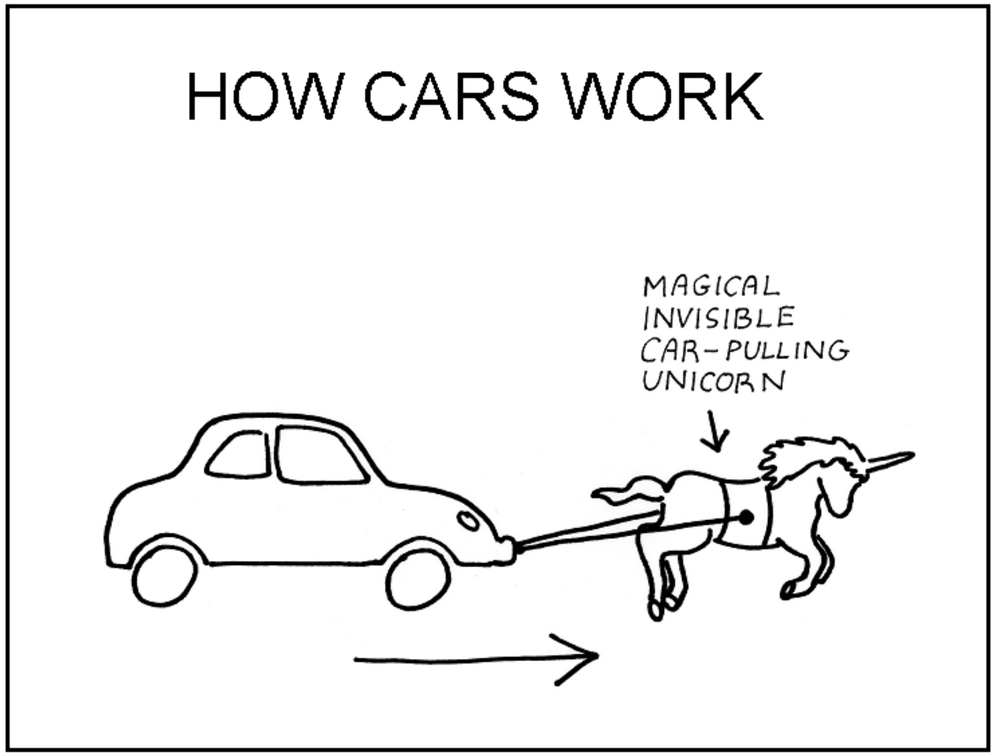
Practical zoology



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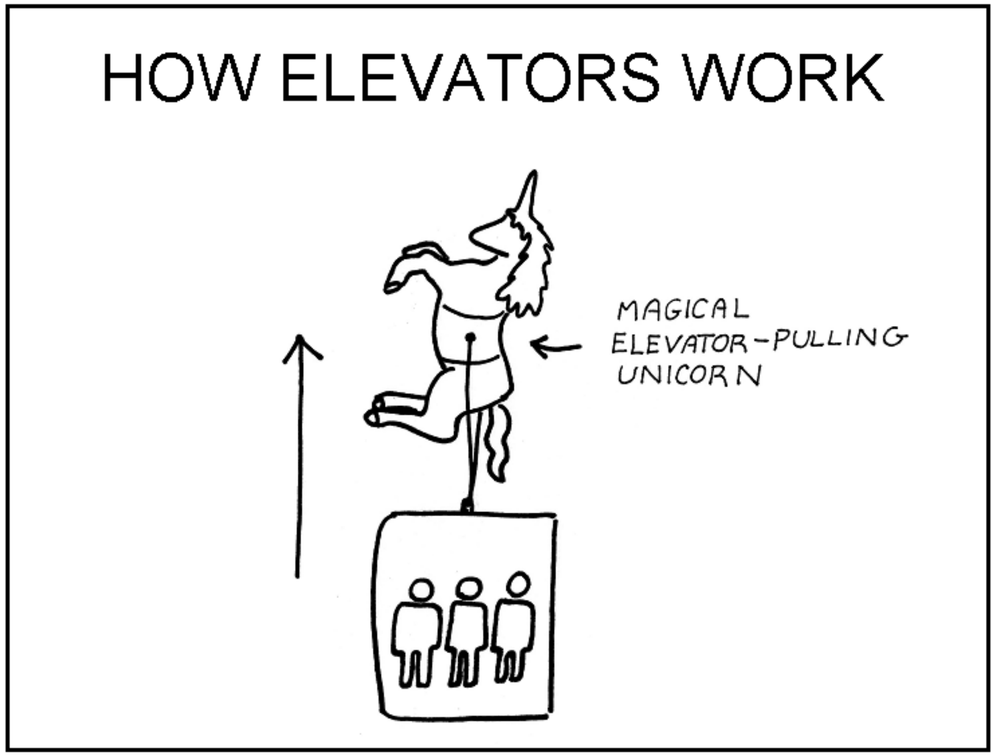
Practical zoology



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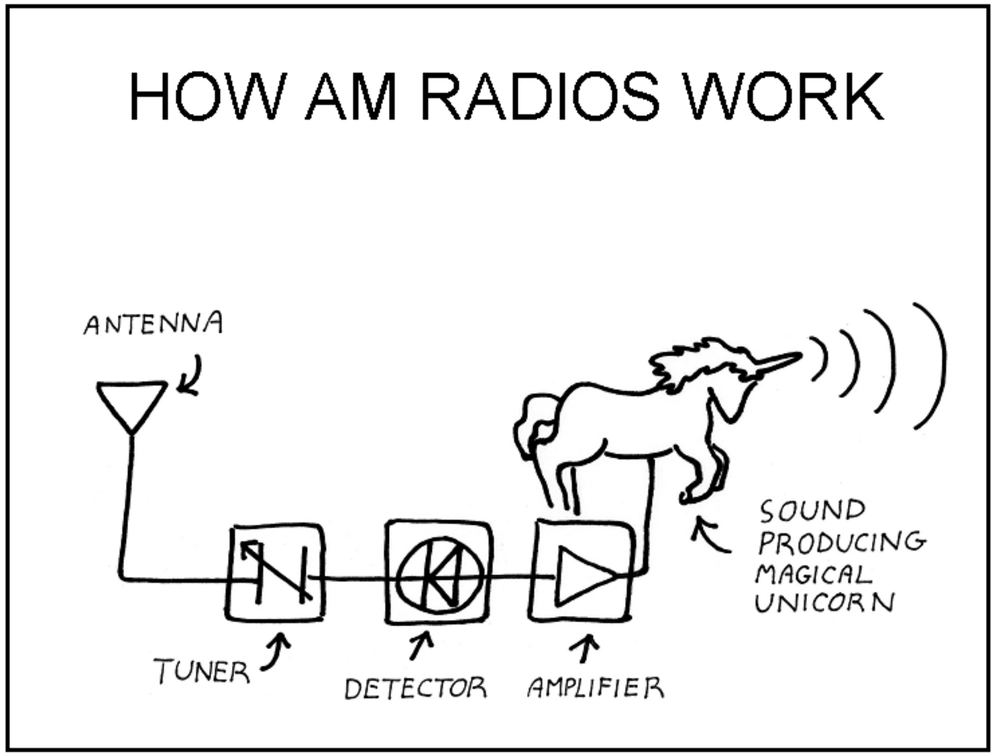
Practical zoology

As I got older, I started to learn that science could explain how most things worked.

However, when there were holes in my knowledge, my mind still just filled in the gaps.

Practical zoology



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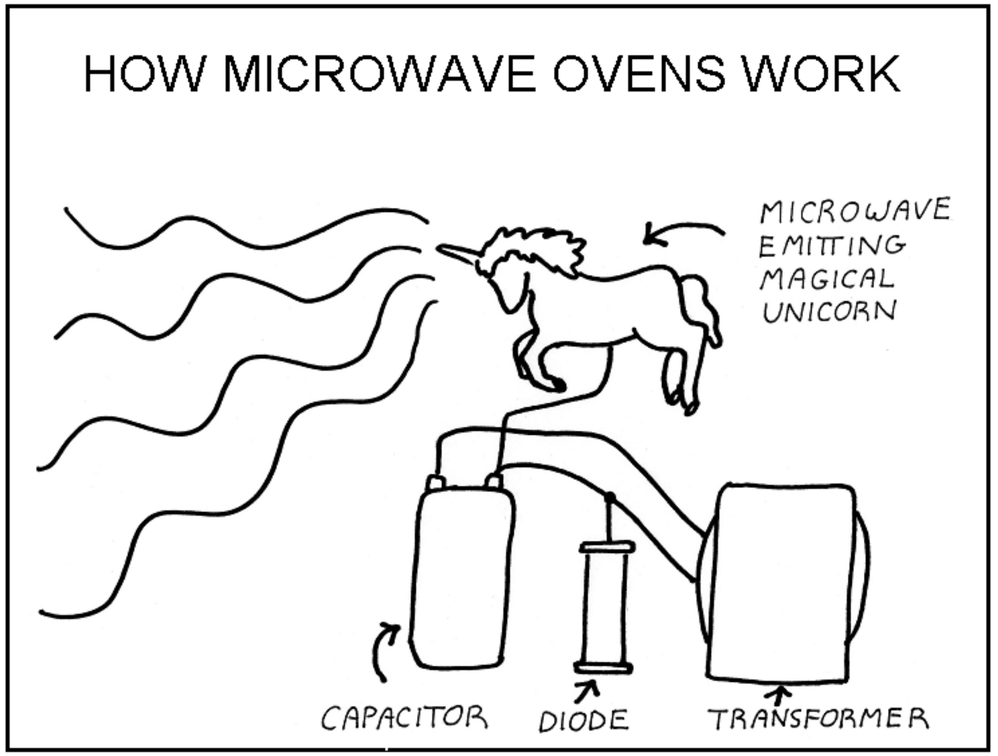

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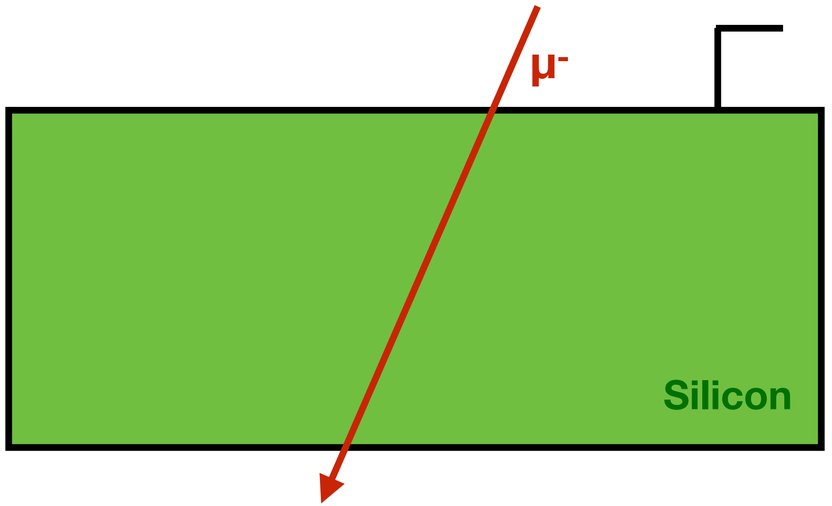
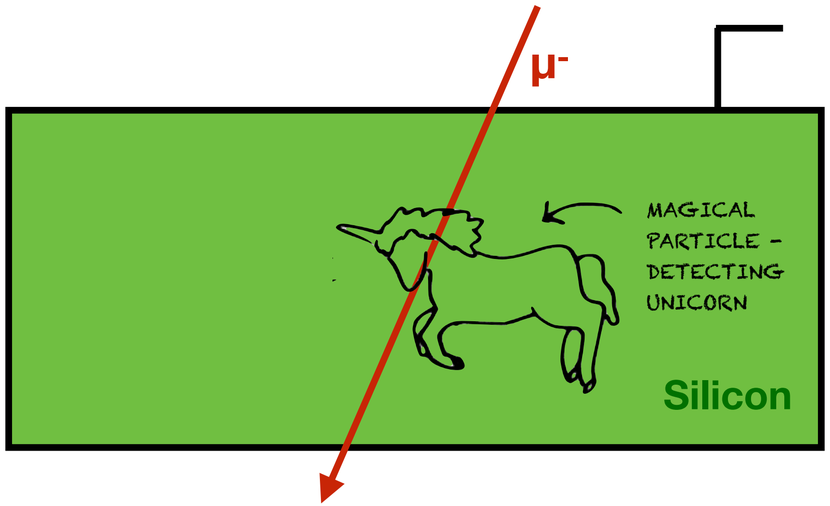
Silicon…



Silicon… zoology?



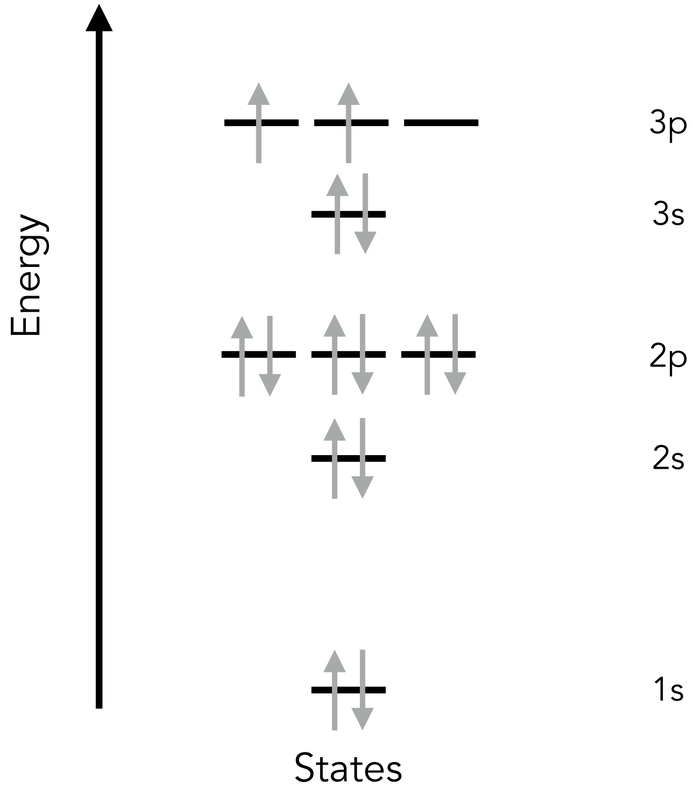
Semiconductors

Discrete energy levels

Electrons within an atom sit in discrete energy levels

- Each of these orbitals hosts two electrons - one spin up and one spin down

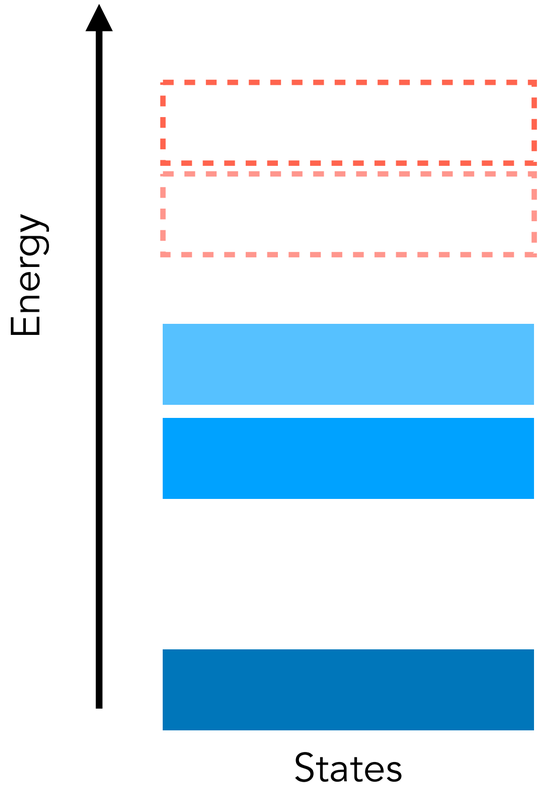
Lower energy states lie closer to the nucleus, while those in the outer shells are the so-called valence electrons that take part in chemical reactions

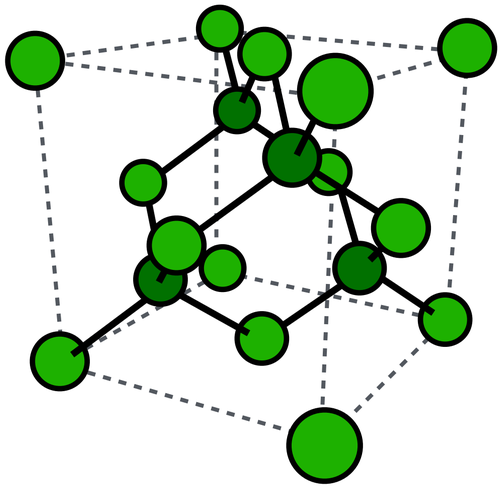


Band structure

In a periodic lattice, the available energy levels split to produce a continuous energy band

The inner bands will be tightly bound to the nucleus, and electrons there are unable to jump to neighbouring atoms





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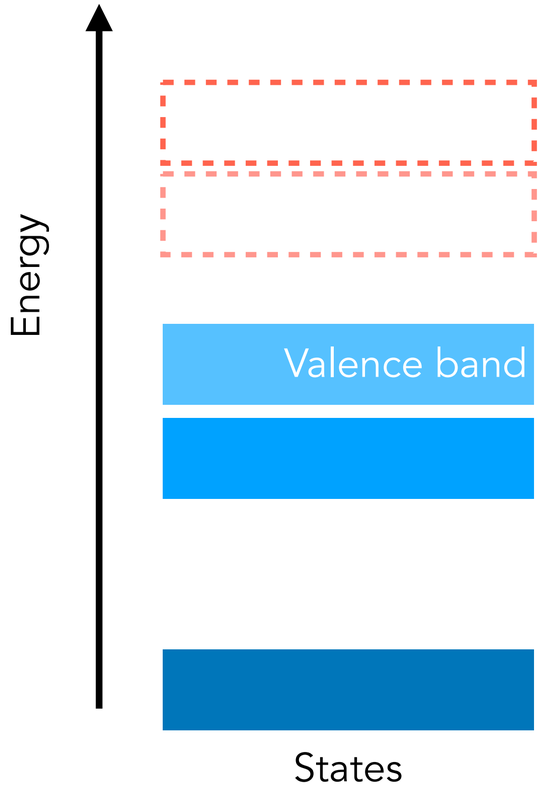
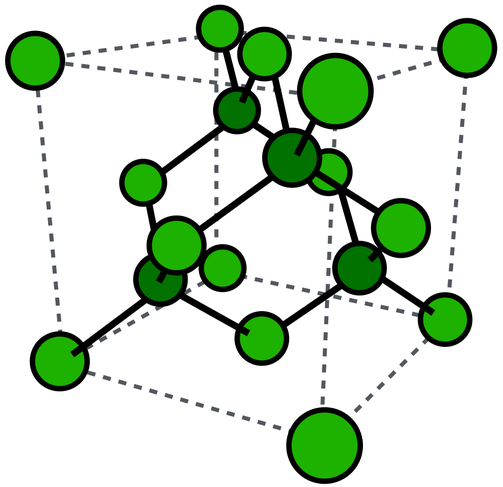
The most interesting bands are

- The **valence band** - the highest occupied band where electrons <u>are not</u> free to move





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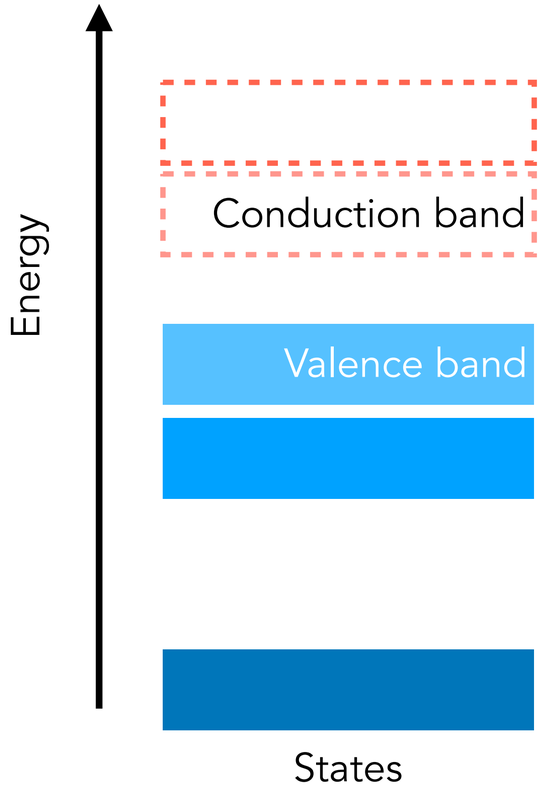
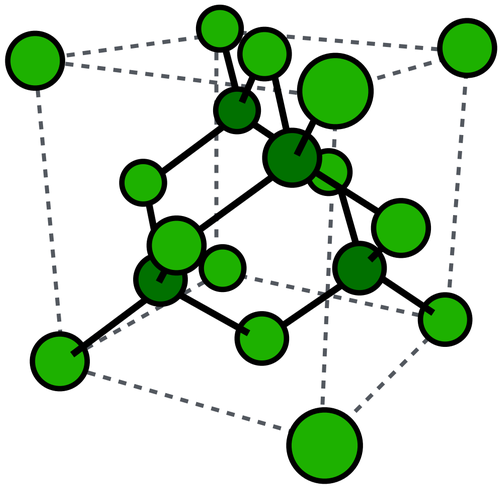
The most interesting bands are

- The **valence band** - the highest occupied band where electrons <u>are not</u> free to move
- The **conduction band** - the lowest energy band where electrons <u>are</u> free to move

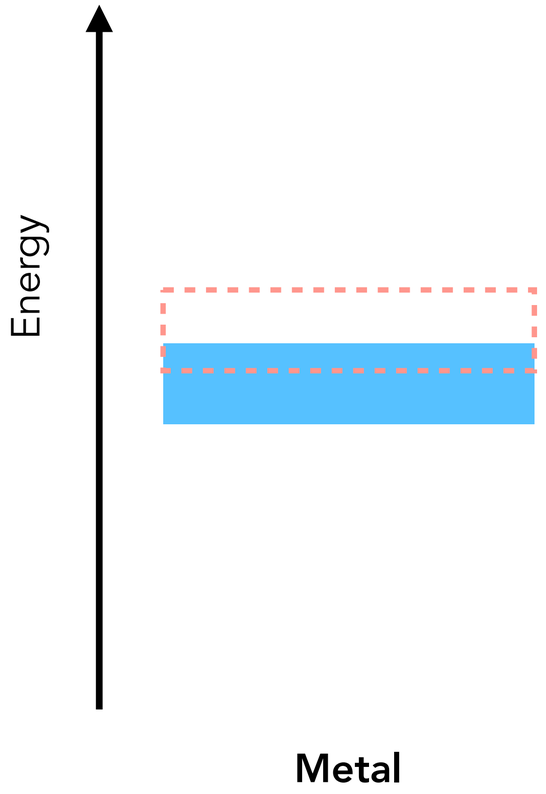




Electrical behaviour

The energy gap between the valence and conduction bands will determine the electrical behaviour of the solid

- **Metals** have overlapping states, so already there are charge carriers (electrons) able to move freely throughout the bulk



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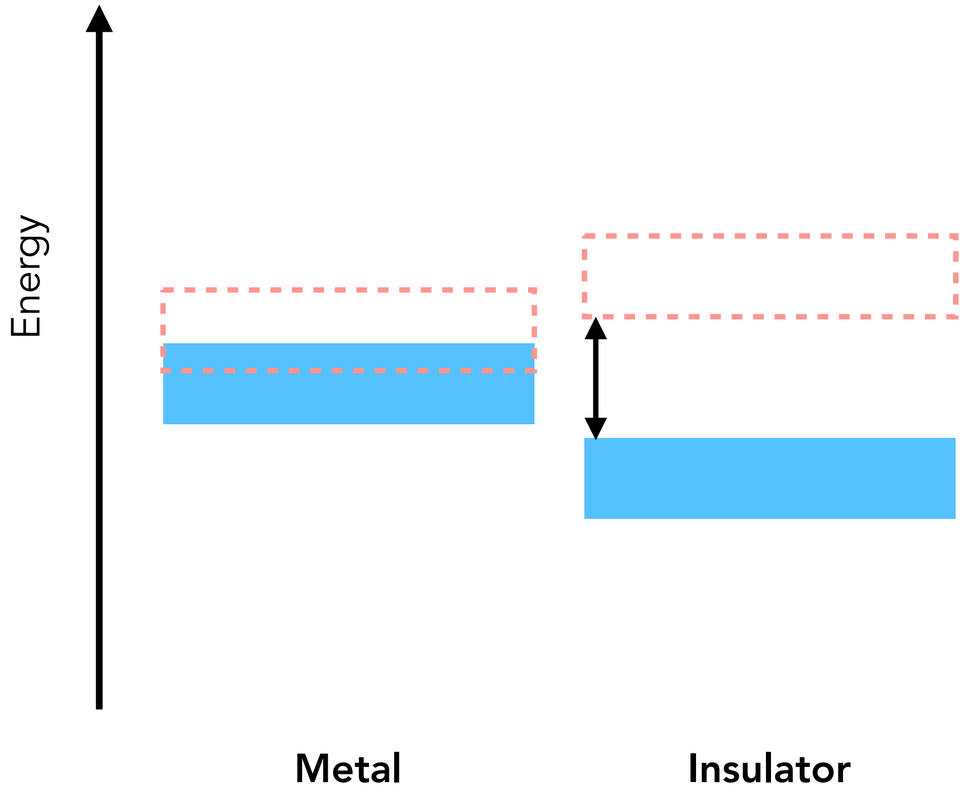

Electrical behaviour

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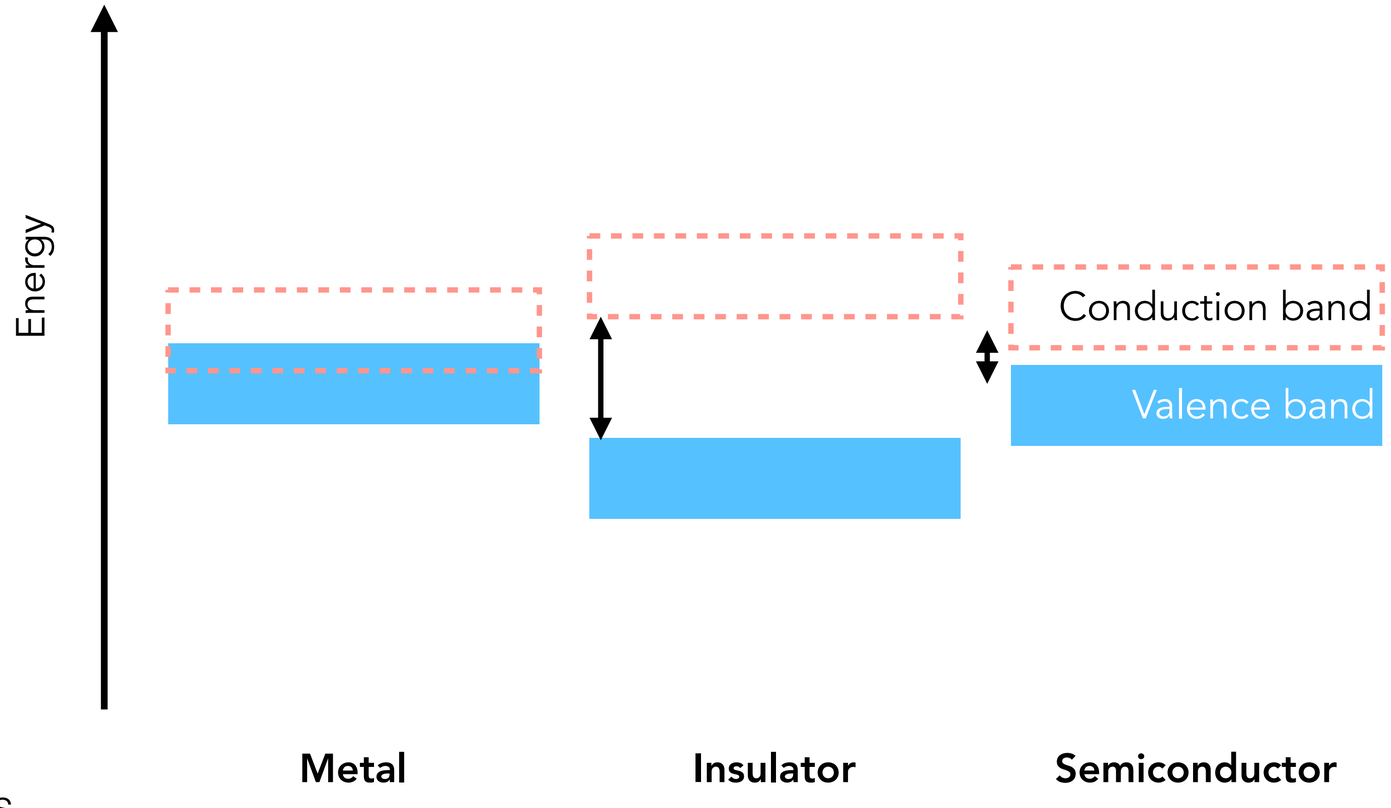
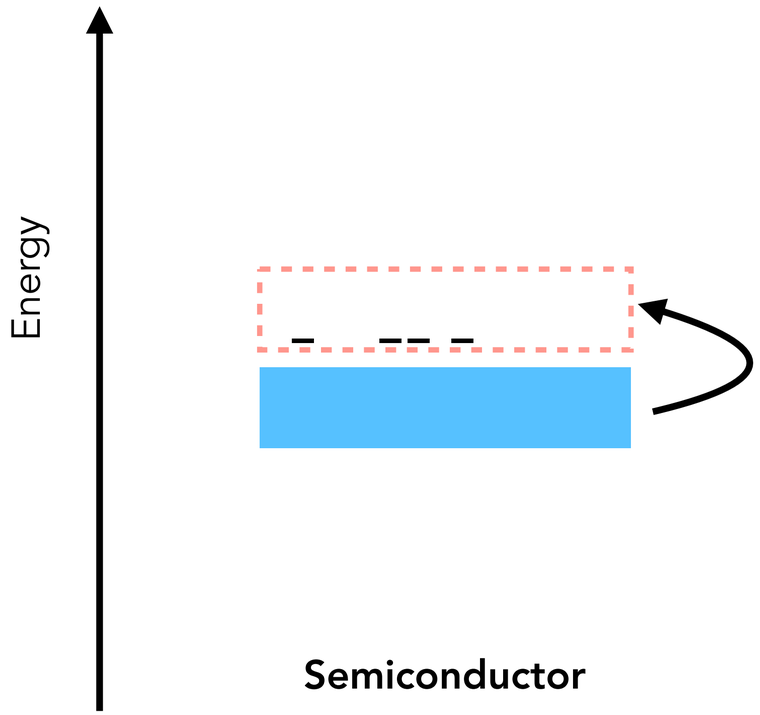
- **Metals** have overlapping states, so already there are charge carriers (electrons) able to move freely throughout the bulk
- **Insulators** have a large **band gap**, leading to poor charge flow
- **Semiconductors** have a **band gap** of ~few eV, giving some charge carriers at room temperature (eg. Silicon ~10^{10} charge carriers cm^{-3} for a density of 5×10^{22} atoms cm^{-3})



Charge carriers in semiconductors

Electrons sitting in the valence band can be promoted into the conduction band with enough energy



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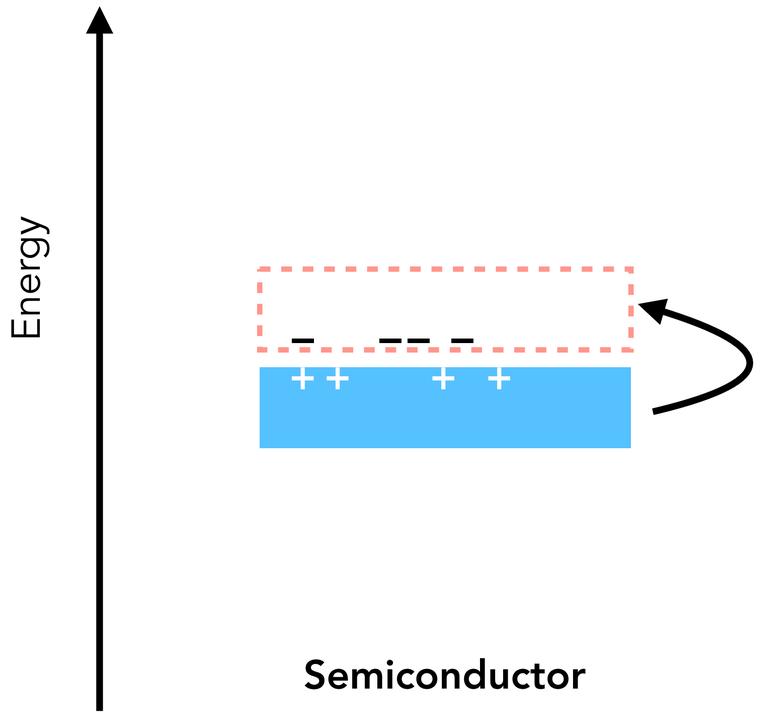
- The gap left by the electron's departure is called a hole



Charge carriers in semiconductors

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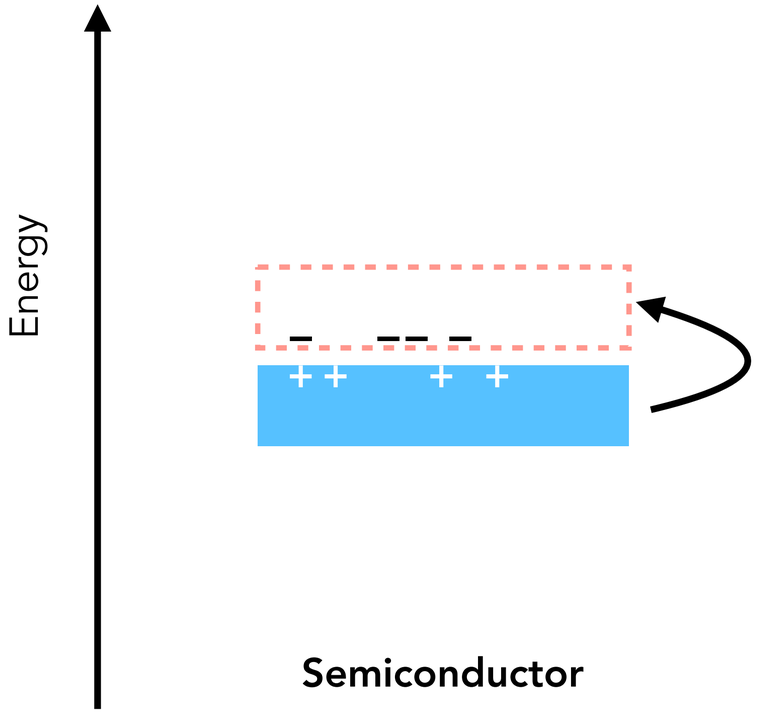
Other electrons within the valence band can move into these holes, such that the hole appears to travel through the material

- Holes are treated as effective particles which move freely in the valence band and allow a current to flow



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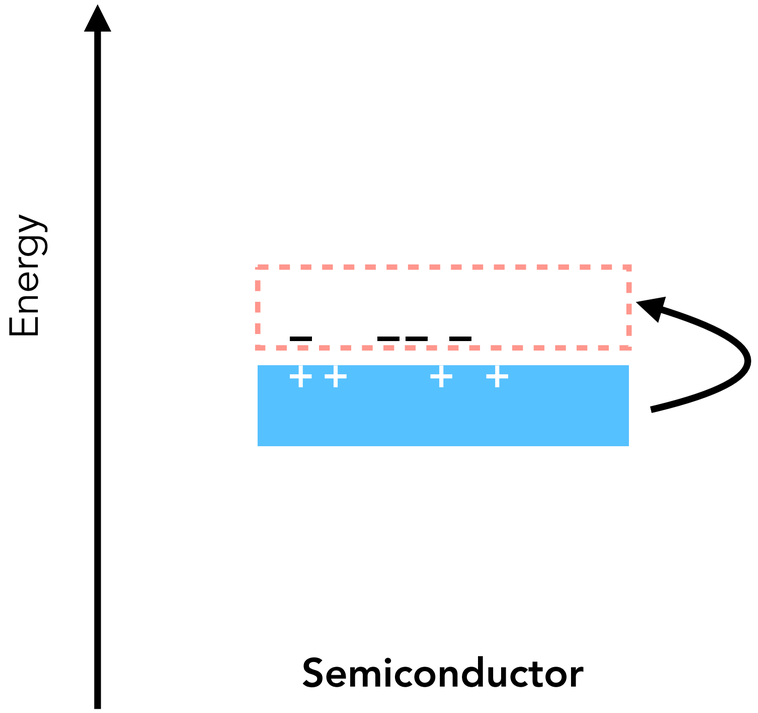
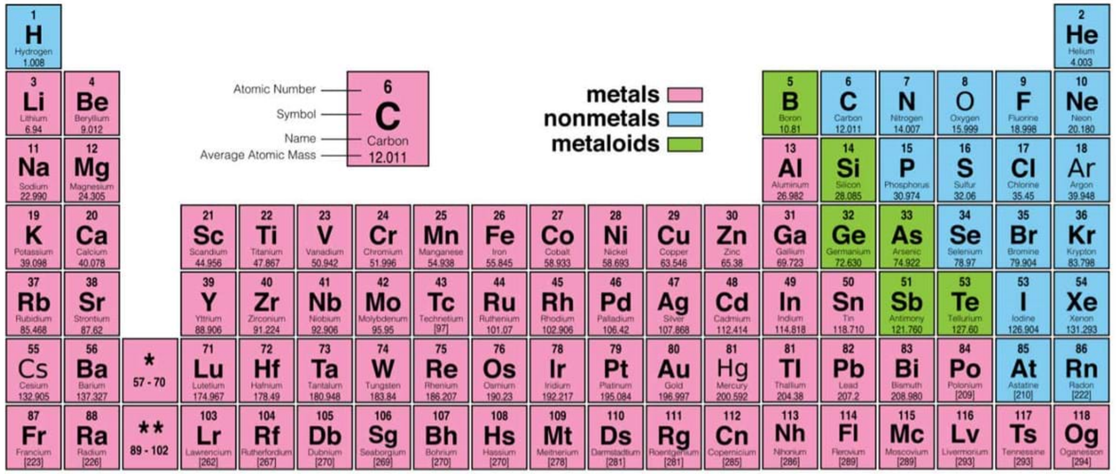
Each movement of an electron from the valence to conduction band produces an **electron-hole pair**

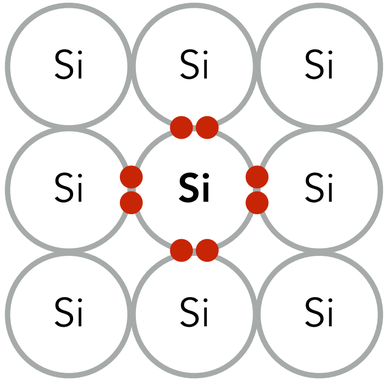


Doping of semiconductors

Silicon is a **group 4** element, and therefore contains 4 valence electrons

- It will therefore form 4 covalent bonds in order to reach a stable configuration





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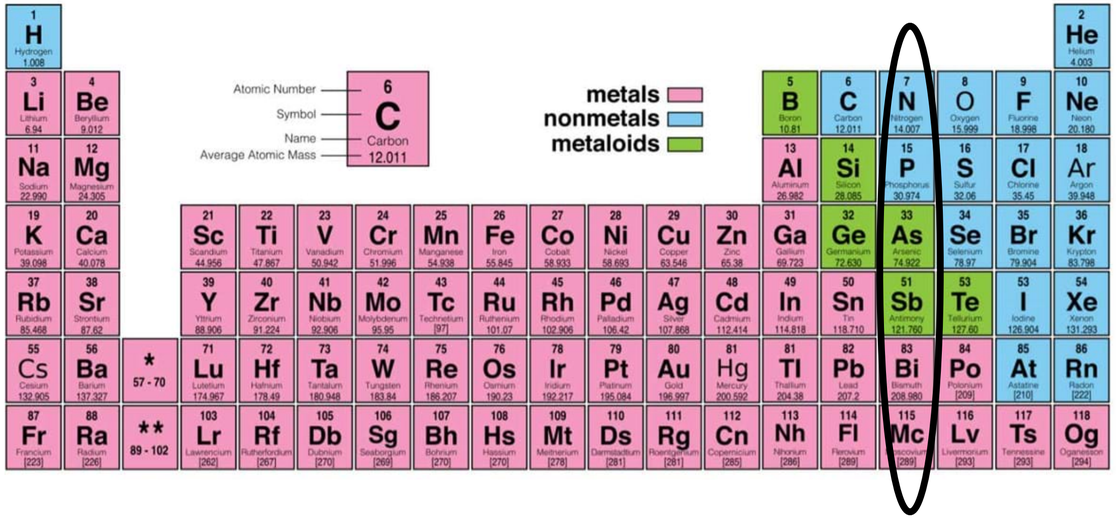
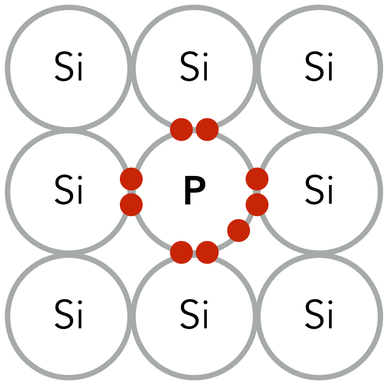
If we introduce a small amount of a **group 5** element, the crystal lattice will remain intact but there will be some atoms with an excess of electrons - **n-type doping**





Doping of semiconductors

Silicon is a **group 4** element, and therefore contains 4 valence electrons

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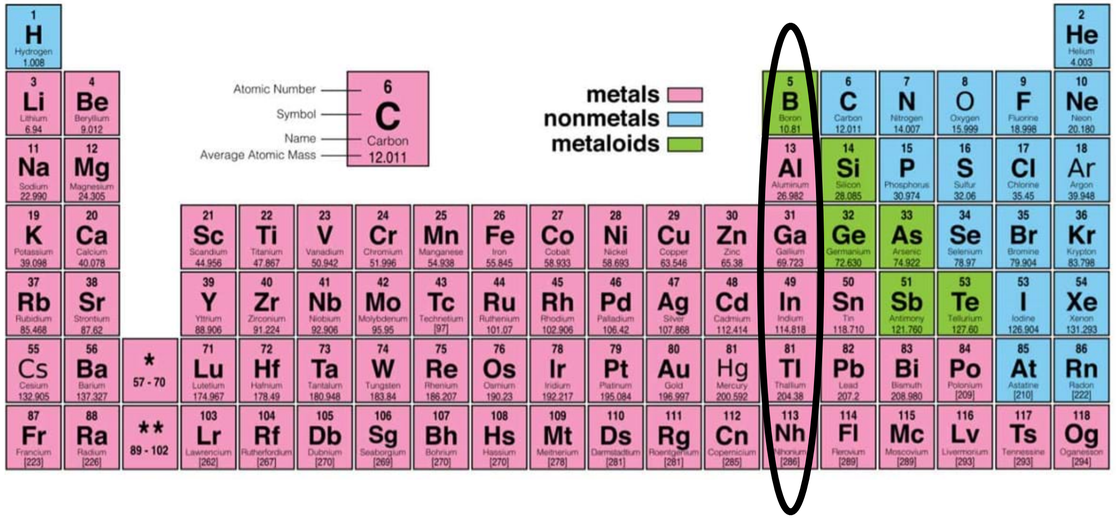
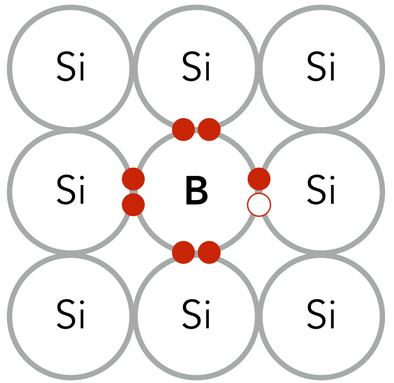
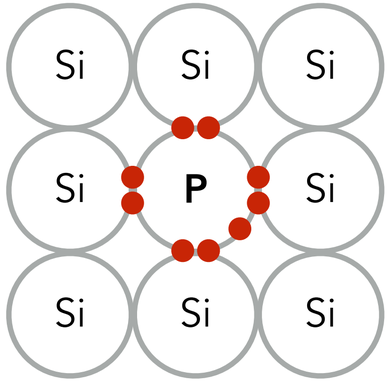
If we introduce a small amount of a **group 3** element, there will be some atoms with an electron deficiency - **p-type doping**

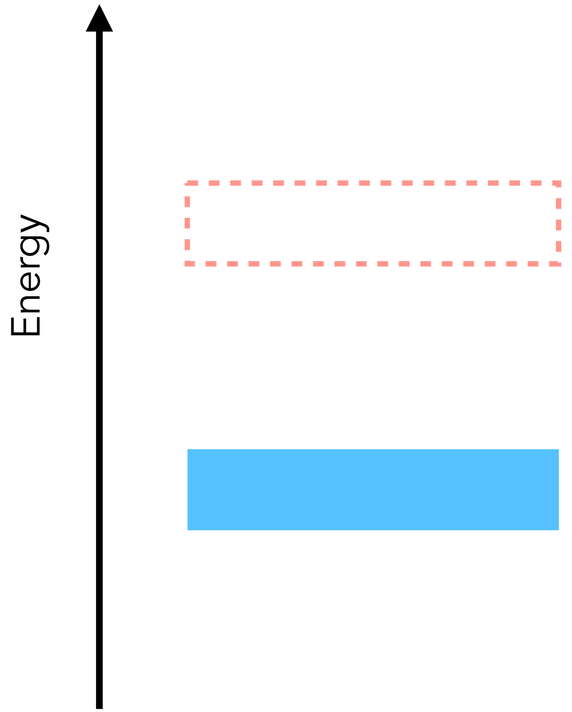




Band structure n-type semiconductors

For n-type doping, there is an excess of electrons in the crystal structure

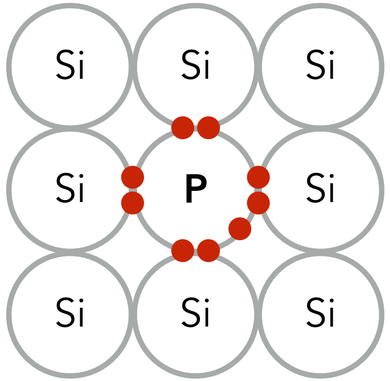


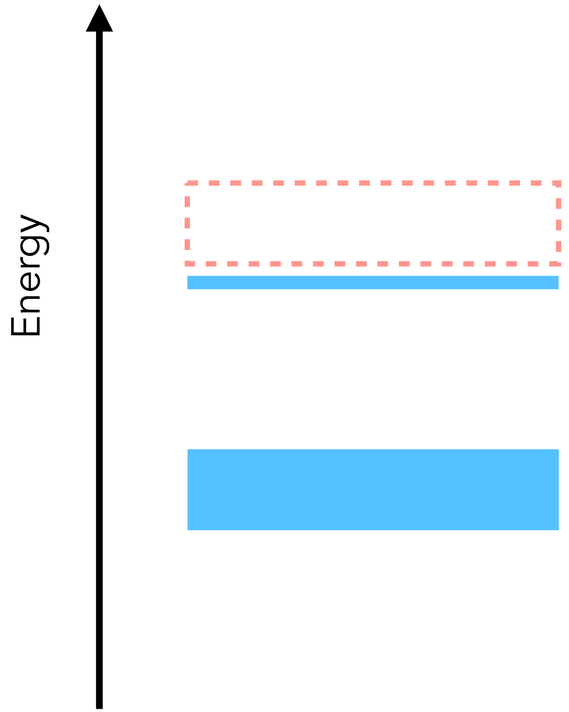


Band structure n-type semiconductors

For n-type doping, there is an excess of electrons in the crystal structure

- These sit within a new band close to the conduction band





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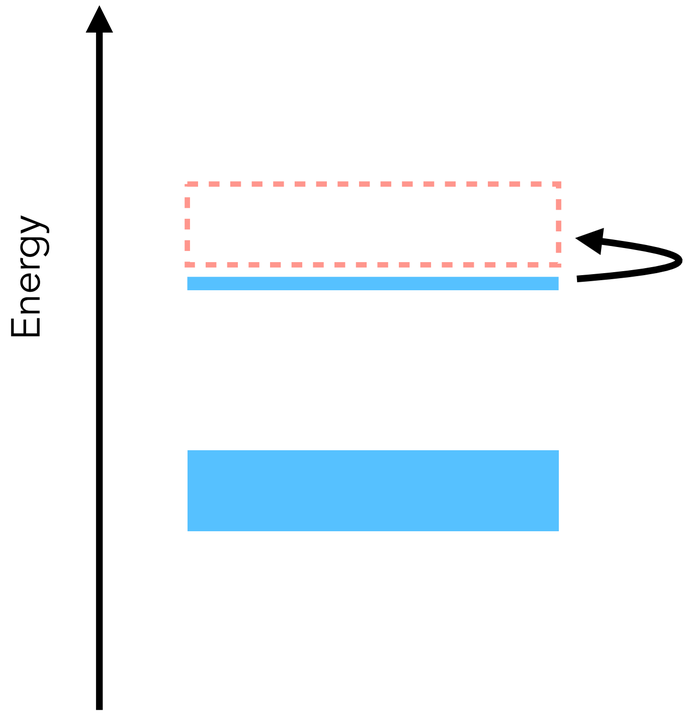
The electrons in this band will almost all move to the conduction band with thermal energy alone



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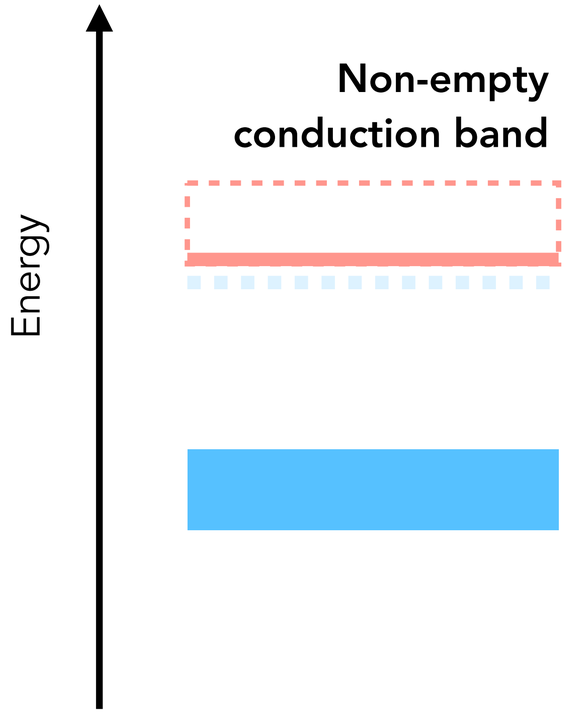
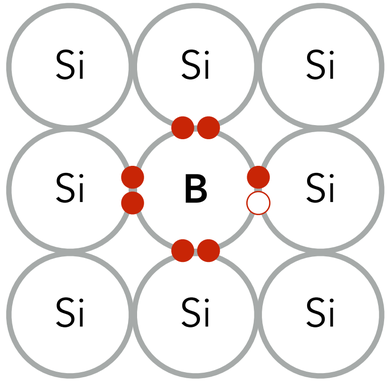
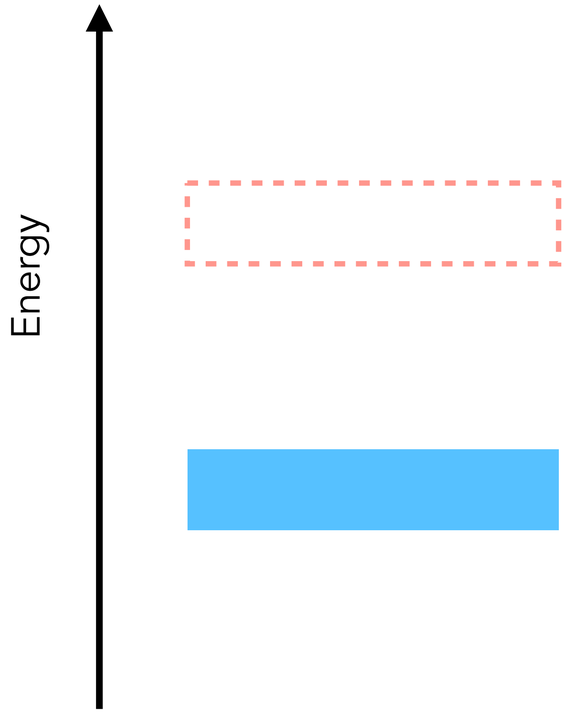
- The majority carriers for n-type materials are electrons in the conduction band
- Significant carrier densities can be achieved introduction tiny fractions of impurities (eg. 1 ppm P = 5×10^{16} electrons cm^{-3} versus 10^{10} cm^{-3} for undoped Si)



Band structure p-type semiconductors

For p-type doping, there is a deficiency of electrons in the crystal structure





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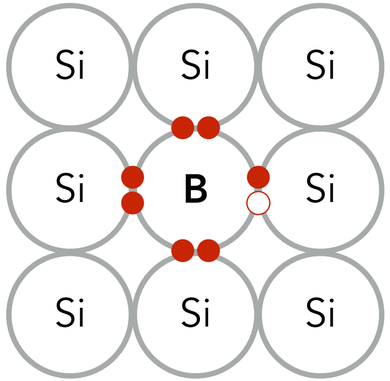

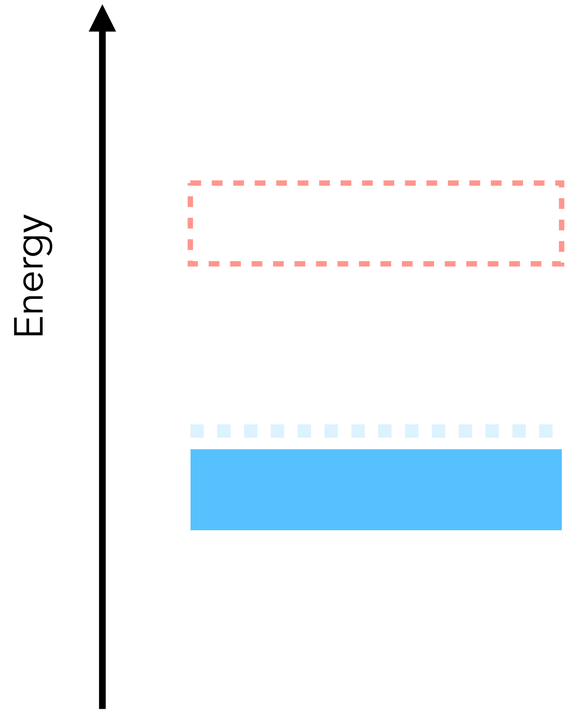

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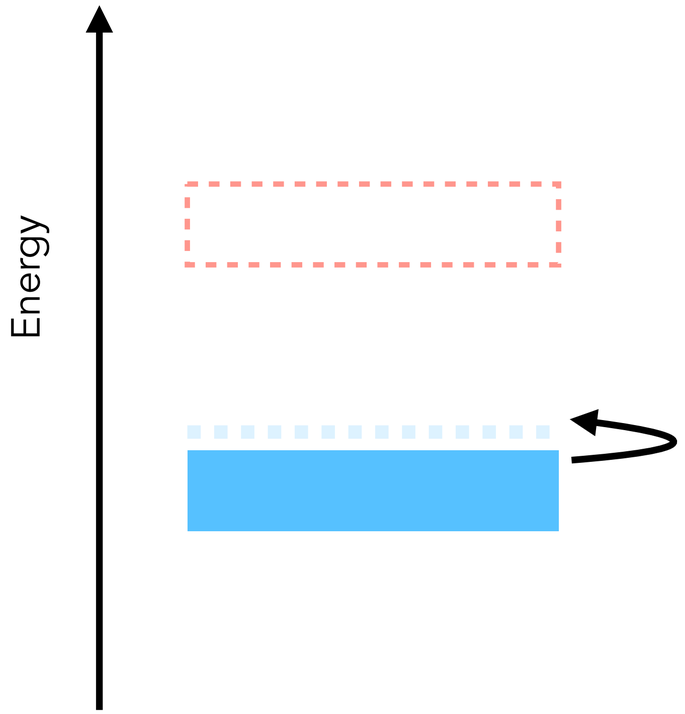

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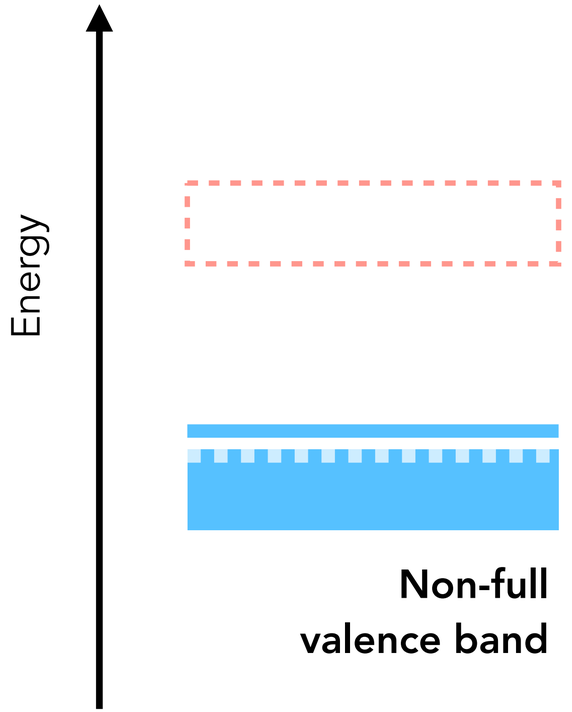
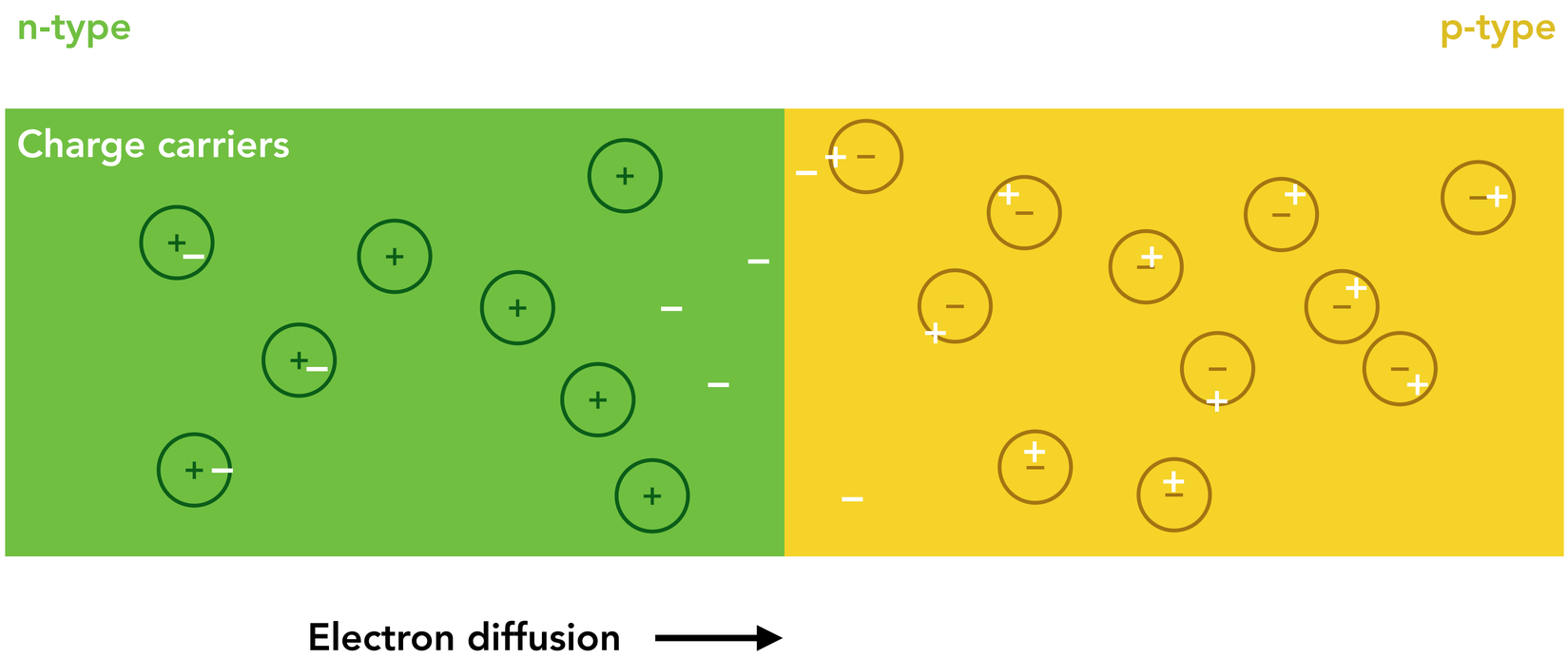


P-N junctions

P-N junctions

Electrically neutral system

P-N junctions - carrier movement



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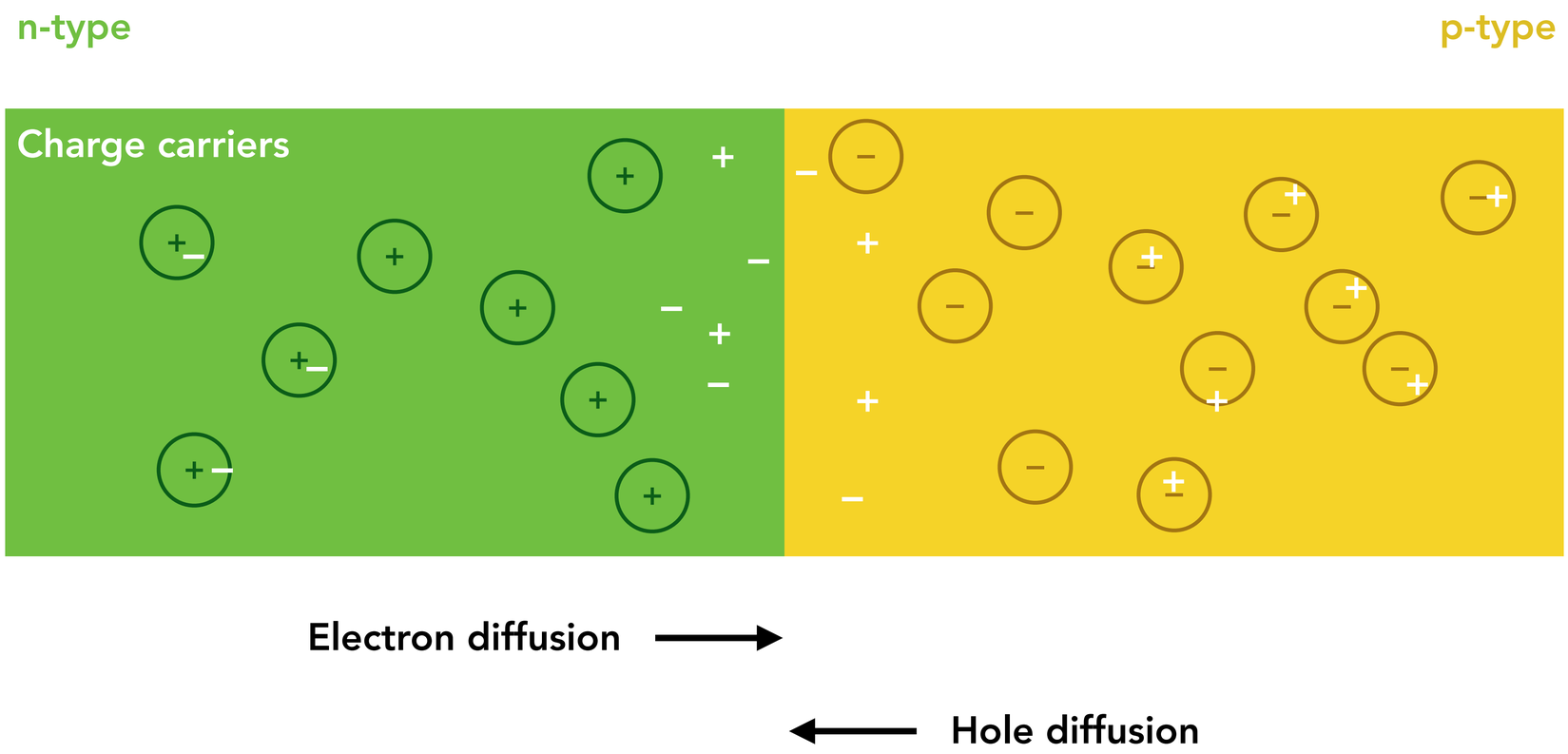

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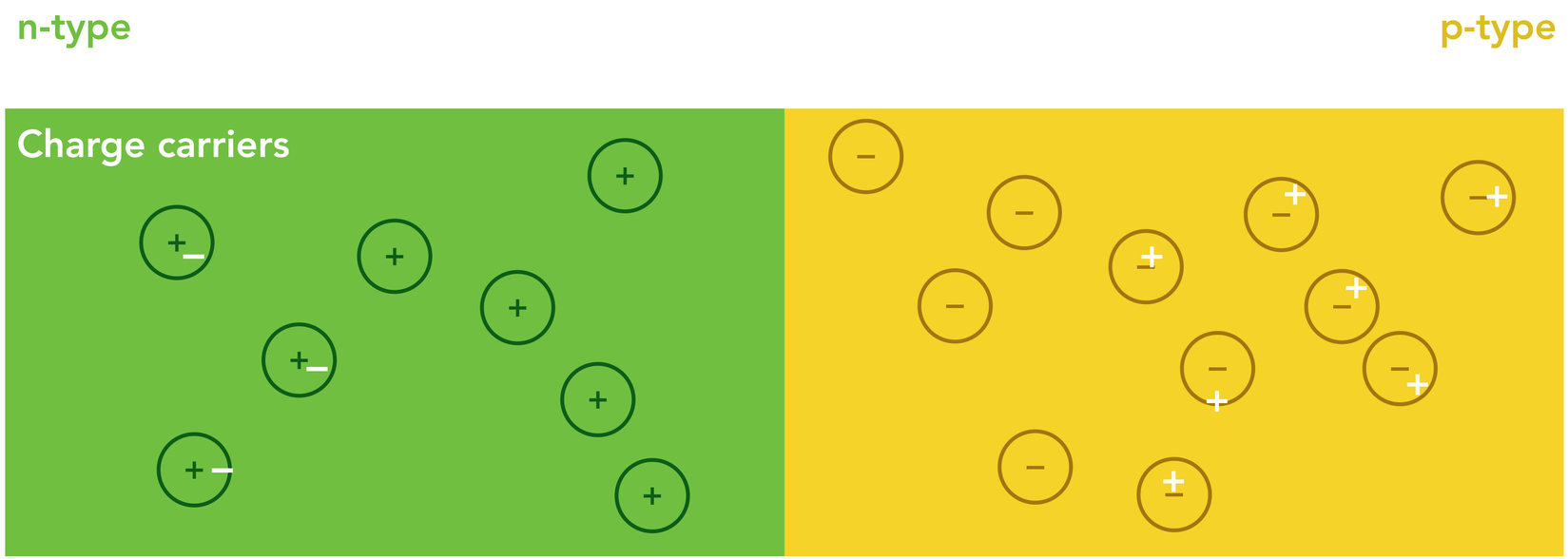
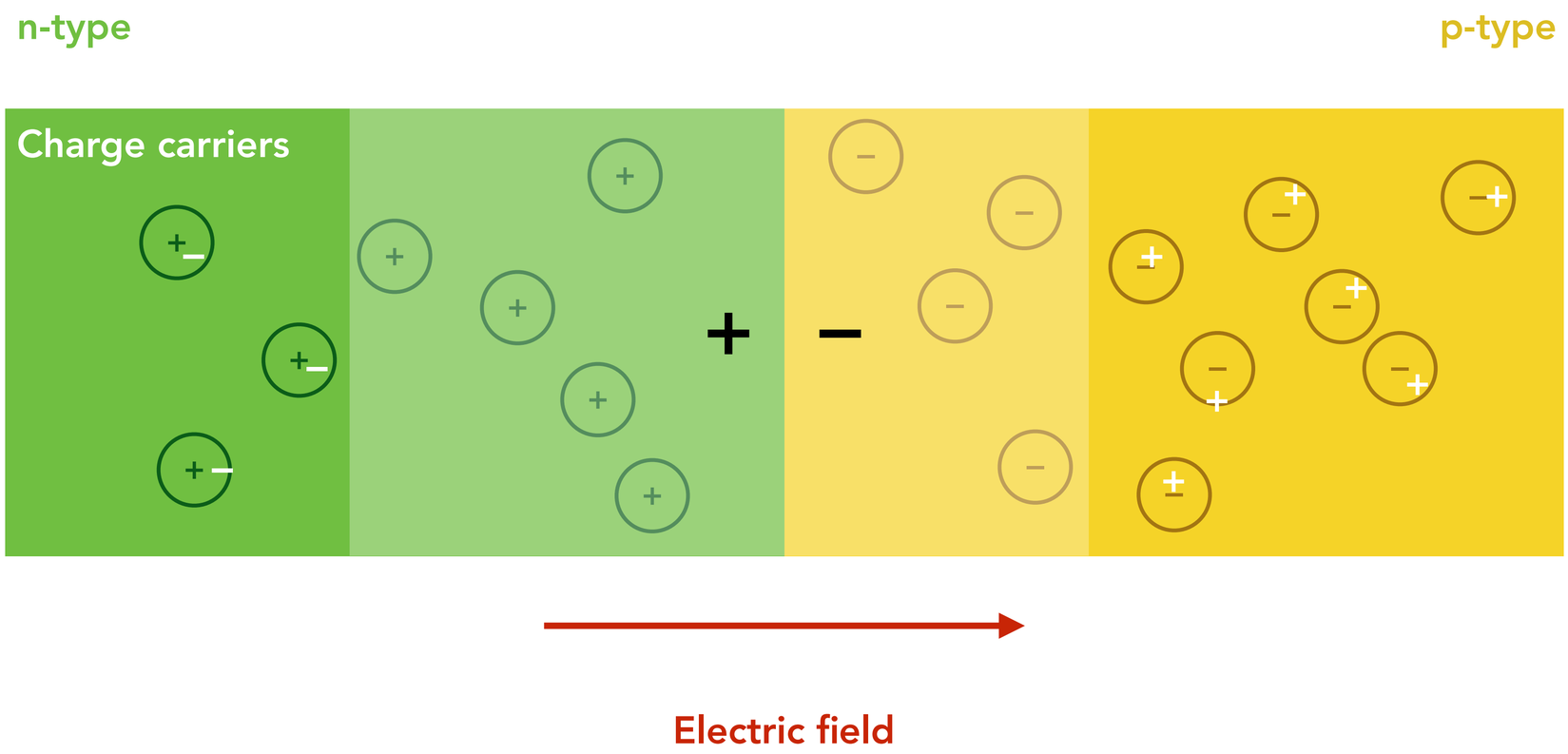


Recombination

P-N junctions - carrier movement



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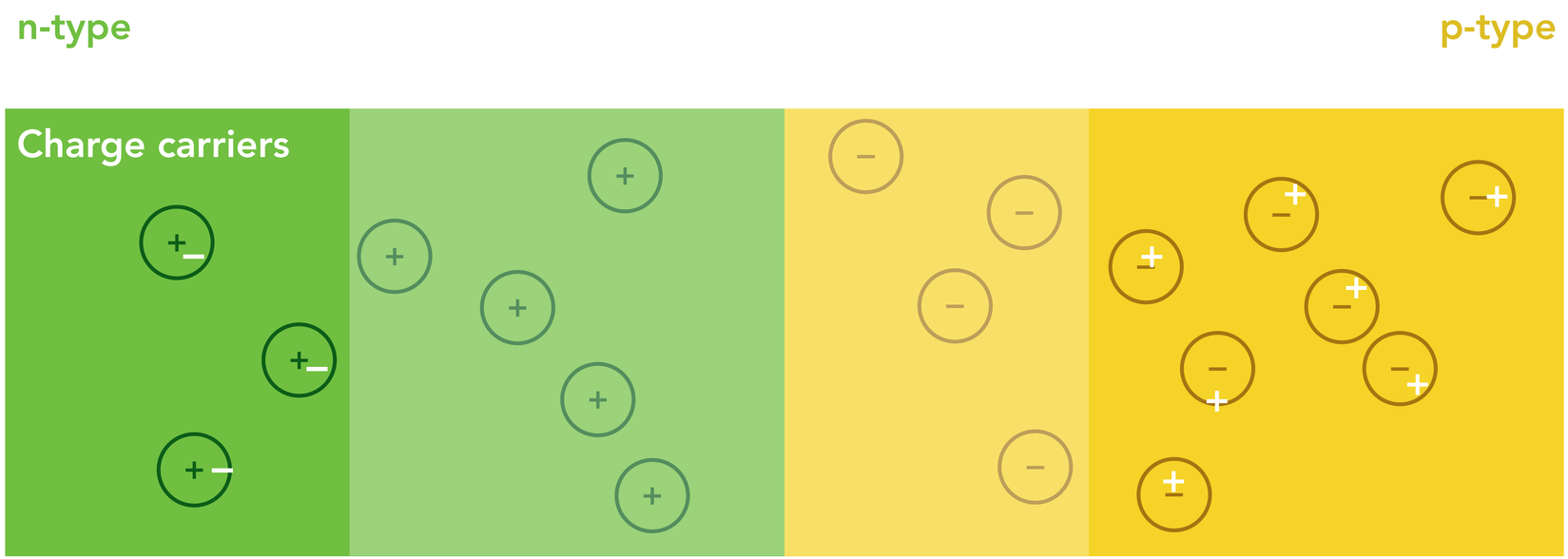
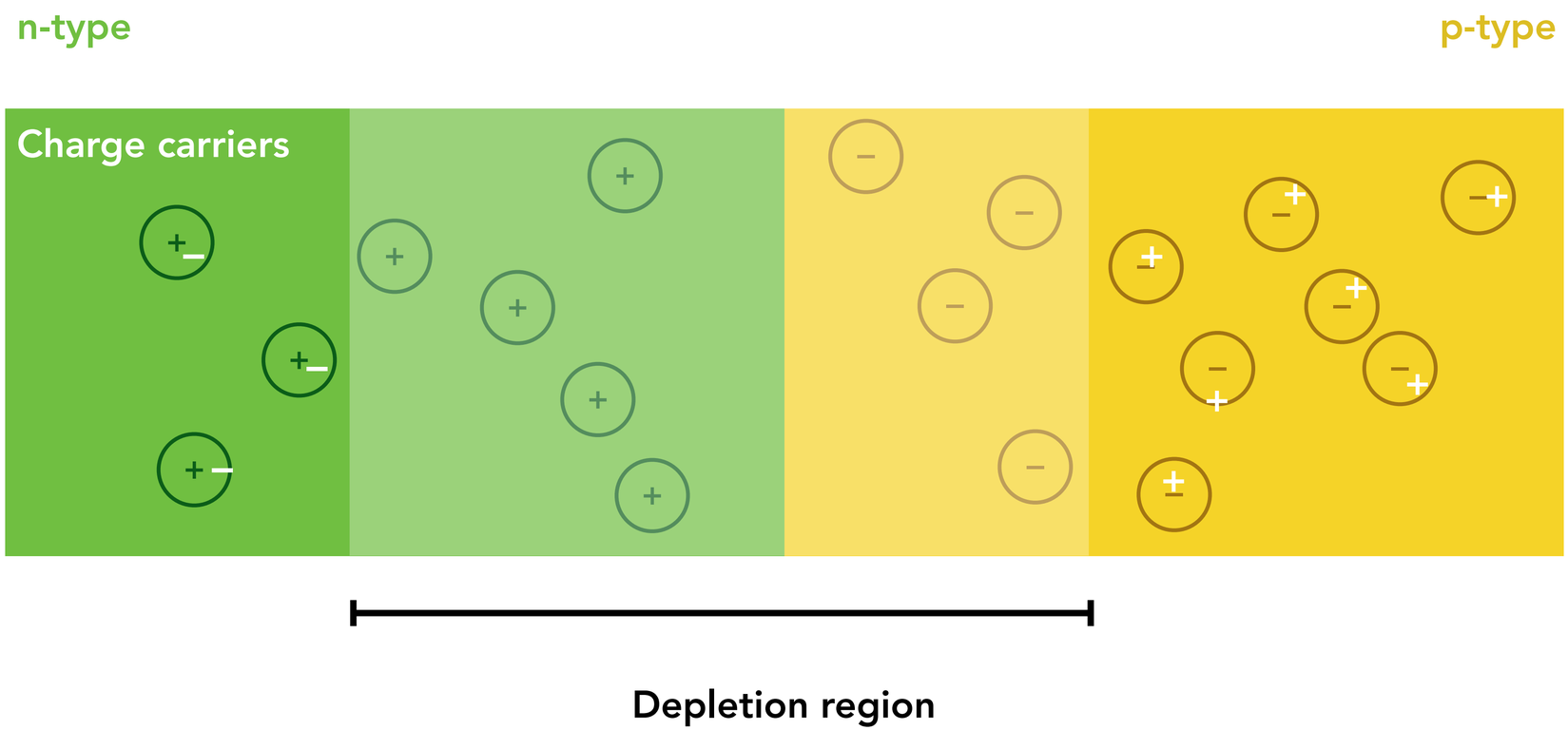


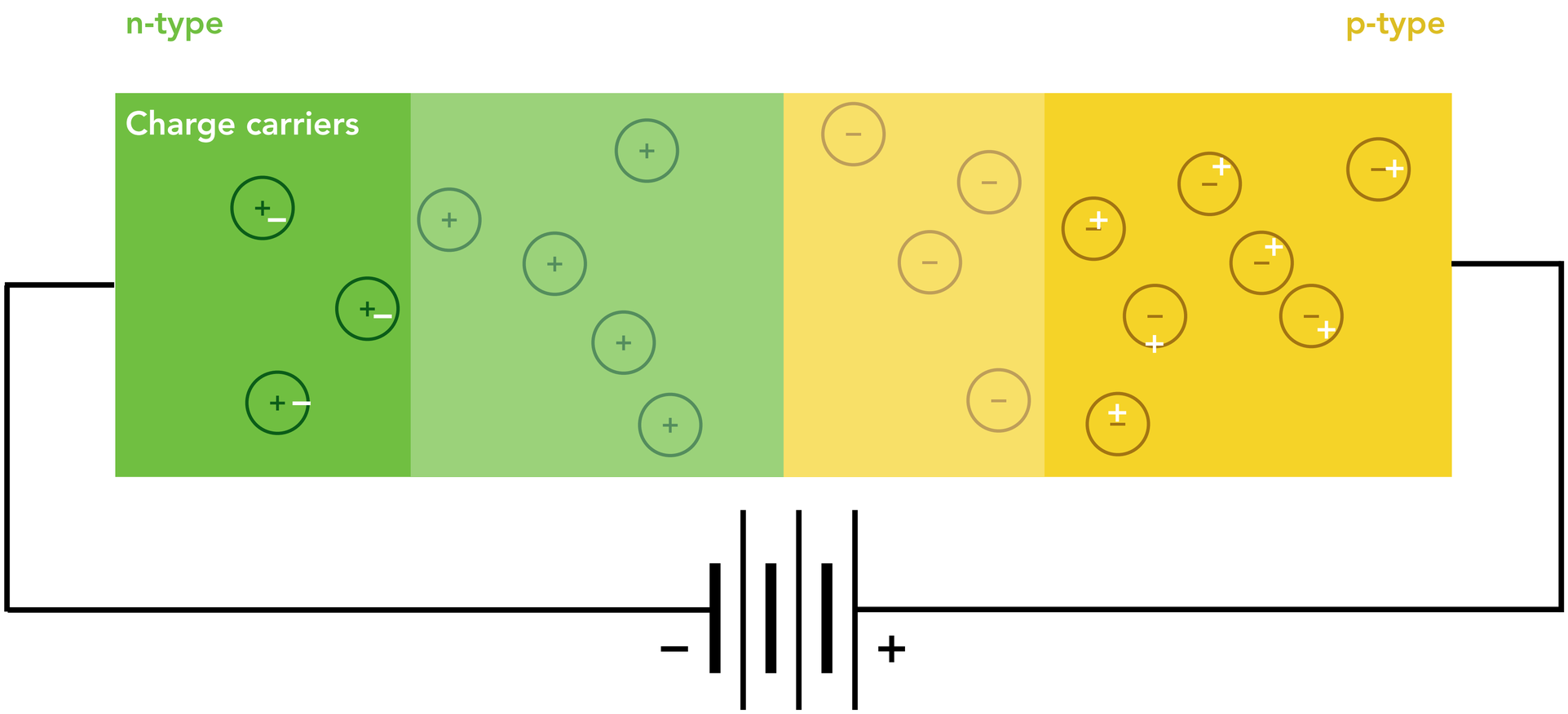
Electron diffusion → ← Electric field acting on electrons

Electric field action on holes → ← Hole diffusion

P-N junctions - built-in depletion



P-N junctions - forward bias



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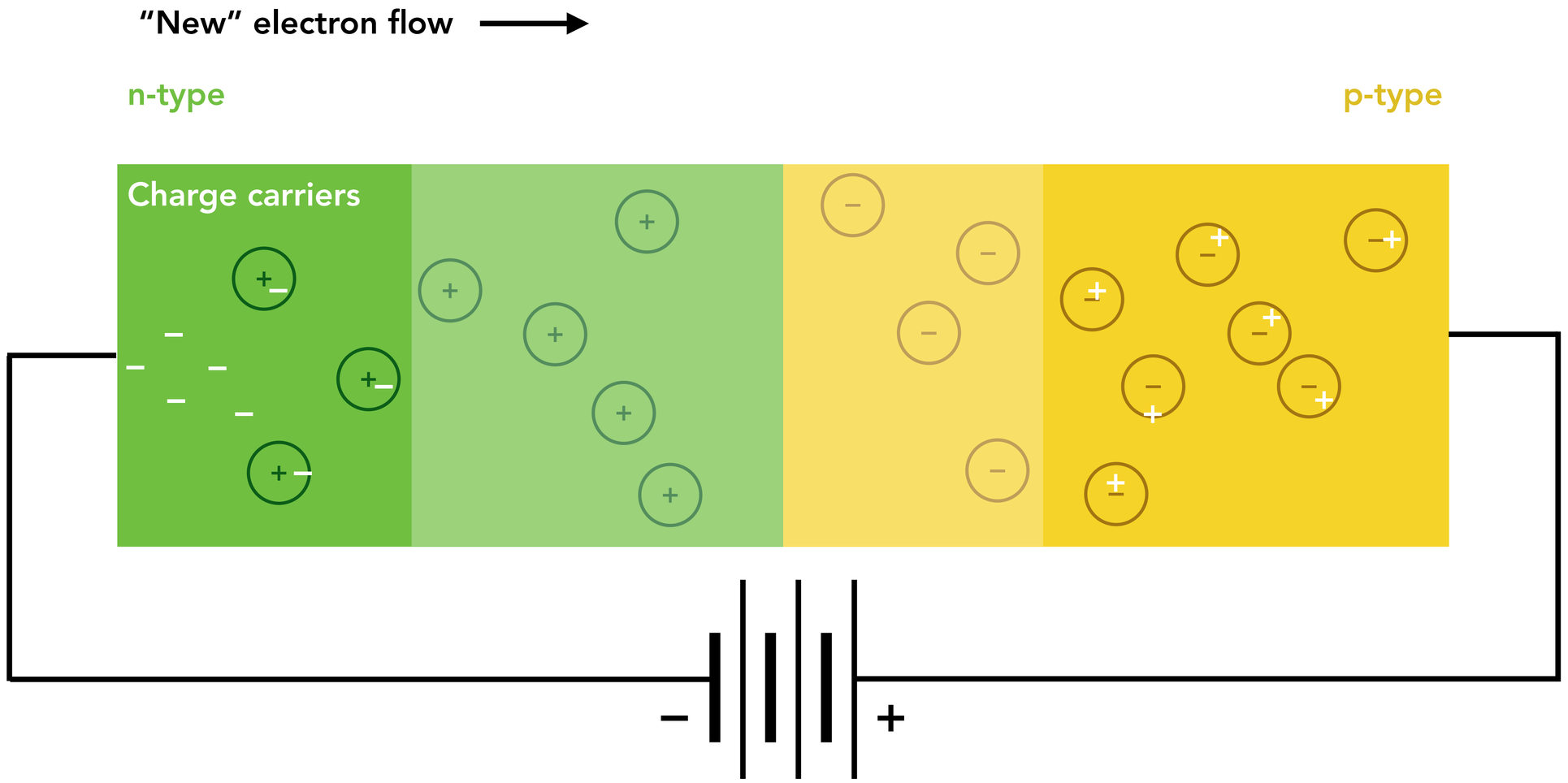

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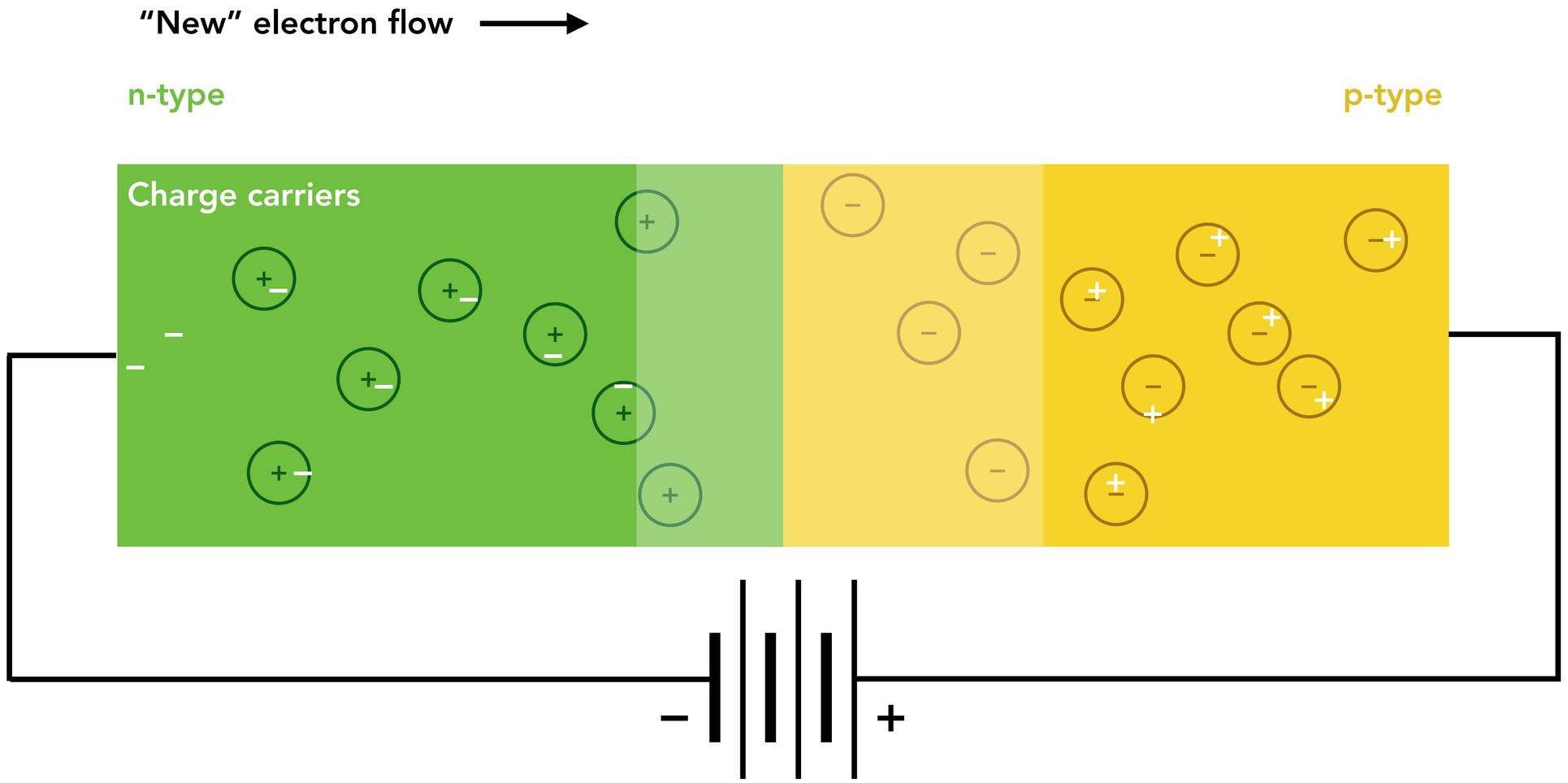

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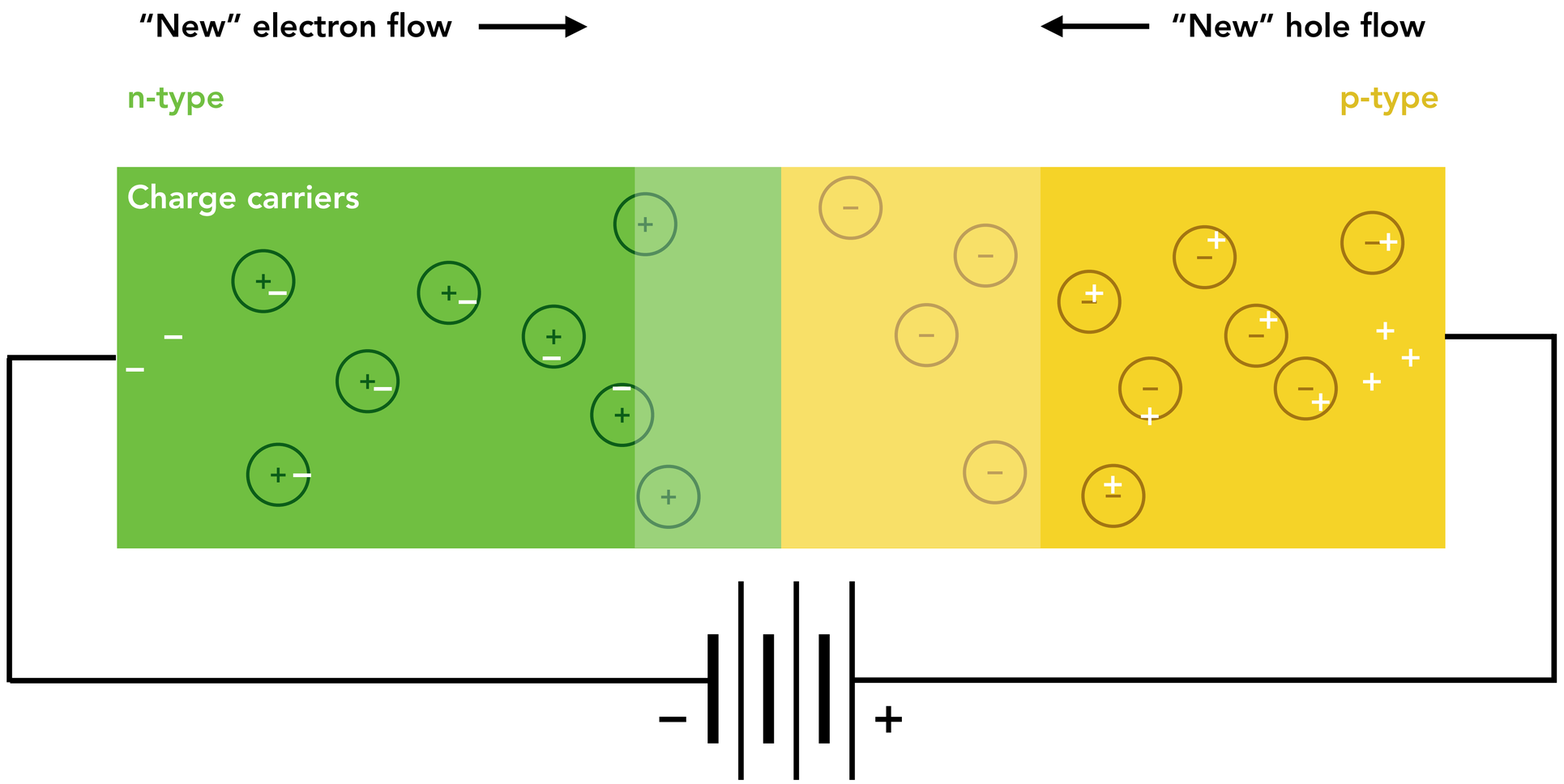

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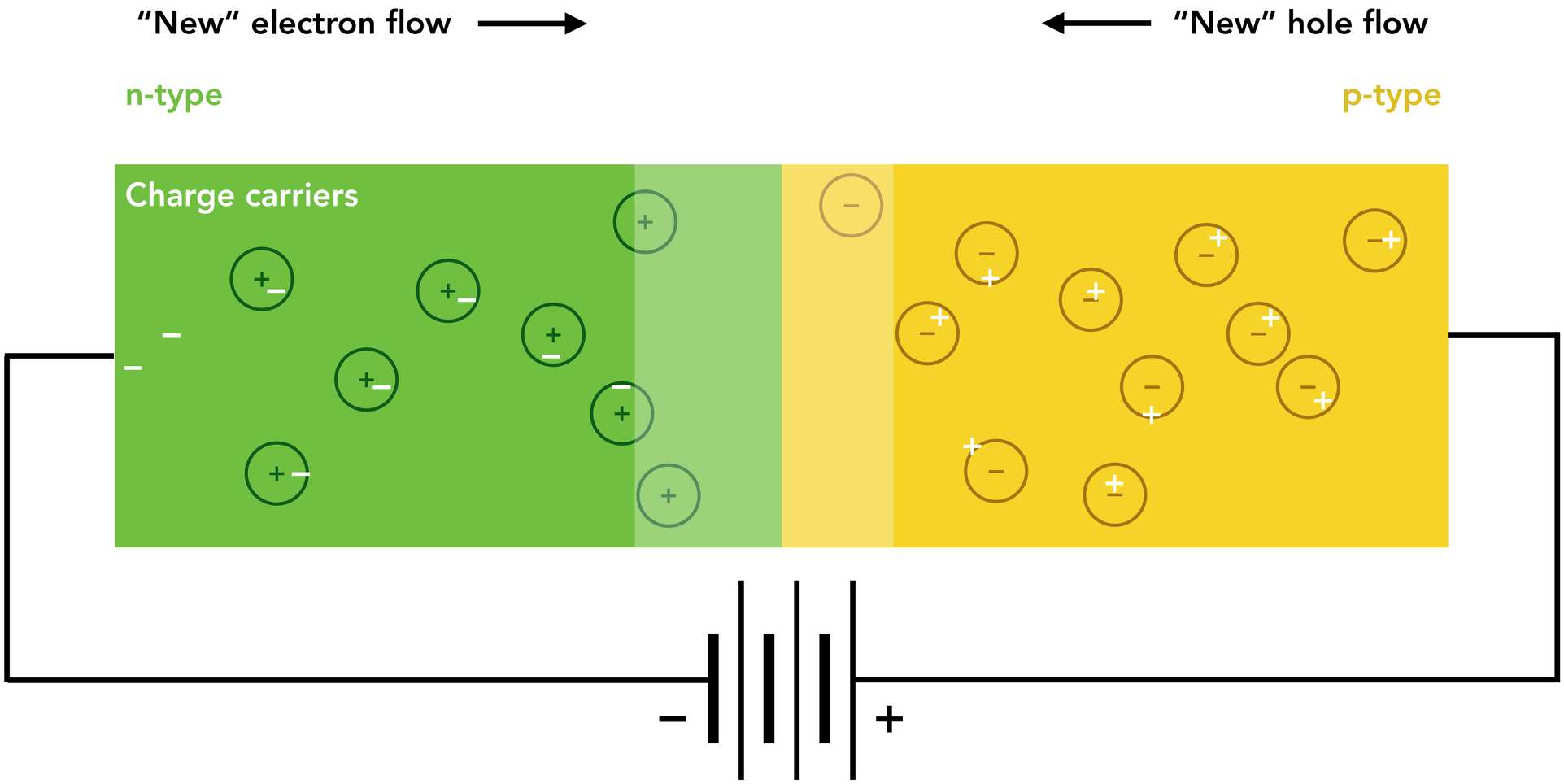
P-N junctions - forward bias



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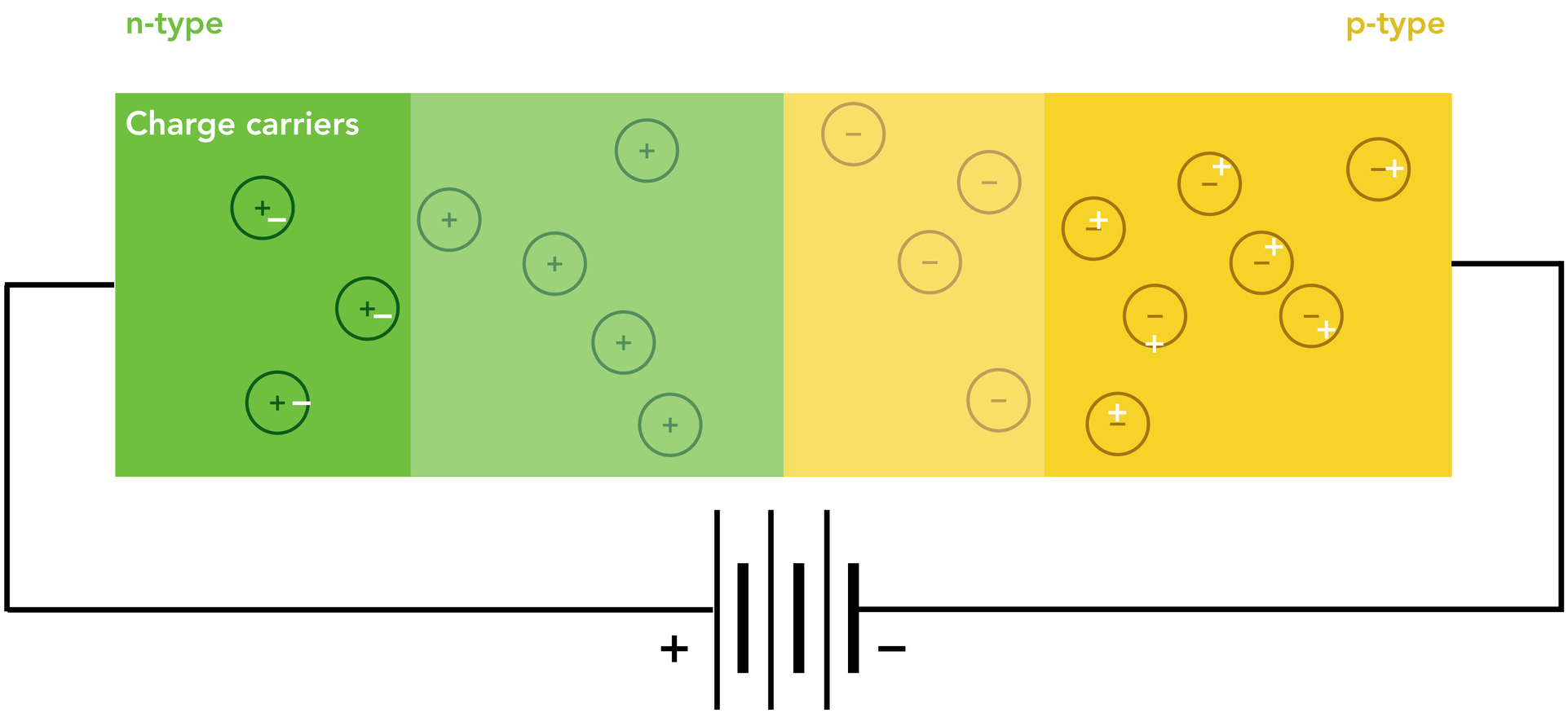

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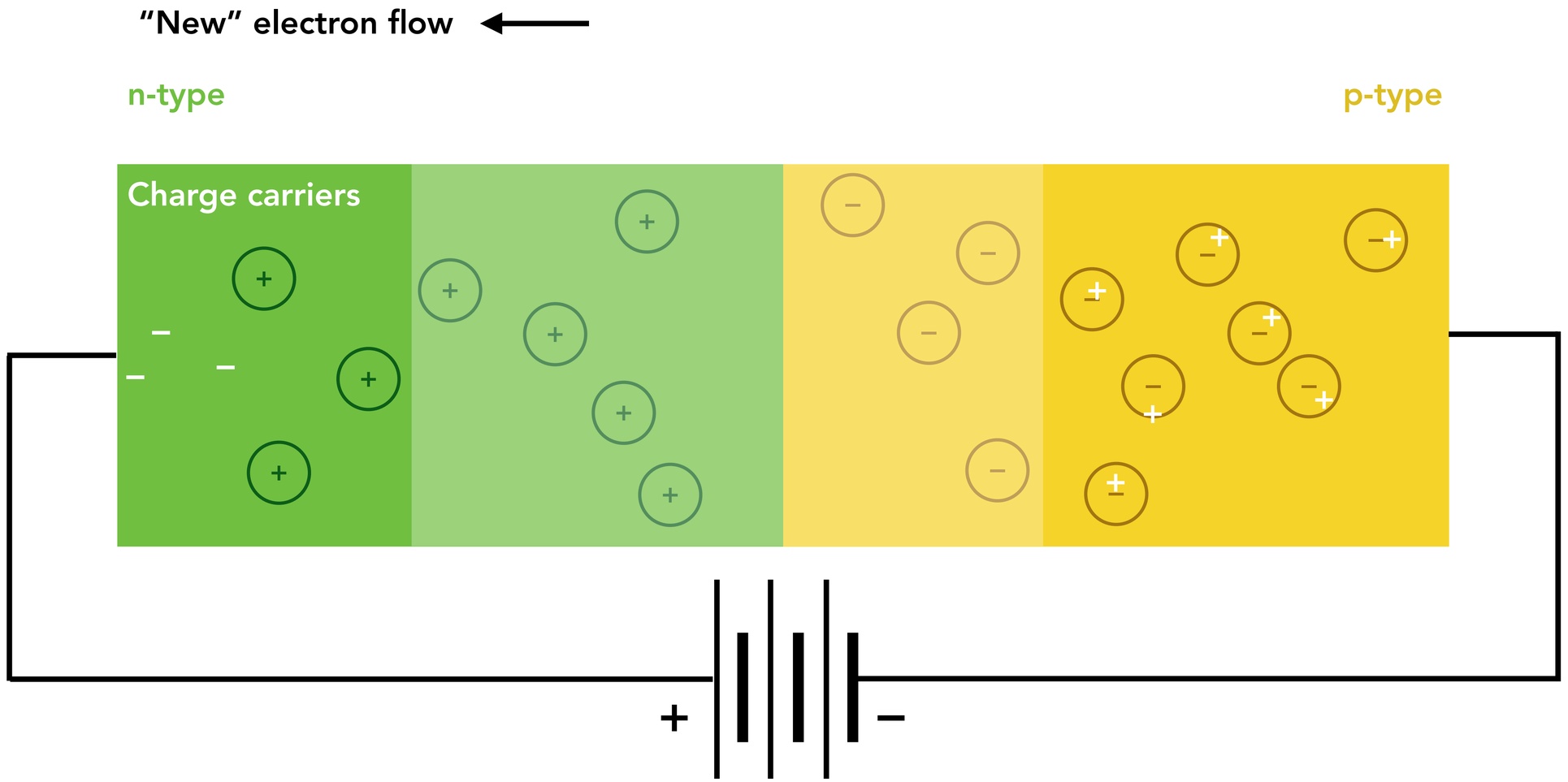

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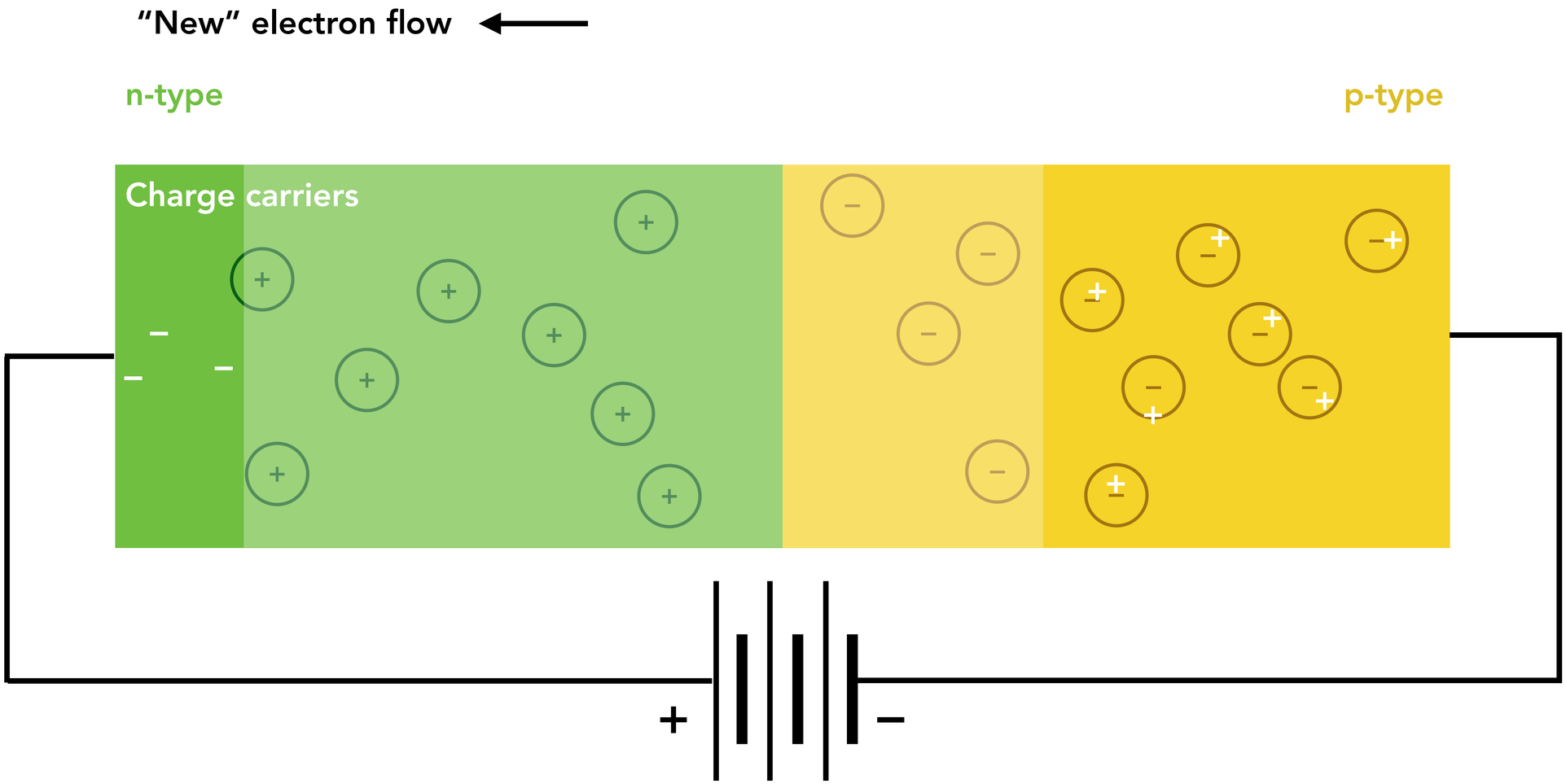

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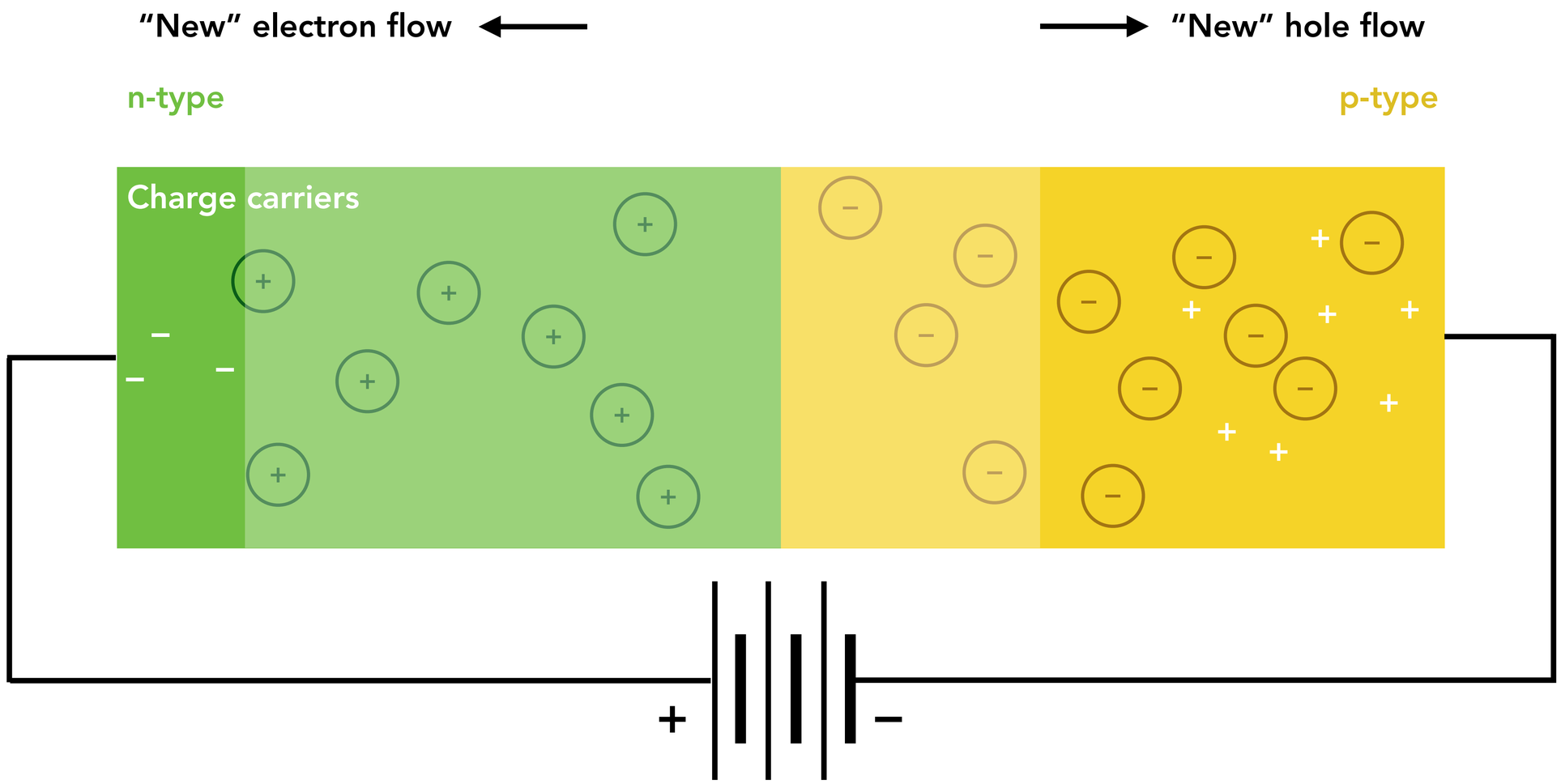

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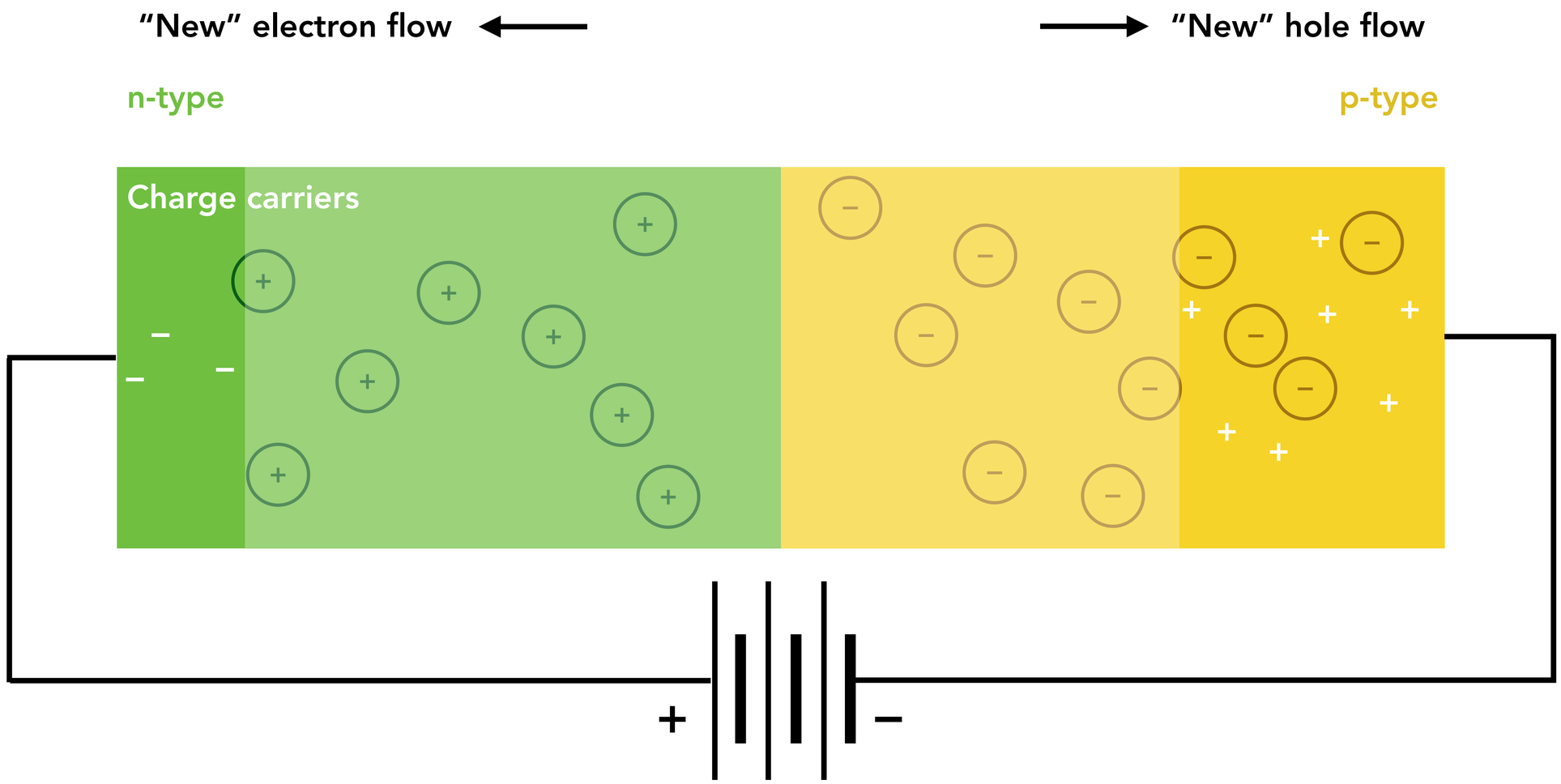

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P-N junctions - external field

Bringing together p-doped and n-doped semiconductors will give rise to a natural region free of charge carriers between the two

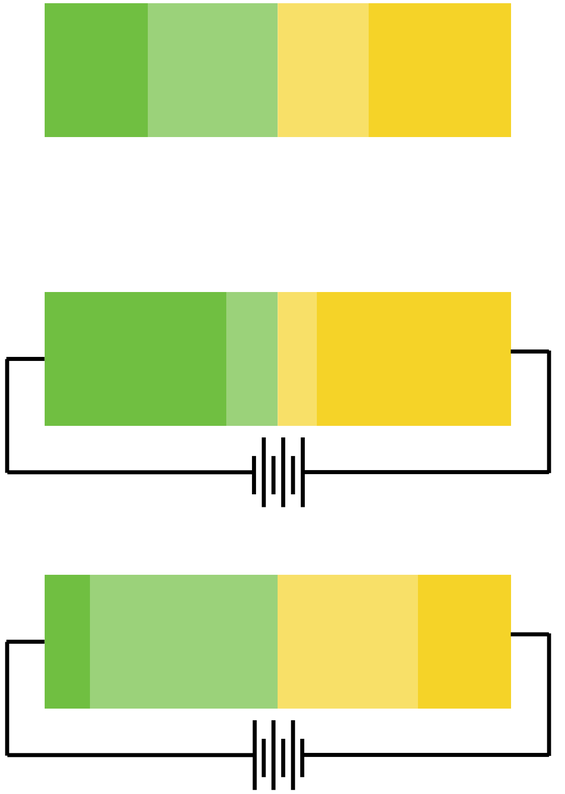
- This built-in depletion region contains an electric field which counters the diffusion of more carriers across the junction

We can forward bias the junction to reduce the depletion width

- Current will flow through the junction once the depletion width has been reduced to 0

We can reverse bias the junction to increase the depletion width

- If one of the regions has no carriers left then it can be said to be fully depleted



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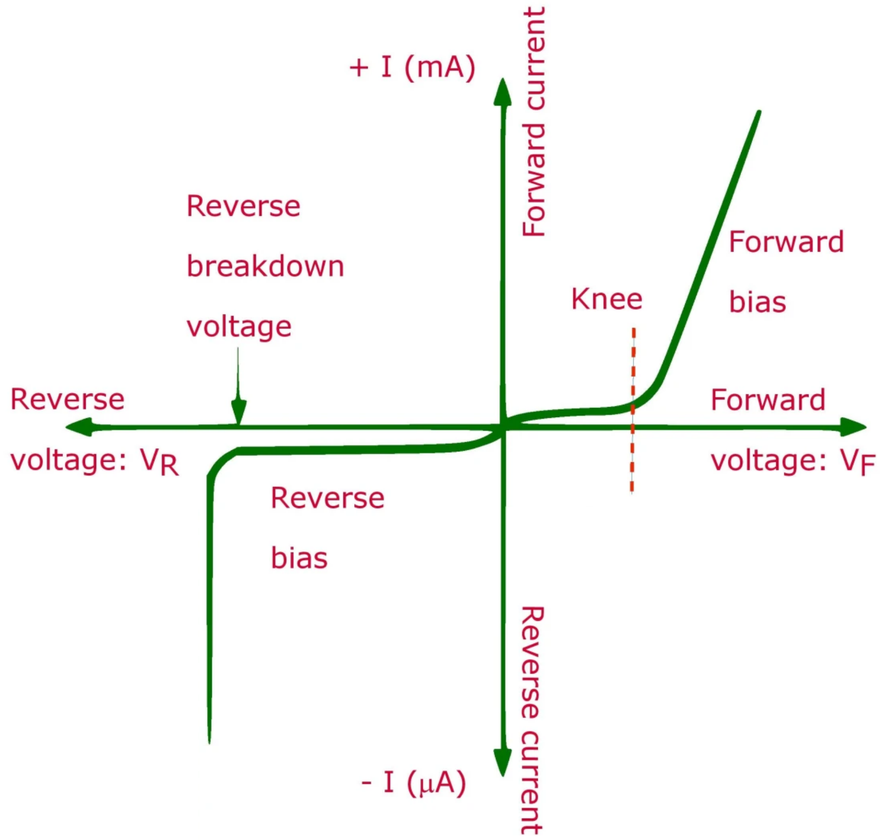
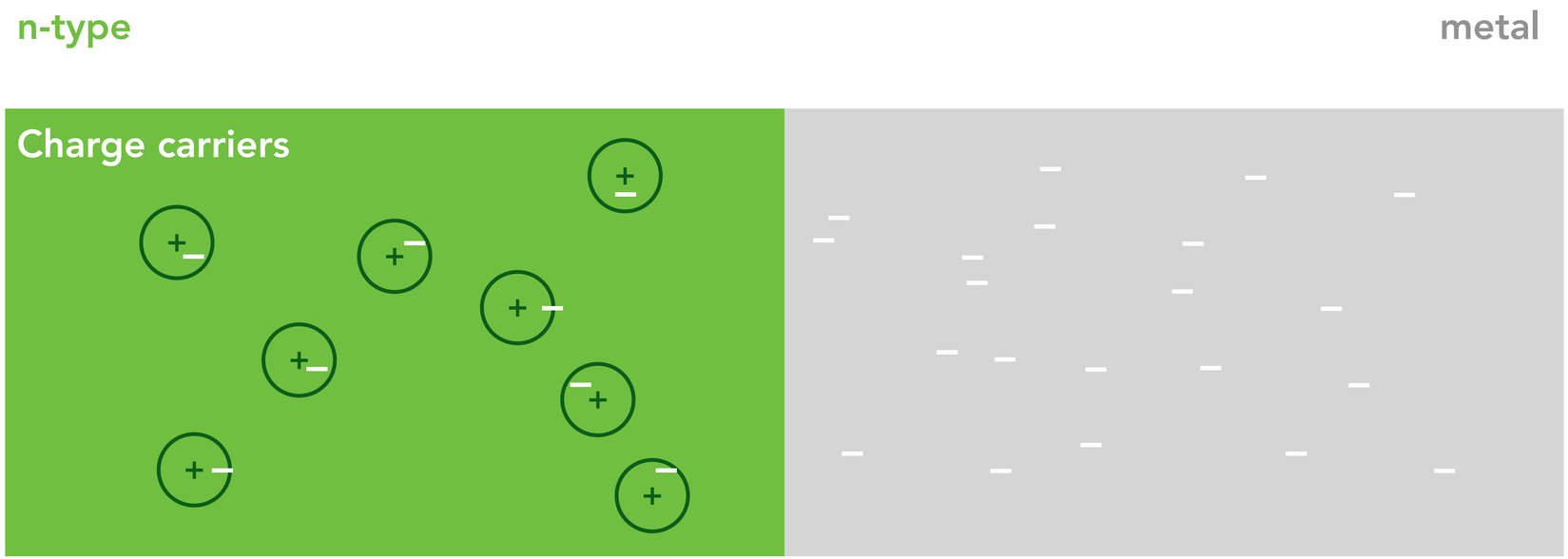


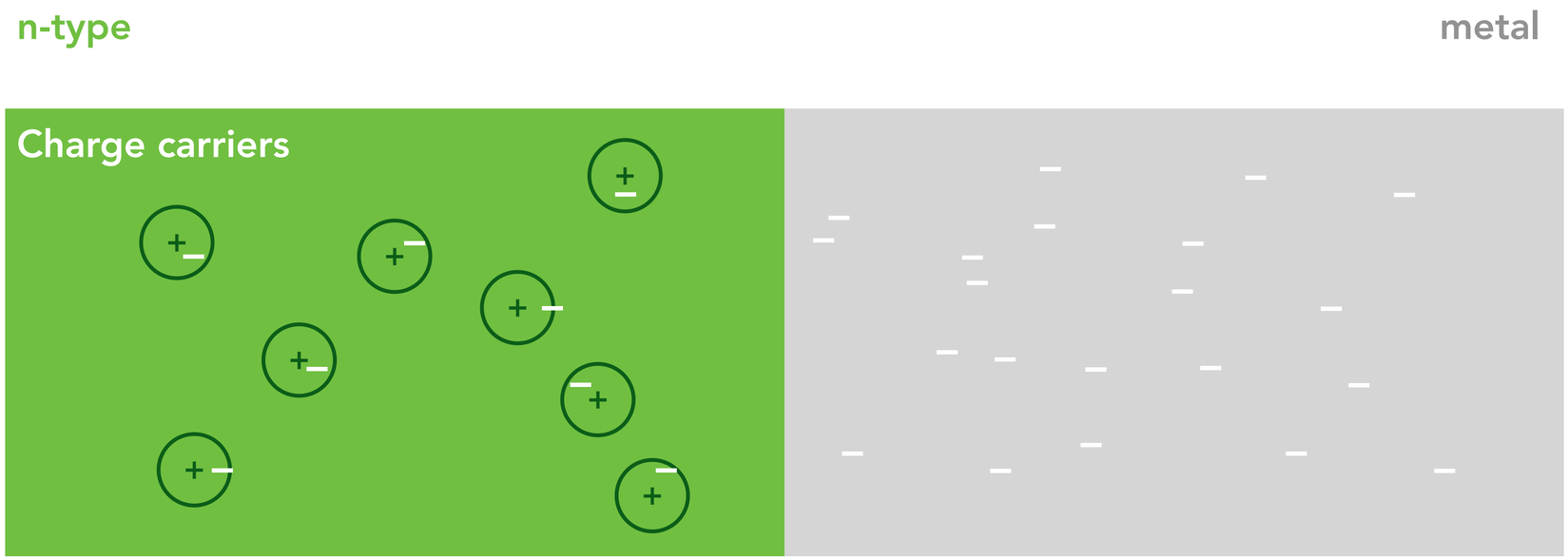
Semiconductor-metal junctions

S-M junctions



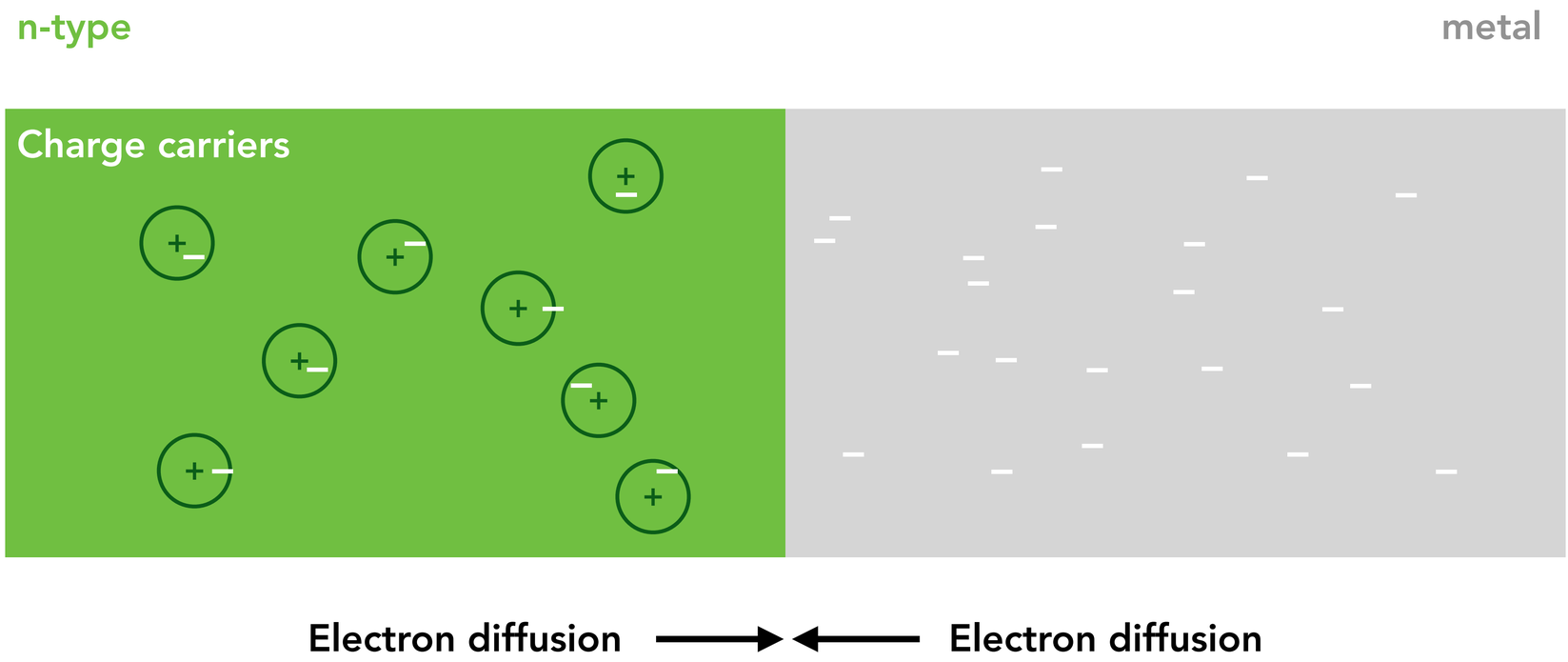
Question: how hard is it to move electrons from (say) the metal to the semiconductor?

S-M junctions



Consider the case where it is **easy** to move from the metal to the semiconductor

S-M junctions - carrier movement



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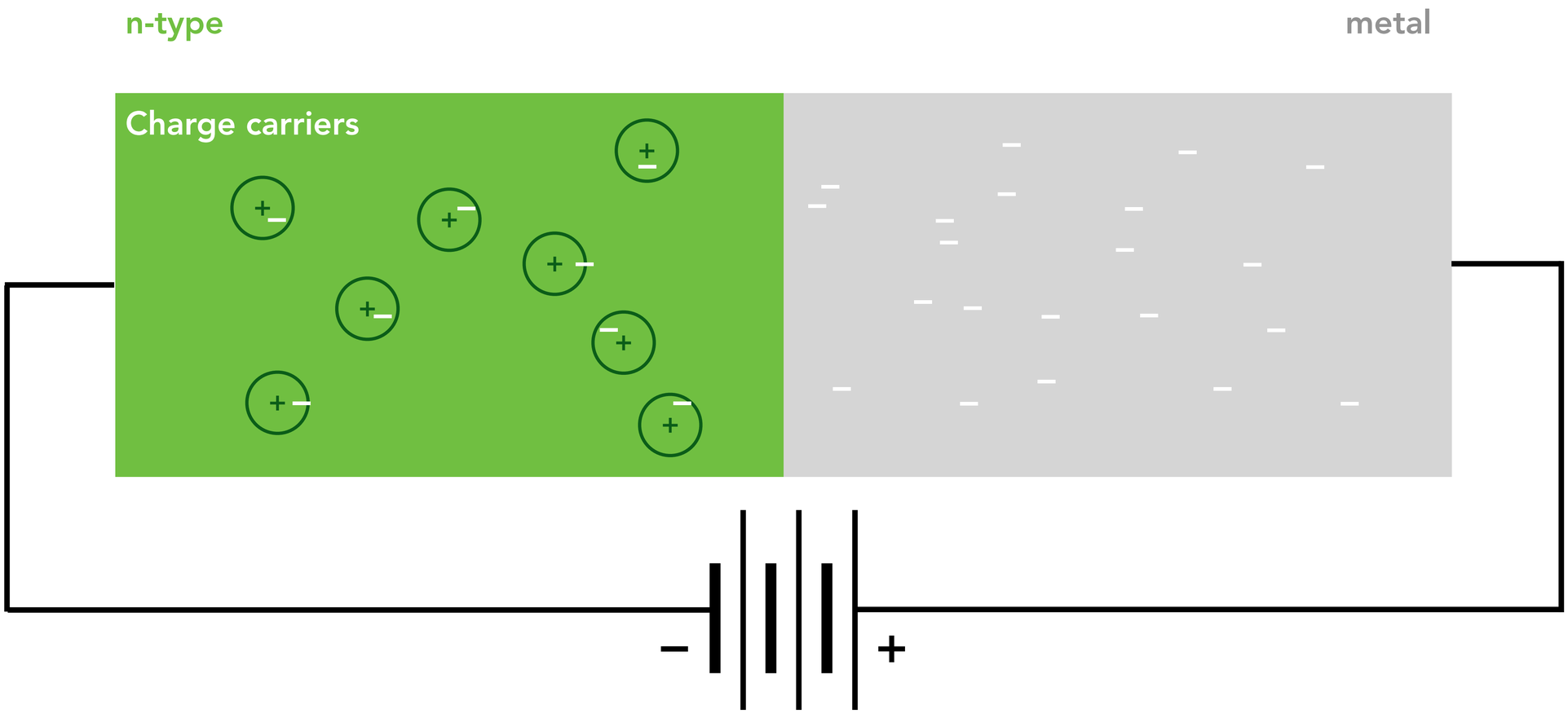
S-M junctions - forward bias



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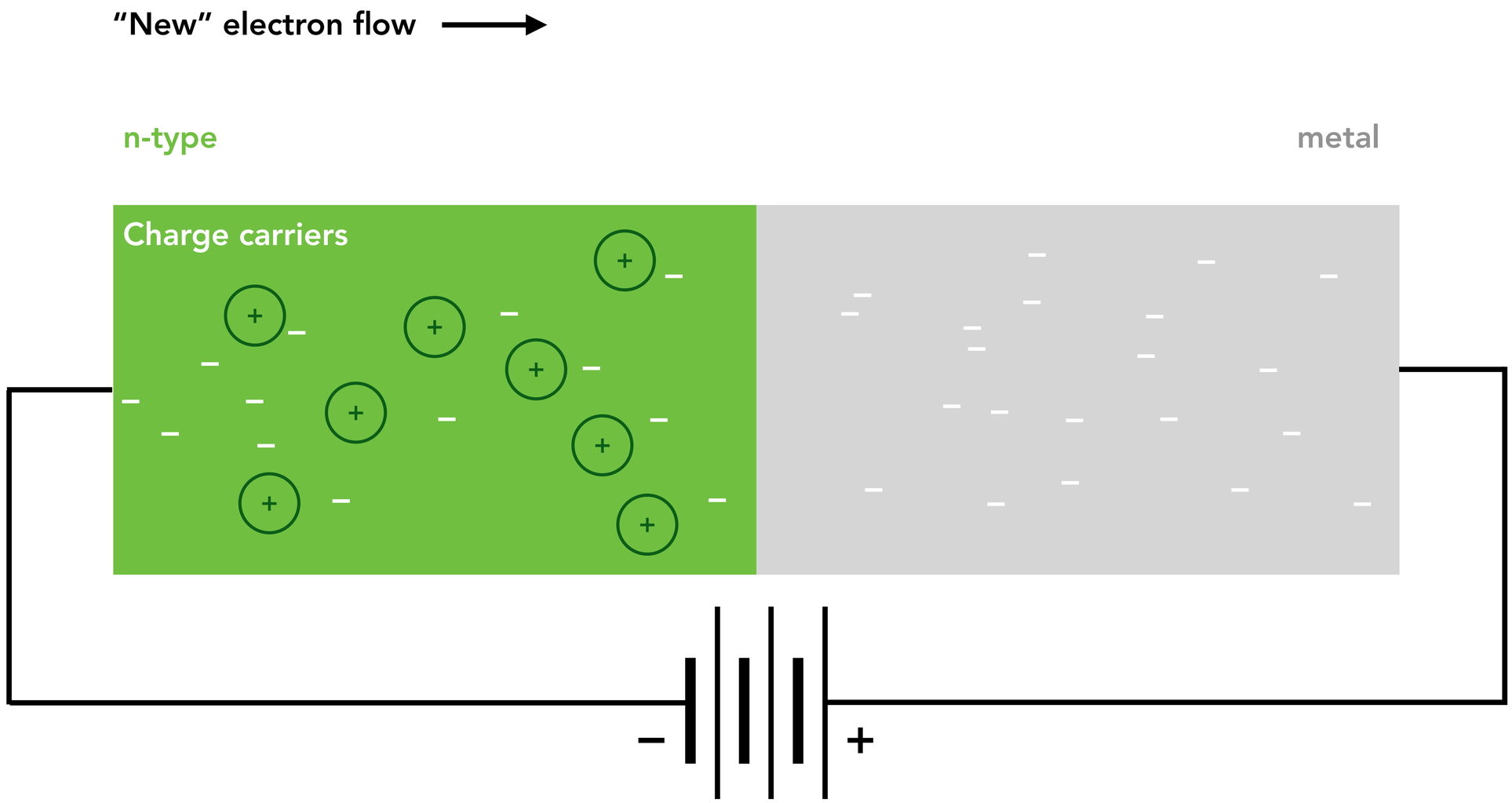
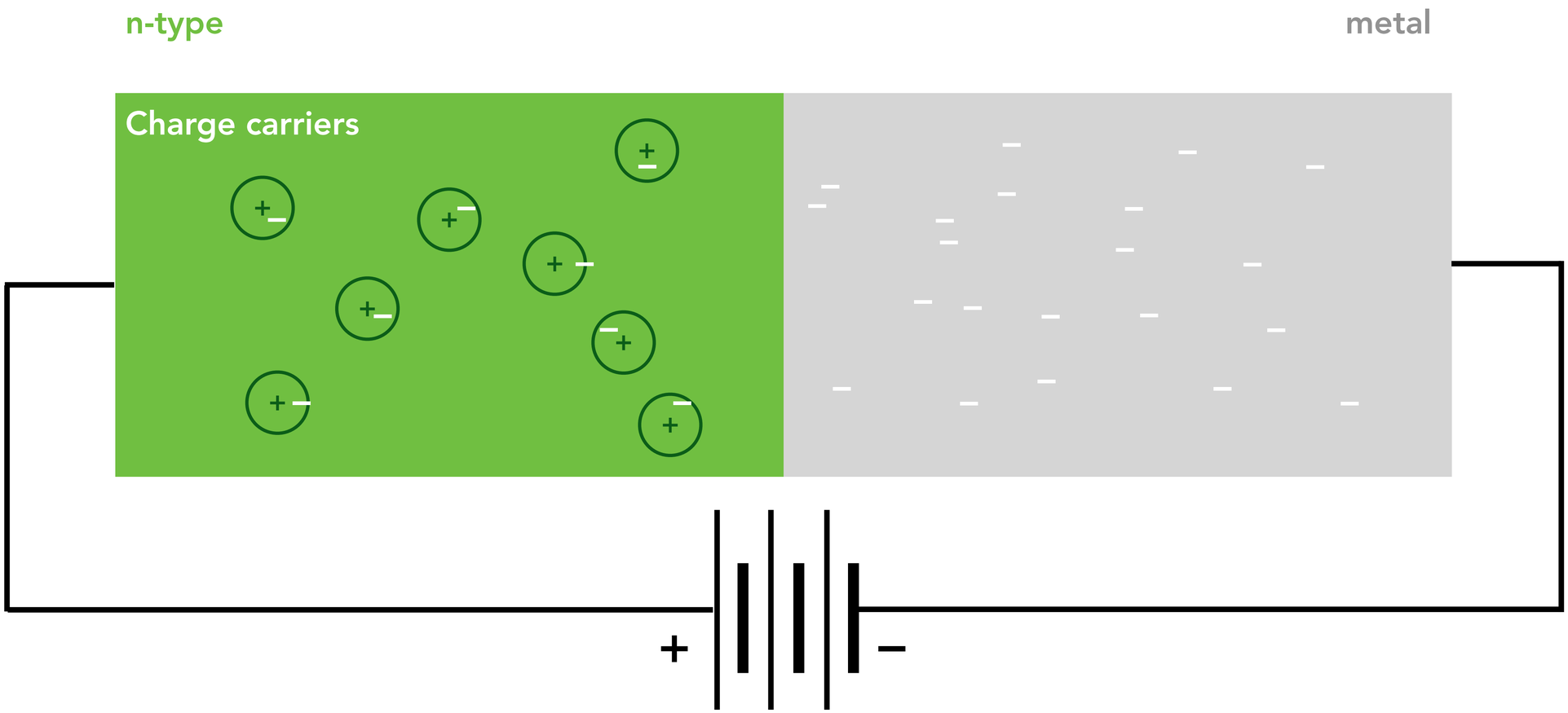


S-M junctions - reverse bias



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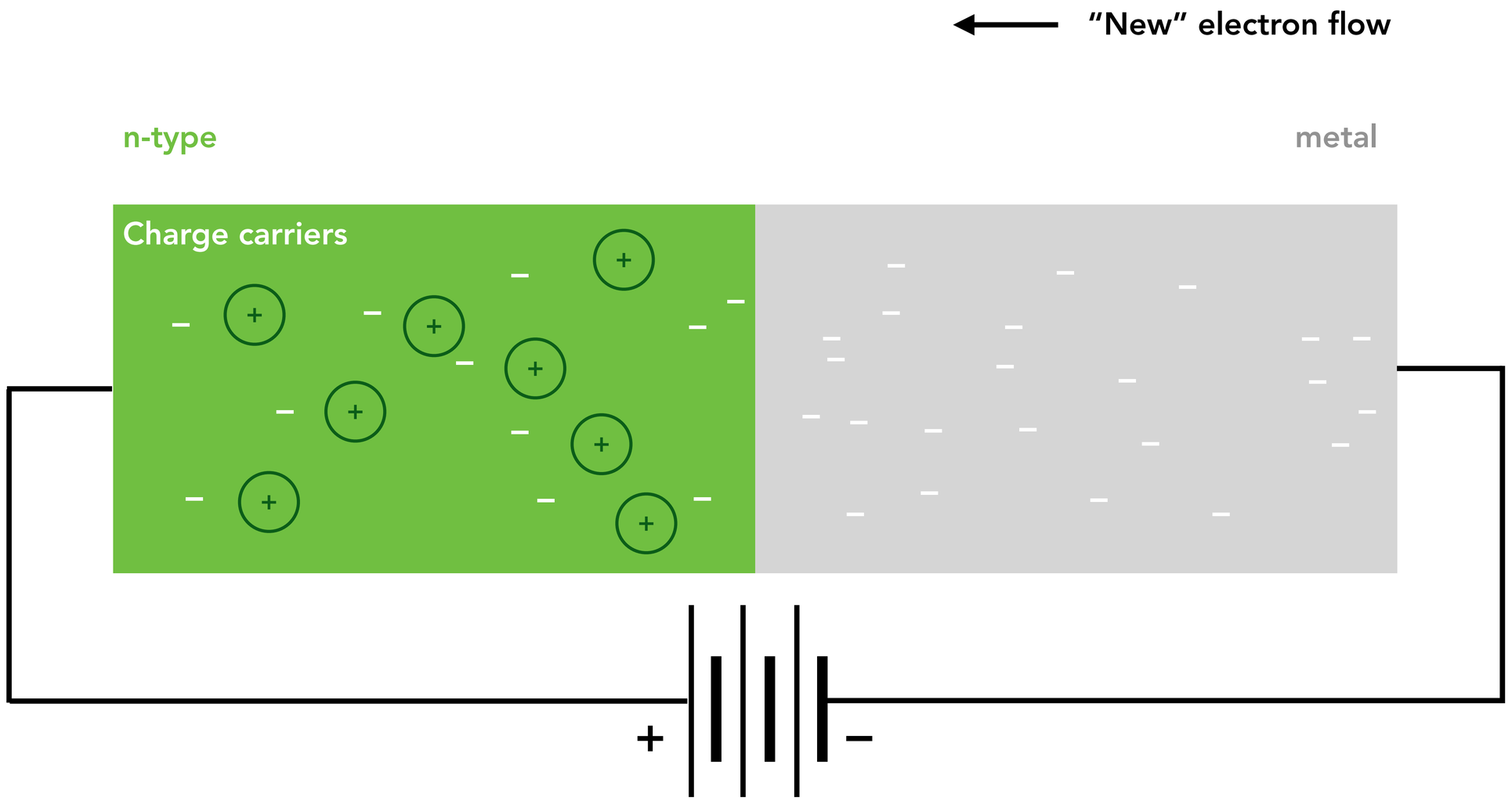

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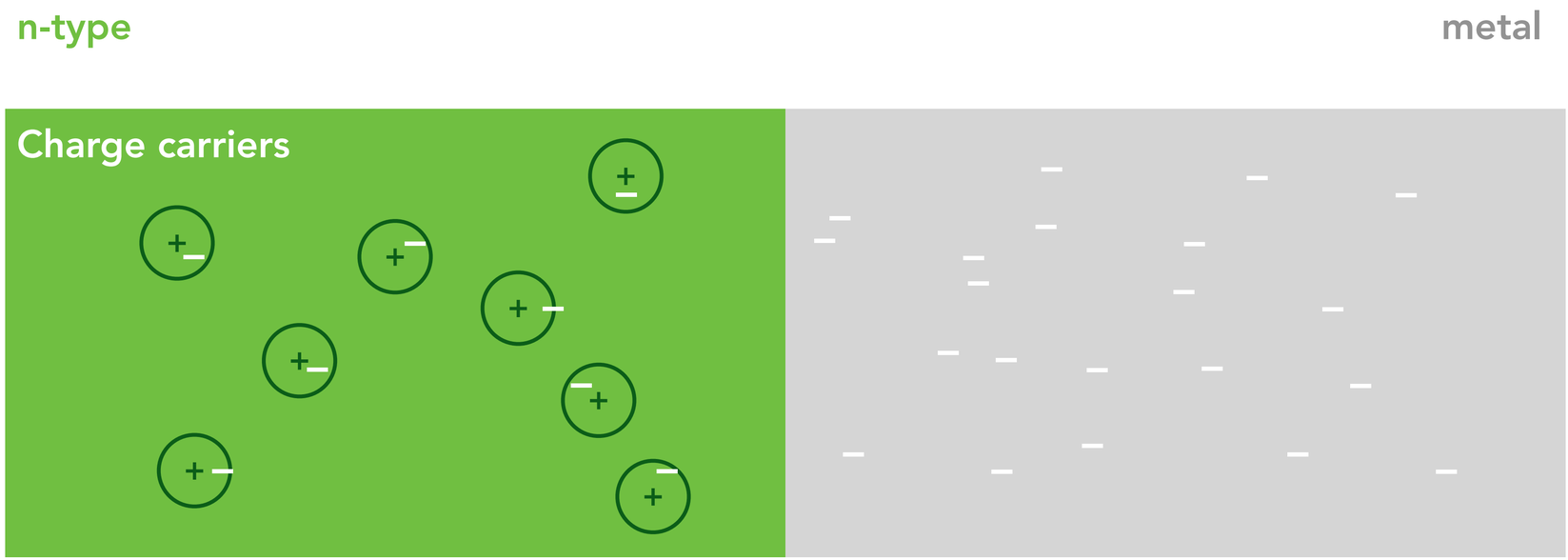
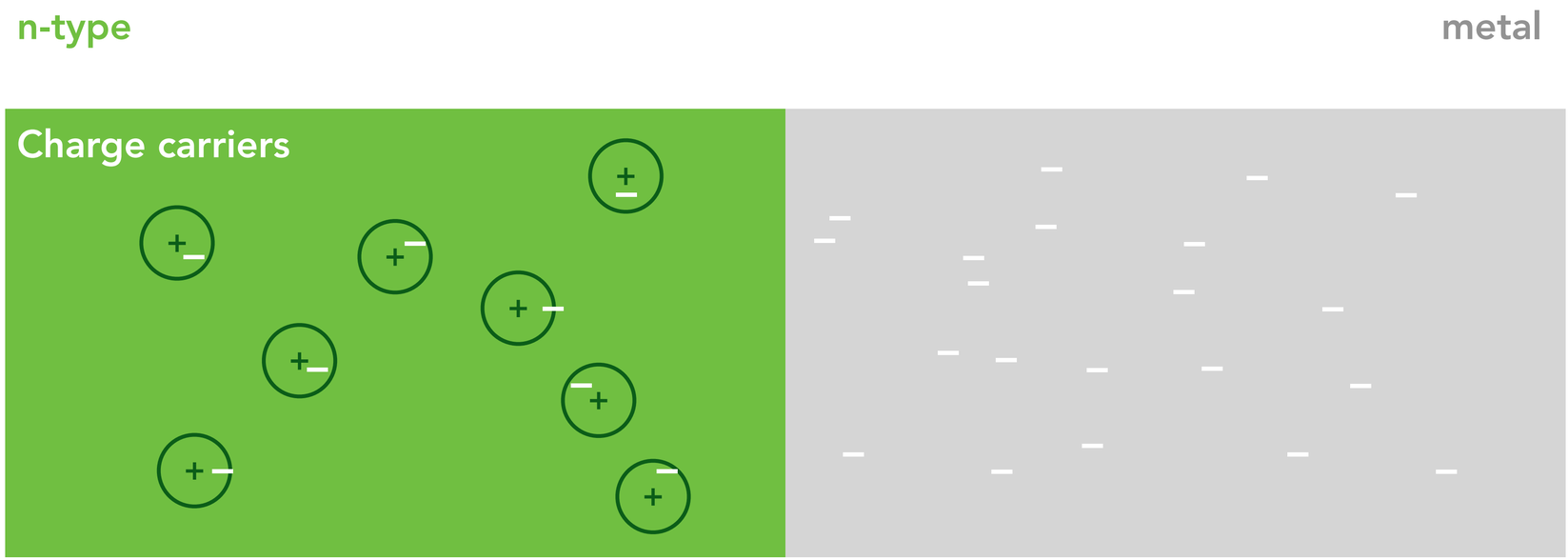


Consider the case where it is **easy** to move from the metal to the semiconductor

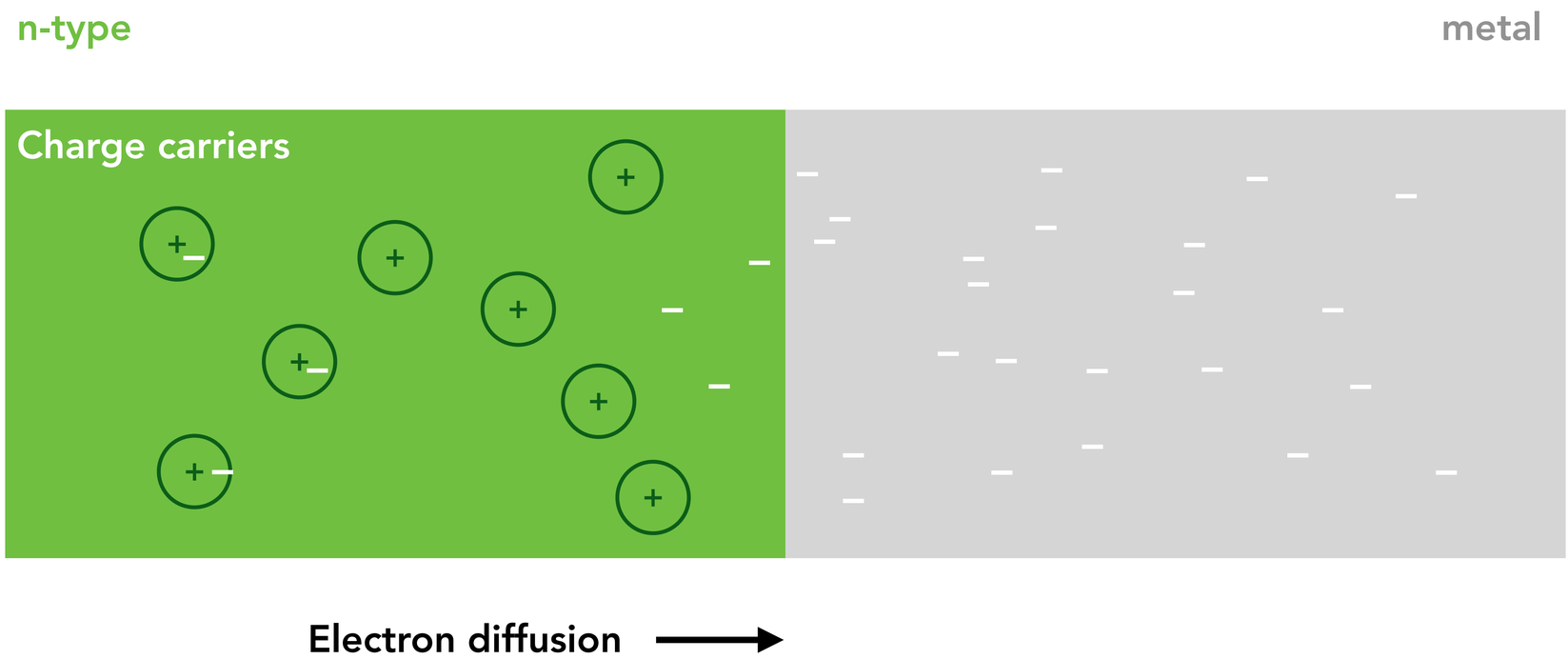
An **Ohmic contact** is created

S-M junctions



Consider instead the case where it is **difficult** to move from the metal to the semiconductor

S-M junctions - carrier movement



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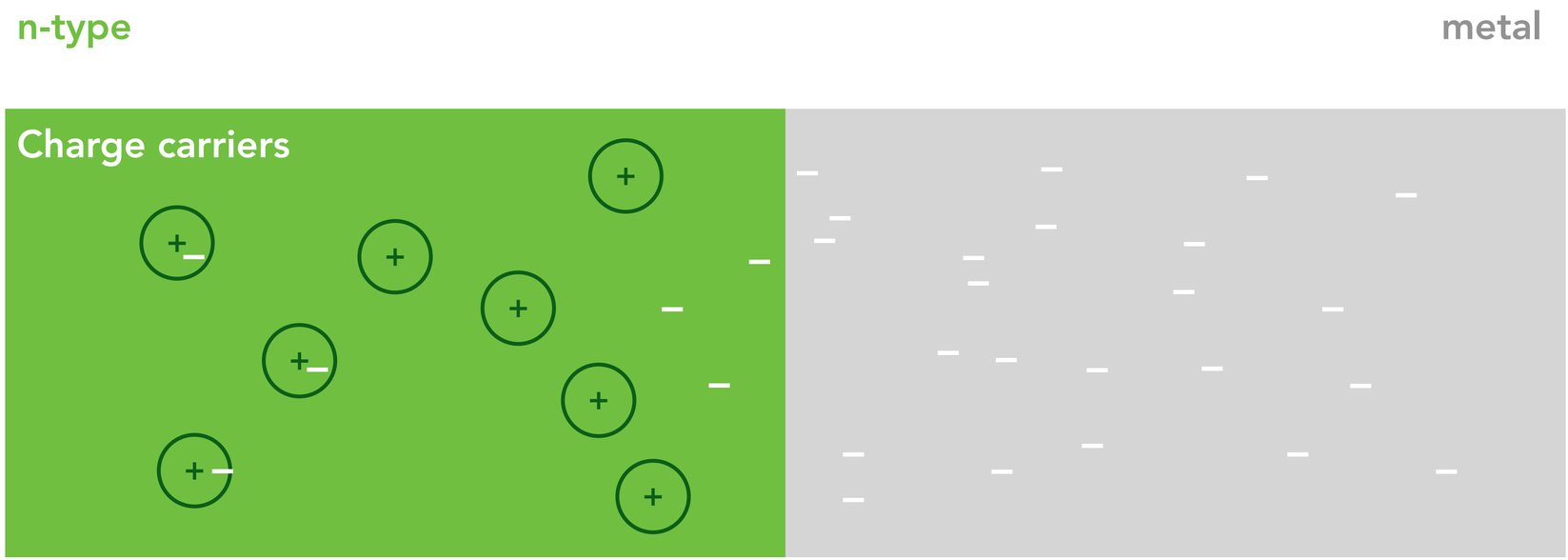
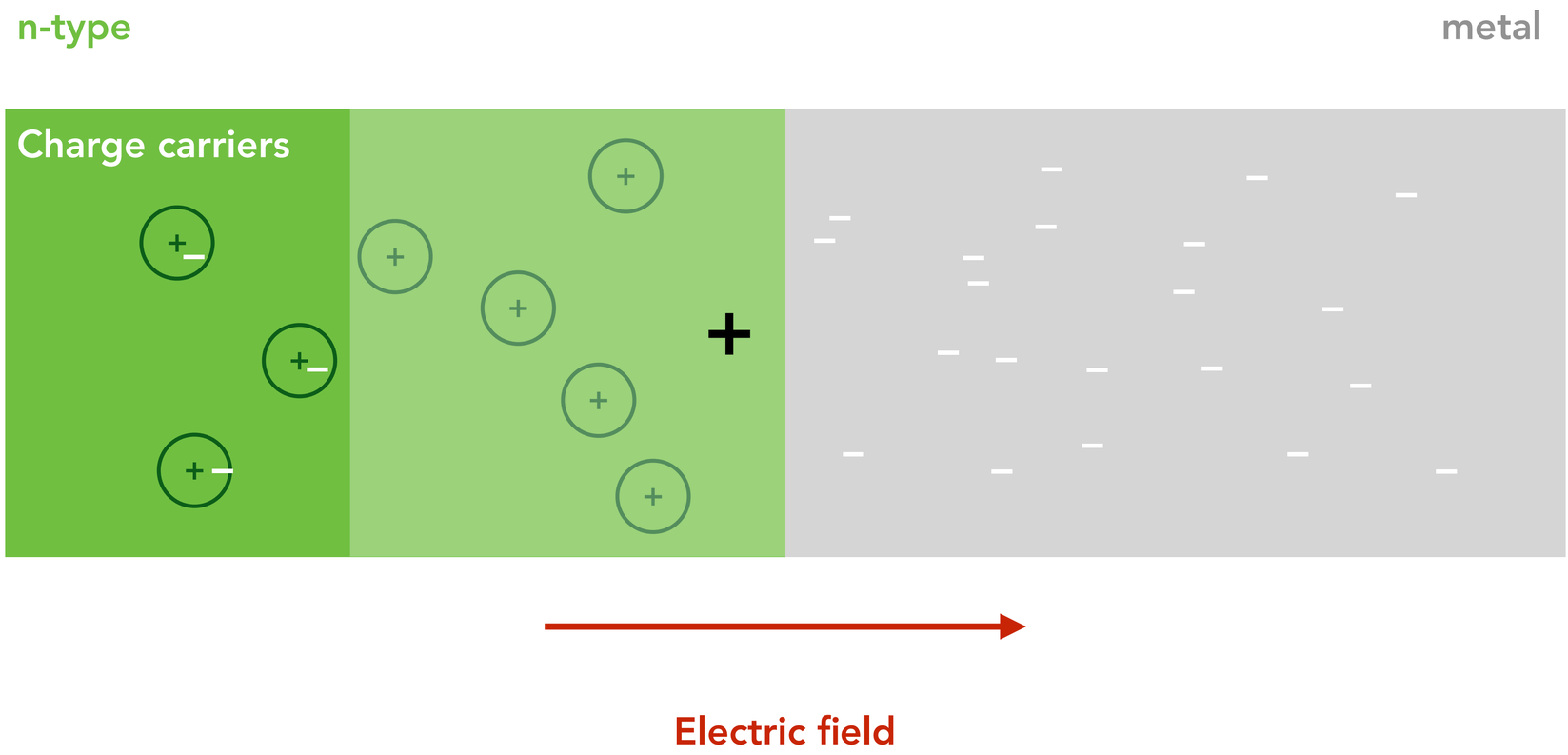


Electron diffusion → ← ~~Energy barrier~~

S-M junctions - carrier movement



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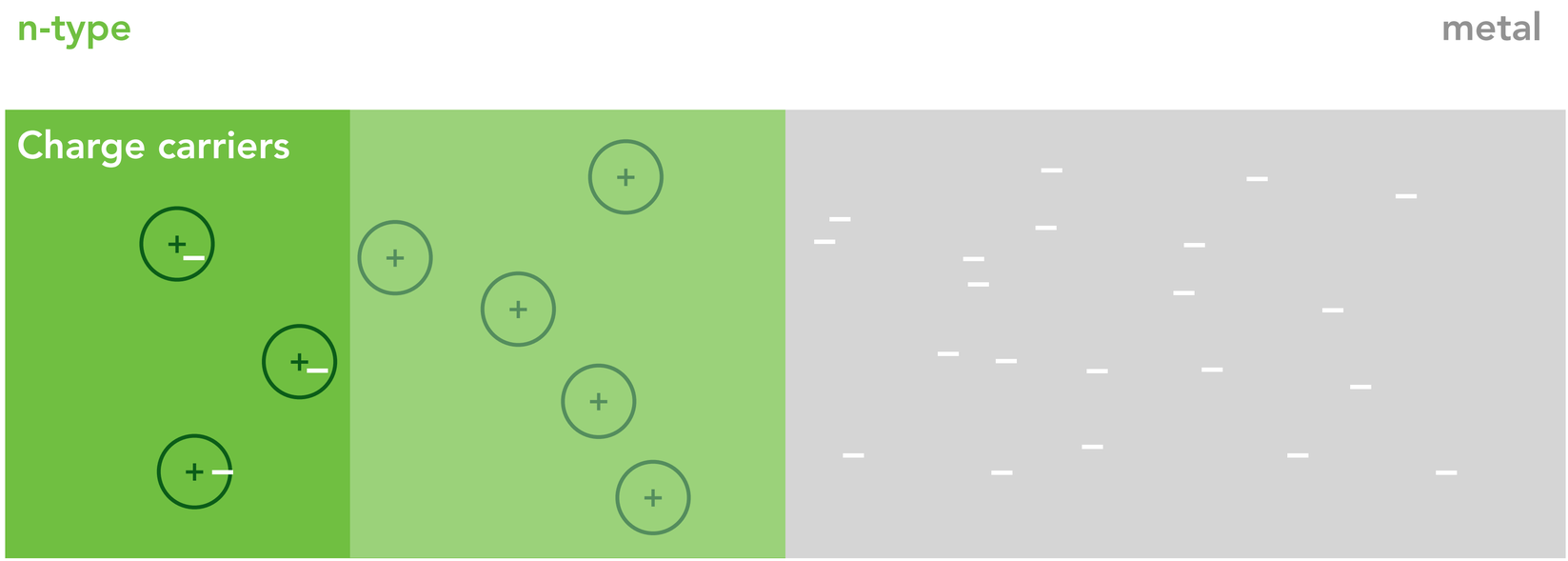

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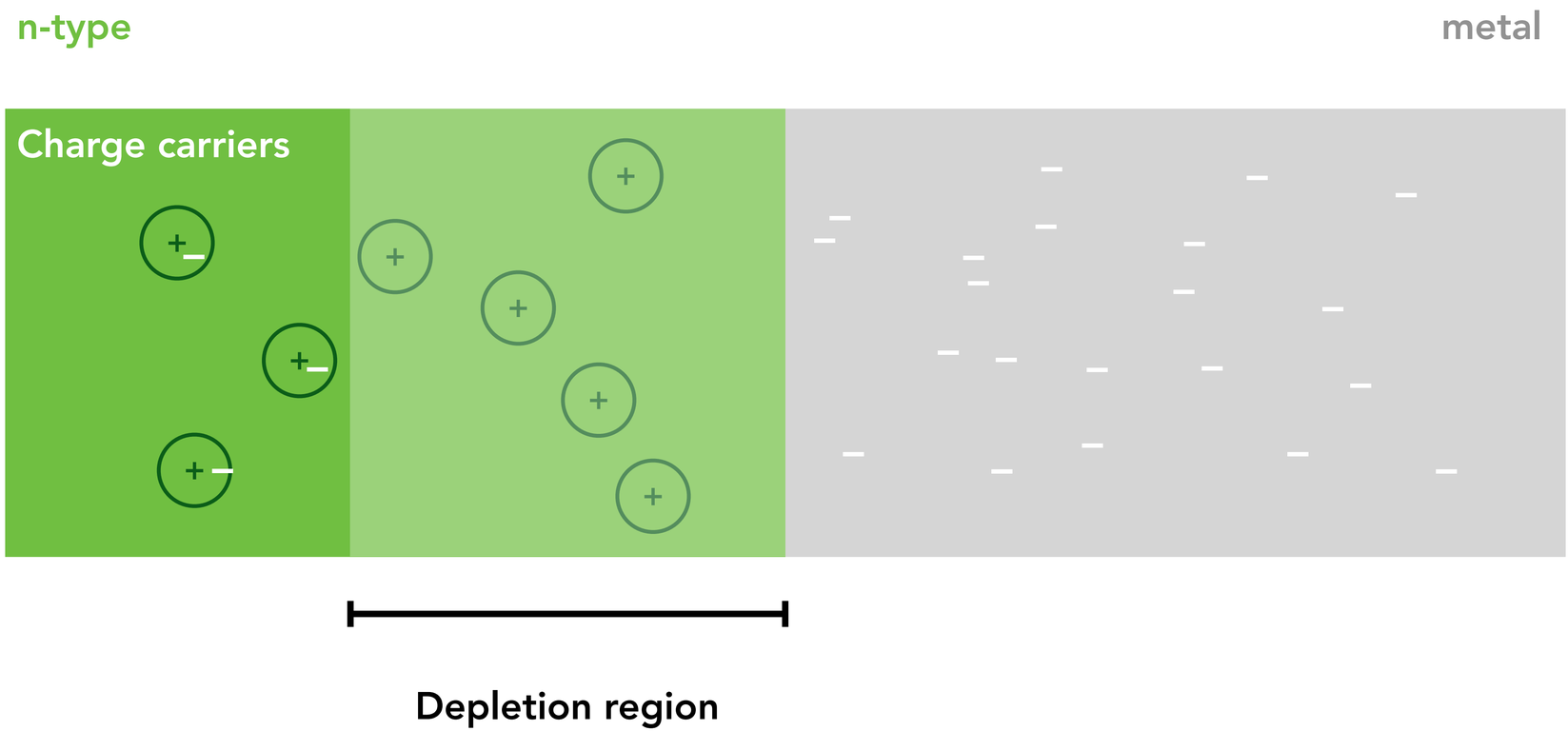

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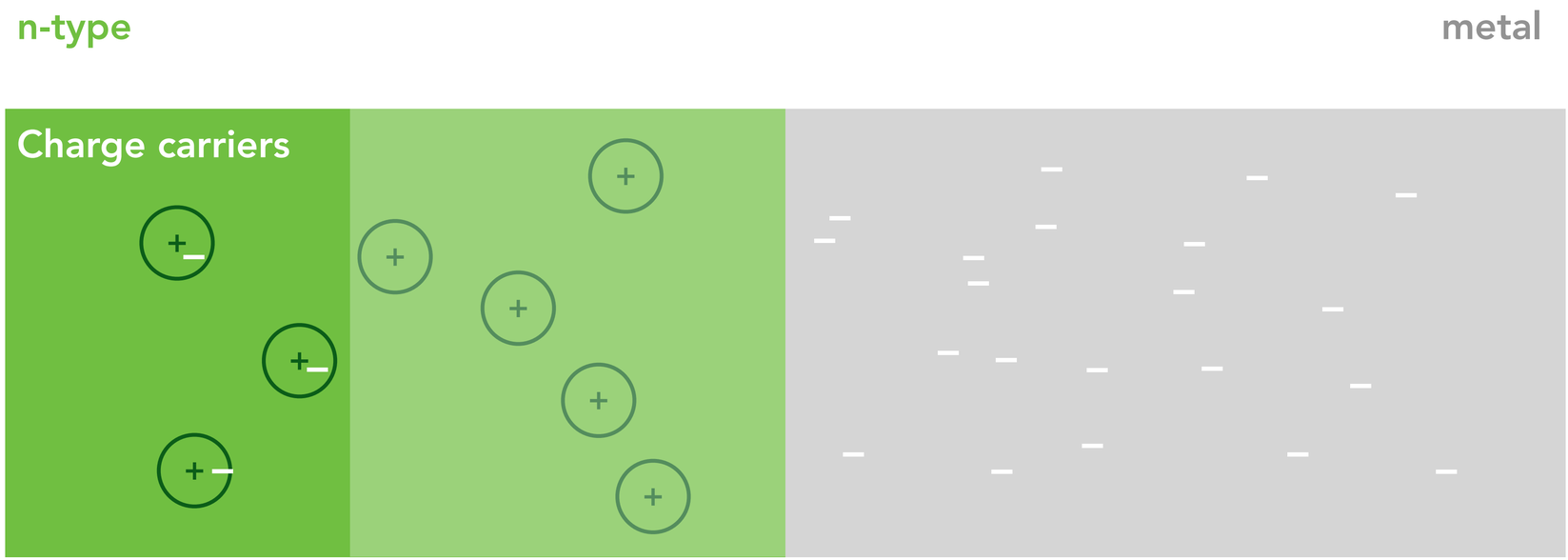

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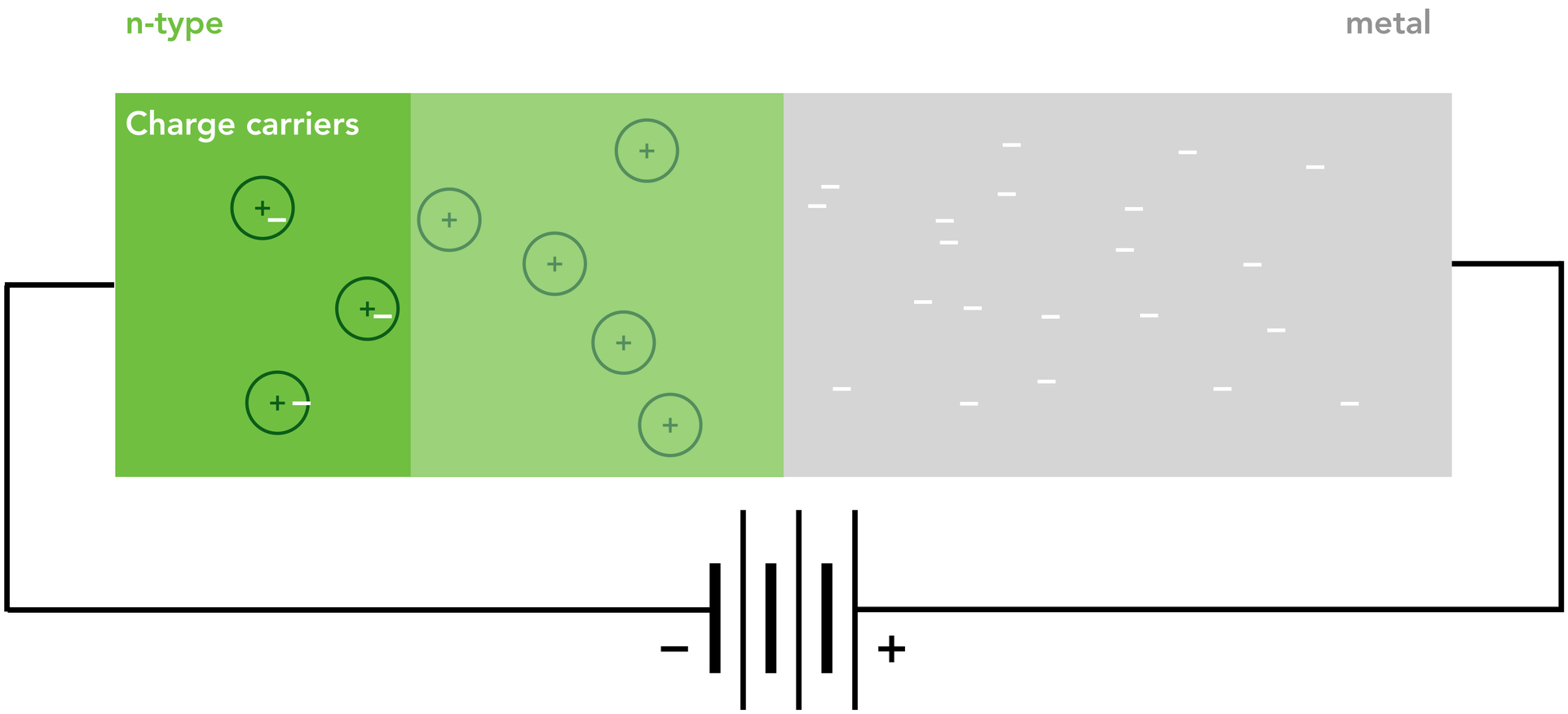
A **Schottky contact** is created

Schottky junctions - forward bias



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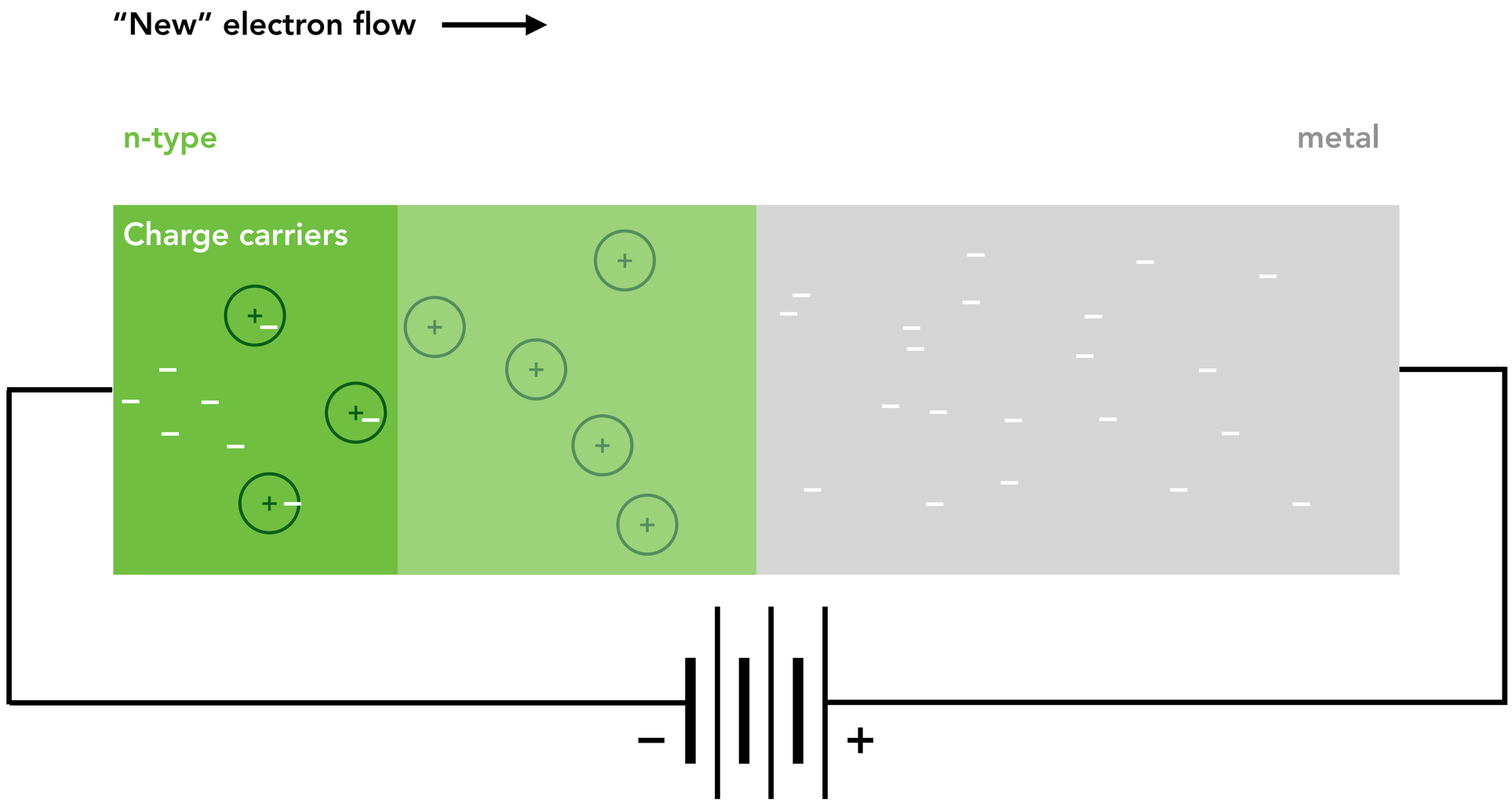

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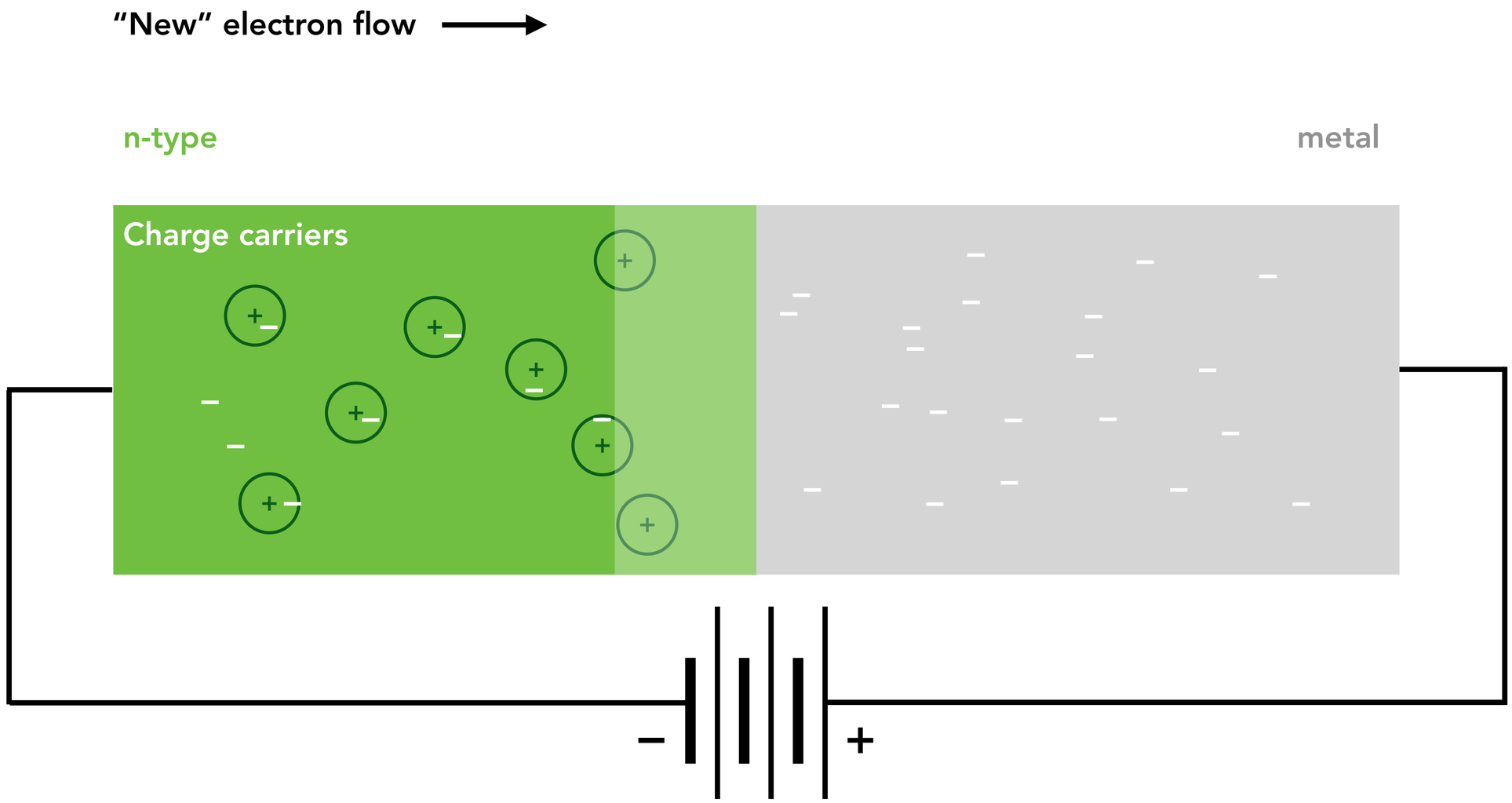

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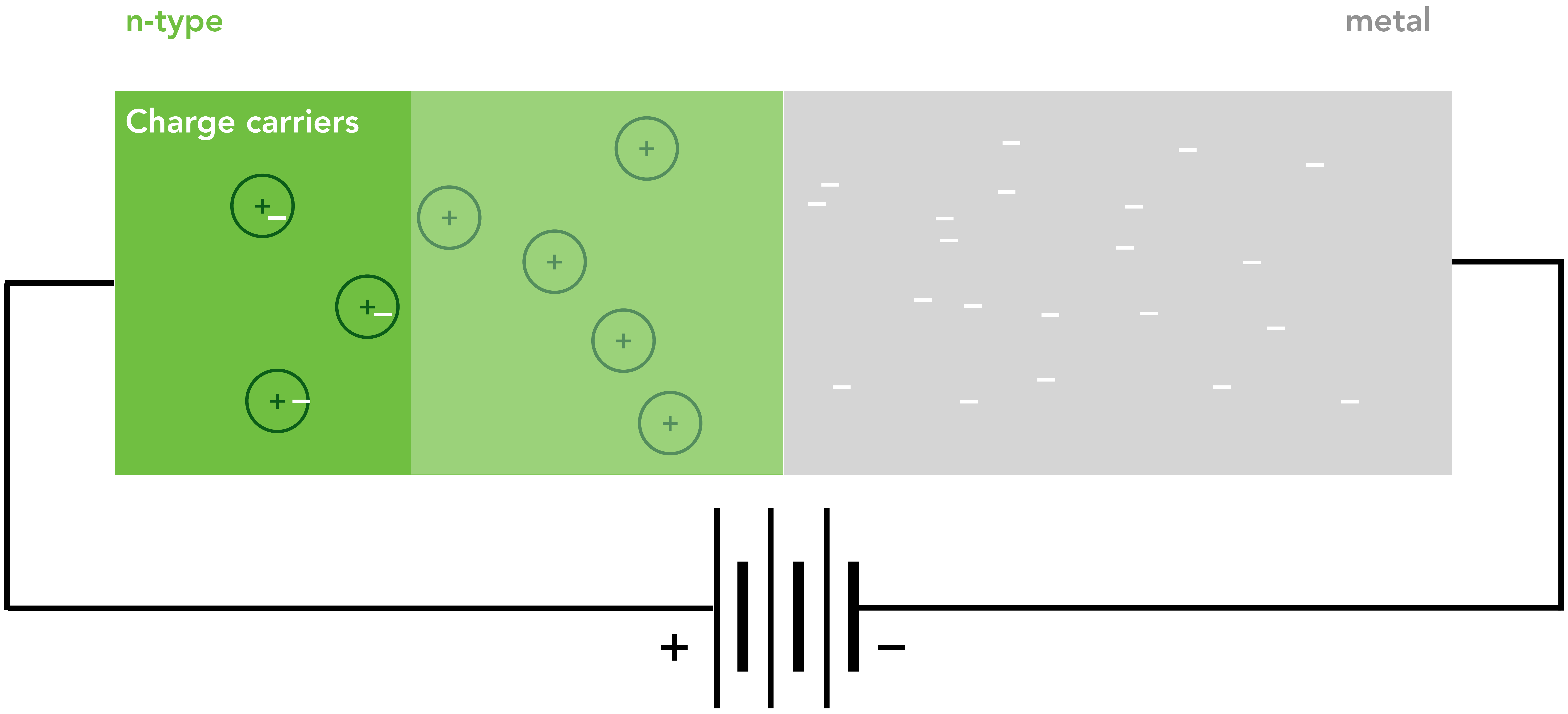

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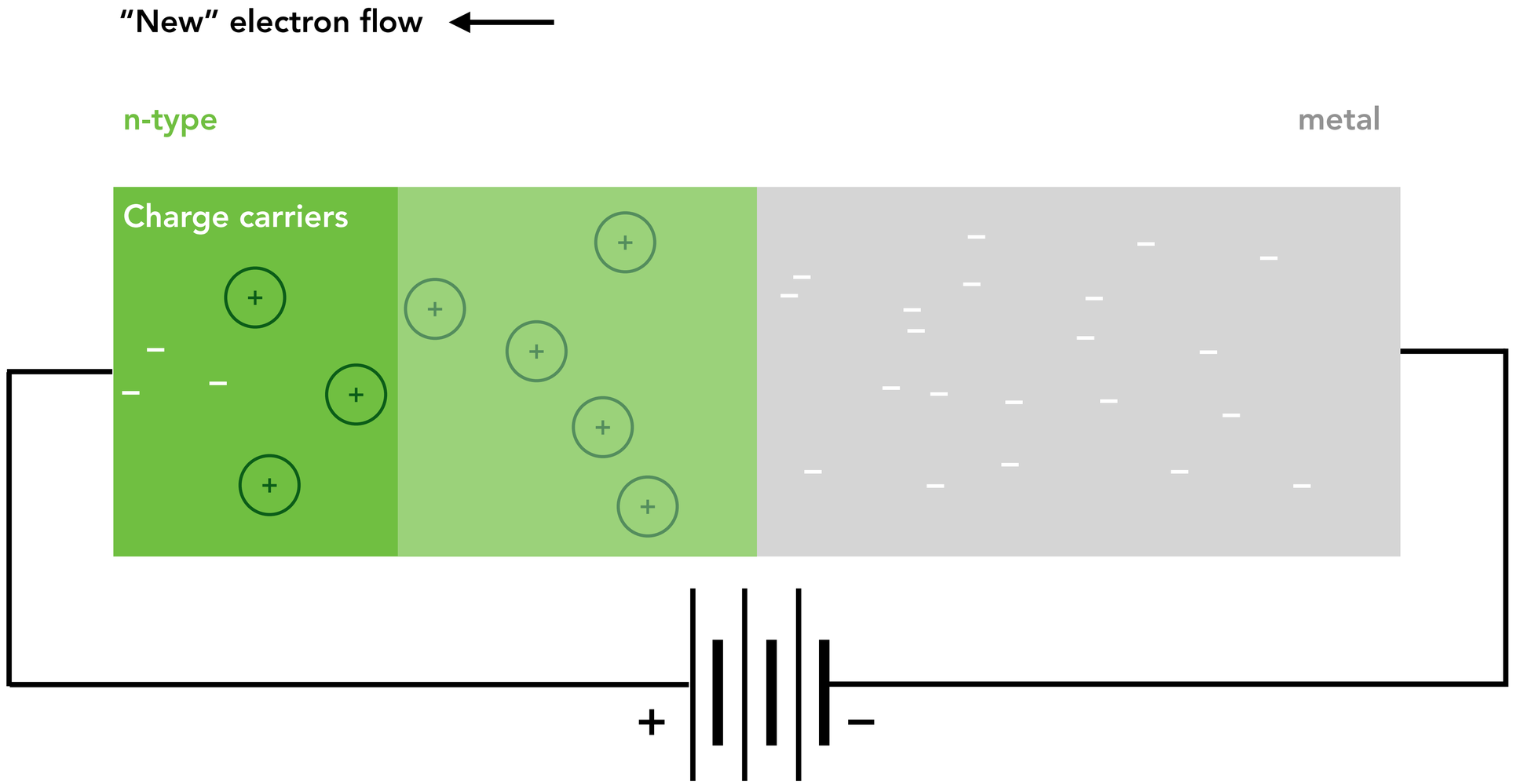

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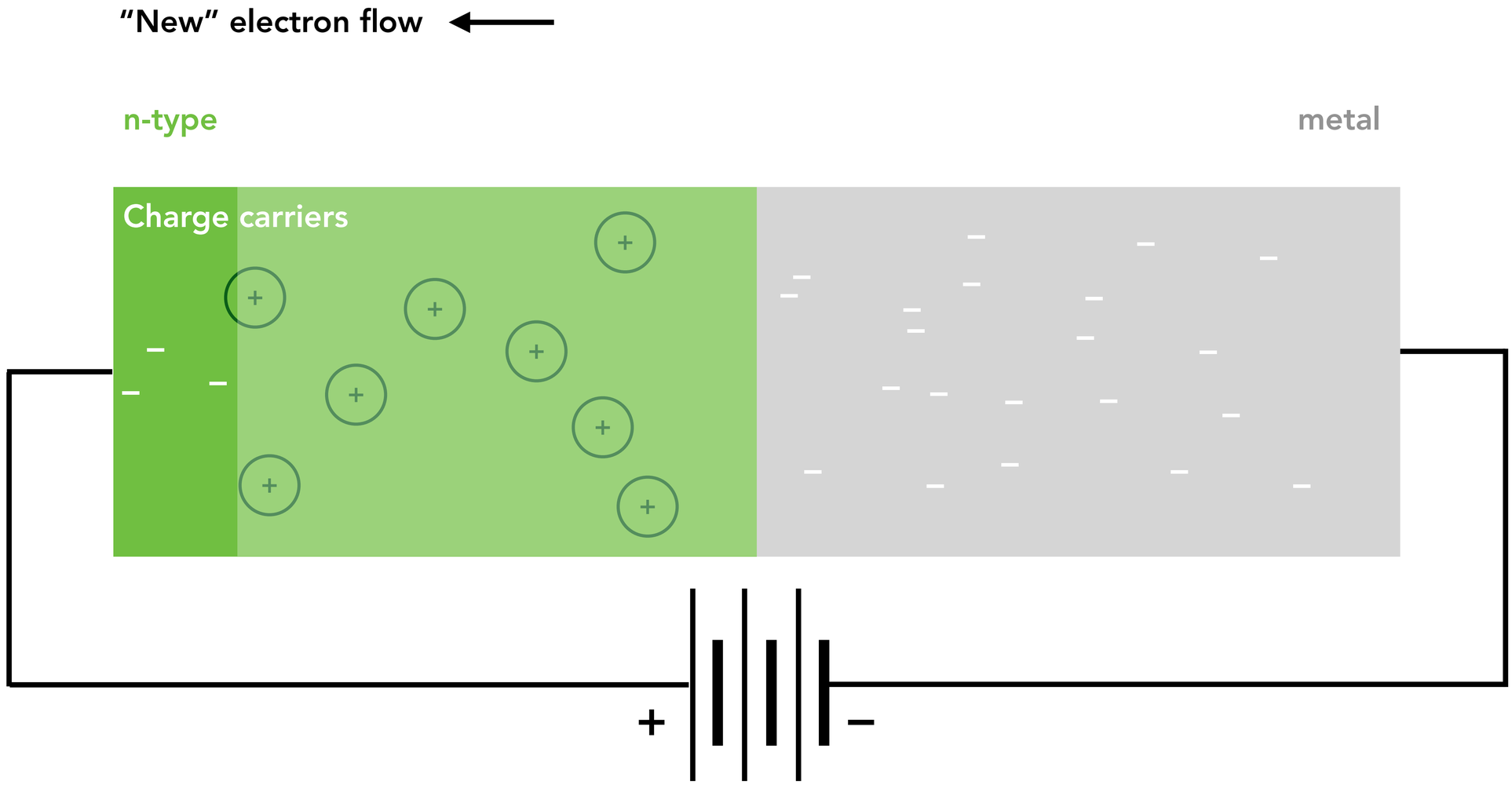

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Schottky junctions - external field

Bringing together a metal and doped semiconductor **can** give rise to a natural region free of charge carriers between the two

- This built-in depletion region contains an electric field which counters the diffusion of more carriers across the junction

We can forward bias the junction to reduce the depletion width

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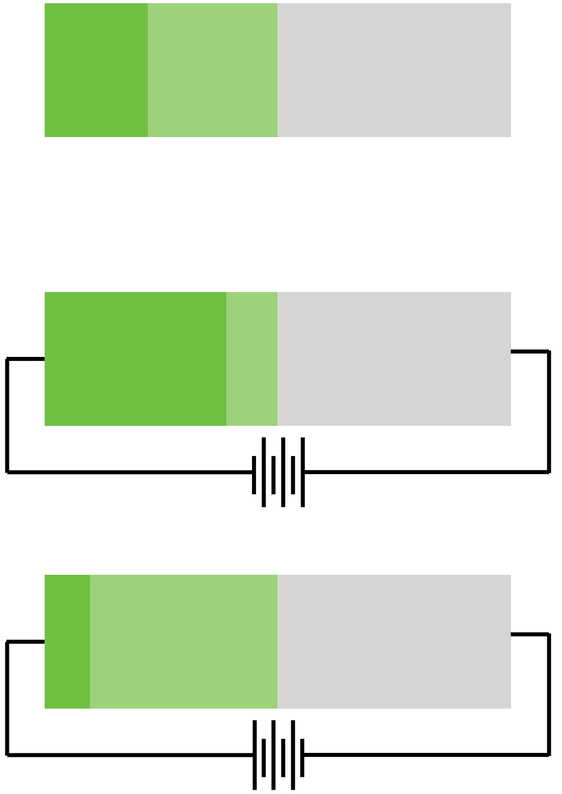

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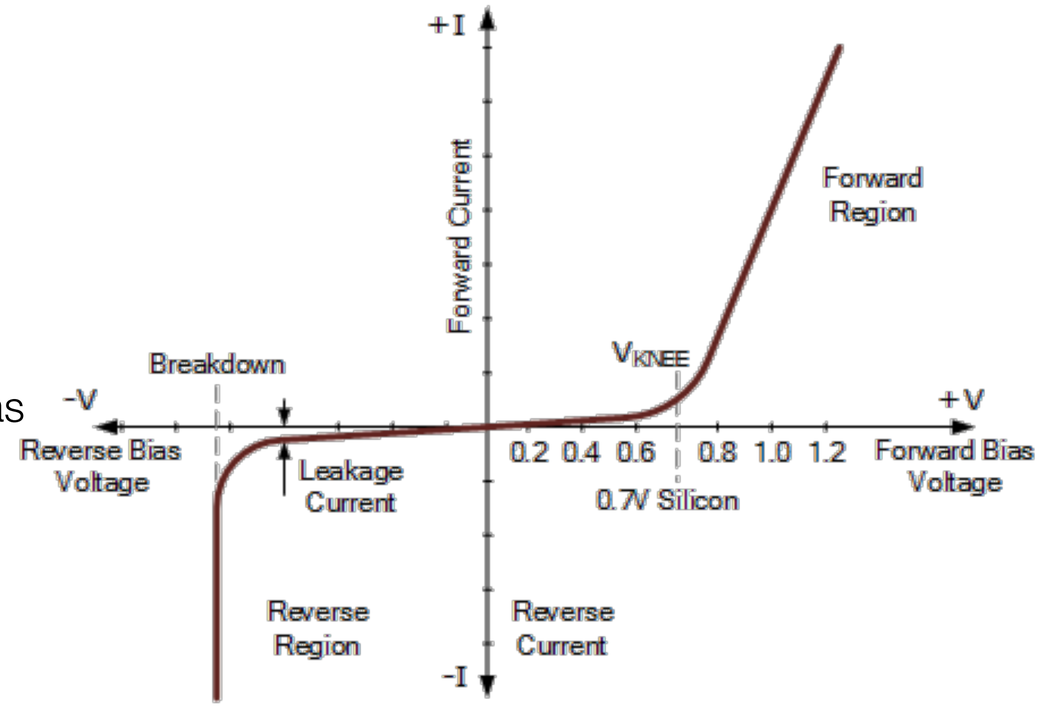

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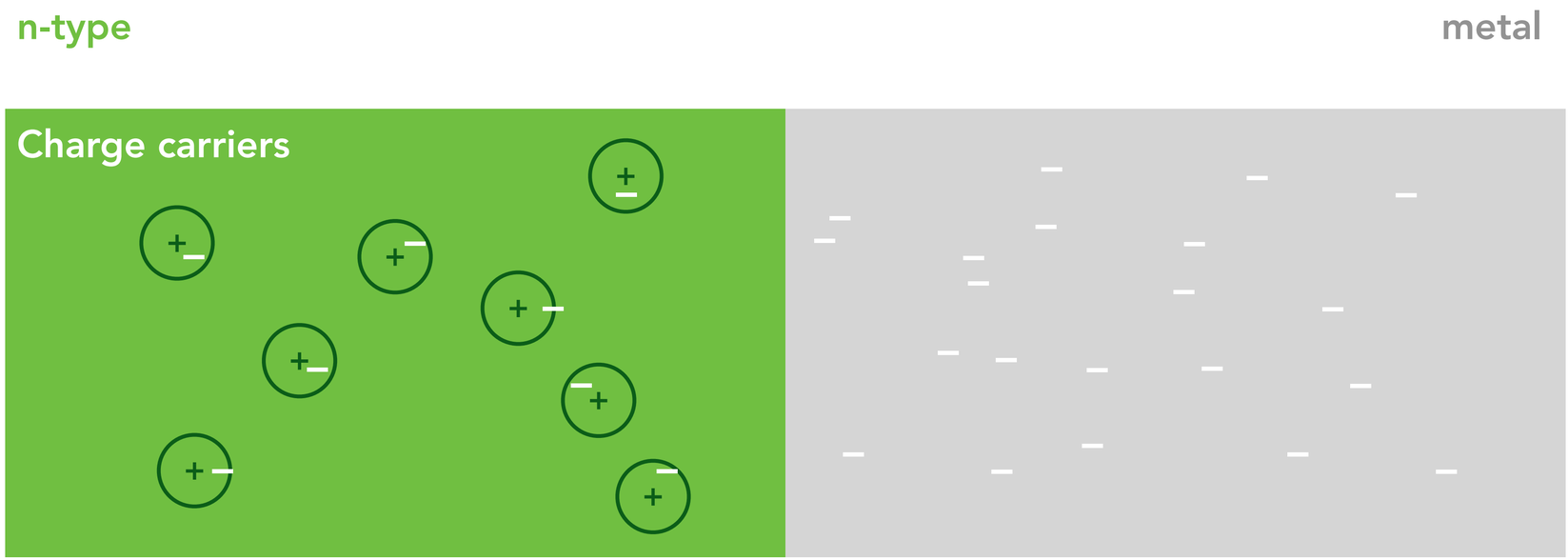
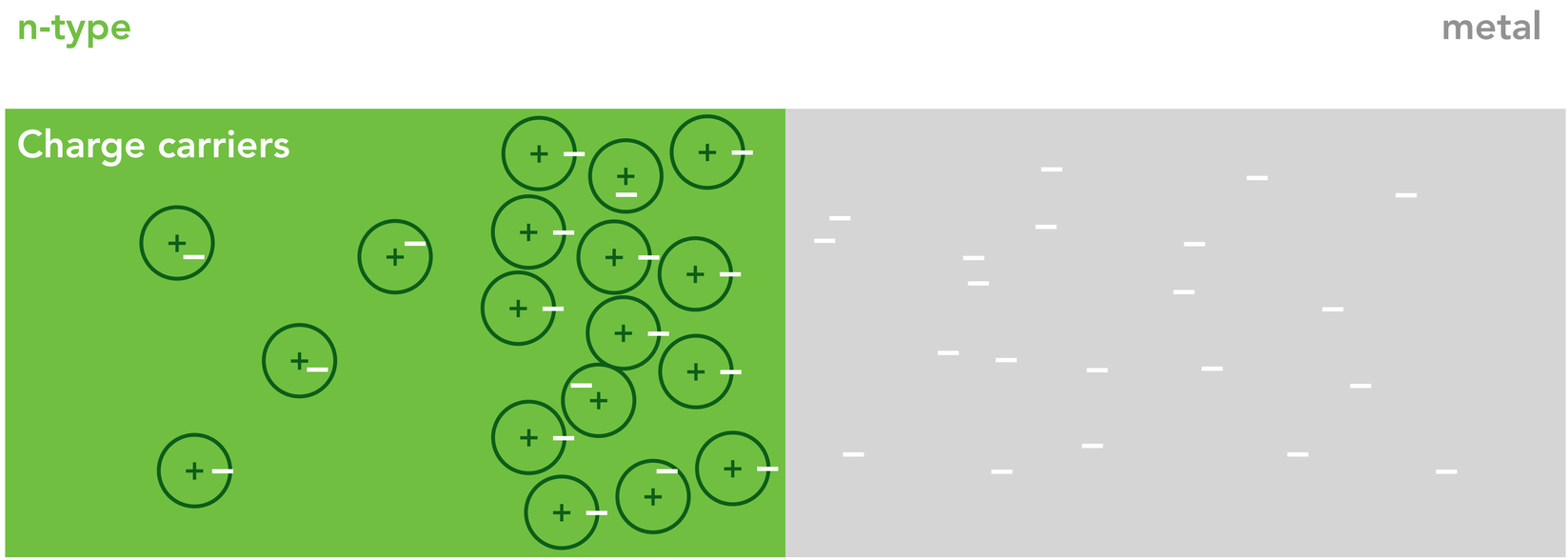


Consider a Schottky diode with a **strongly doped** n-type semiconductor

Schottky junctions - NB



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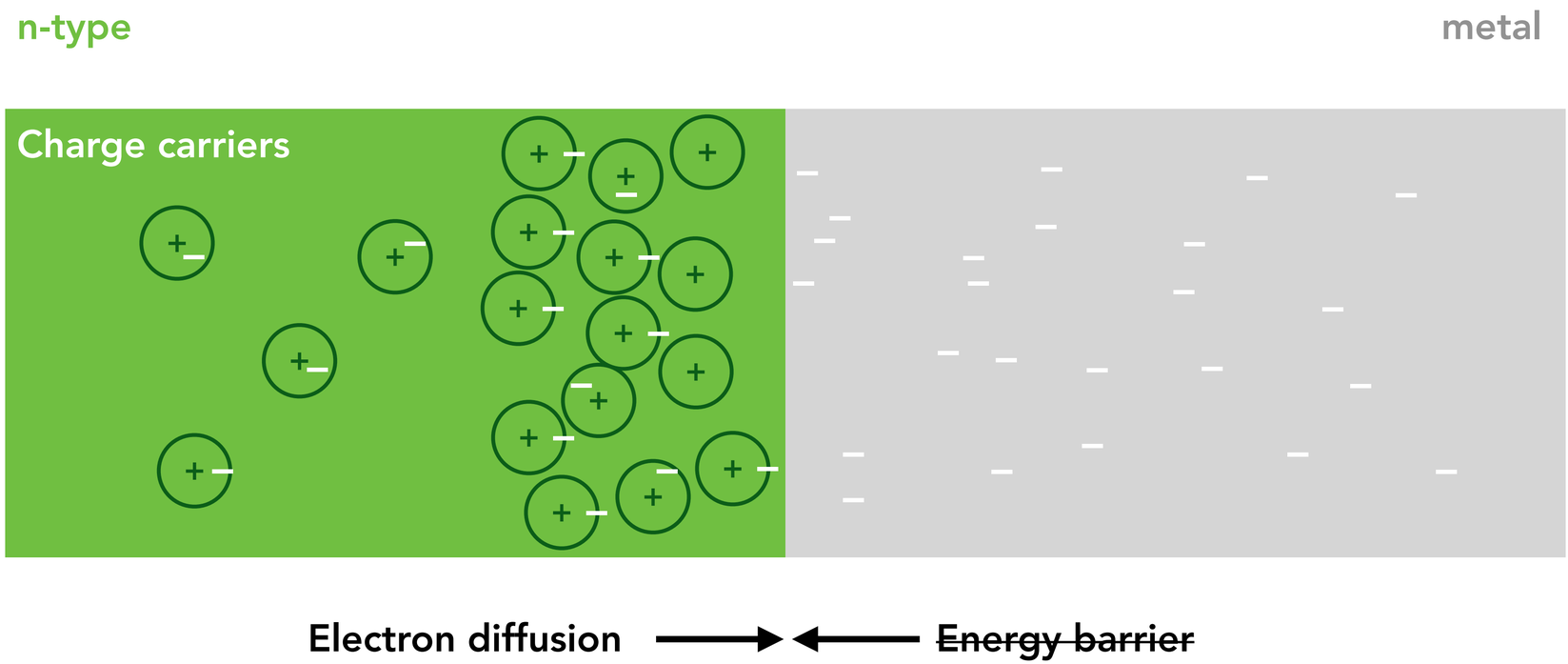

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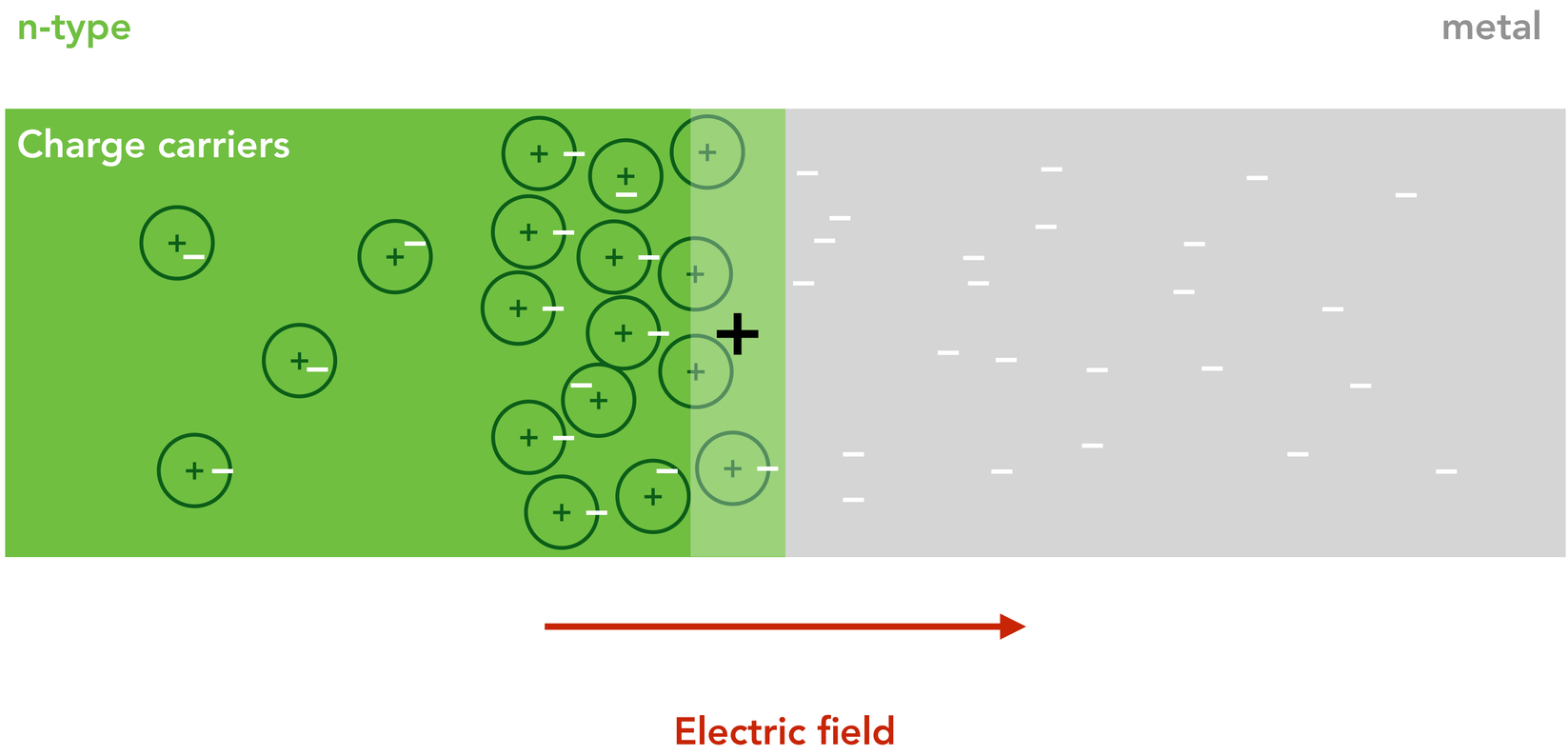

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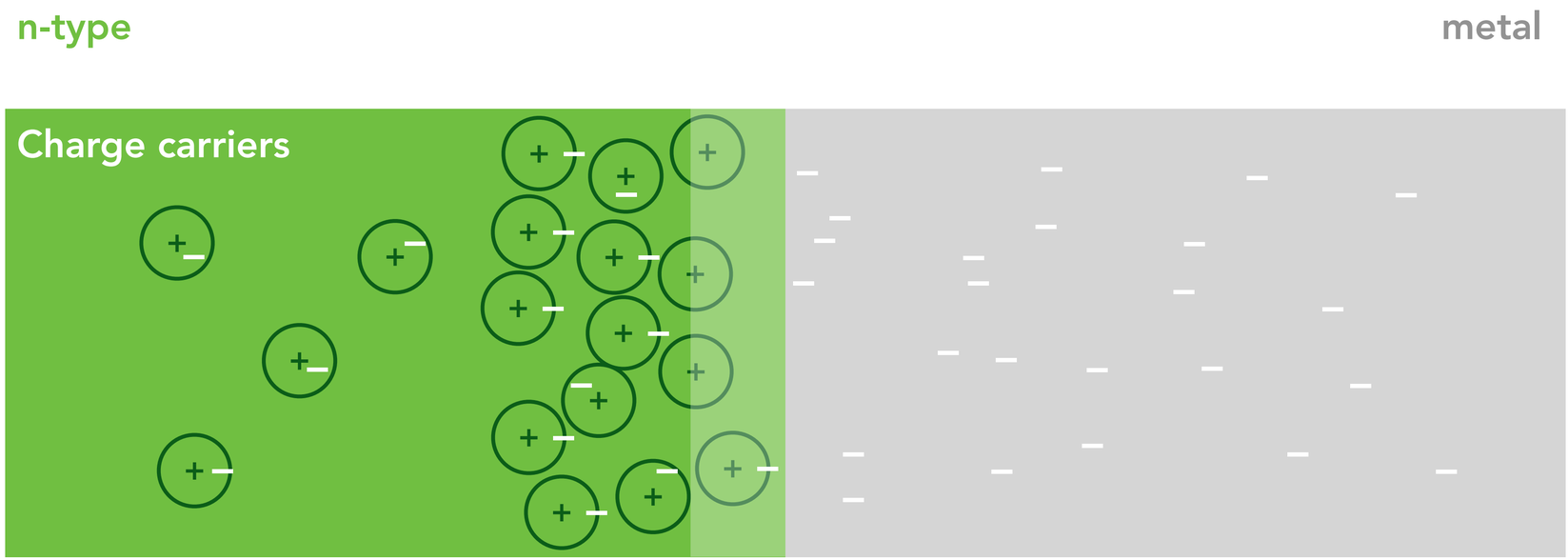


Consider a Schottky diode with a **strongly doped** n-type semiconductor

The depletion width will get smaller and smaller until it looks like an **Ohmic contact**

Transistors

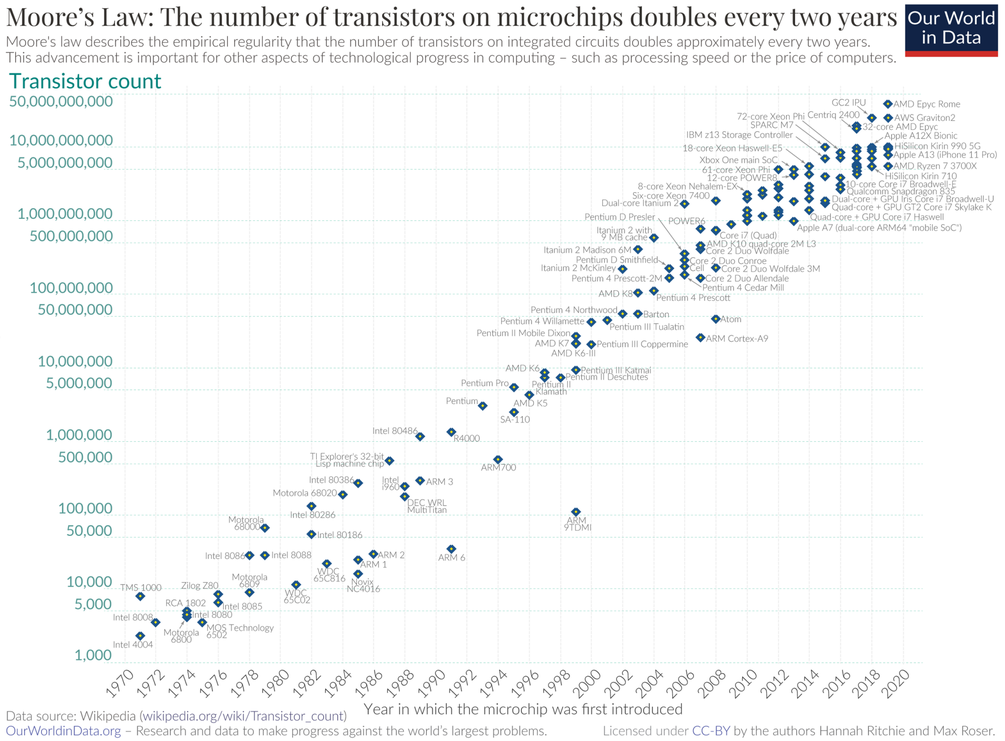
Transistors

Transistors play a crucial role in all modern technology, and are the reason that the semiconductor industry is so vast

- First transistors invented in ~1947
- First MOSFET in 1960

Latest generation of devices contain >100B transistors in an area of 30 x 30 mm^2

- Couldn't find more up-to-date numbers, but in 2014 Forbes calculated there had been 3 x 10^{21} transistors manufactured (cf. 3 x 10^{13} cells in human body)



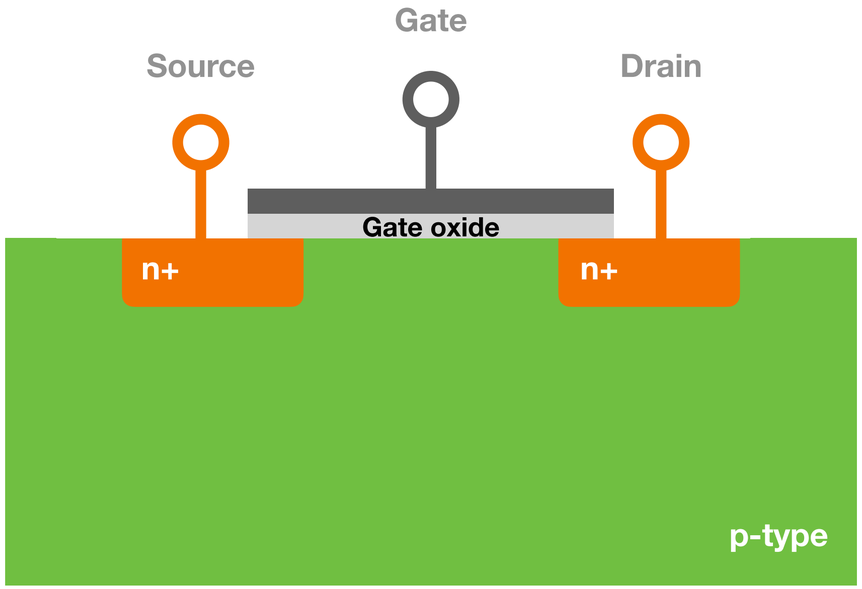
Anatomy of a transistor

Transistors are very much like Bach - variations on a theme…

- There are many kinds of transistors even just in silicon, ranging from the most commonly used MOSFETs, to MISFETs, JFETs, bipolar junction transistors, point-contact transistors, Schottky transistors…

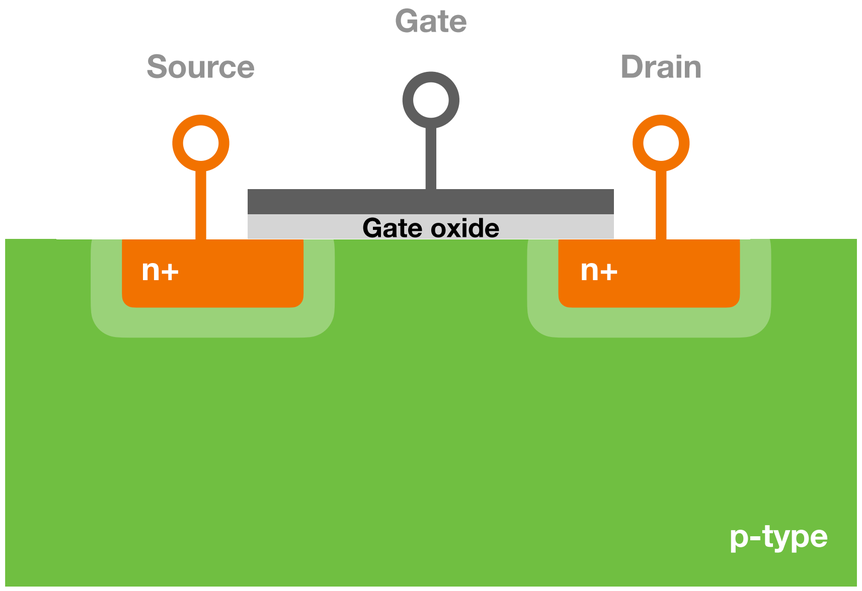
For today we are going to limit ourselves to discussing Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

- Again, there are many variations but we will consider *enhancement-mode MOSFETs*



Operating principles

MOSFETs consist of two doped regions - the *drain* and the *source* - on a lightly doped substrate, with insulating *gate oxide* sitting between the doped wells and a conductive *gate*



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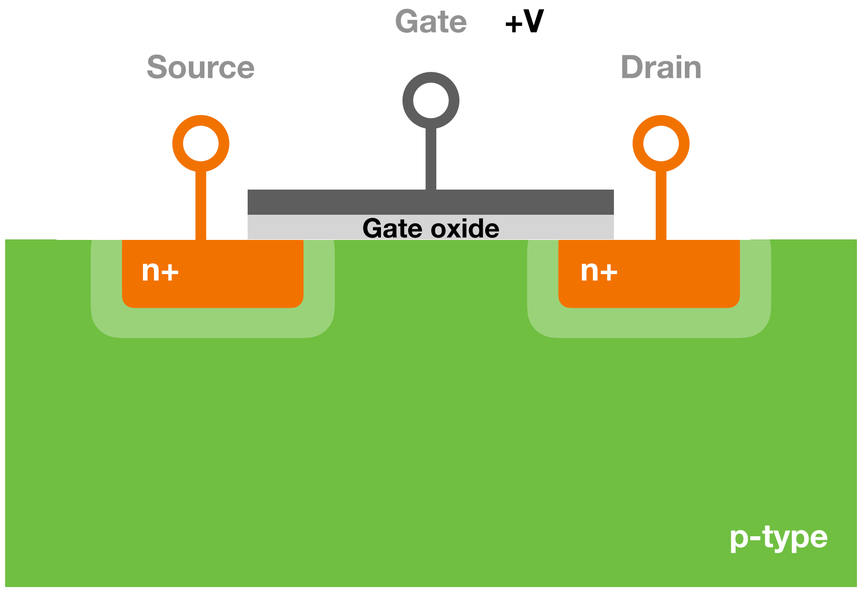

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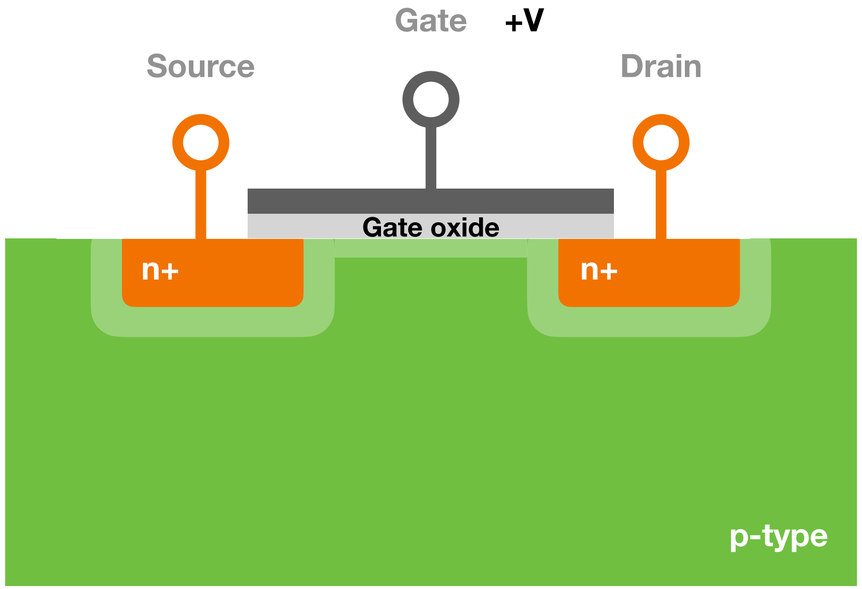

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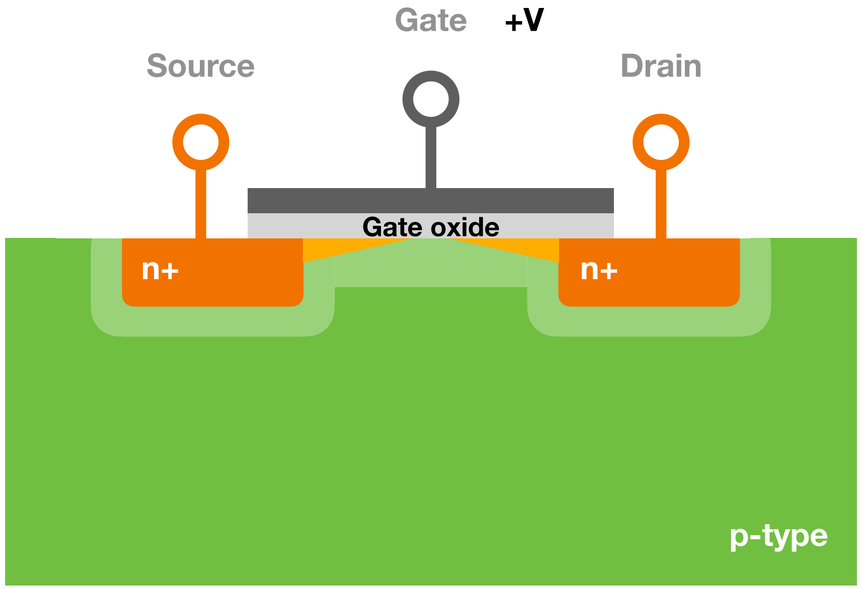
- With enough voltage it draws electrons from the source and drain



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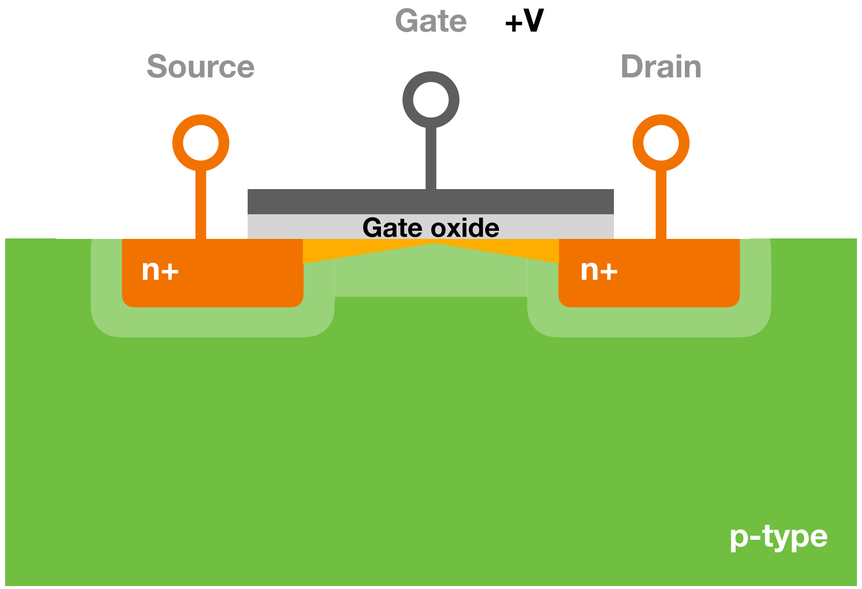
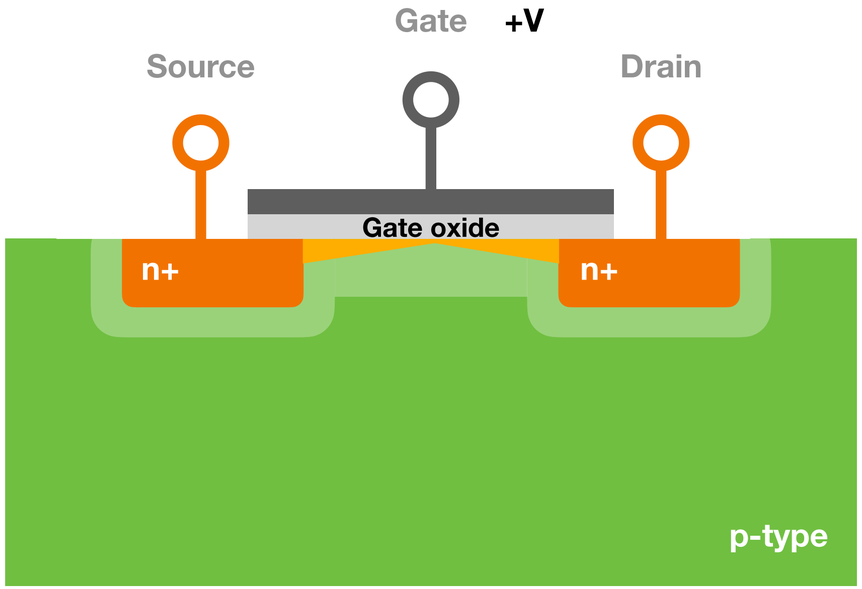
- With enough voltage it draws electrons from the source and drain
- Once these two regions join, an *inversion channel* is formed (minority carrier channel) => effectively a switch with a threshold voltage



Operating principles

With no potential difference across the source and drain, there is no flow of current (making it pretty useless)



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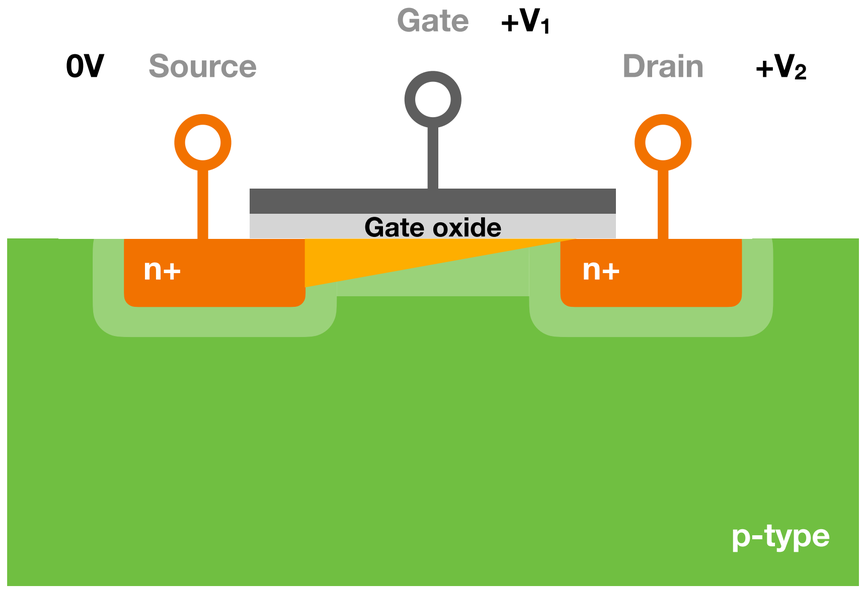

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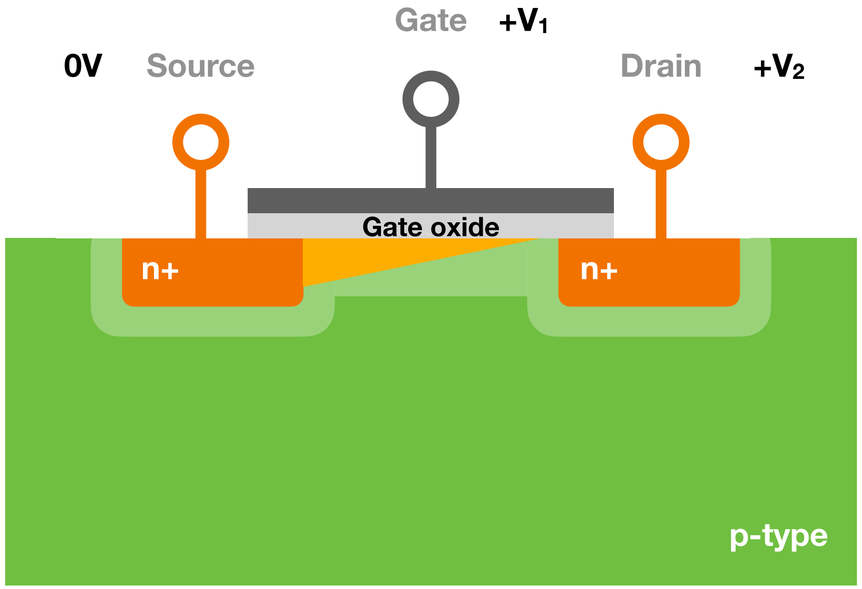
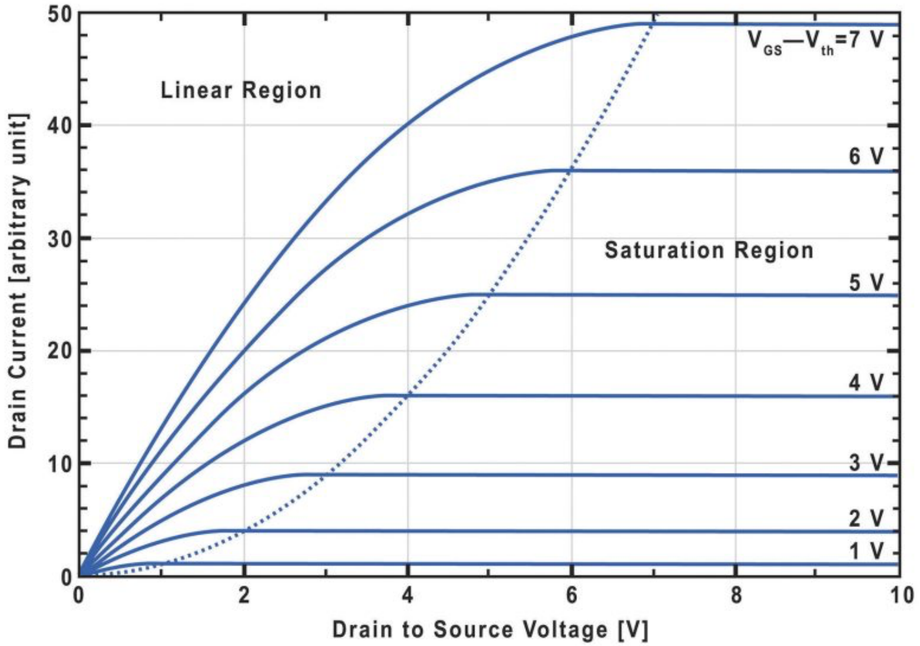
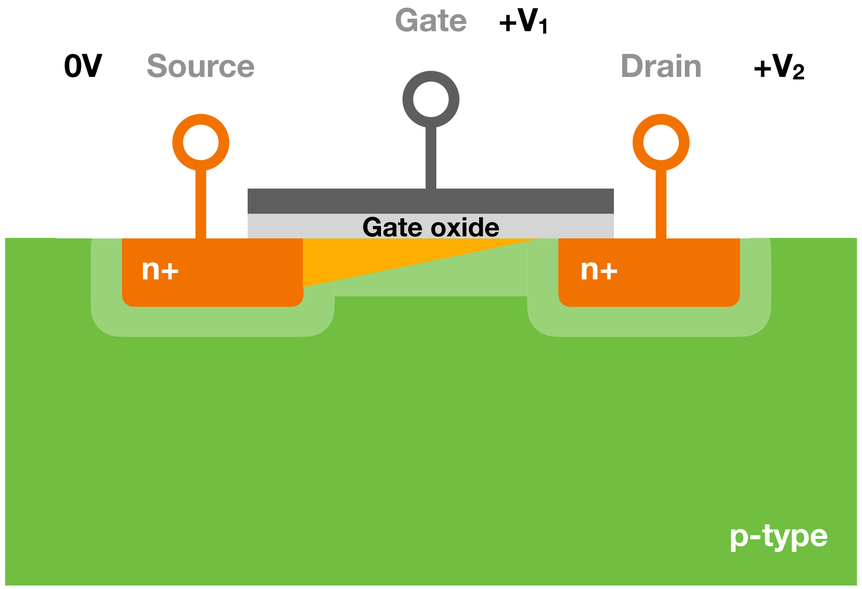
- Increasing the potential difference leads to “pinch off” - the inversion channel is cut off due to the higher potential close to the drain - current still flows but is saturated and no longer increases with voltage



Operating principles



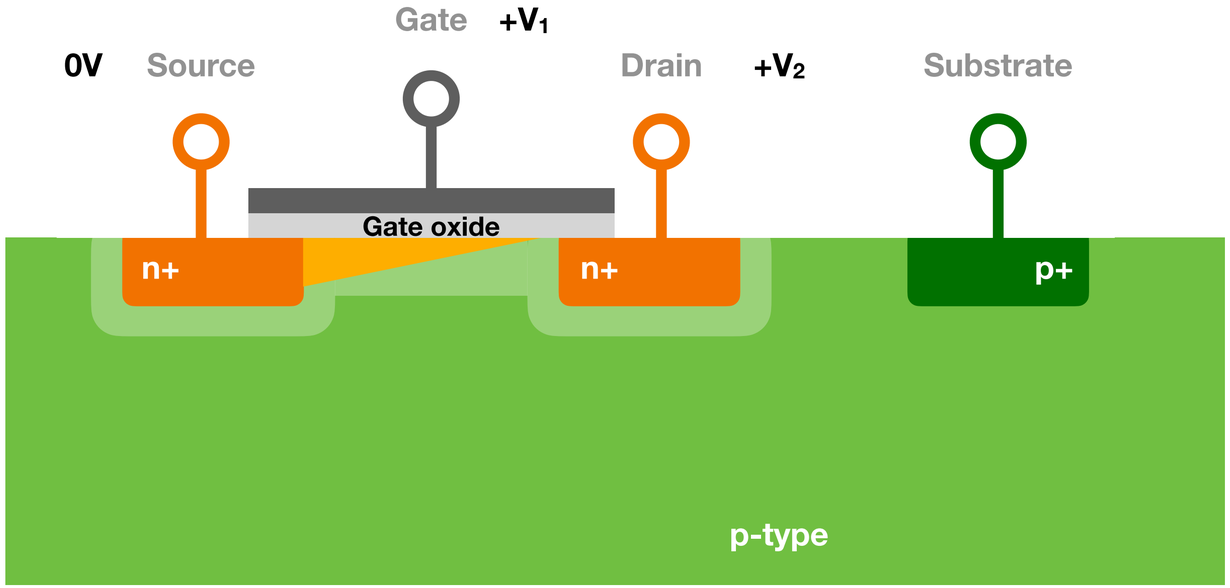


Operating principles

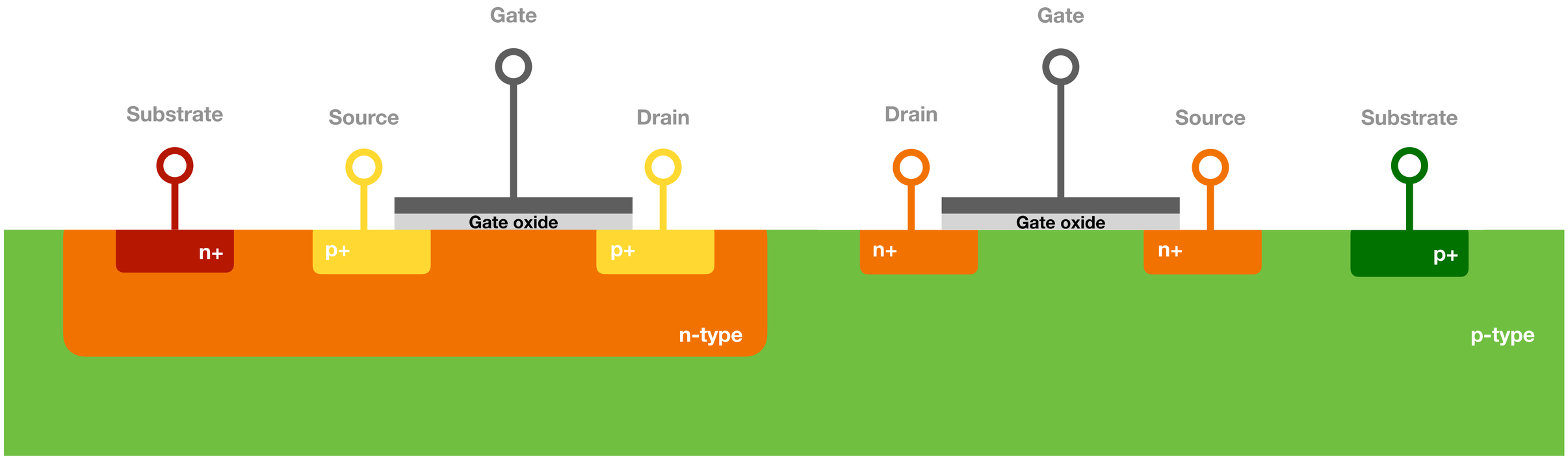
Since we are talking about potential differences it is worth pointing out that the substrate potential can also be controlled

- This is an nMOSFET - analogous devices with **n** and **p** swapped are imaginatively called pMOSFETs

Both behave slightly differently due to the difference in carriers and relative potentials, but the real power comes in comibination



CMOS


Gate
Substrate
Source
Drain
Drain
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Source
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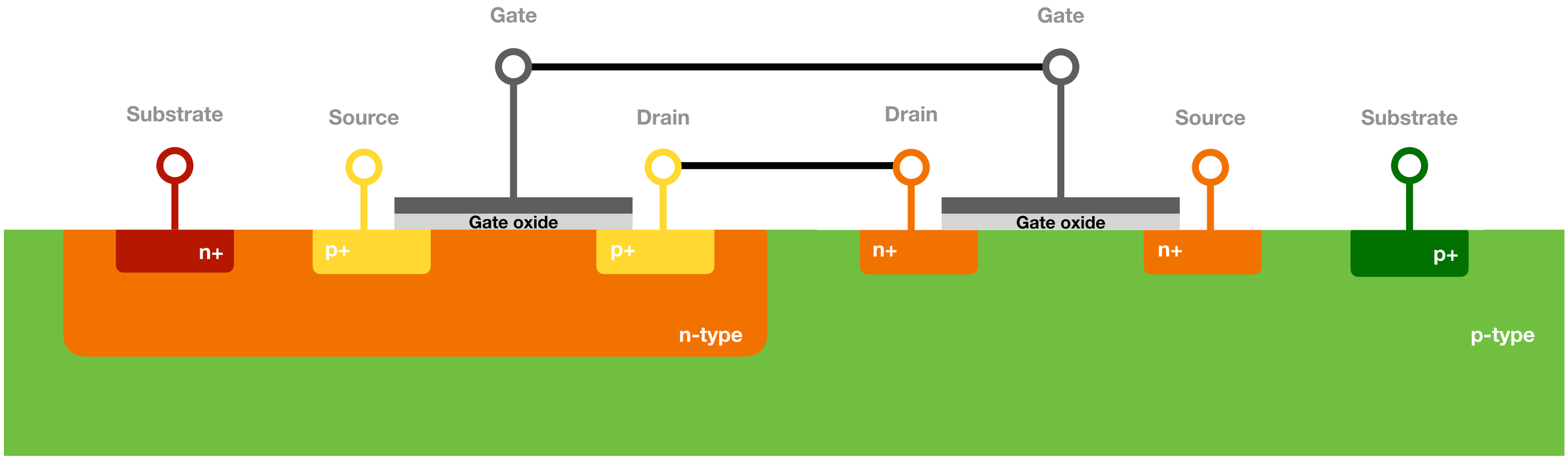
Gate oxide
Gate oxide
n+
p+
p+
n+
n+
p+
n-type
p-type

CMOS


Gate
Gate
Substrate
Source
Drain
Drain
Source
Substrate
Gate oxide
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n+
p+
p+
n+
n+
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n-type
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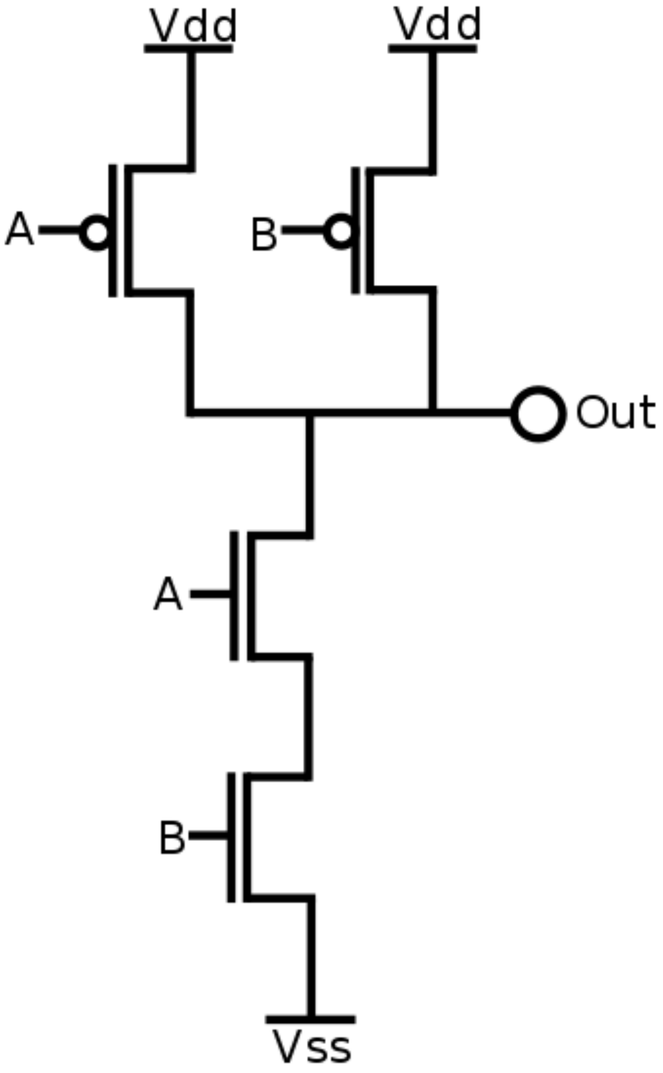
CMOS in person

Consider an NAND gate

- Effective Out = $\overline{AB}$
- Always **on** unless both inputs are **on**



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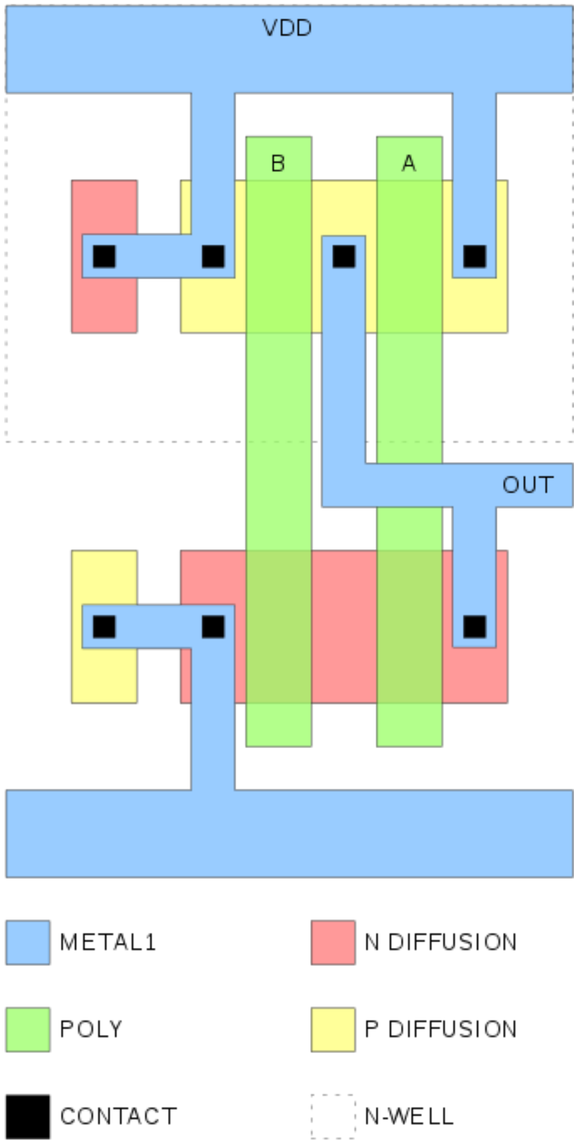

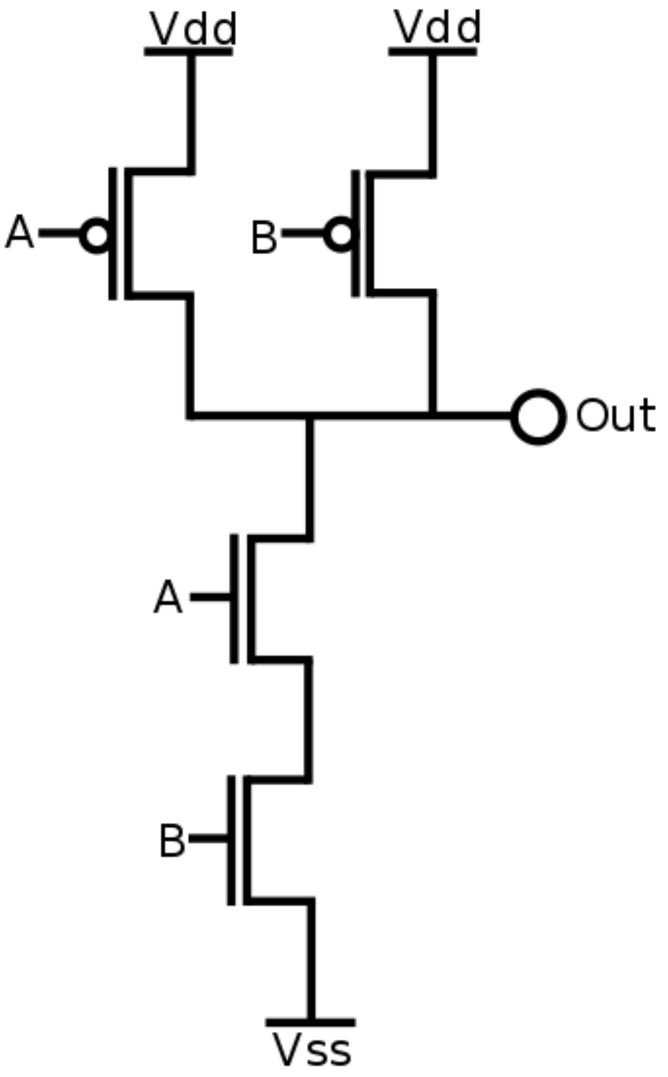

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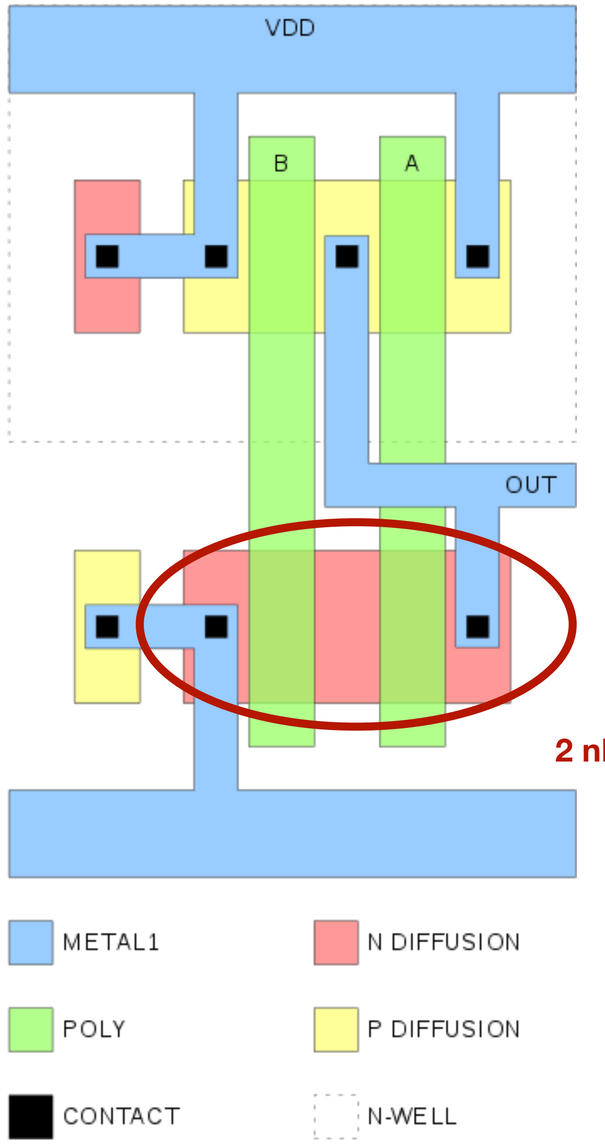

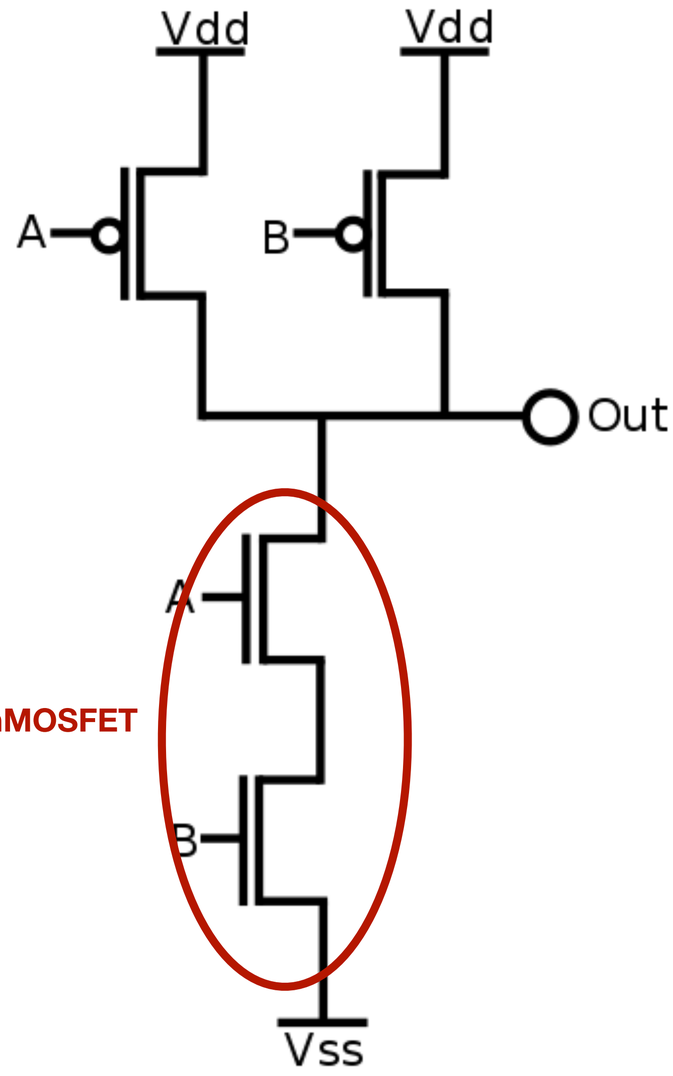

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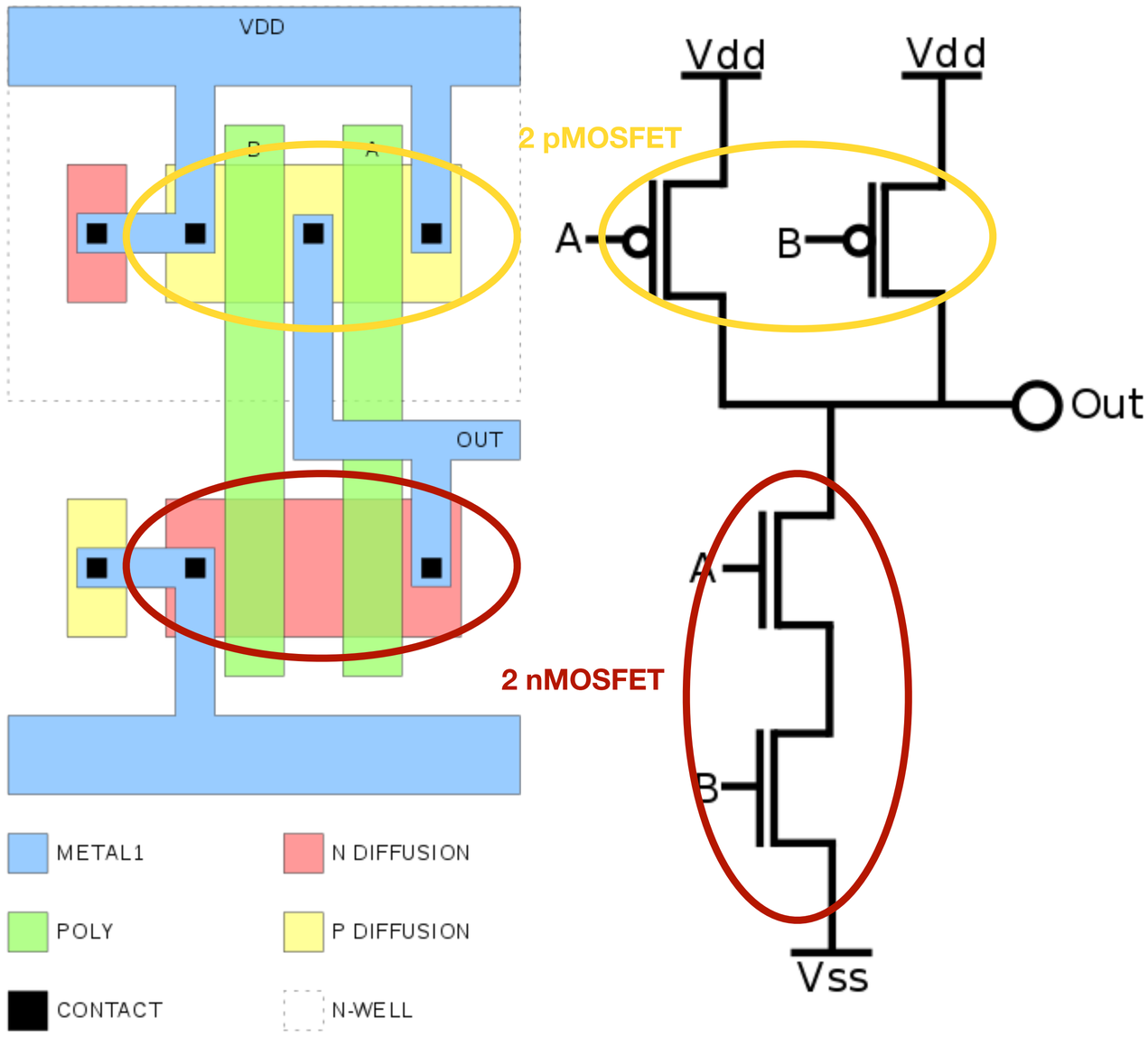
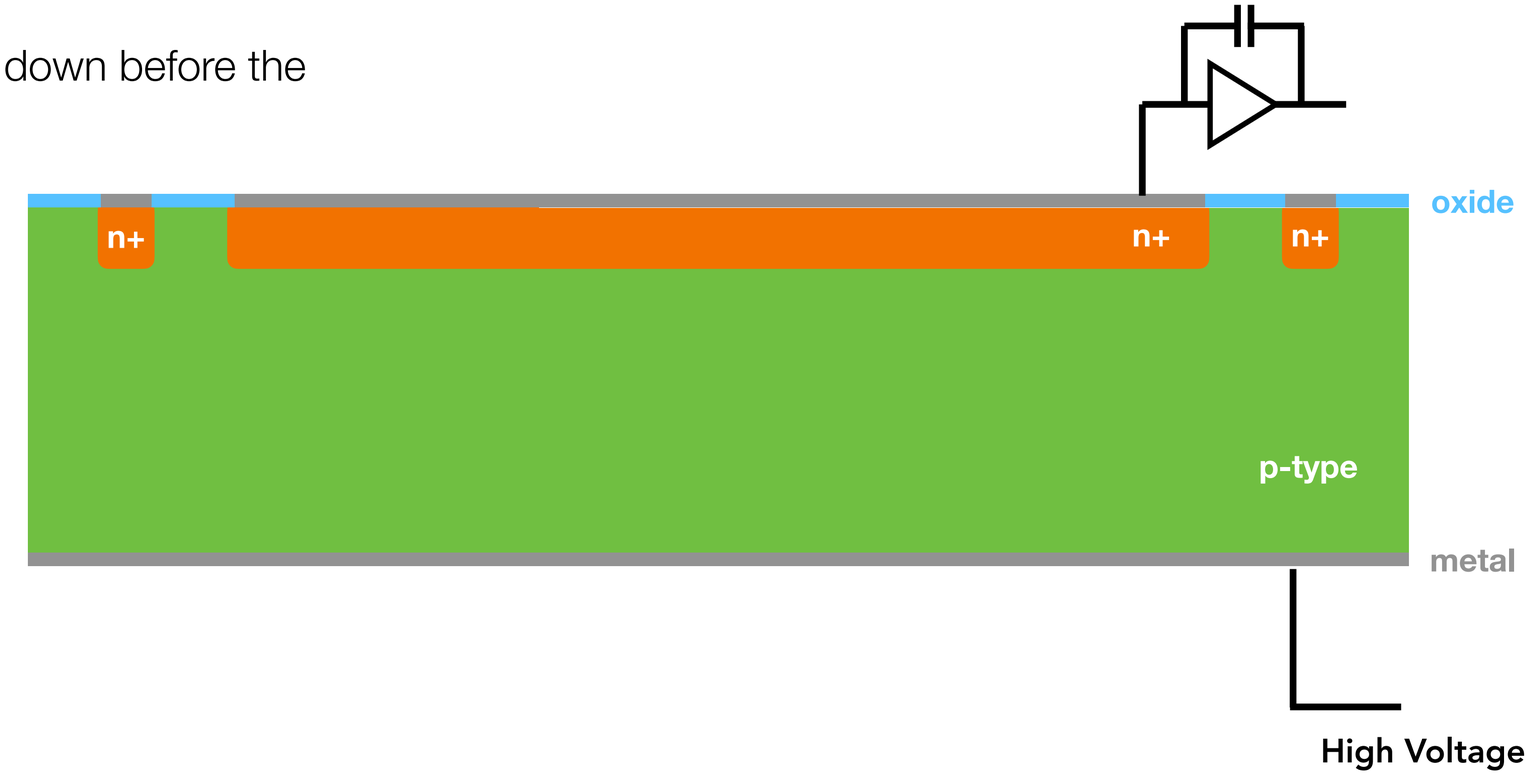


Semiconductor detectors

Basic anatomy - 0D

One of the most basic types of detector is simply a PN-diode

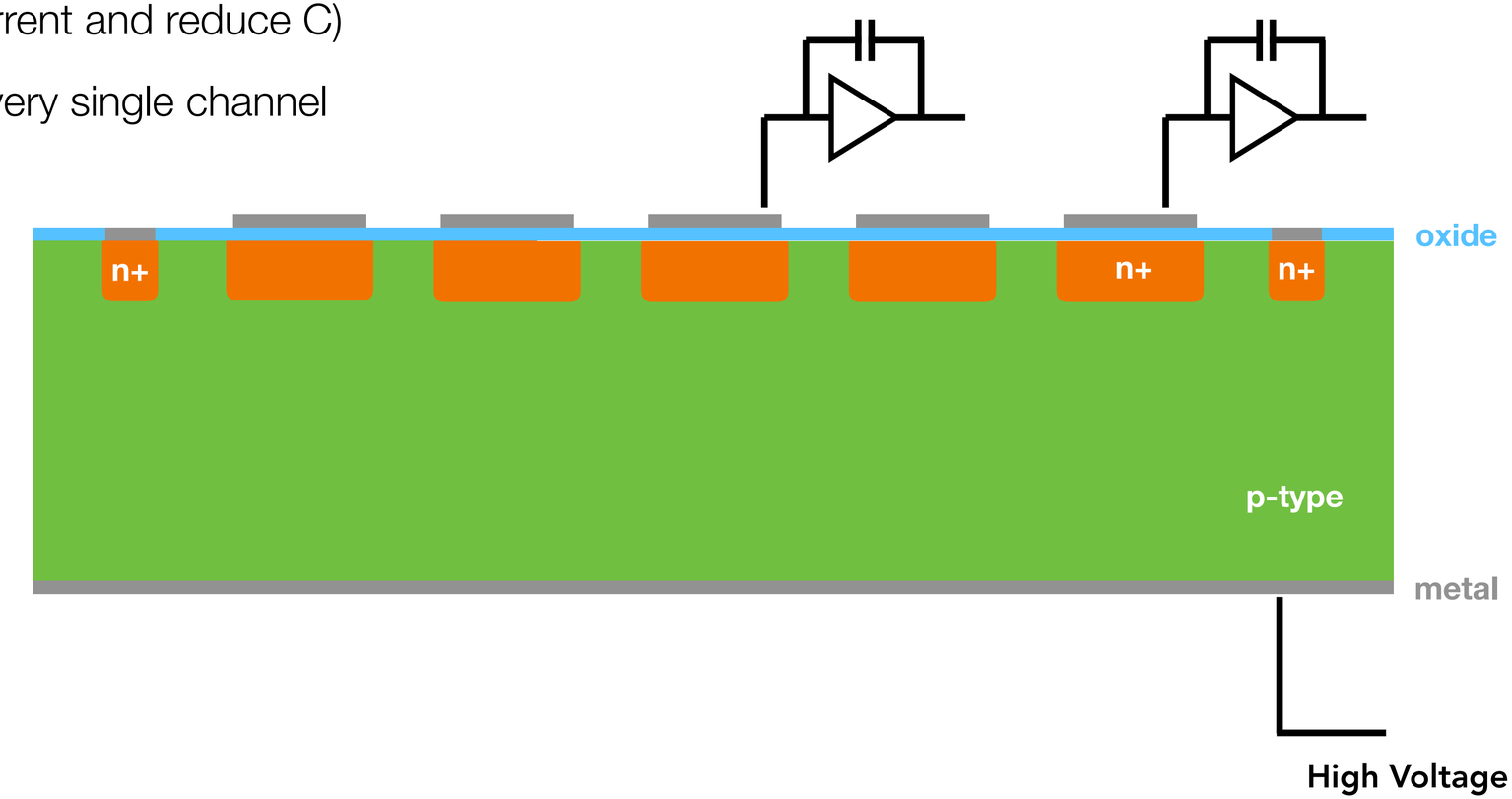
- Large area, highly doped region ~10^{18} cm^{-3}
- High resistivity bulk ~10^{12} cm-3
- *Guard rings* to step the high voltage down before the physical edge
- Back-side HV contact
- Top side contact to read out



Basic anatomy - 1D

Moving on to a single, long *strip detector*

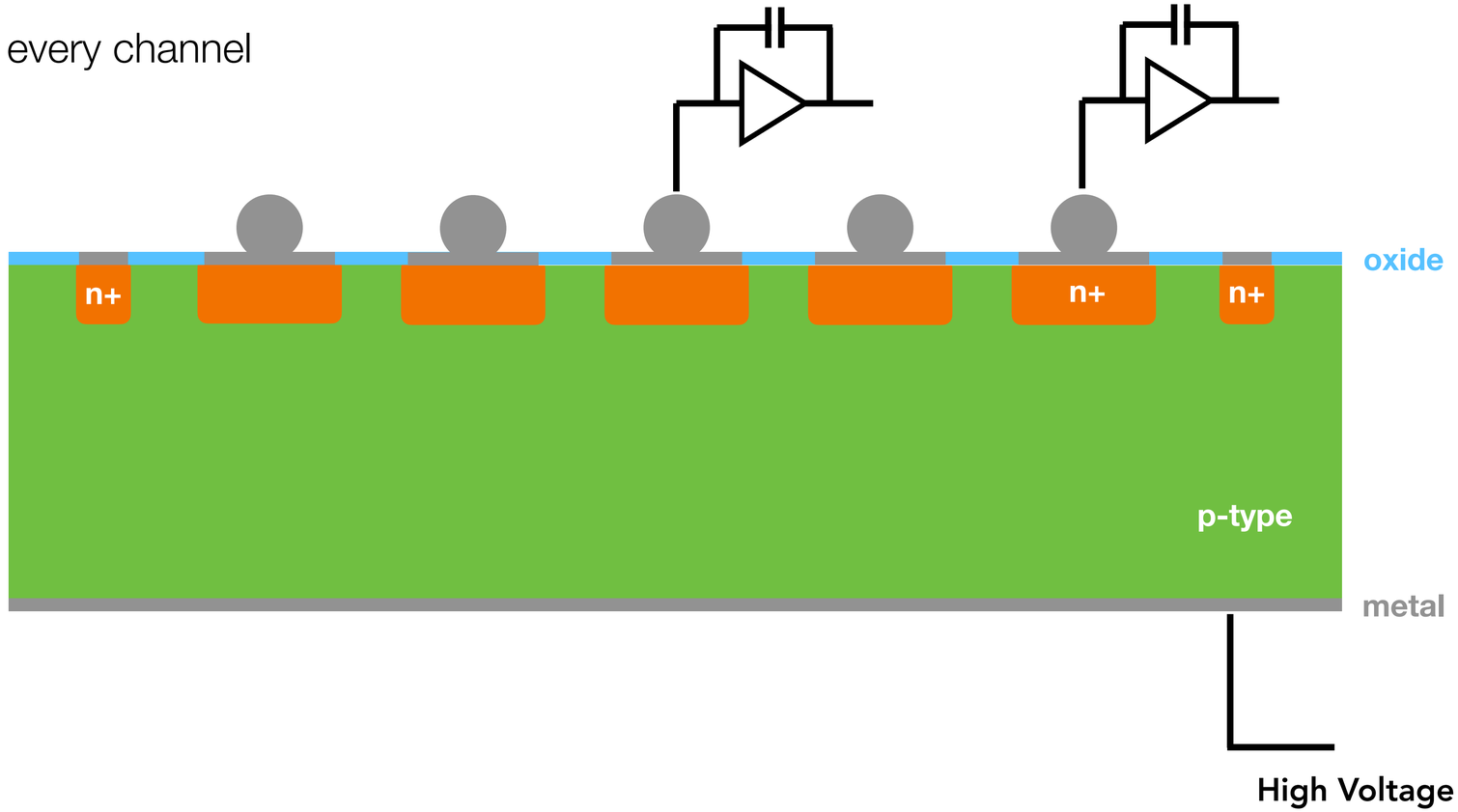
- Strips many cm long, with capacitive readout of the strips rather than DC (to avoid leakage current and reduce C)
- Dedicated electronics to read out every single channel individually on a separate ASIC
  - Wire bond each strip “manually”



Basic anatomy - 2D

Finally, pixel detectors

- Now segmented in 2D
- Typically separate readout ASIC, with every channel *bump-bonded* to its own diode



Signal formation

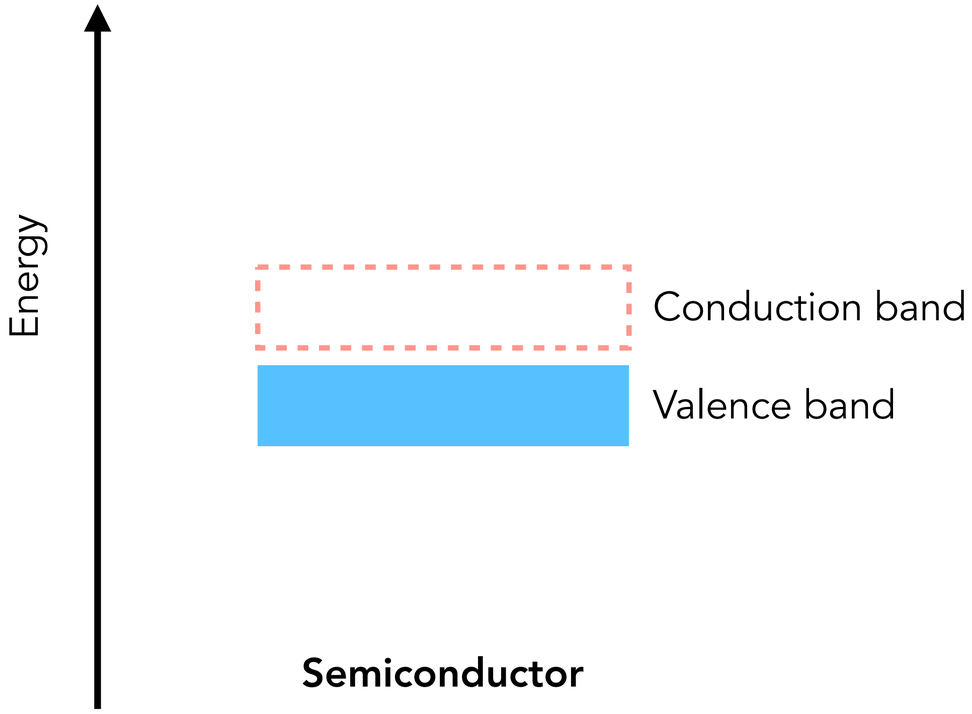
Charge carrier creation

As we depleted our PN-junction, we removed the free charge carriers

- We can continue to do this until the function is *fully depleted*

Under these circumstances the only free charge carriers moving around will be those that have enough thermal energy

- This is a small number for silicon at room temperature



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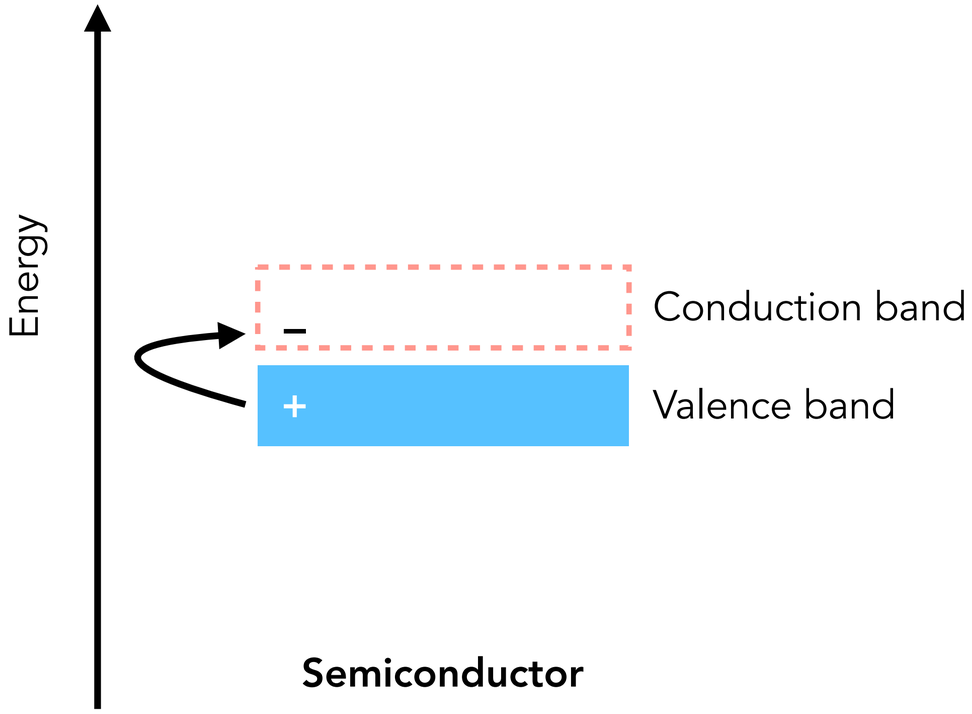
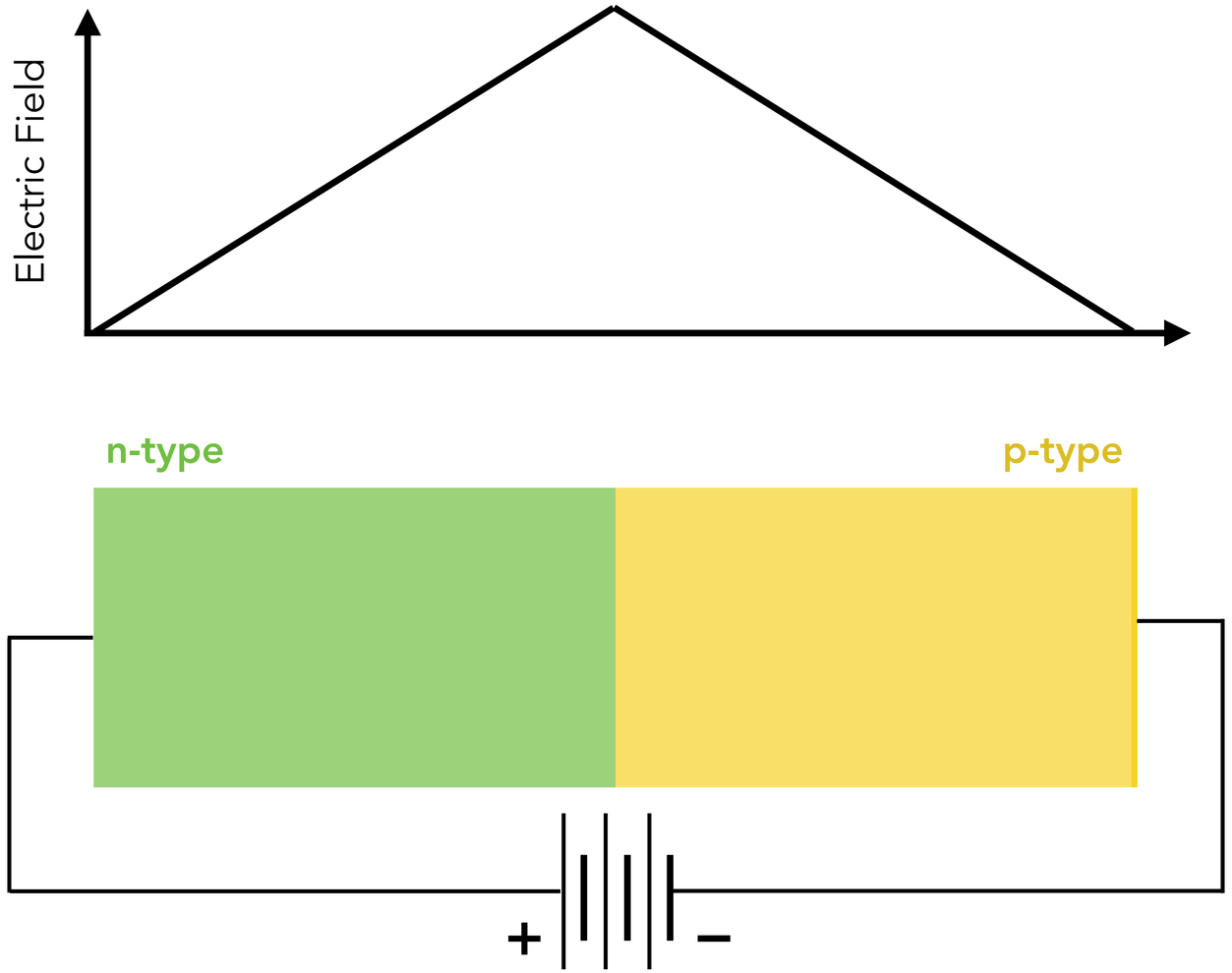
If a particle interacts with the silicon, it can transfer energy onto individual electrons and promote them to the conduction band

- This is the foundation of solid-state particle detection



Charge carrier motion



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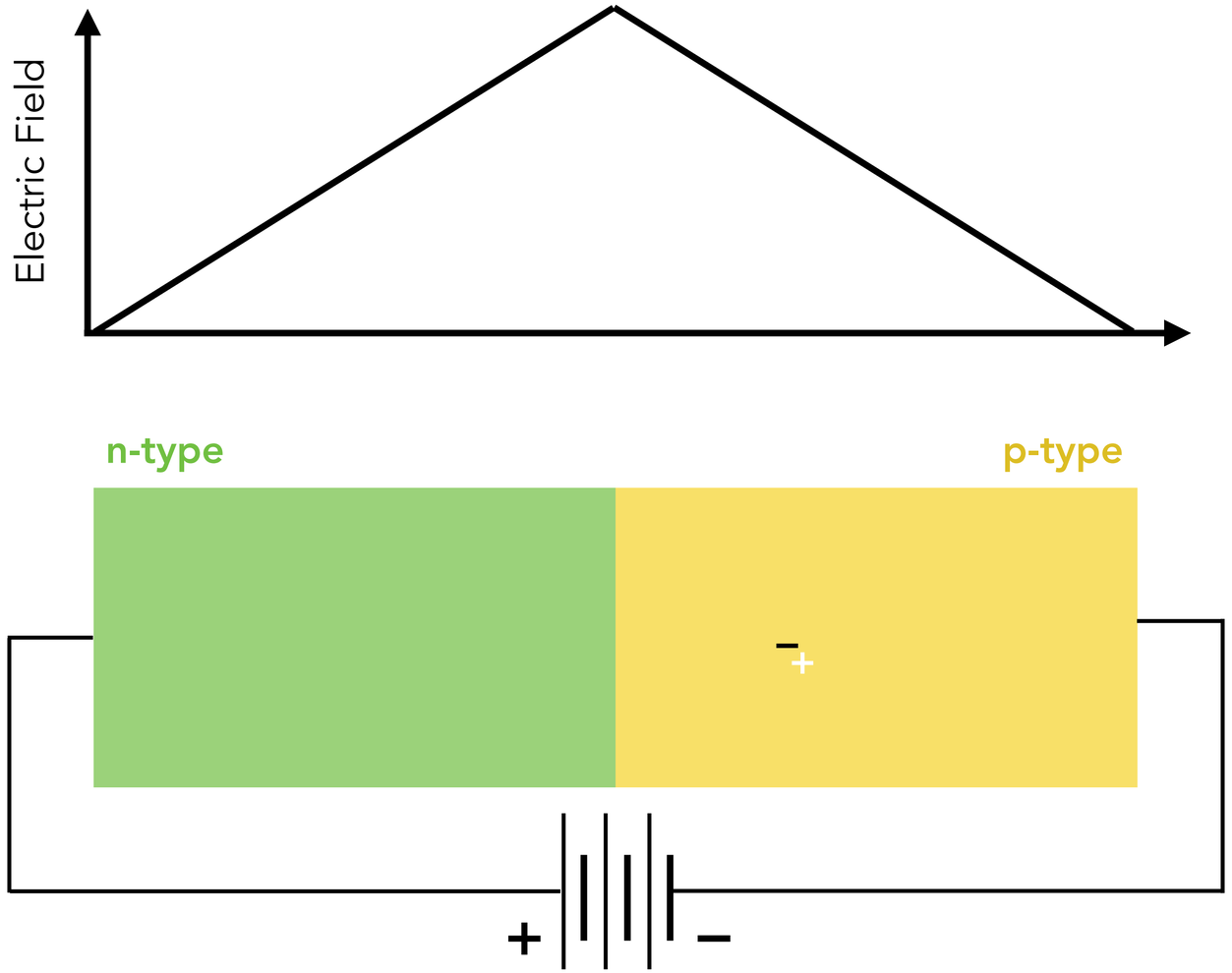

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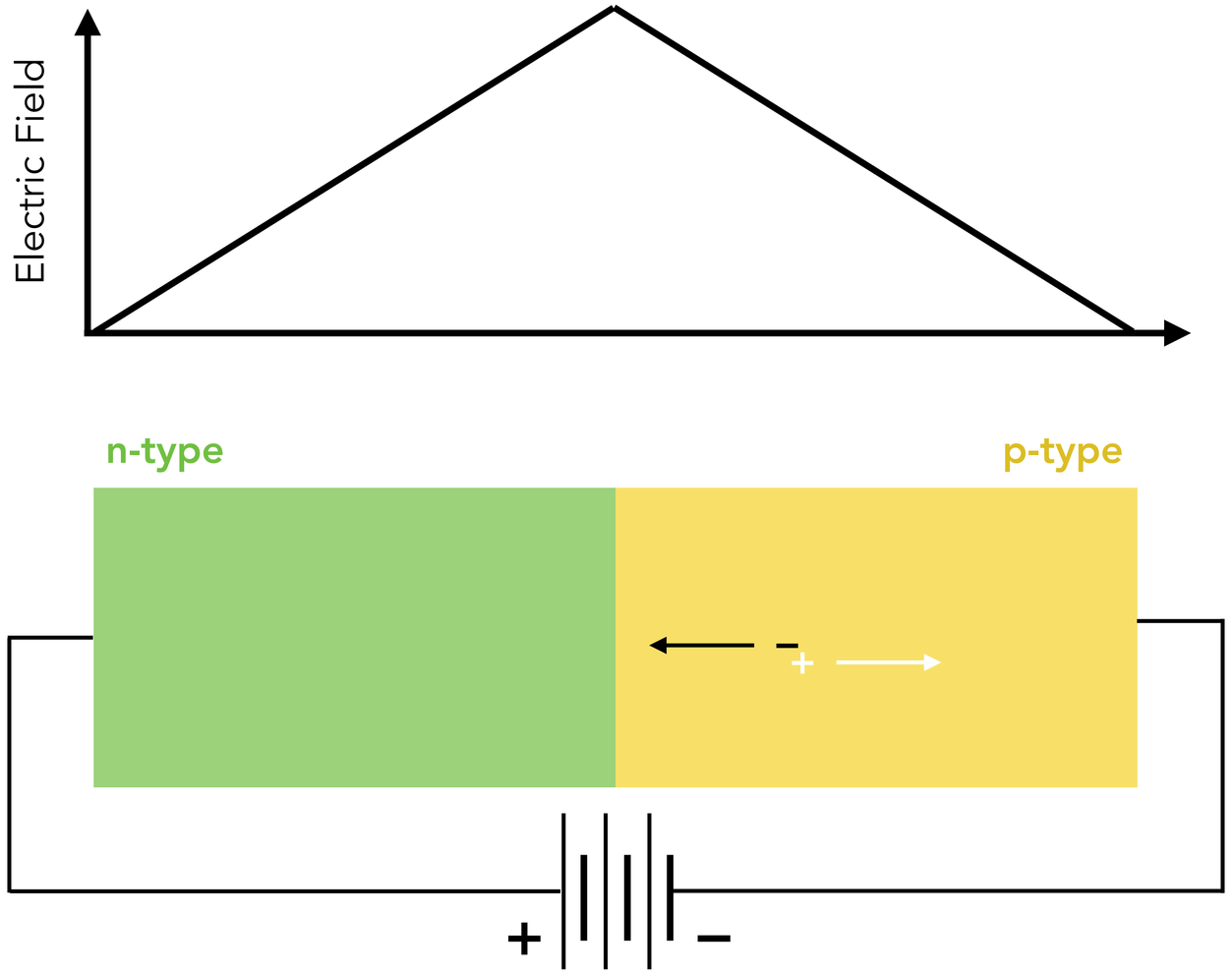

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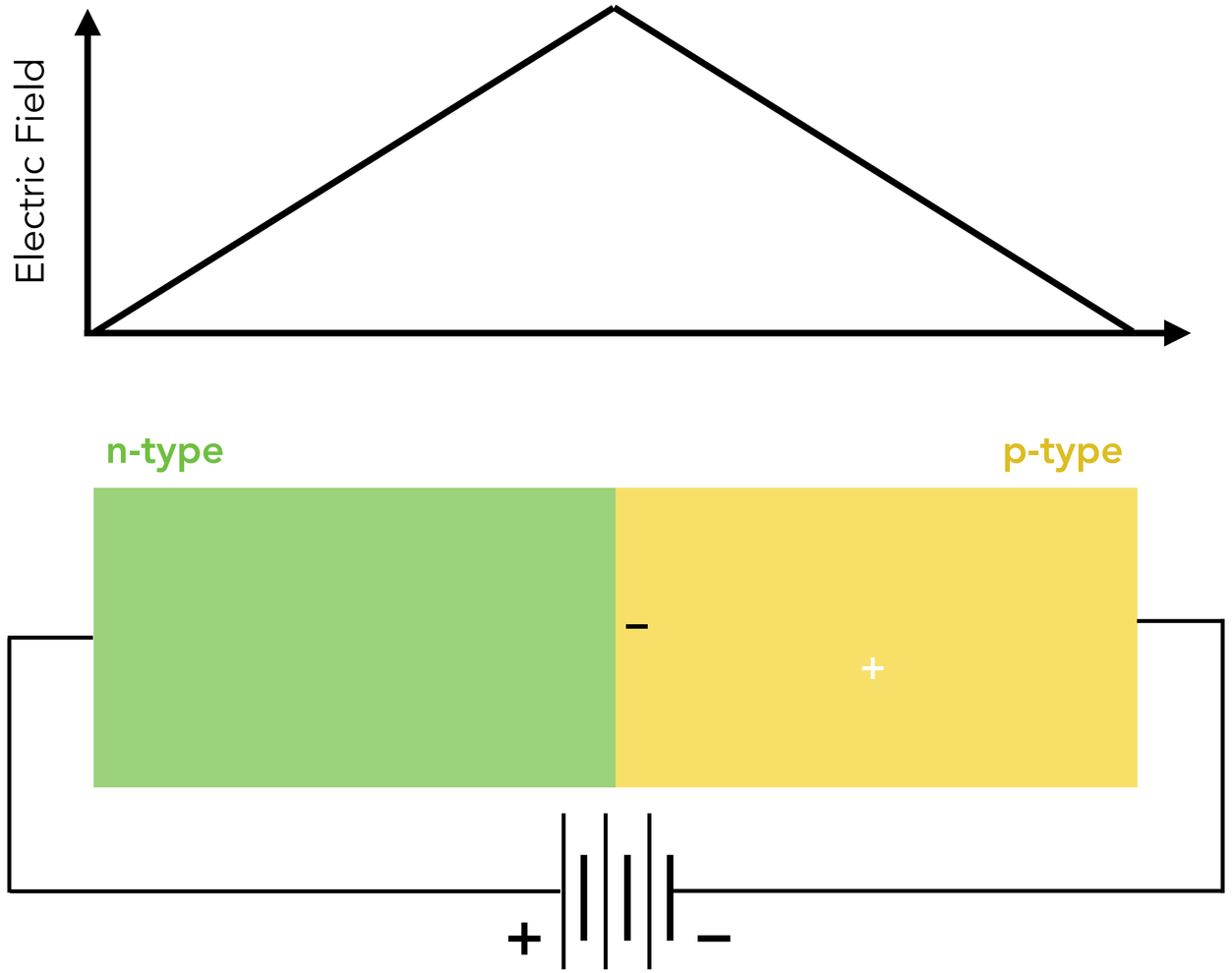

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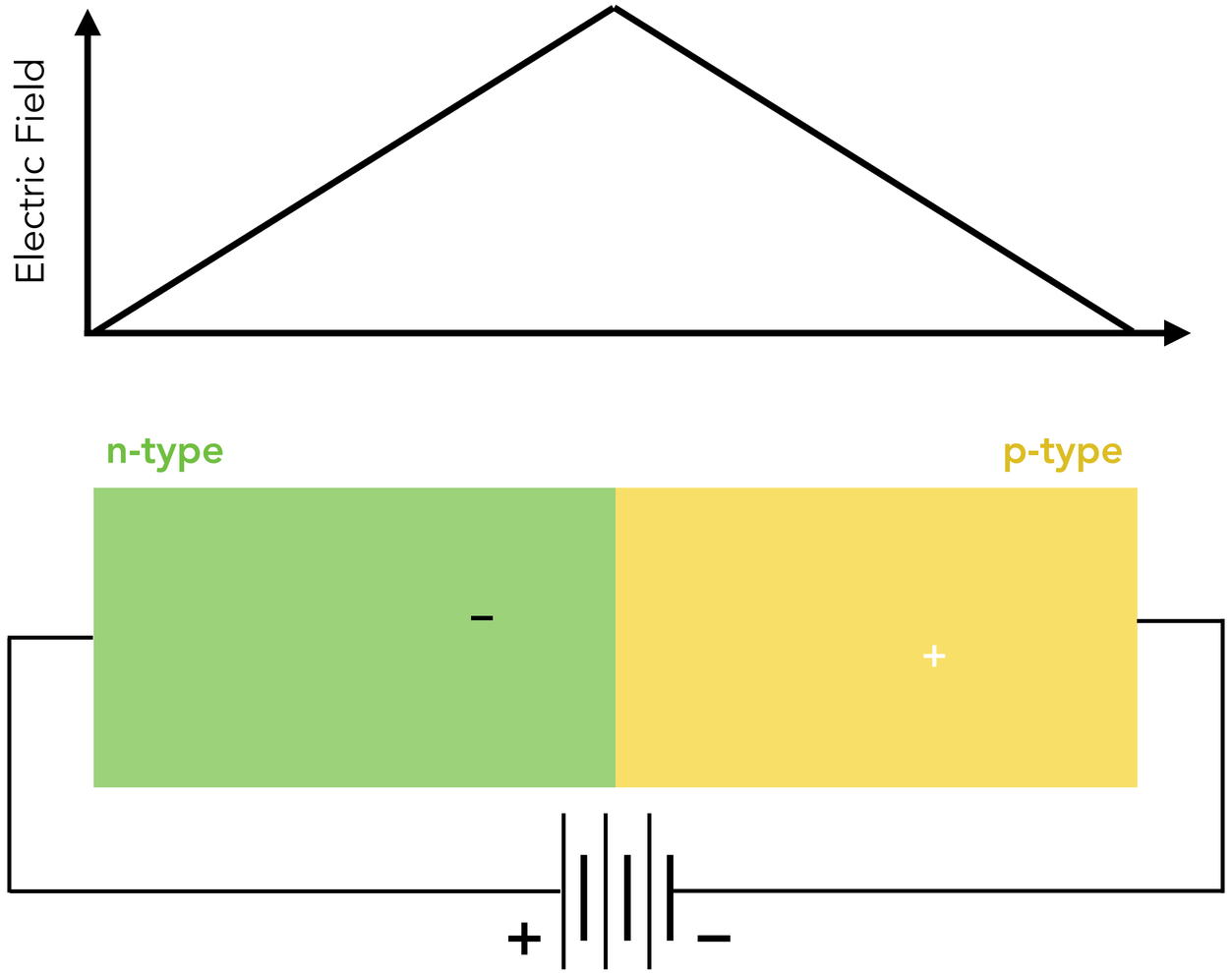
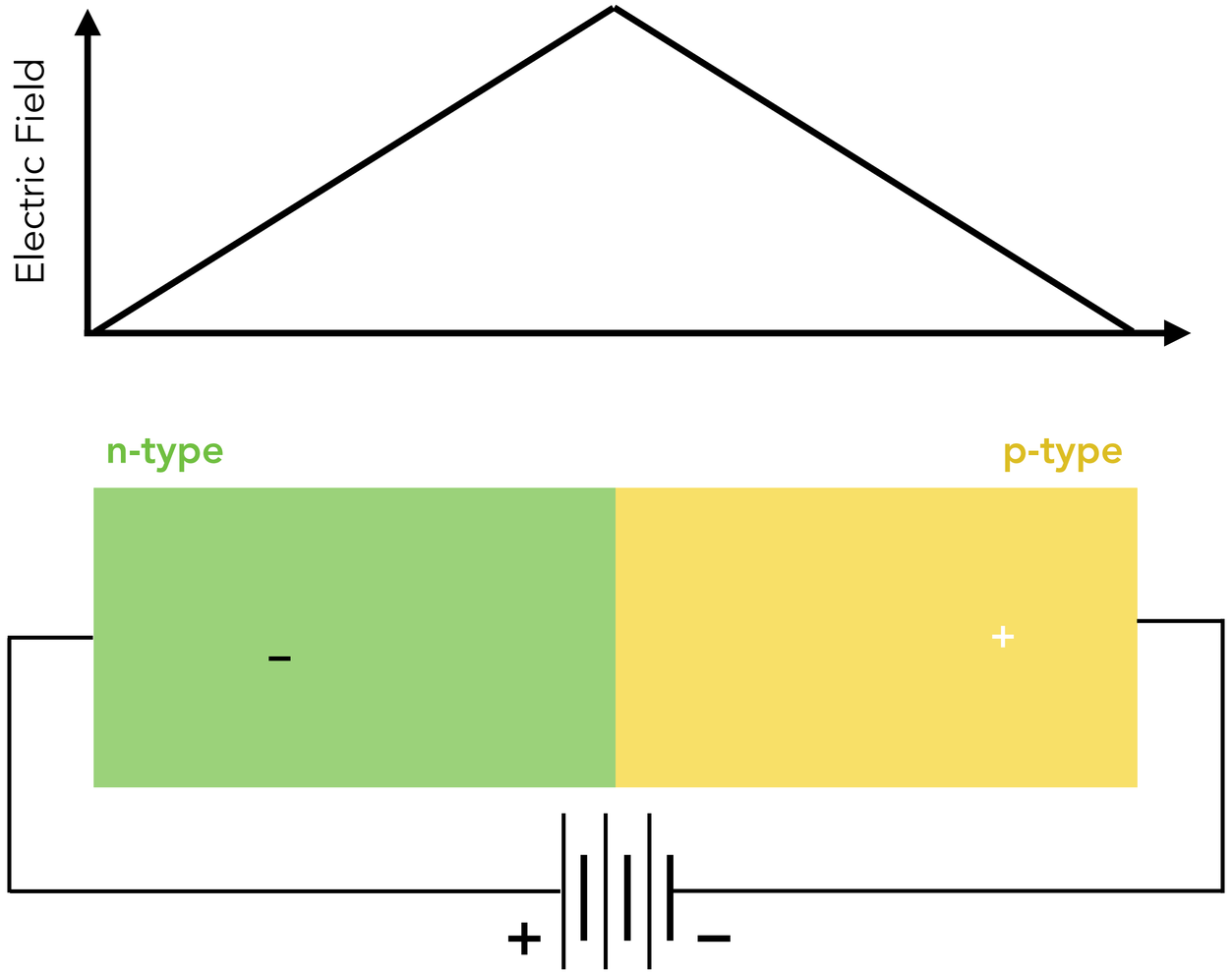
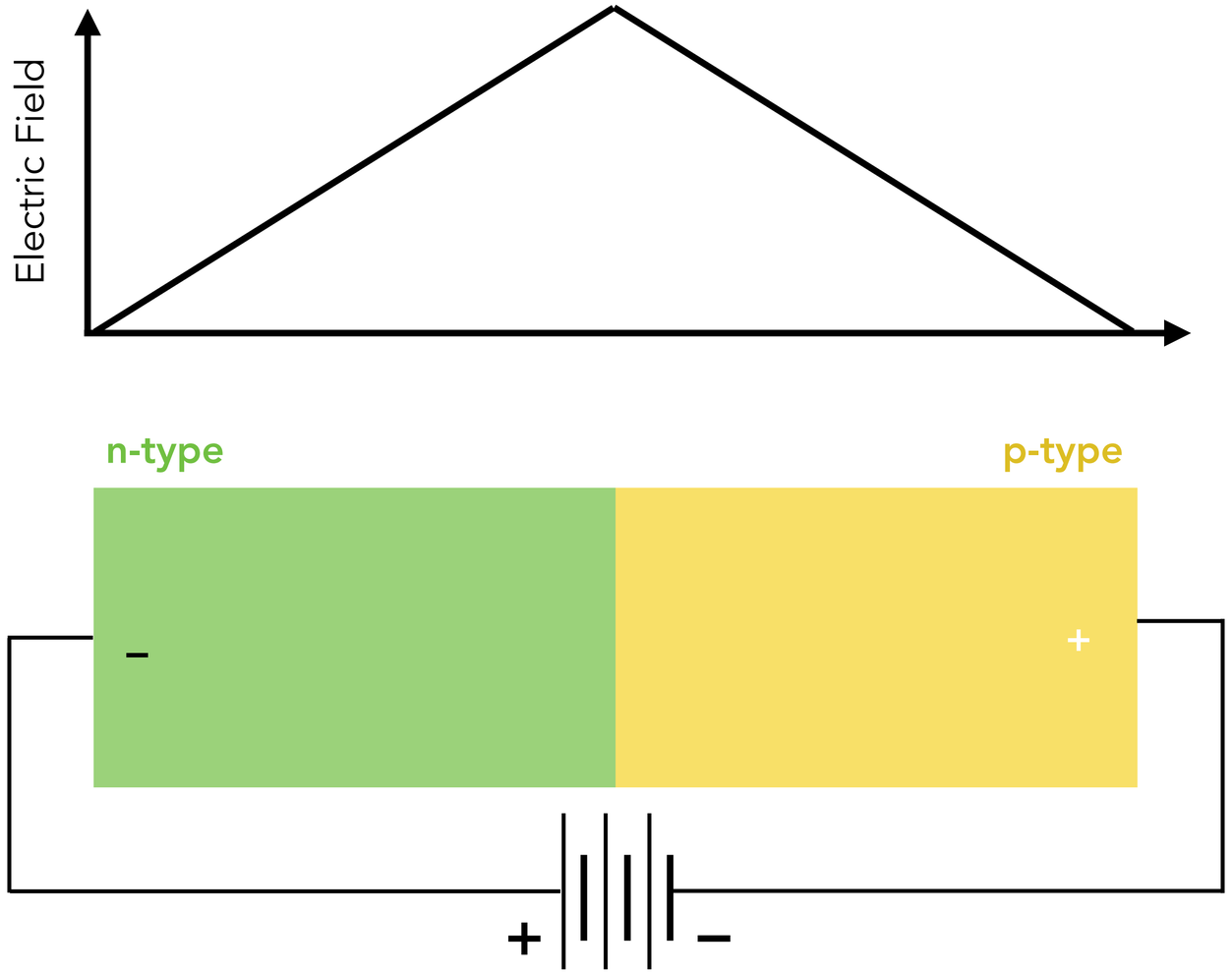


Charge carrier motion



Charge carrier motion



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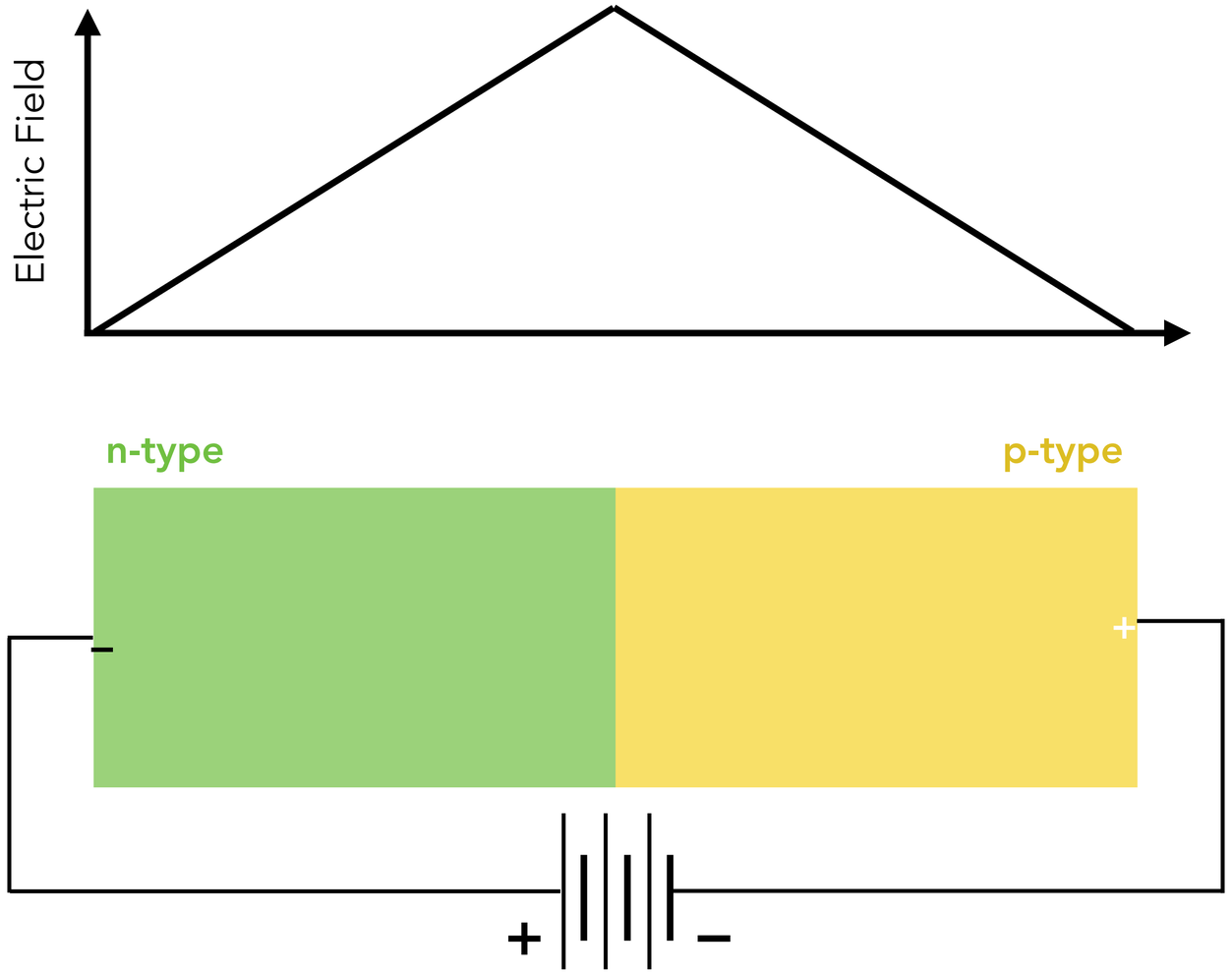
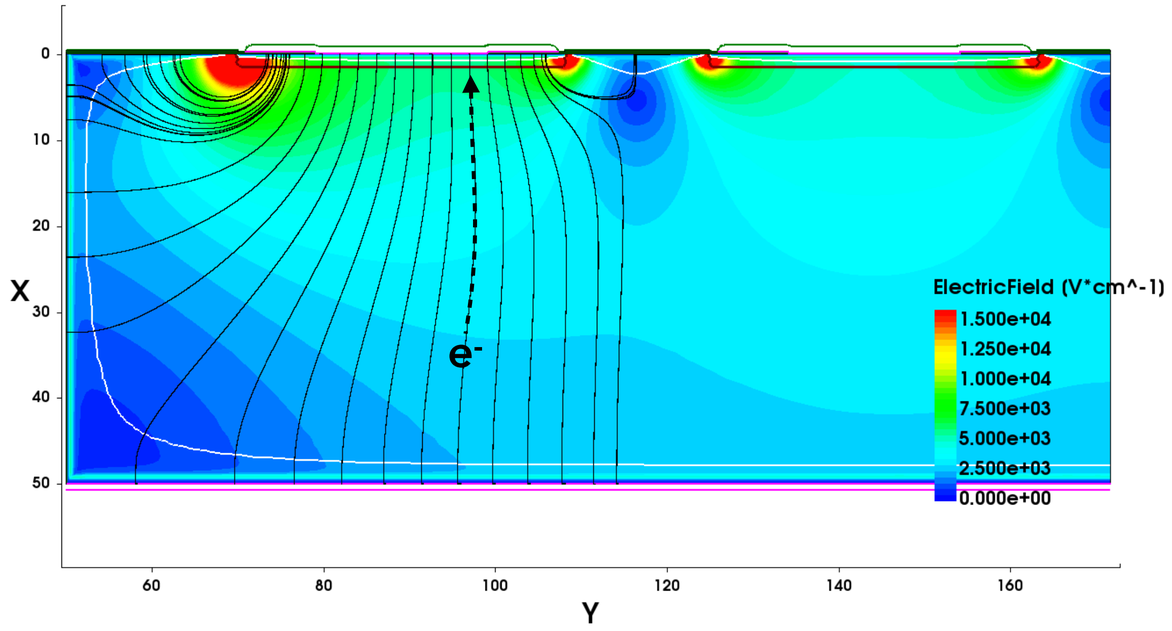


Charge collection

Typically we only collect one species of charge carrier - often electrons (as they travel faster) but historically p-on-n detectors were popular due to availability of high-resistivity n-type wafers

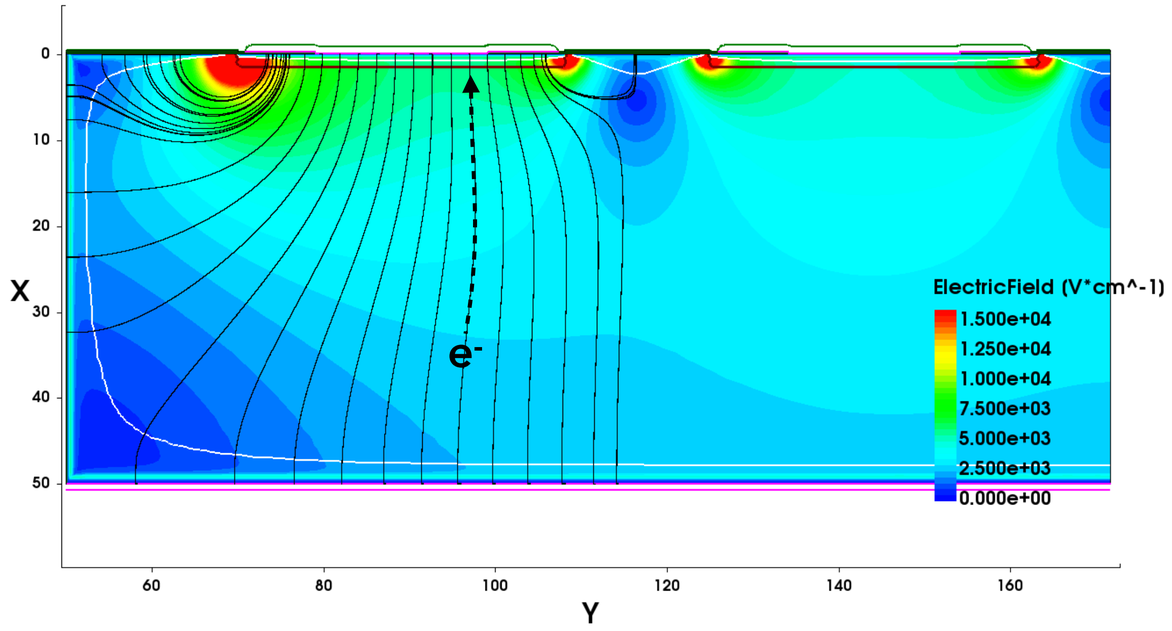
- Built-in depletion widths of only a few microns
- Charge carriers follow the electric field lines within the sensor



Induced current

In a simplistic approach, one can consider the signal at the collection node as being the sum of all of the charges that end up there

- This is true, but in fact a signal is generated *as each charge carrier starts to move*



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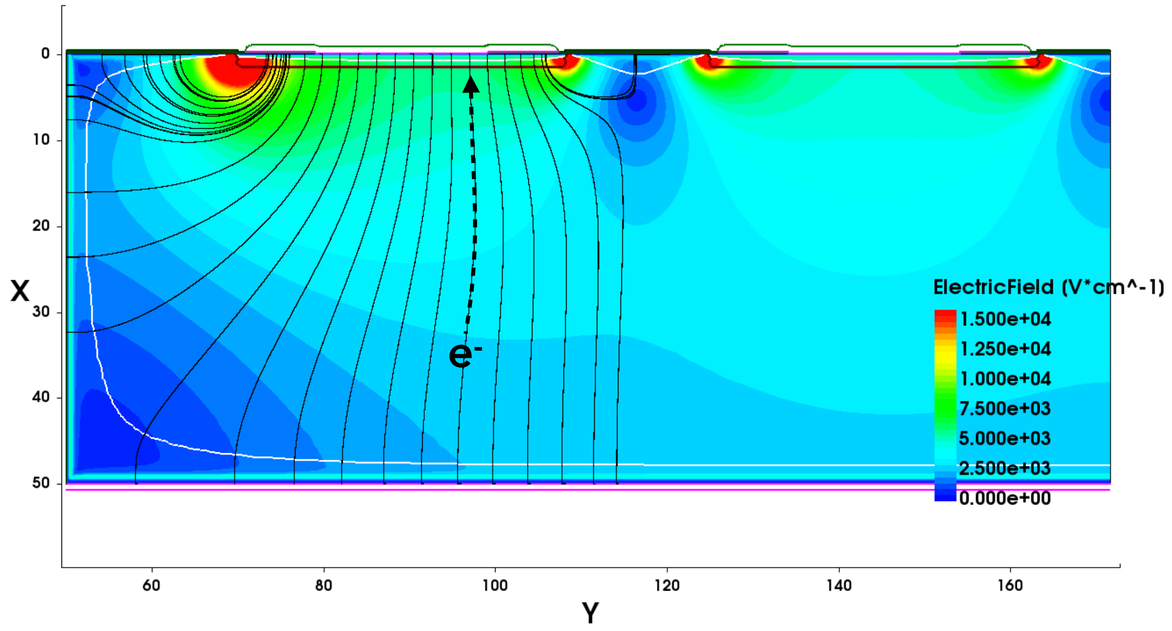
- This is described by Ramo-Shockley theorem

$$I_{ind}(t) = -\frac{q}{V_w}\mathbf{E}_n\left(\mathbf{x}_q(t); V_w\right) . \frac{d}{dt}\mathbf{x}_q(t)$$



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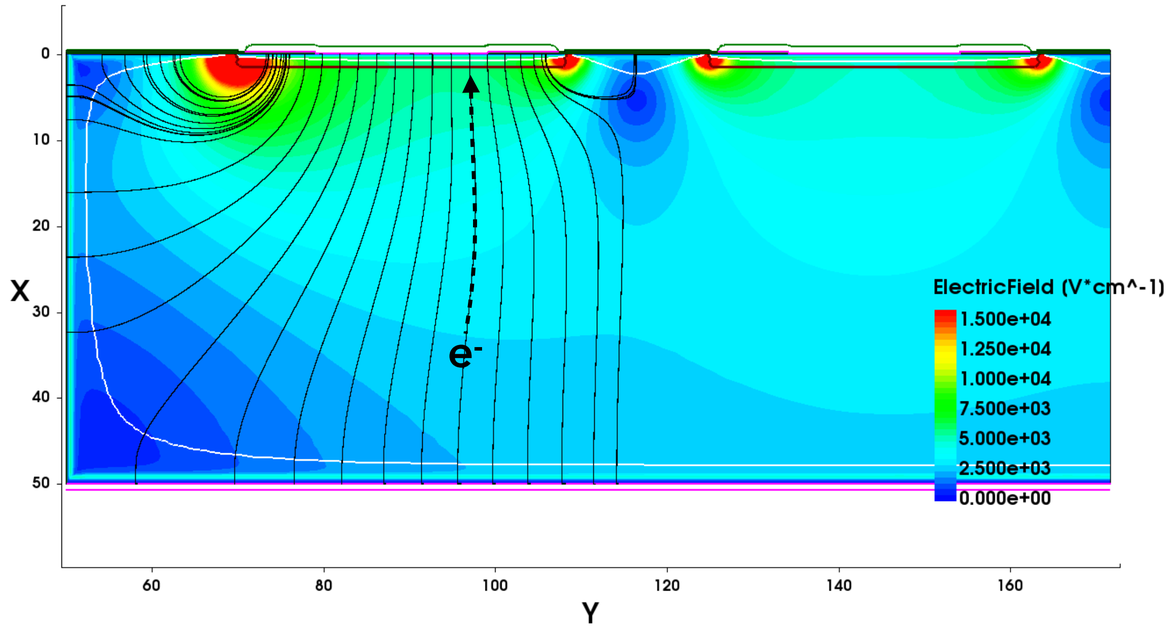
- This is basically dictated by the **weighting field**



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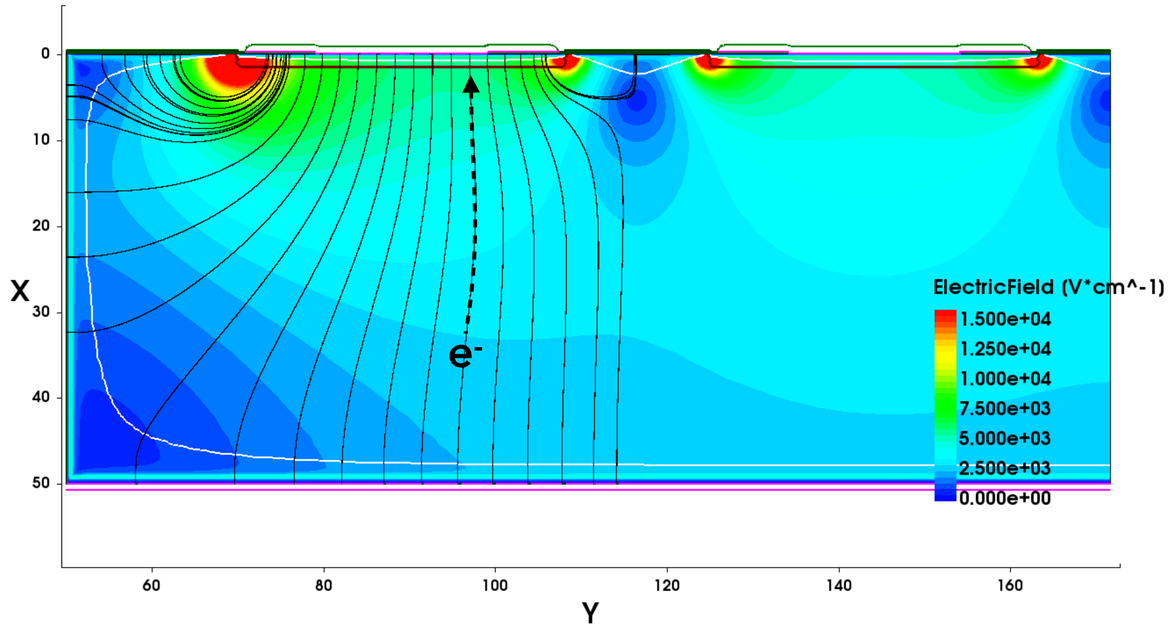
- This is basically dictated by the **weighting field** and the **velocity**



Charge carrier generation

Generating charge carriers

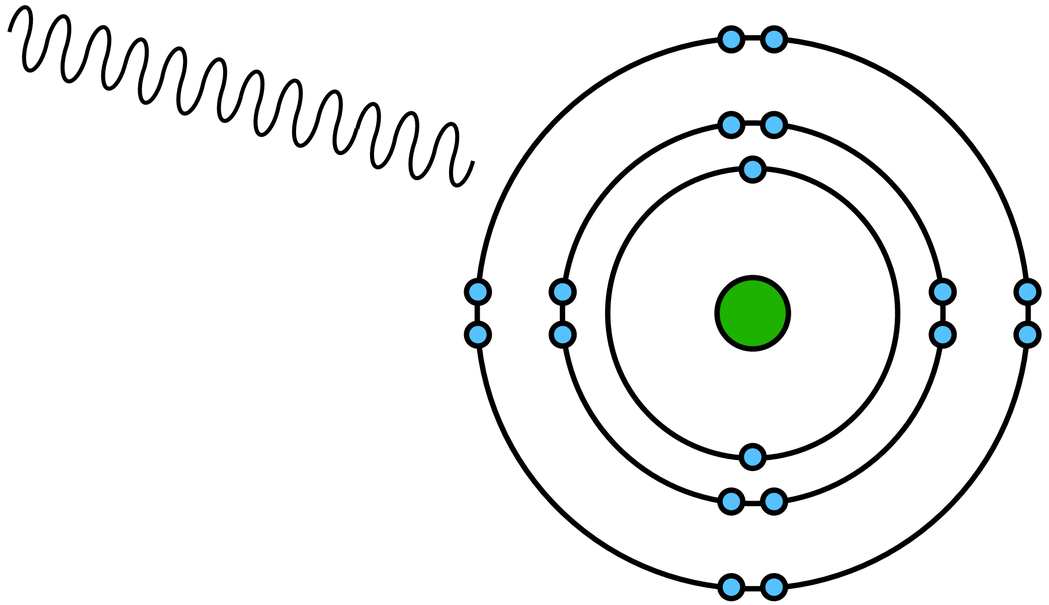
Different particles will interact different with the electrons in our silicon

- Photons have no mass
- Electrons are identical in mass
- Other charged particles are substantially heavier

Photon interactions

Photon interactions depend heavily on the energy of the photon and the density of electrons in the medium, but the following options are available:

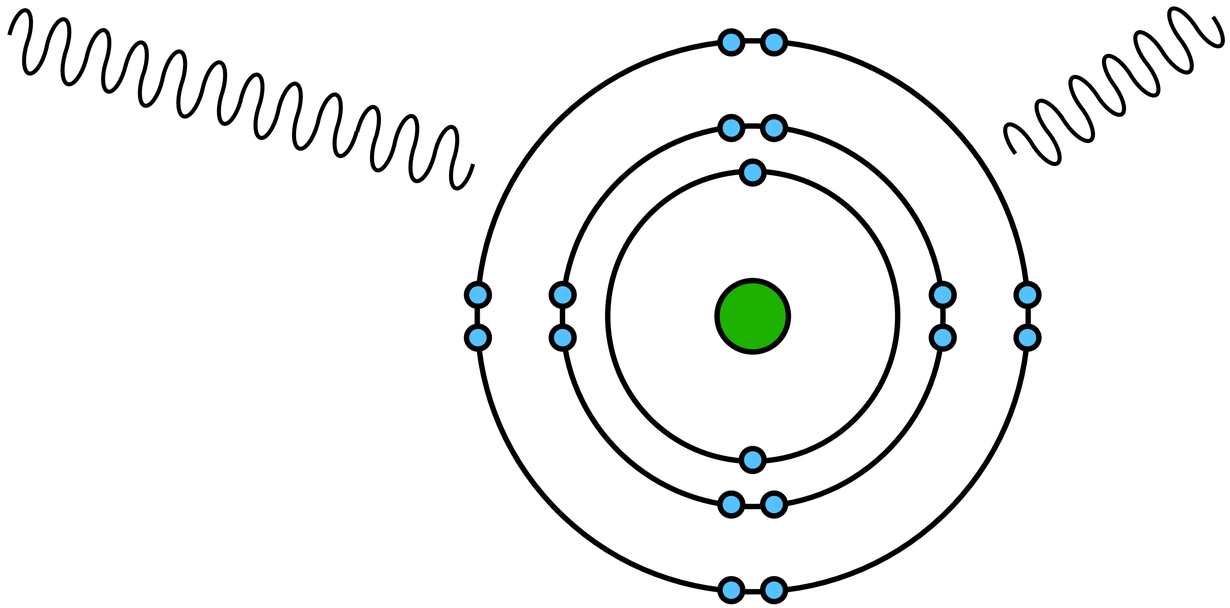
- Elastic scattering (Rayleigh)
- Absorption (photoelectric effect)
- Inelastic scattering (Compton)
- Conversion into matter (pair production)



Photon interactions - Rayleigh scattering

Rayleigh scattering is elastic scattering - so there is no transfer of energy to the medium

- This doesn't help us much to detect anything…

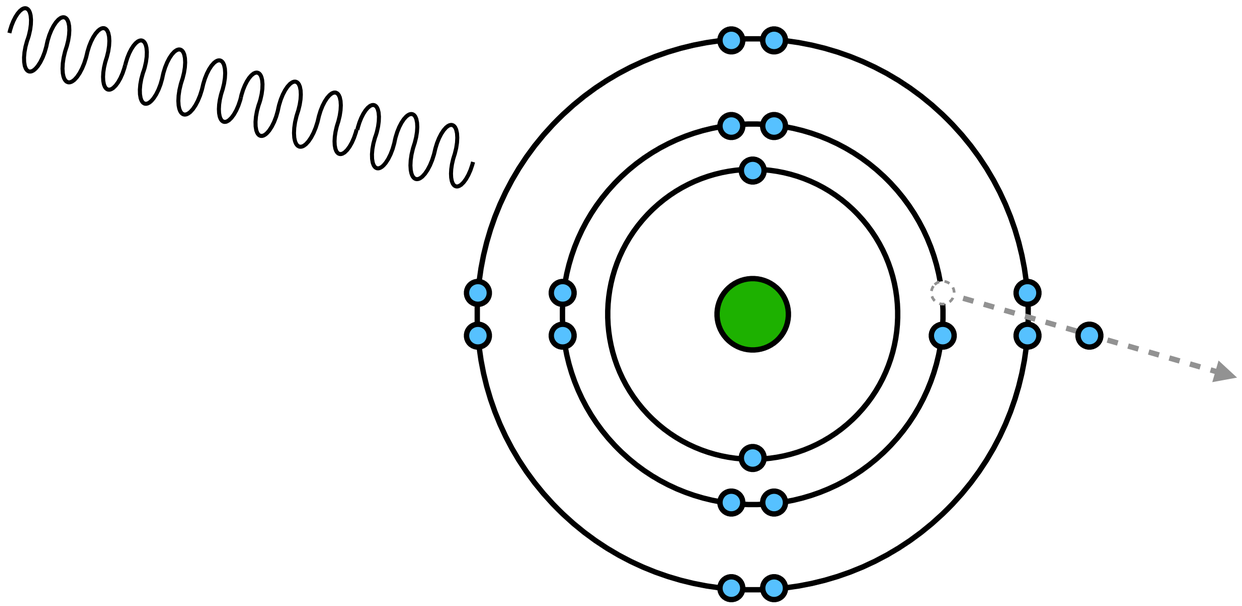


Photon interactions - photoelectric effect

In the photoelectric effect the photon is fully absorbed by an atom, which ejects an electron with energy E_{photon} - $E_{binding}$

- The process involves the whole atom to facilitate momentum transfer
- For this reason, it occurs mainly for inner electrons (K shell)
- The cross section depends strongly on atomic number Z, and drops off rapidly with photon energy:

$$\sigma \propto \frac{Z^4}{E^3}$$



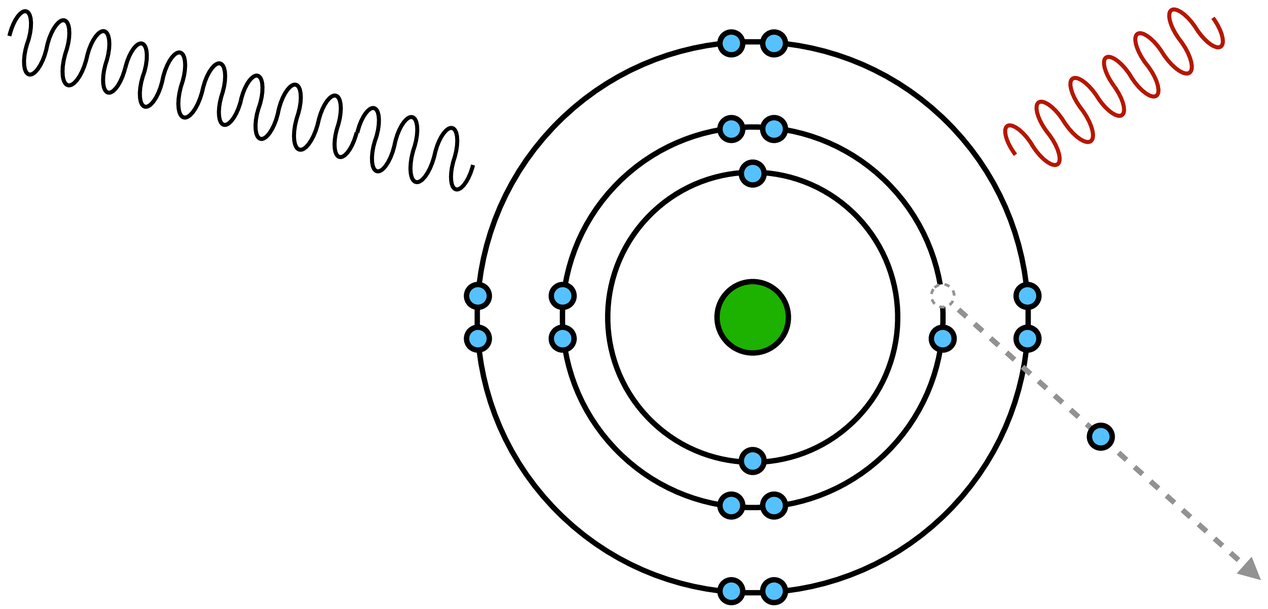
Photon interactions - Compton scattering

Compton scattering involves the *inelastic* scattering of photons from individual electrons

- Some of the photon energy is transferred to the electron

$$\frac{1}{E_f} - \frac{1}{E_i} = \frac{1}{m_e c^2}(1 - cos\theta)$$

- A lower energy photon will be scattered through angle θ
- The cross section is directly proportional to the electron density

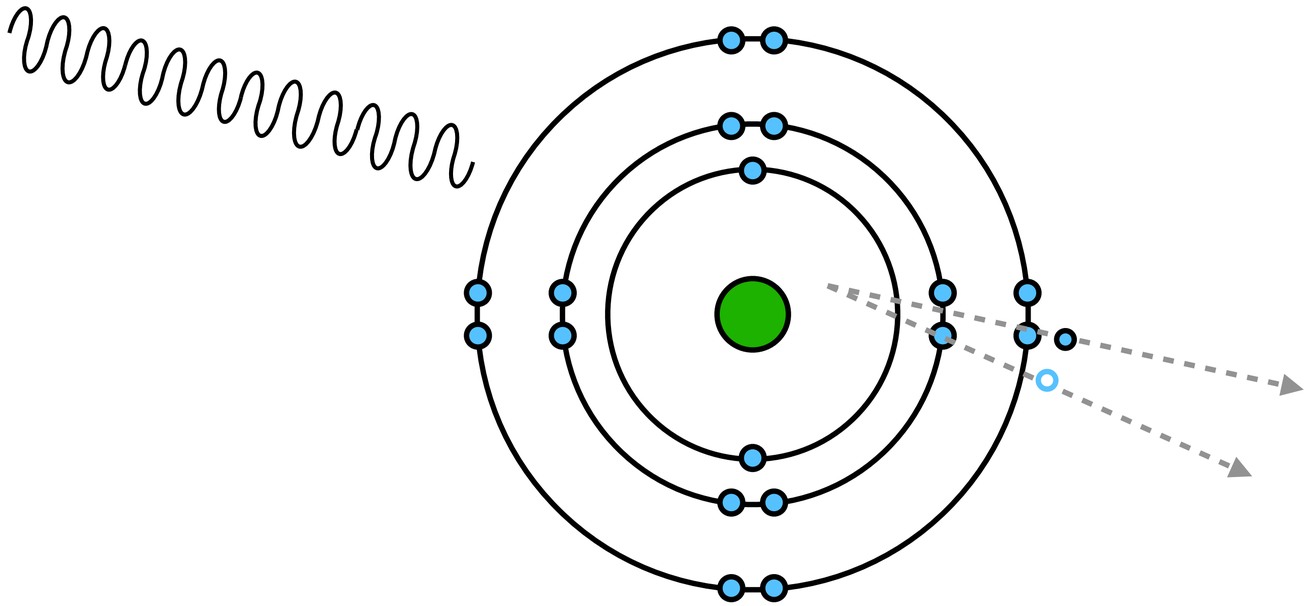


Photon interactions - pair production

Once the photon energy exceeds 1.022 MeV (twice the electron rest mass) then it can interact to produce an electron-positron pair

- As in the photoelectric effect, the nucleus is involved in the interaction to conserve momentum
- The corresponding cross-section varies with the atomic number and grows slowly with photon energy

$$\sigma \propto Z^2$$



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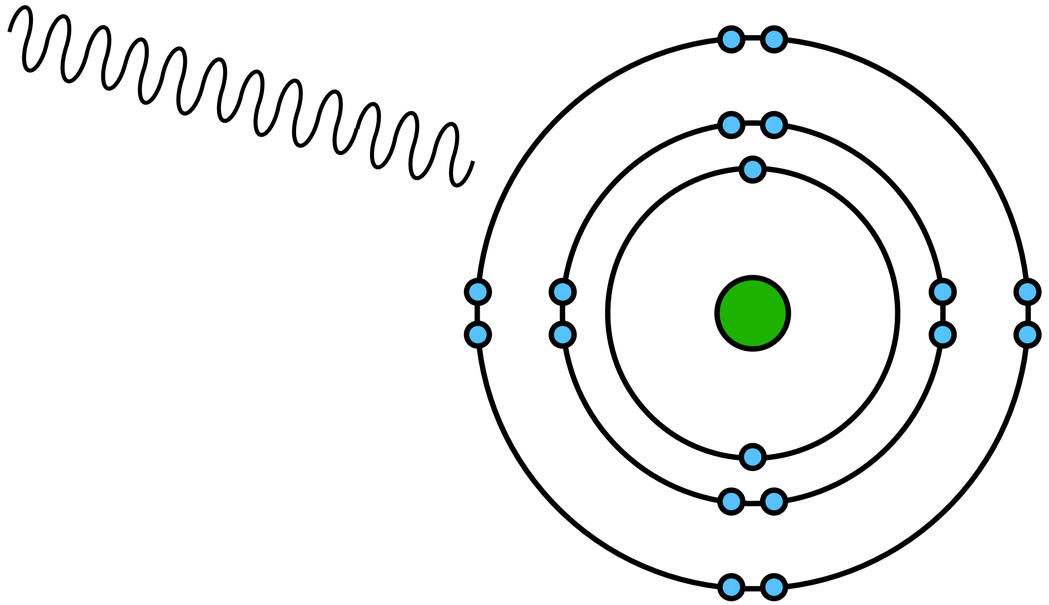

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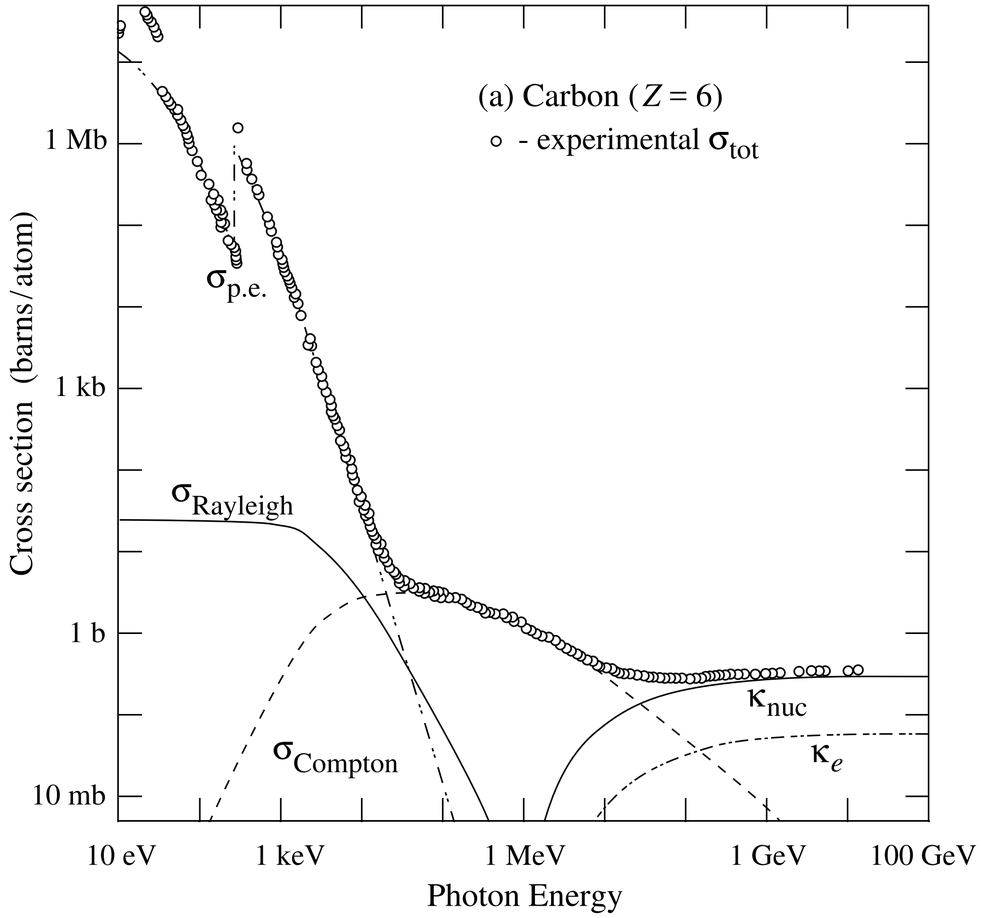

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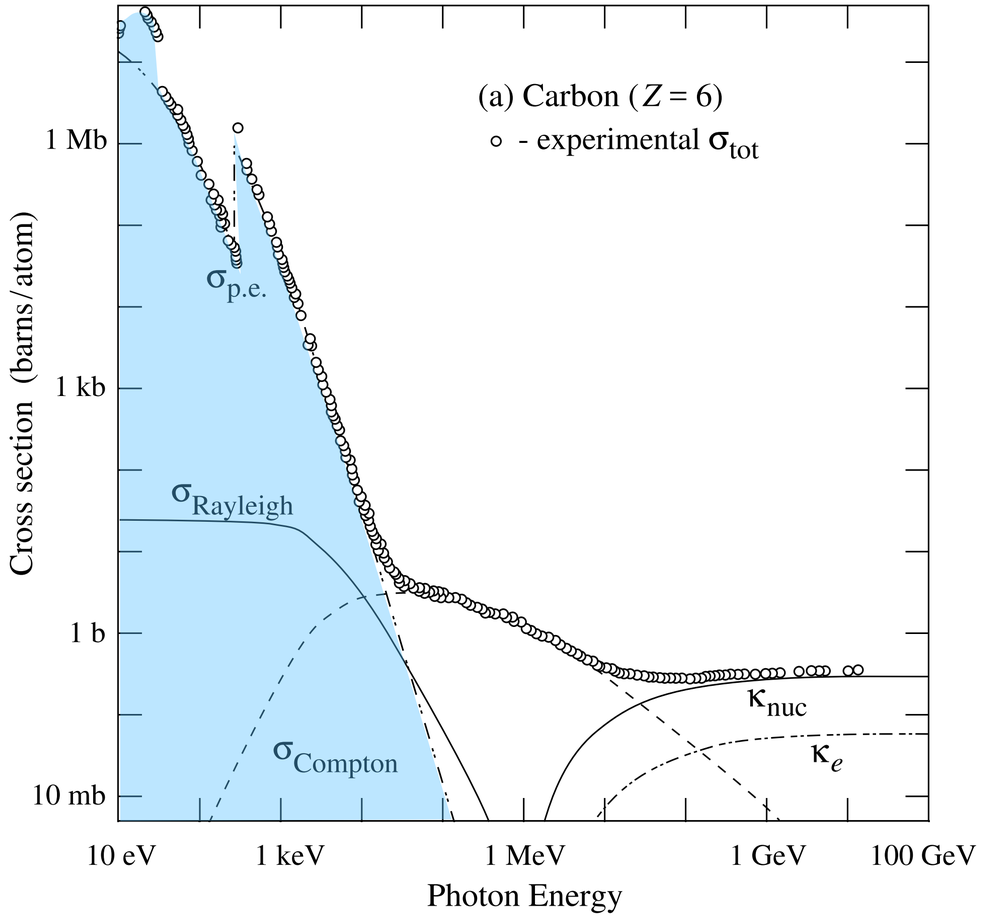

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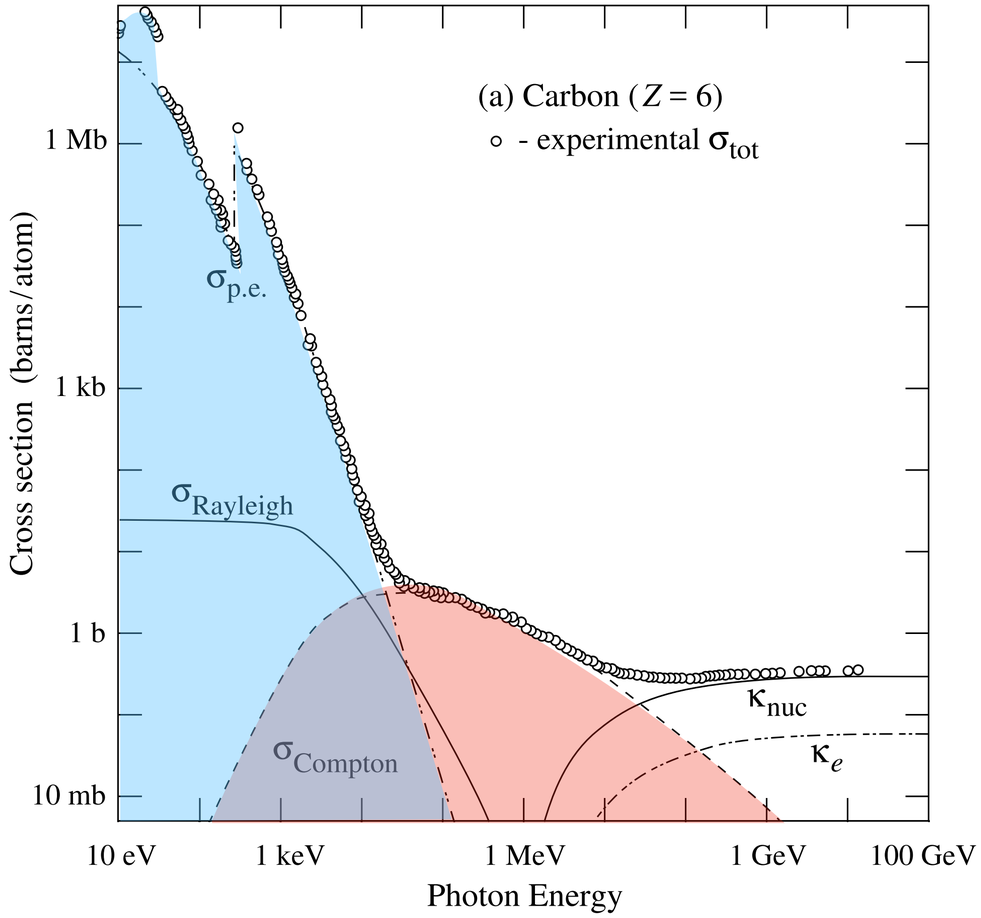

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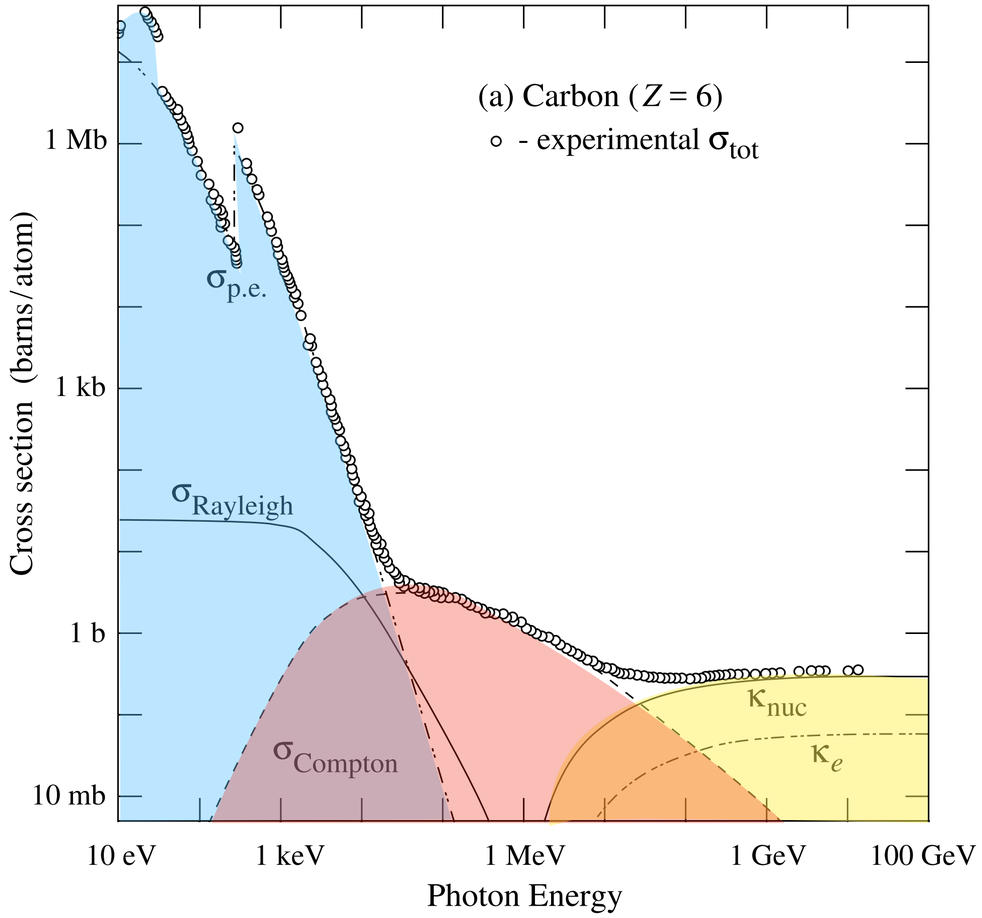

Interaction probability

For the purpose of photon detection, the end-result is that different photon energies interact more or less depending on the detection medium

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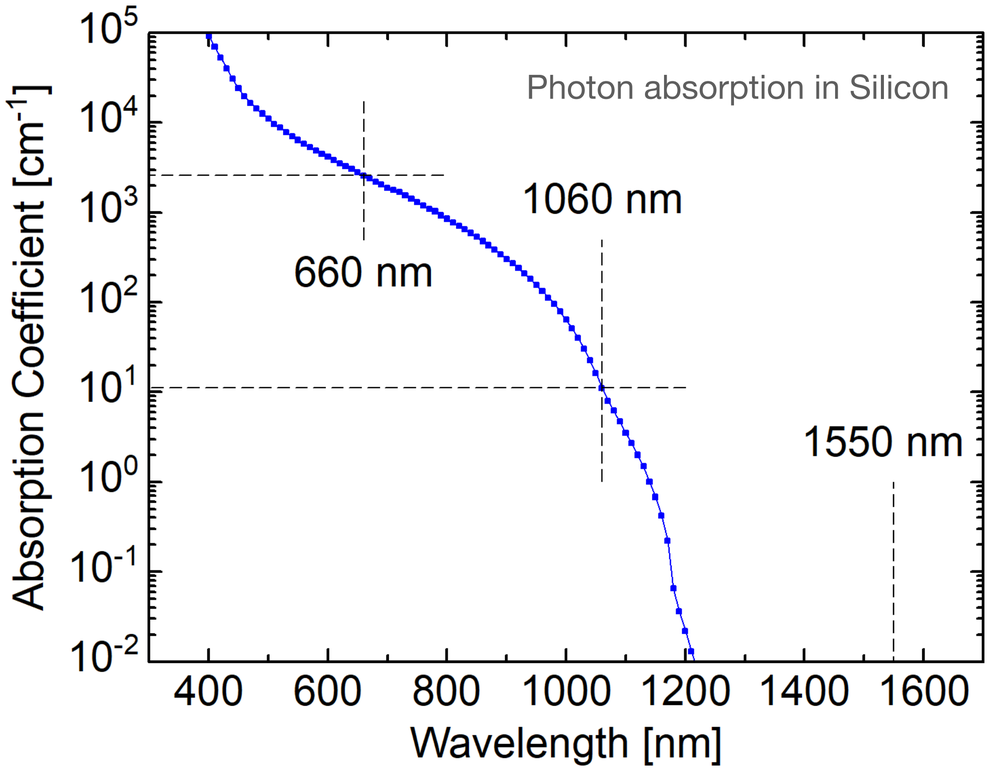
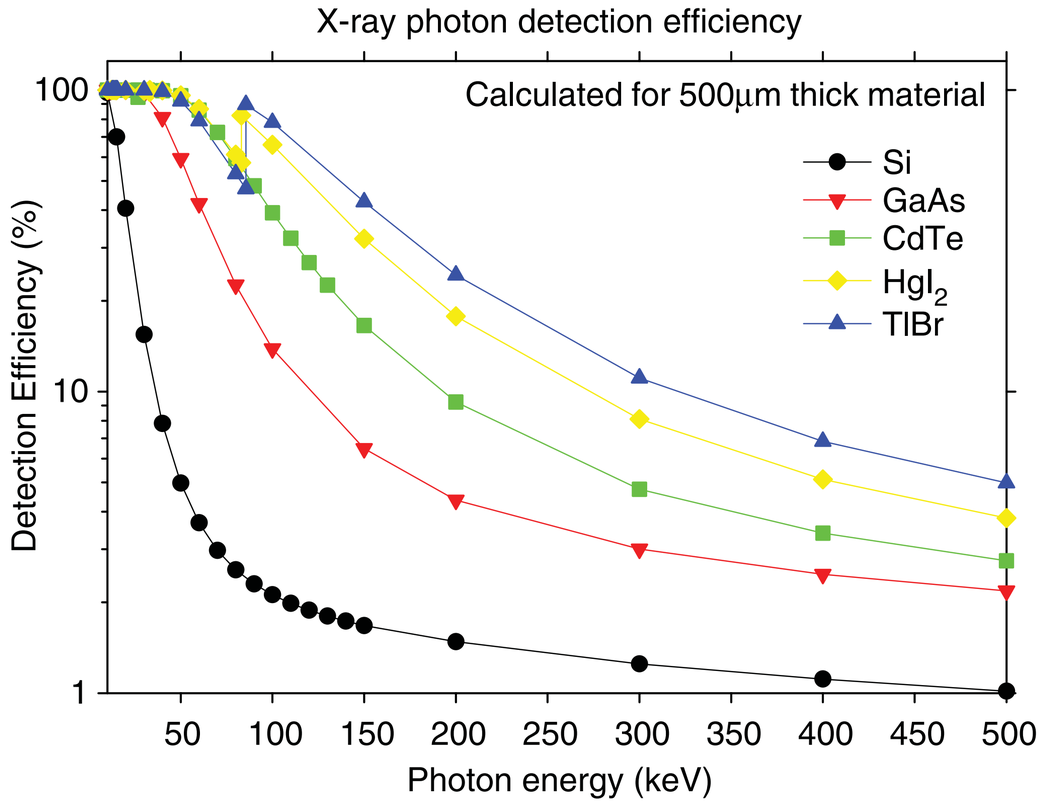


Interaction probability

For the purpose of photon detection, the end-result is that different photon energies interact more or less depending on the detection medium

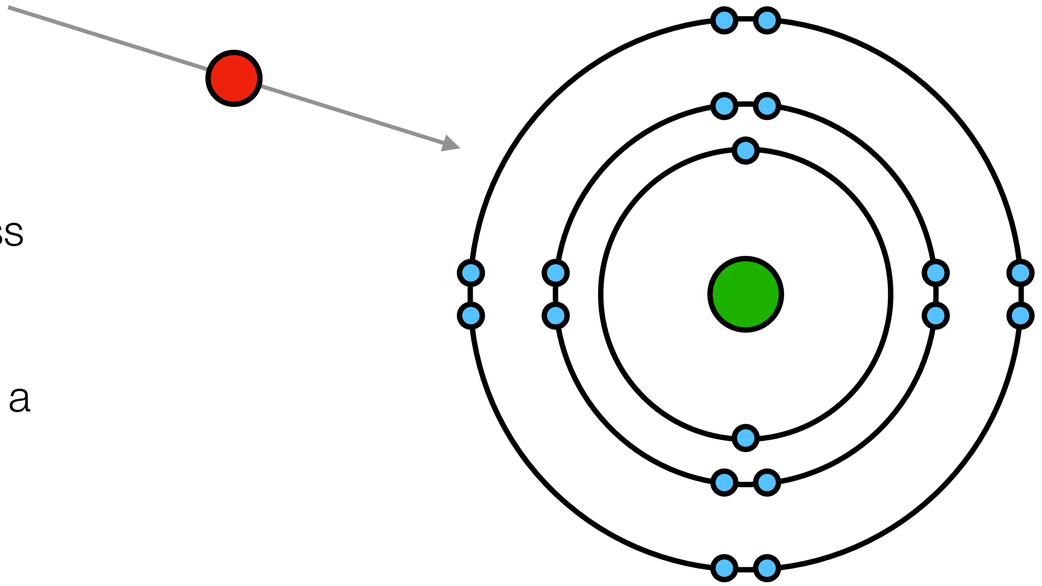
- At low energies materials become transparent
- At higher energies thicker sensors or higher Z materials are often needed in order to ensure that photons interact
- Many x-ray detectors focus on non-silicon sensors such as CdTe, GaAs - but note that silicon benefits from the entire microelectronics industry; everything from single crystal quality to fabrication



Particle interactions

For particles traversing a material, energy is lost through a series of ionisation events, where energy is transferred to individual electrons which are promoted to the conduction band (and may have enough energy to cause further ionisations)

- For electrons this is a bit more tricky since the mass of the two objects is the same
- For all other particles, we can assume that there is a series of interactions, which will distort the particle path and result in energy transfer

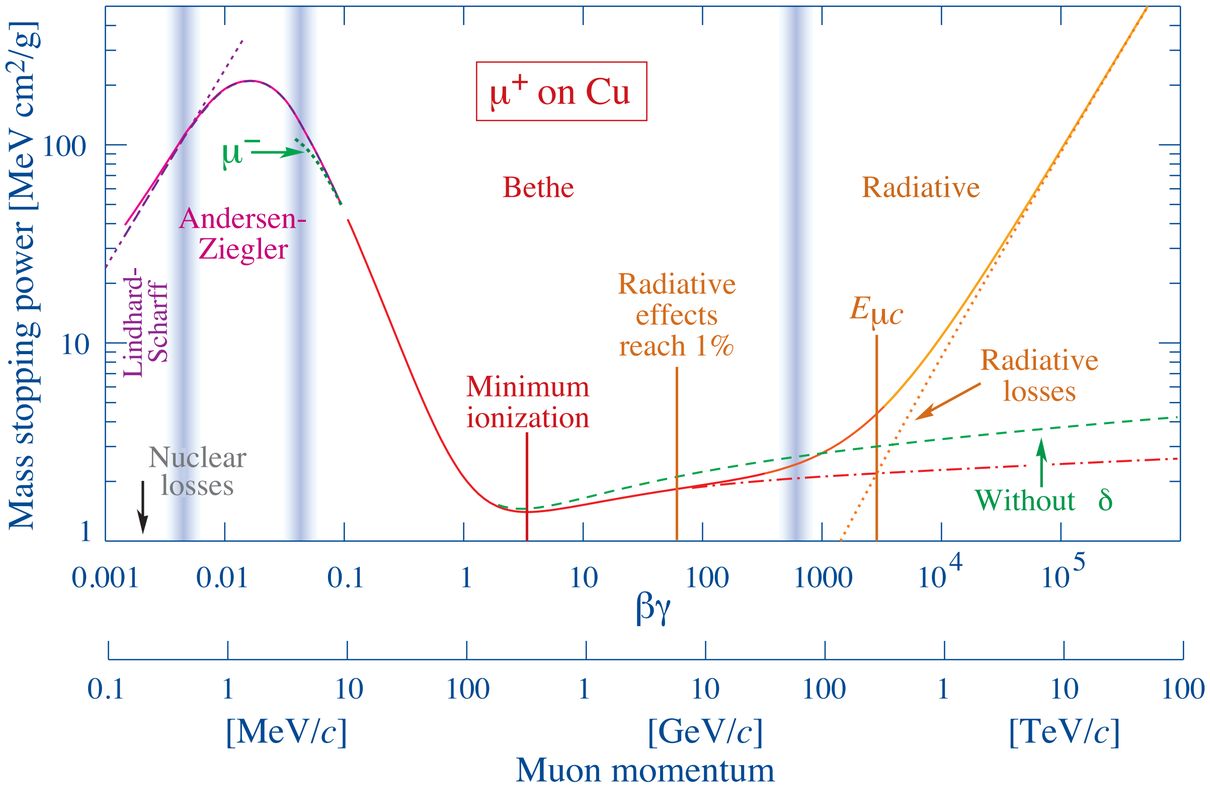


Particle interactions

The energy loss, dE / dx, is described by the Bethe-Bloch equation

$$\frac{dE}{dx} \approx \left(\frac{e^2}{4\pi\epsilon_0}\right)^2 \frac{4\pi z^2}{m_e v^2} NZ \left[ln\frac{2m_e v^2}{I} - ln\left(1-\frac{v^2}{c^2}\right) - \frac{v^2}{c^2}\right]$$

The energy loss is proportional to:



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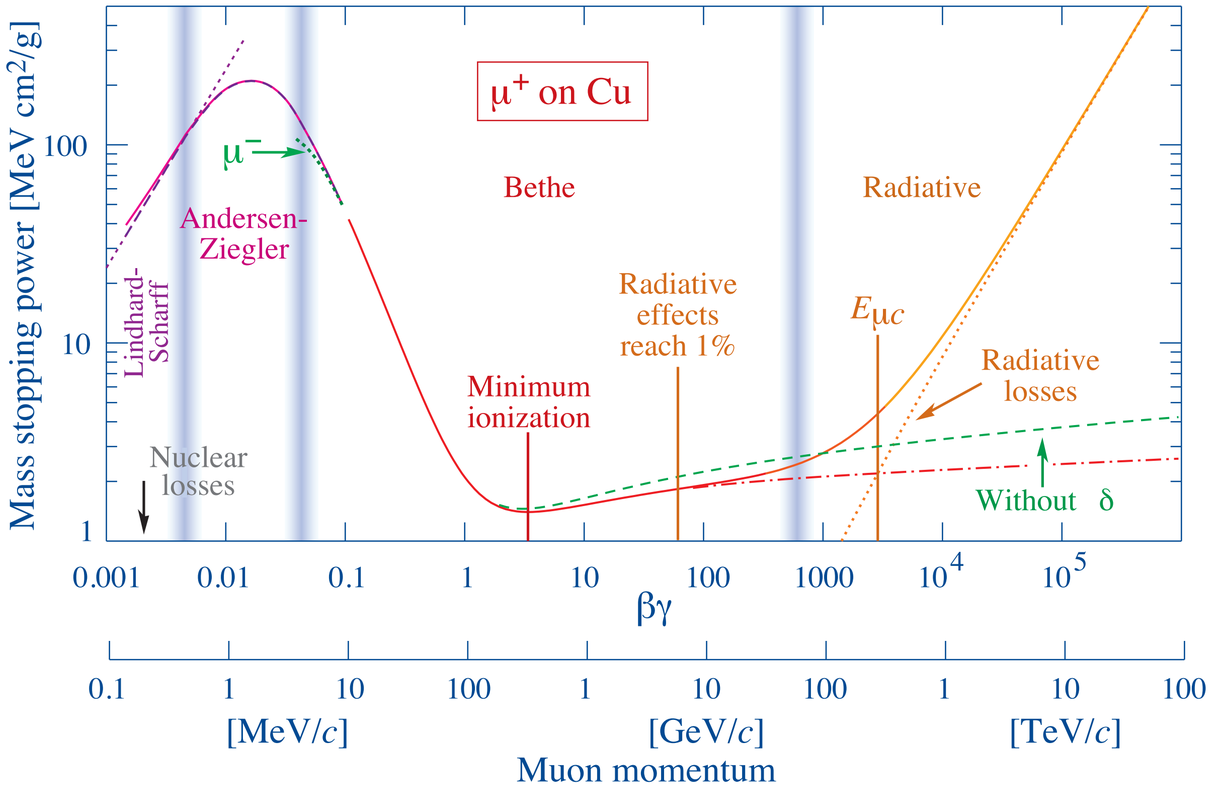
The energy loss is proportional to:

- The electron density



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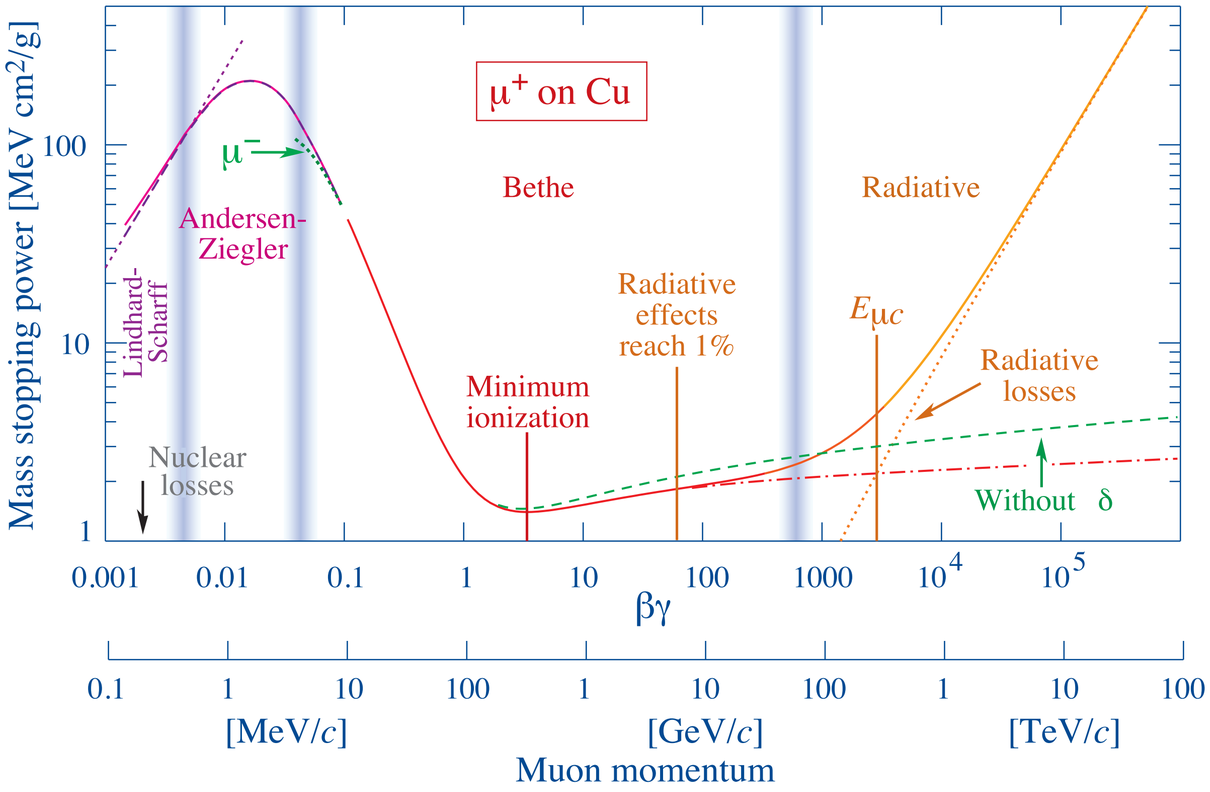
The energy loss is proportional to:

- The electron density
- The particle mass (at non-relativistic energies)



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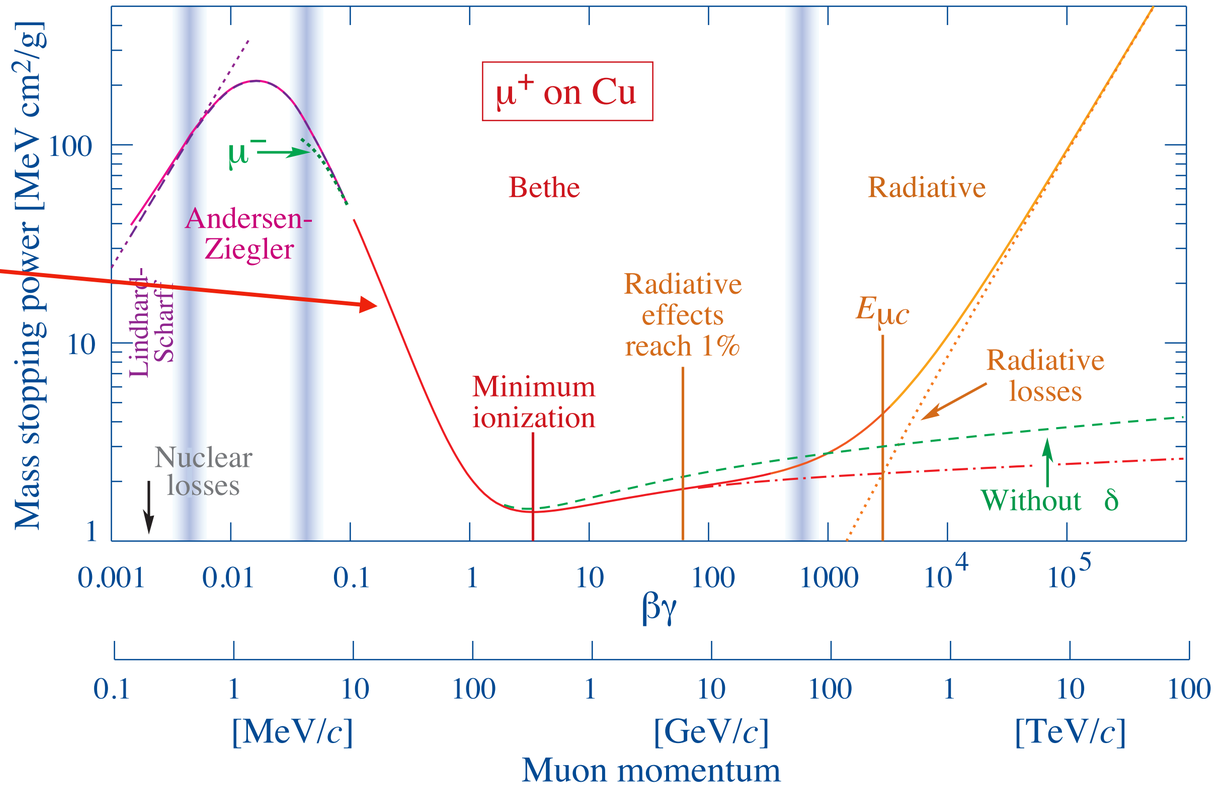
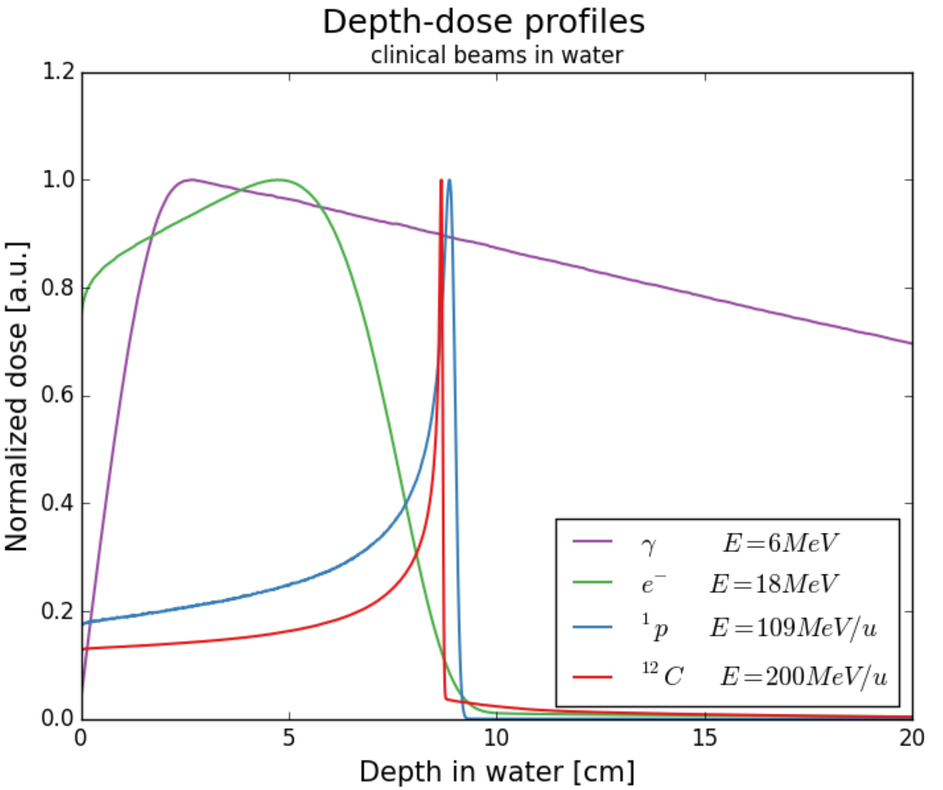
- β^{-2} when relativistic



Bragg peak

In some cases the particle energy is not high enough to pass fully through a given medium

- As the energy gets lower, the probability to interact increases, the higher the energy transfer per unit length
- This leads to a peak in energy as the particle reaches it's end-point - the **Bragg peak**
- This is relevant for detectors, but more important when thinking of targeted radiotherapy: the target zone can have a substantially higher dose than the surrounding healthy tissue



Radiation-induced defects

Radiation-induced defects

Particle interaction with a detector can lead to either

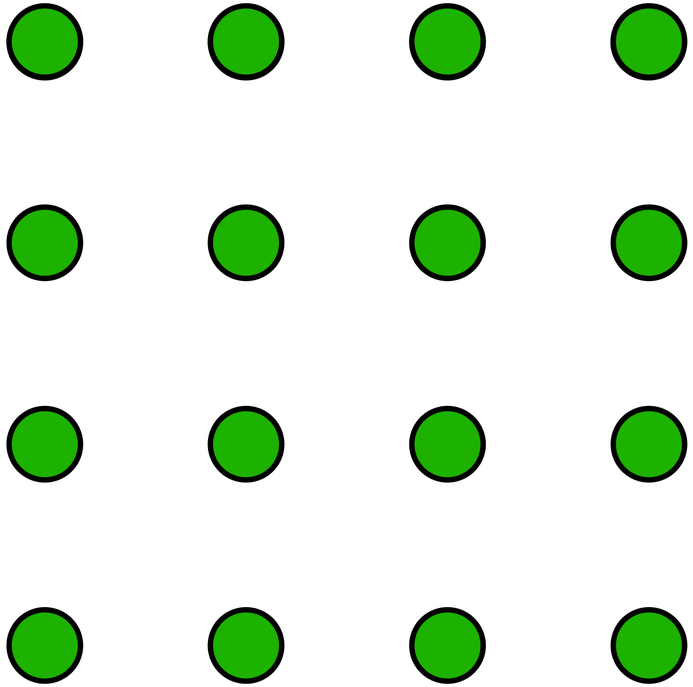
- Non-ionising energy loss
- Ionising energy loss

This could conceivably have detrimental effects

- Non-ionising effects - lattice displacements
- Gradual build-up of charge
- Single large charge deposit effects

Non-ionising energy loss (NIEL)

Depending on the incident radiation type, damage can be done to the periodic silicon lattice, representing displacement of atoms from their regular positions



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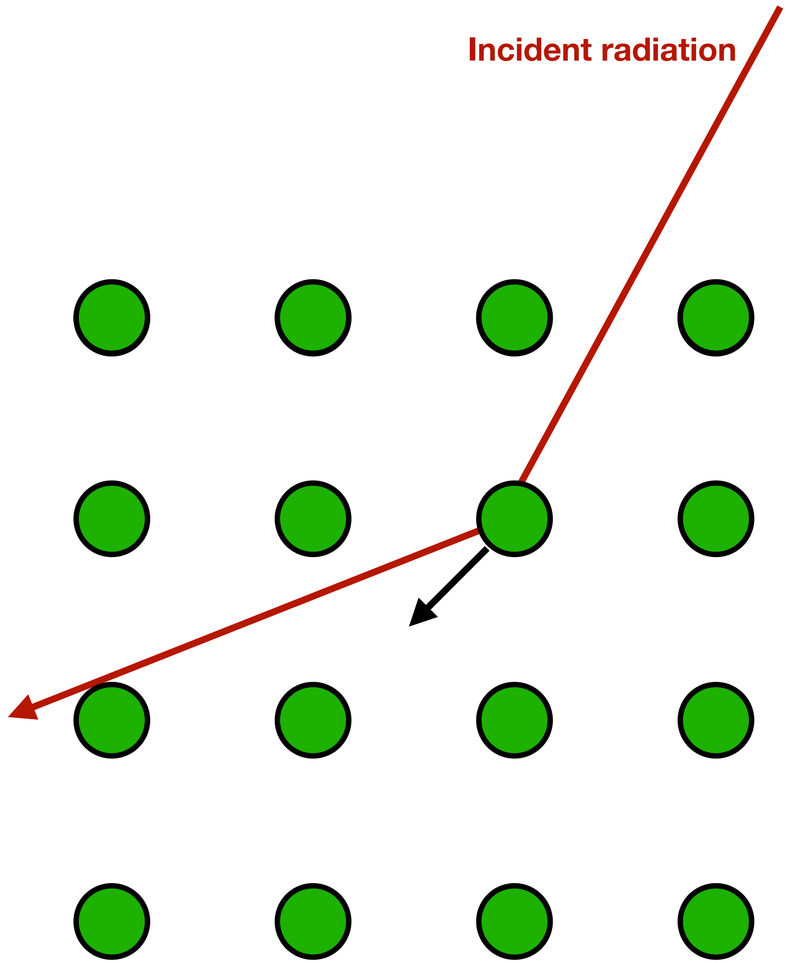
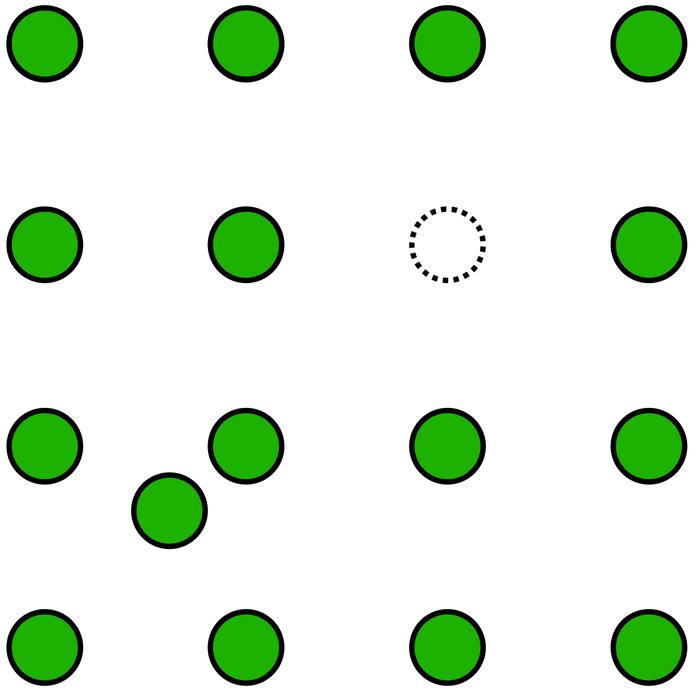
- Nuclear recoil leads to ejection of the silicon atom from the lattice



NIEL

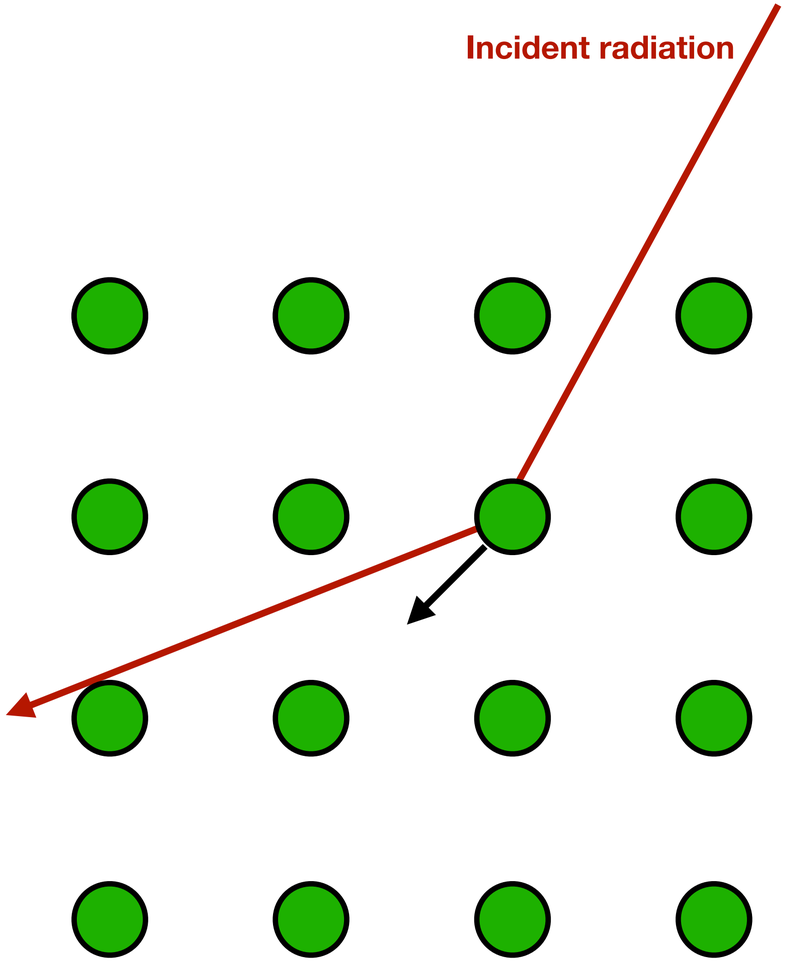
Depending on the incident radiation type, damage can be done to the periodic silicon lattice, representing displacement of atoms from their regular positions

- Nuclear recoil leads to ejection of the silicon atom from the lattice
- We produce **two** defects - an interstitial silicon atom, and a vacancy in the lattice (Frenkel defect)



NIEL

Alternatively, our incident radiation could impart enough energy onto the silicon atom that it is able to further displace atoms within the lattice



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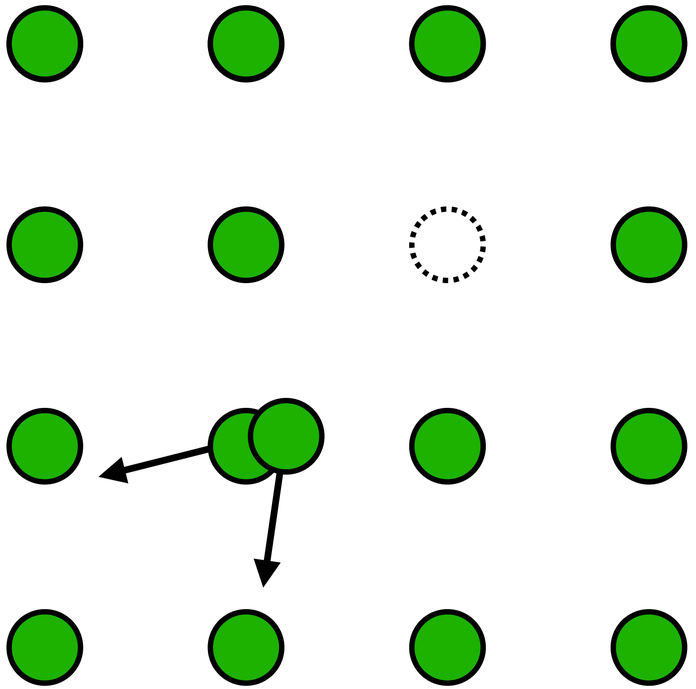

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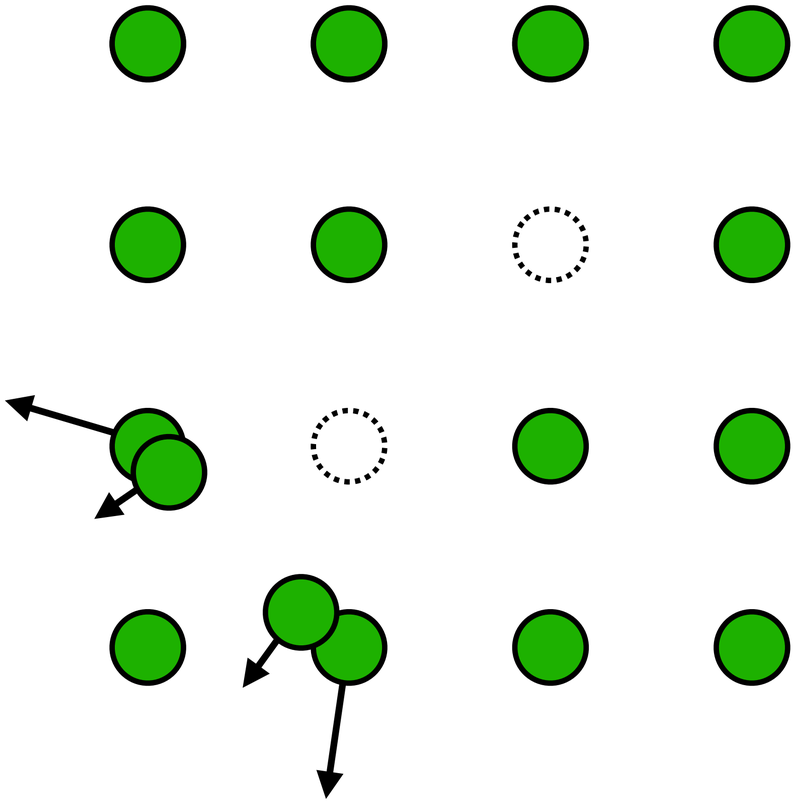

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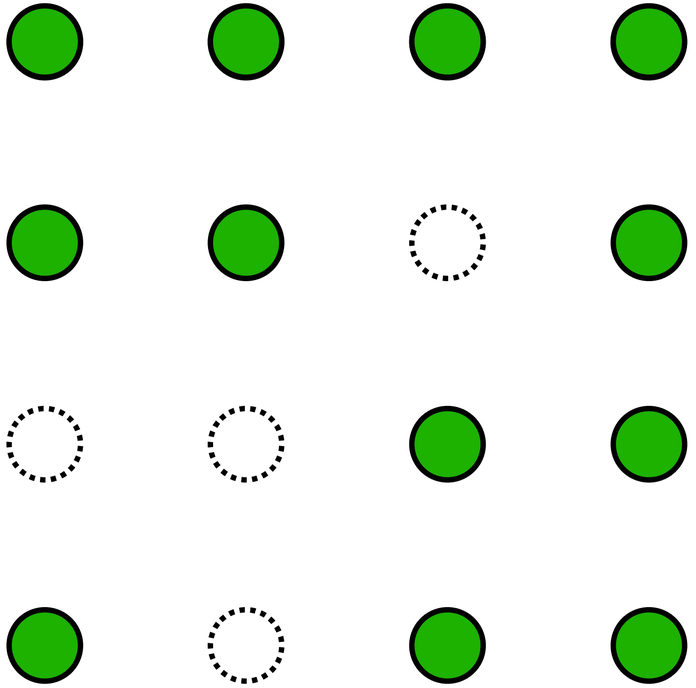
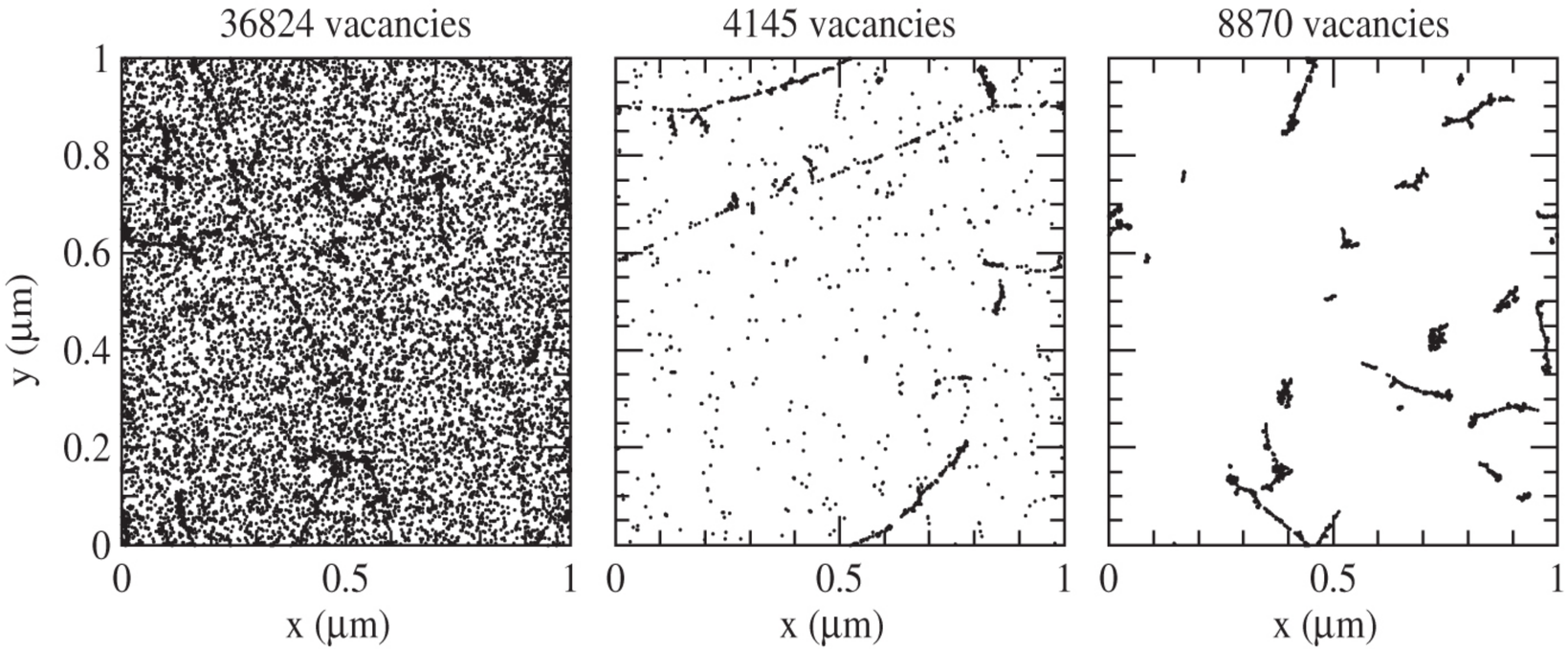
- We often distinguish between “point” defects and “cluster” defects to highlight these two separate cases



NIEL

All irradiated to 10^{14} cm^{-2}
Depth 1 μm



10 MeV protons **24 GeV protons** **1 MeV neutrons**

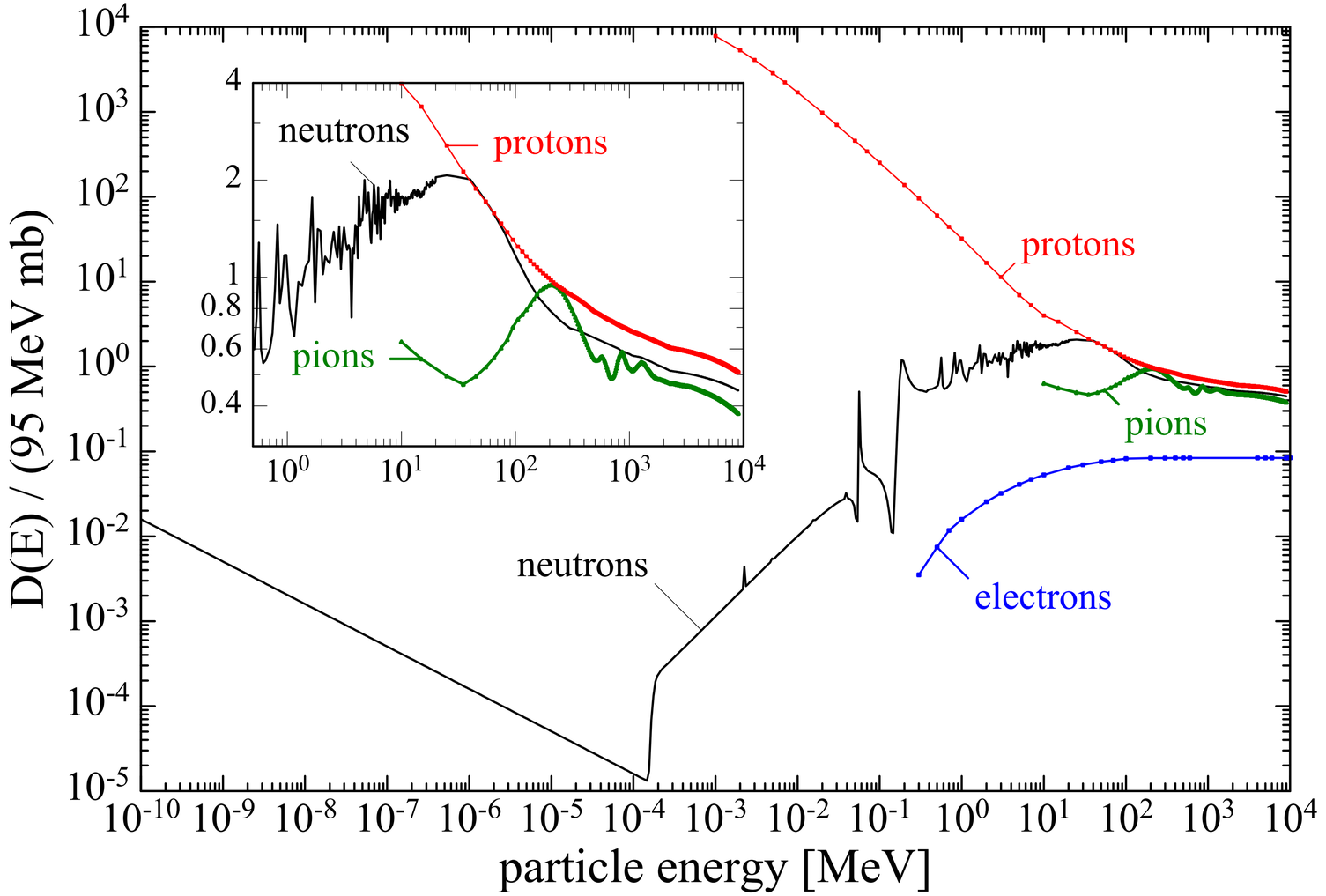
NIEL scaling hypothesis

The NIEL scaling hypothesis is:

> Damage effects by energetic particles in bulk material can be described by the total non-ionising energy loss to the lattice

Measurements of NIEL are generally expressed in units of 1 MeV n_{eq} cm^{-2}, and the damage inflicted by any particle of any energy can be expressed using a hardness factor, *k*

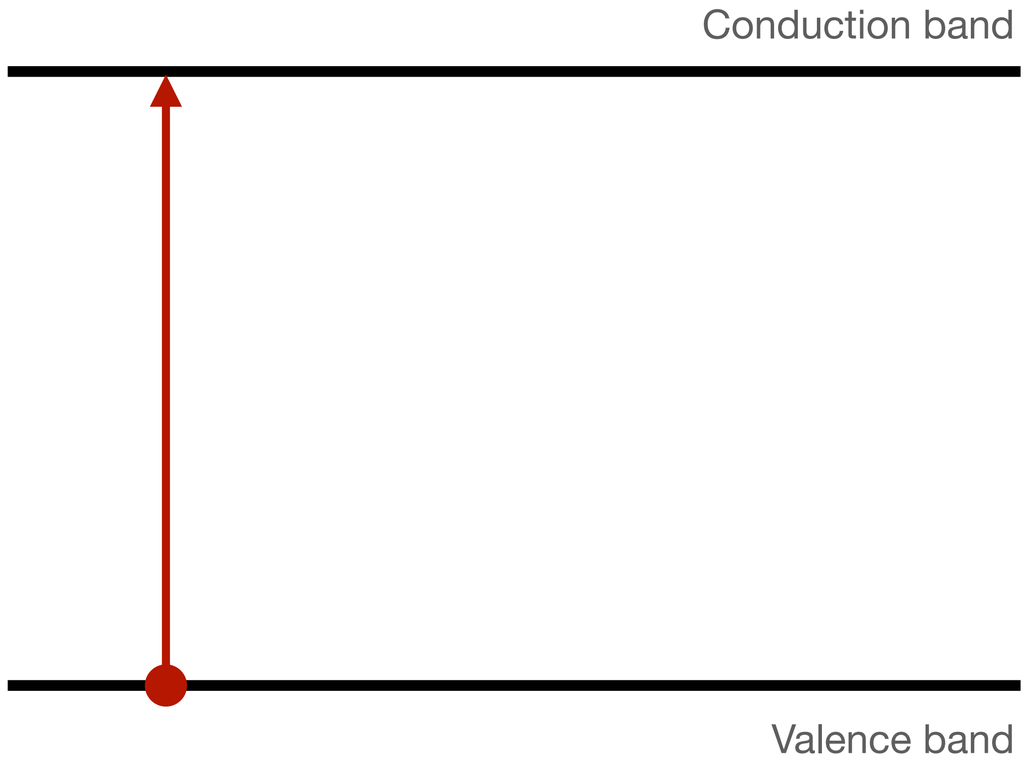
Hardness factors for different particles in silicon



Energy levels in semiconductors

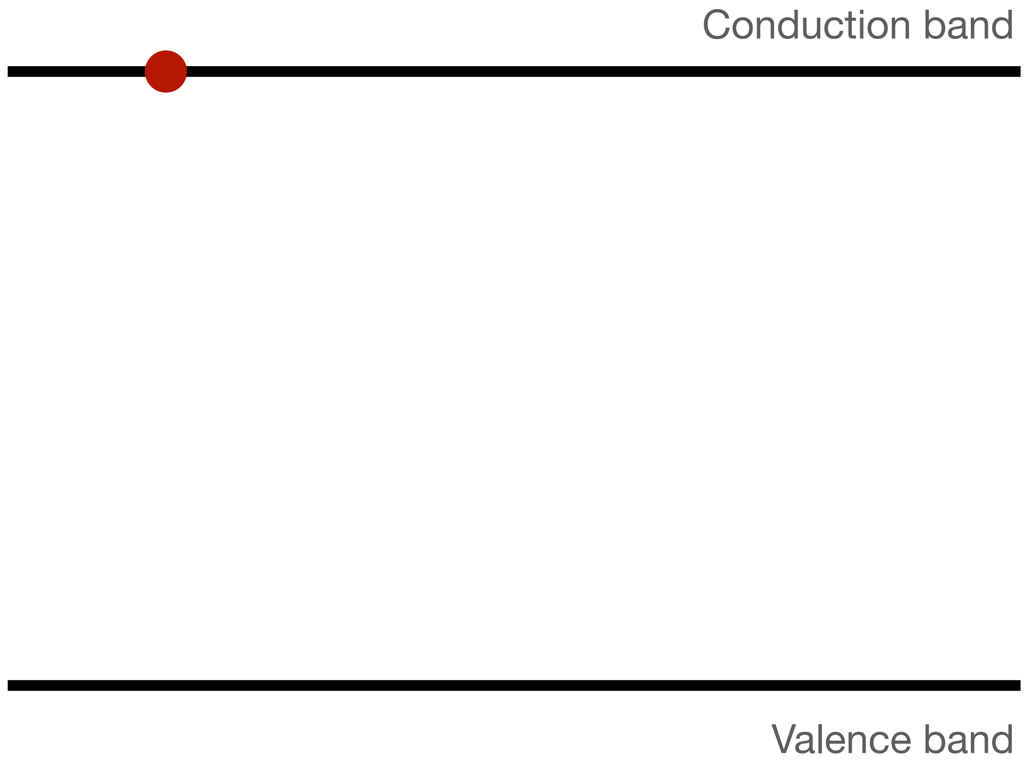
Charge carrier production in semiconductors relates to transitions from the valence to conduction band

- In depleted silicon detectors, this is the mechanism by which interacting particles are observed



Energy levels in semiconductors

Where this goes wrong after irradiation damage is the introduction of additional energy levels in the band gap



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Where this goes wrong after irradiation damage is the introduction of additional energy levels in the band gap

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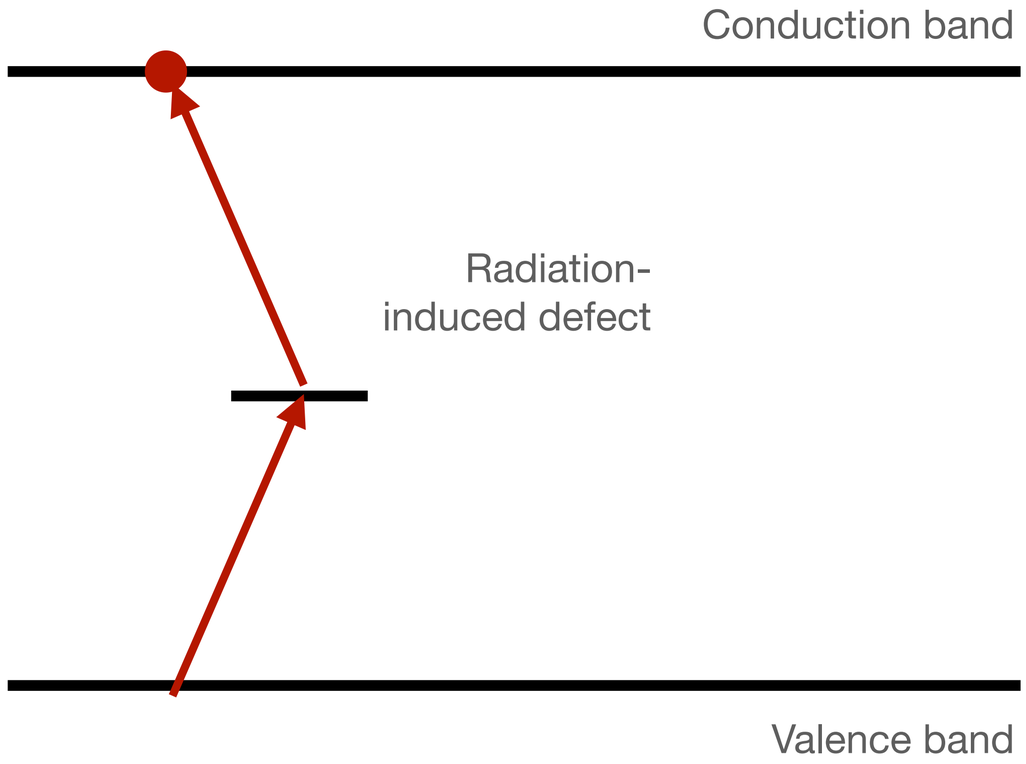

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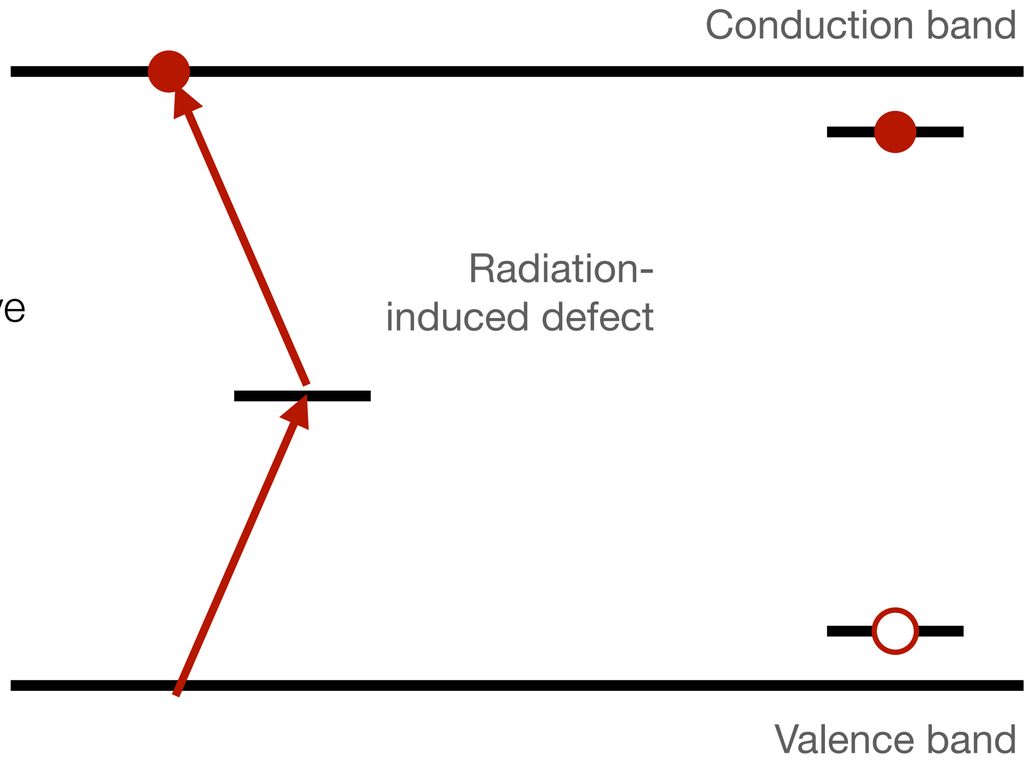

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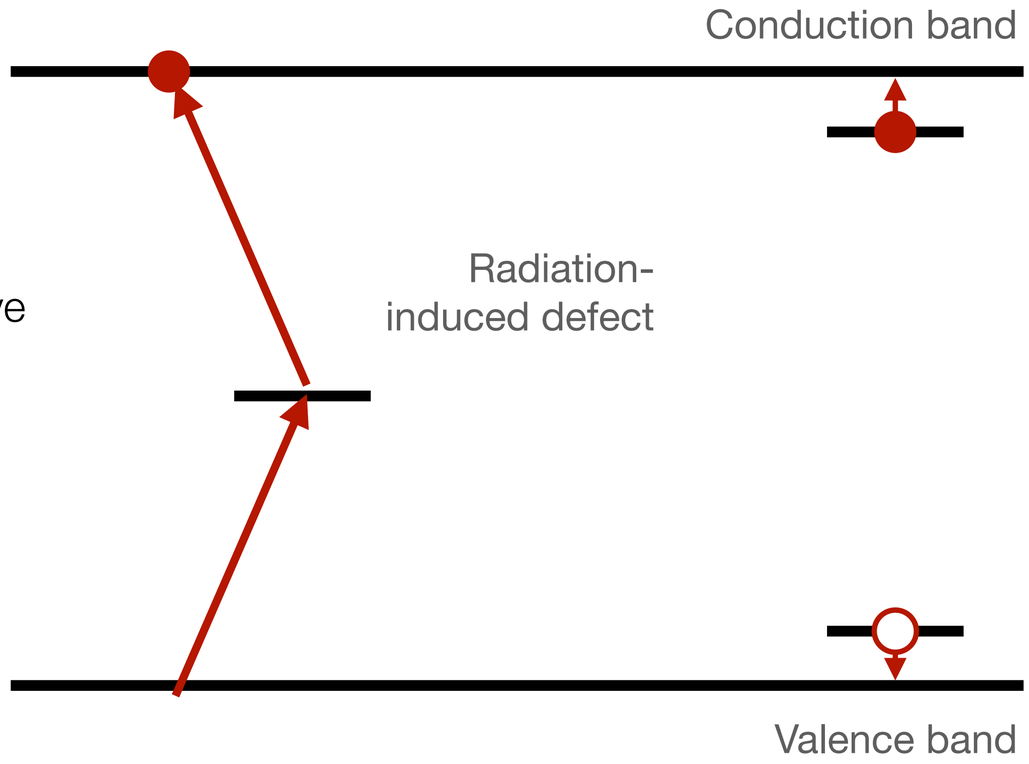

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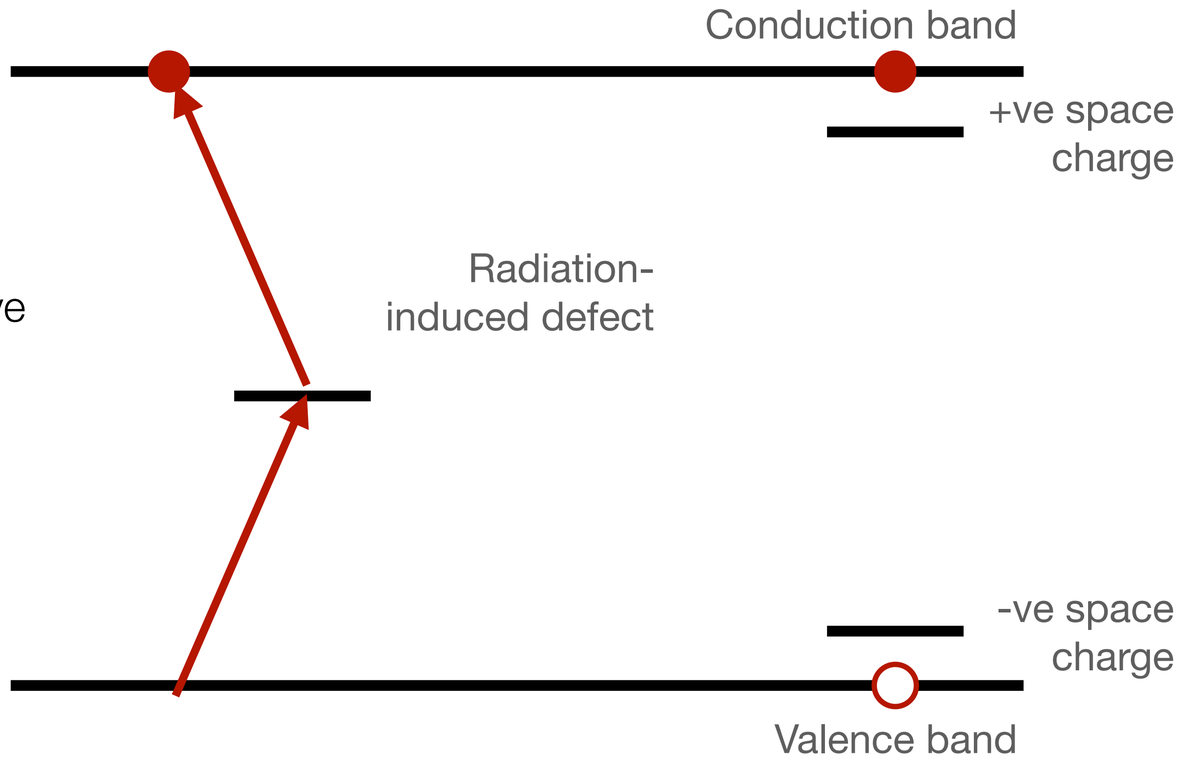

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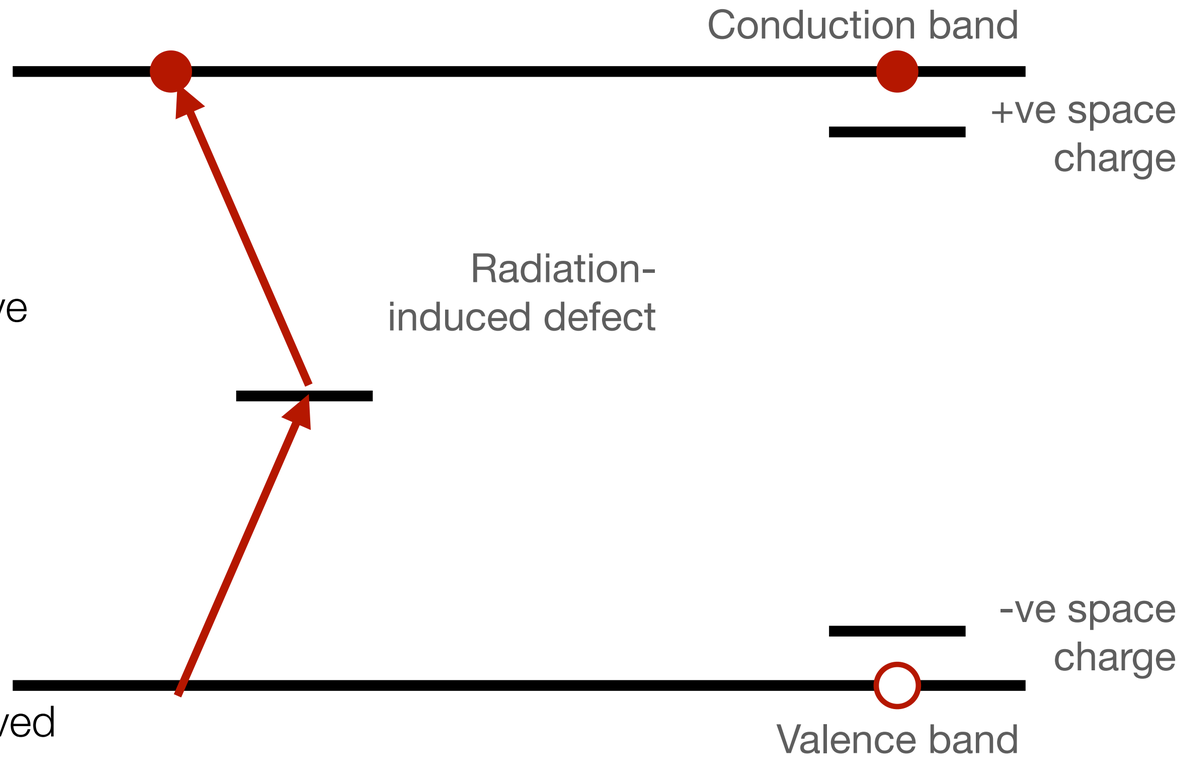
In addition, charge carriers can become trapped in defect centres

- Depending on the emission time can reduce the observed signal
- Use carriers with highest mobility!

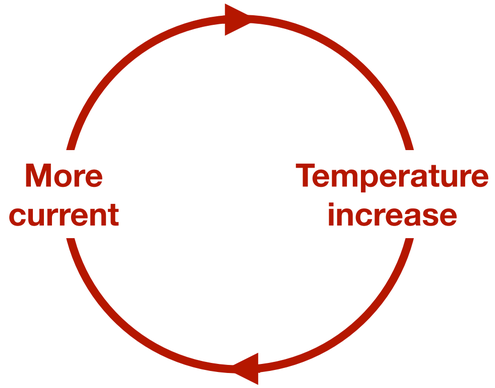


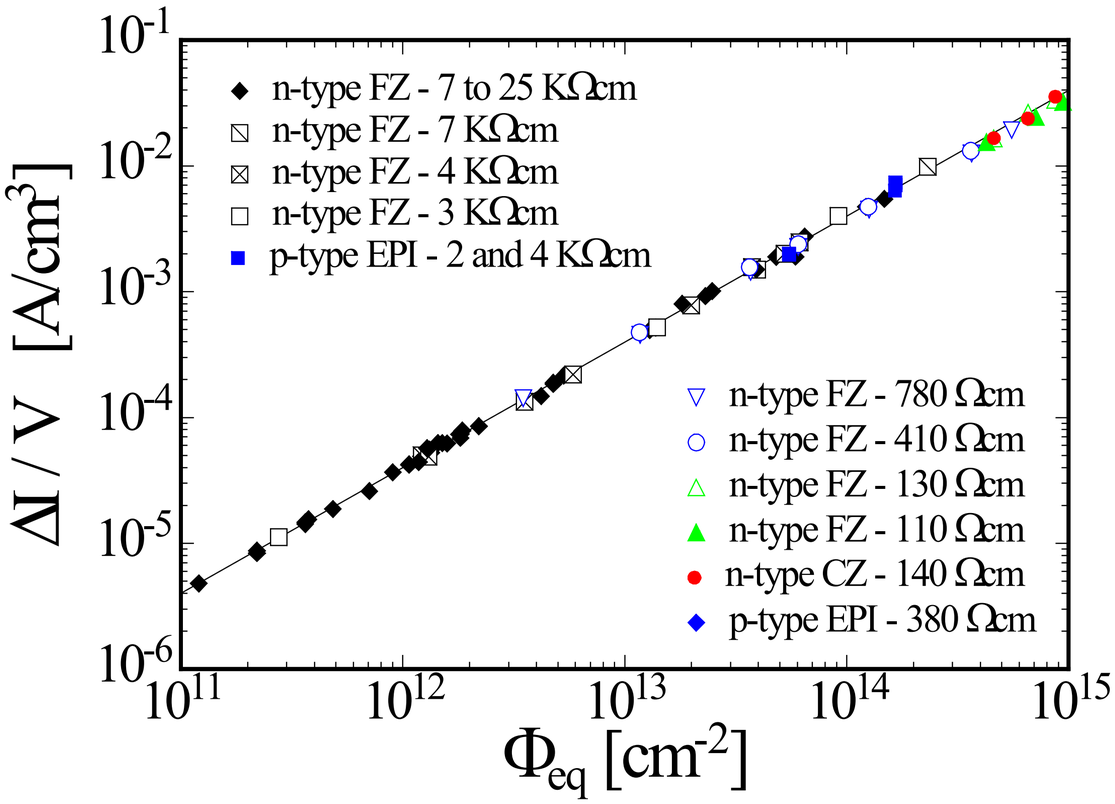
NIEL damage - leakage current

Leakage current increase matches well the NIEL scaling hypothesis over several orders of magnitude

Several significant consequences

- Increased current (noise) in the readout electronics
- Increased power consumption
- Risk of **thermal runaway**





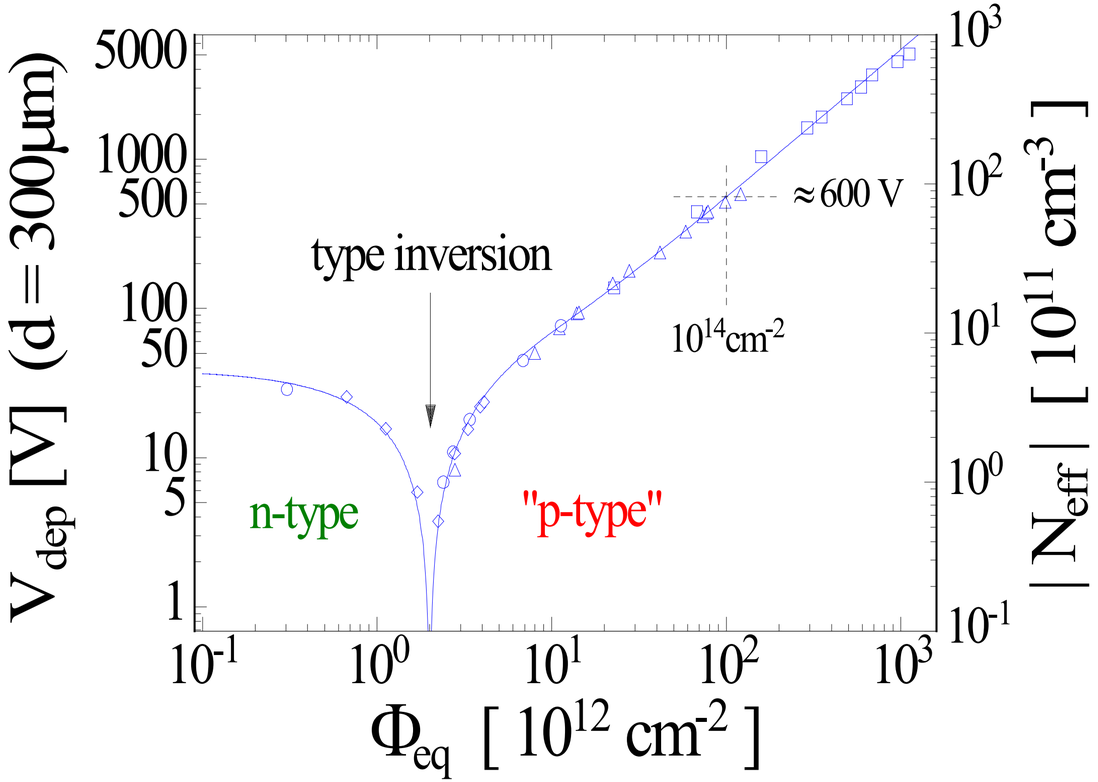
NIEL damage - space charge

The space charge and depletion characteristics are a result of doping - deliberately introduced energy levels that lie in the band gap

- Defects can perform the same role

In silicon, bulk damage produces predominantly *acceptor sites*, effectively turning the material more p-type

- For n-type bulk silicon this means that the device undergoes **type inversion**
- The sensor will get progressively harder to fully deplete after significant doses



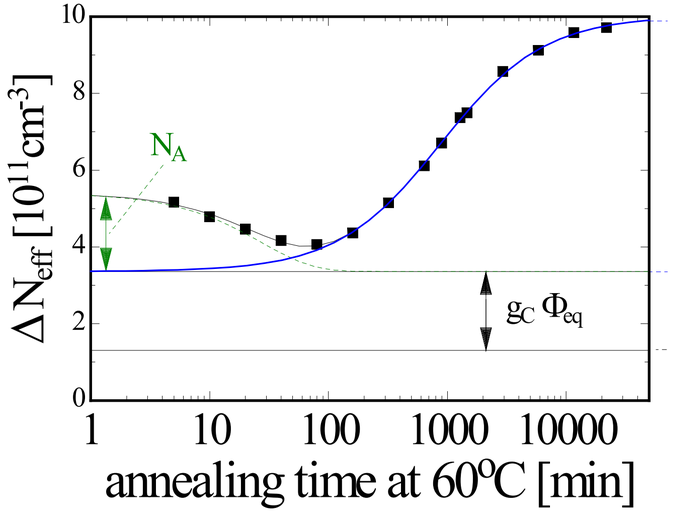
Annealing

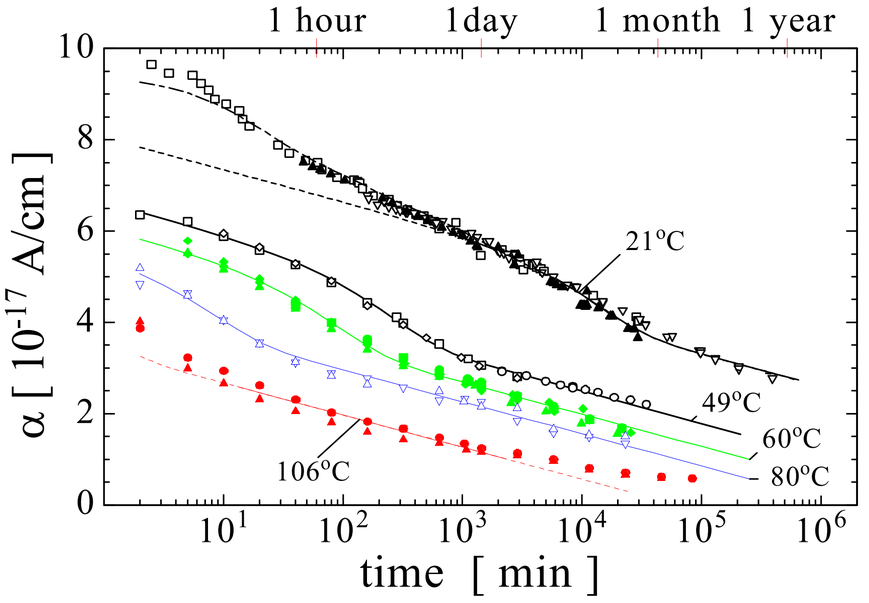
Defects in the lattice are not stationary!

- They can move around, recombine, make friends…

Keeping materials at ambient or raised temperatures can be used to repair some of the damage

- However, not all annealing is beneficial - operate detectors cold and anneal for specific set periods





Total ionising dose - TID

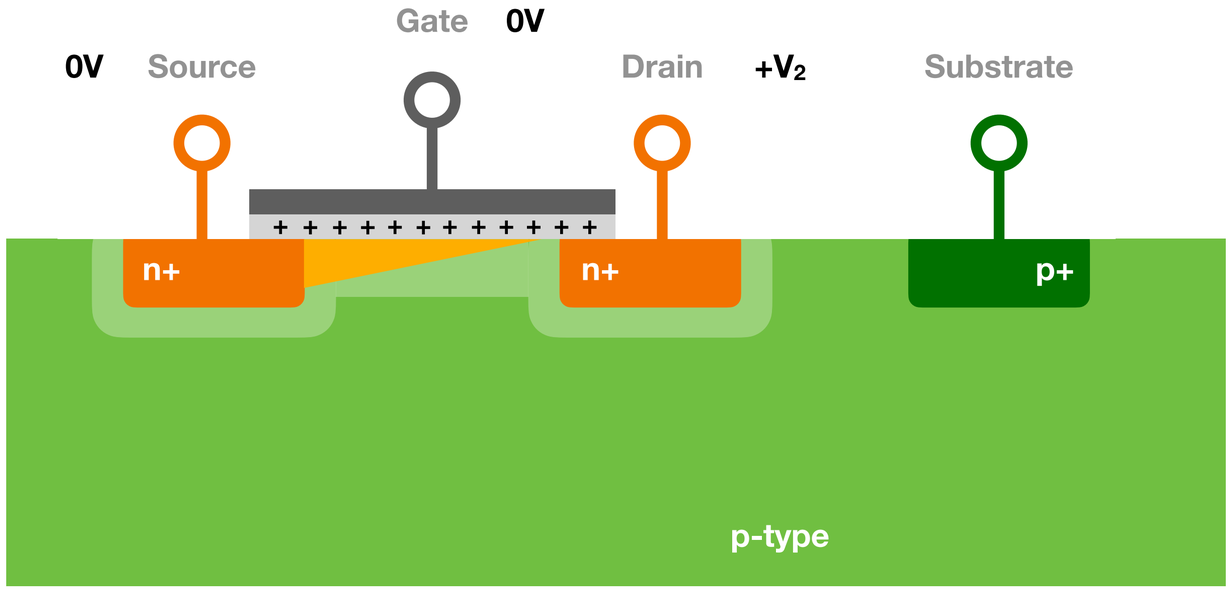
While ionising losses in the bulk constitute signal, and non-ionising losses create crystal defects, a separate issue arises with ionising dose in area susceptible to

- These are typically interfaces and surfaces
- Large effect on electronics - oxide charge build up!
- Total dose measured in *Grays* - joule/kg or *rad* (1 rad = 0.01 Gy)

Oxide charge accumulation leads to several detrimental effects

- Shift in threshold voltage
- Increase in leakage current
- Eventually transistors can’t be switched on/off

TID effects



Single event upsets/effects (SEU / SEE)

It is possible for large charge deposits to directly affect transistors or other electronic blocks

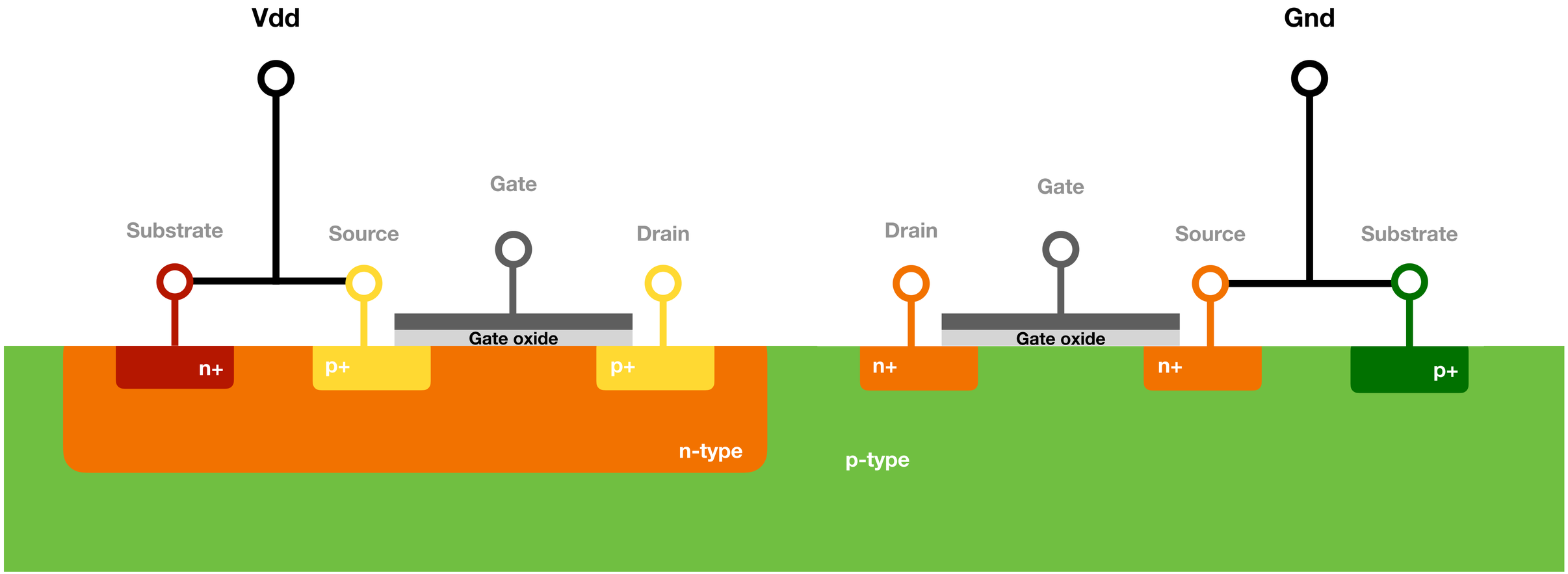
These effects can be as innocent as flipping individual bits in a register

- Triplicate important circuitry and take majority vote
- Live with it, depending on number of bits expected and impact

Much more dangerous cases

- Issues like latch-up can physically destroy the electronics!

Latch-up in CMOS



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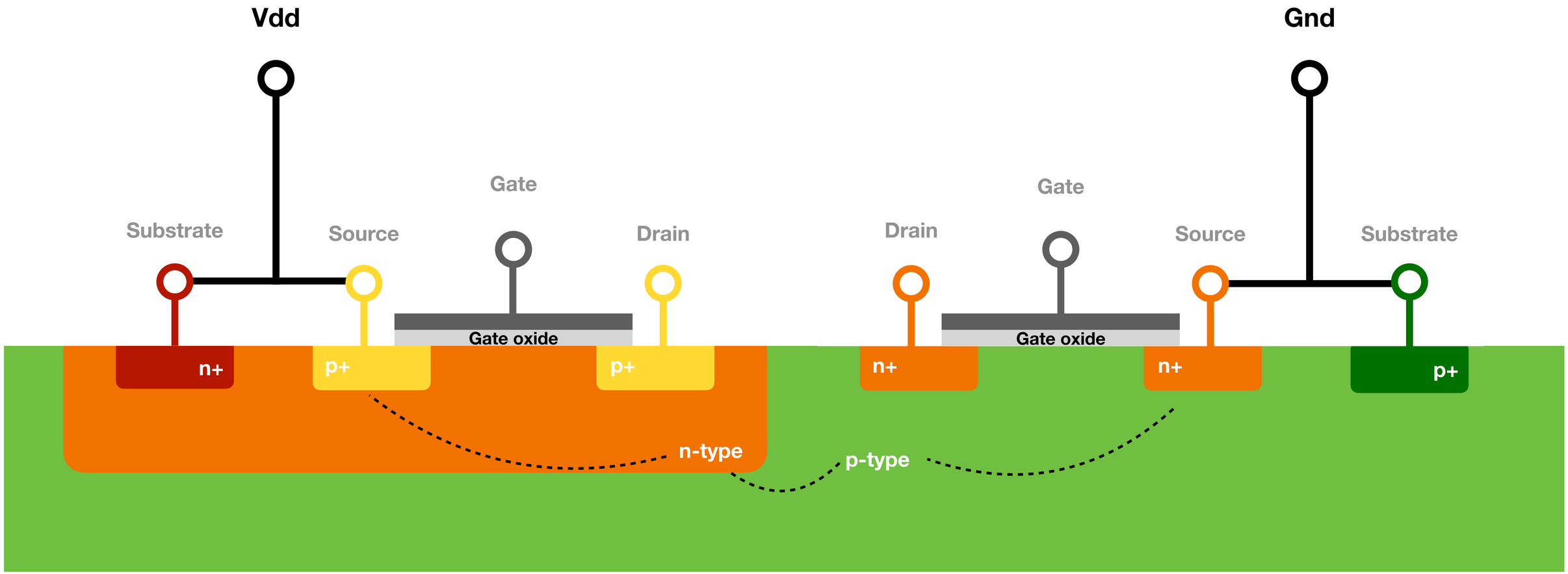
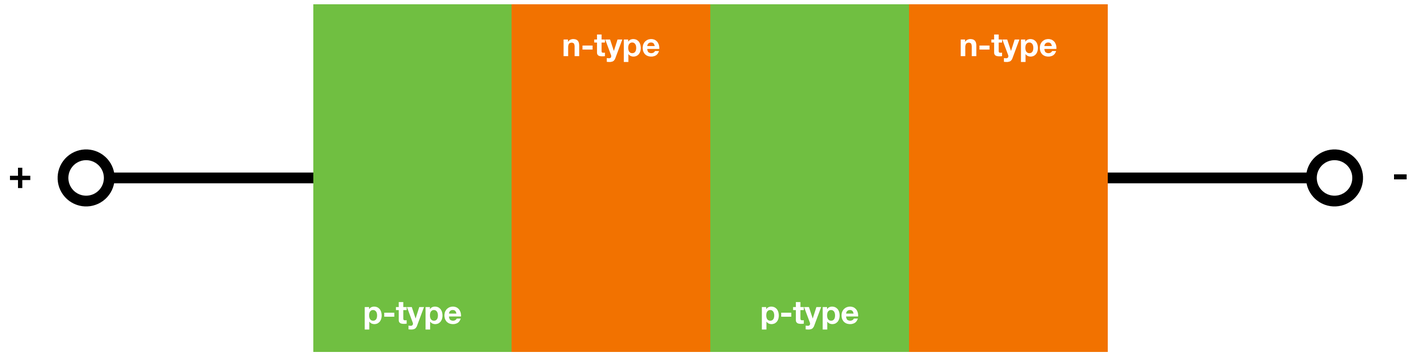


Thyristor

The parasitic PNPN structure in a CMOS block is equivalent to a device called a *thyristor*

- 3 PN junctions in series



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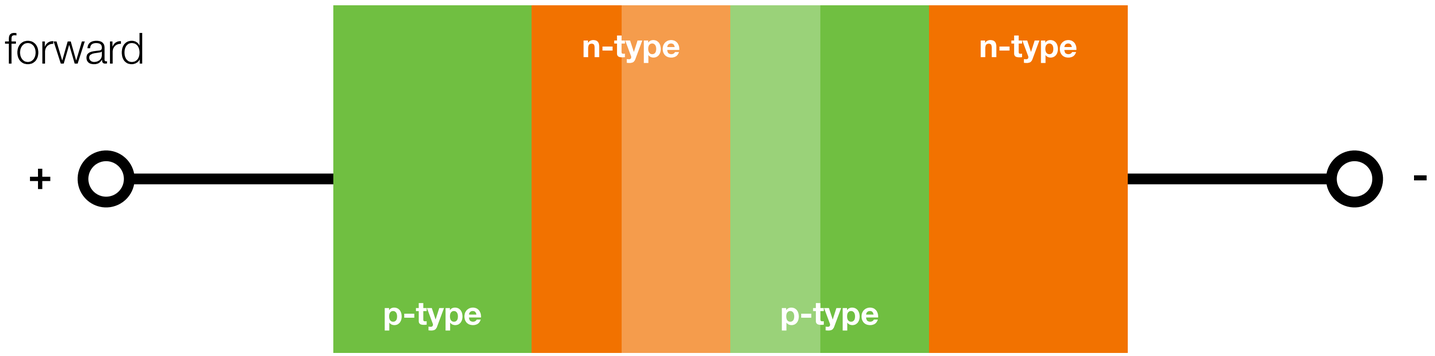
Under these conditions, two of the junctions are forward biased and one is reverse biased

- No current flows while there is a depleted junction in the centre



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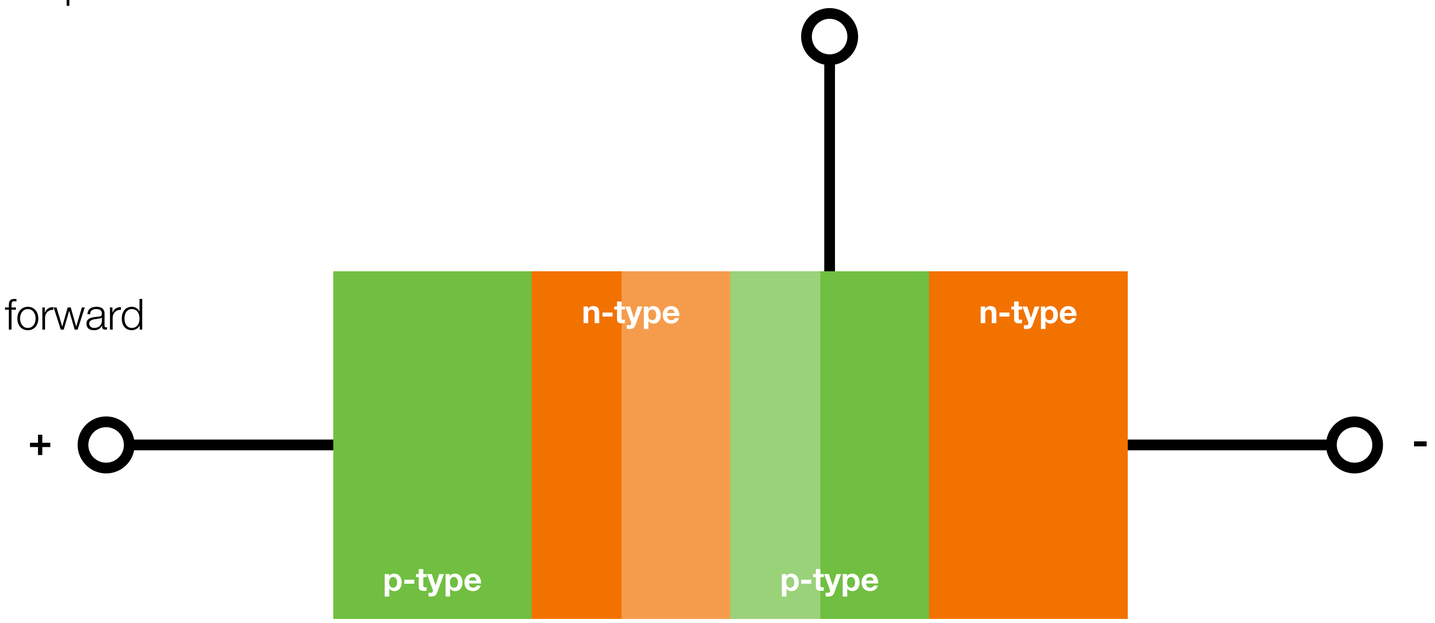
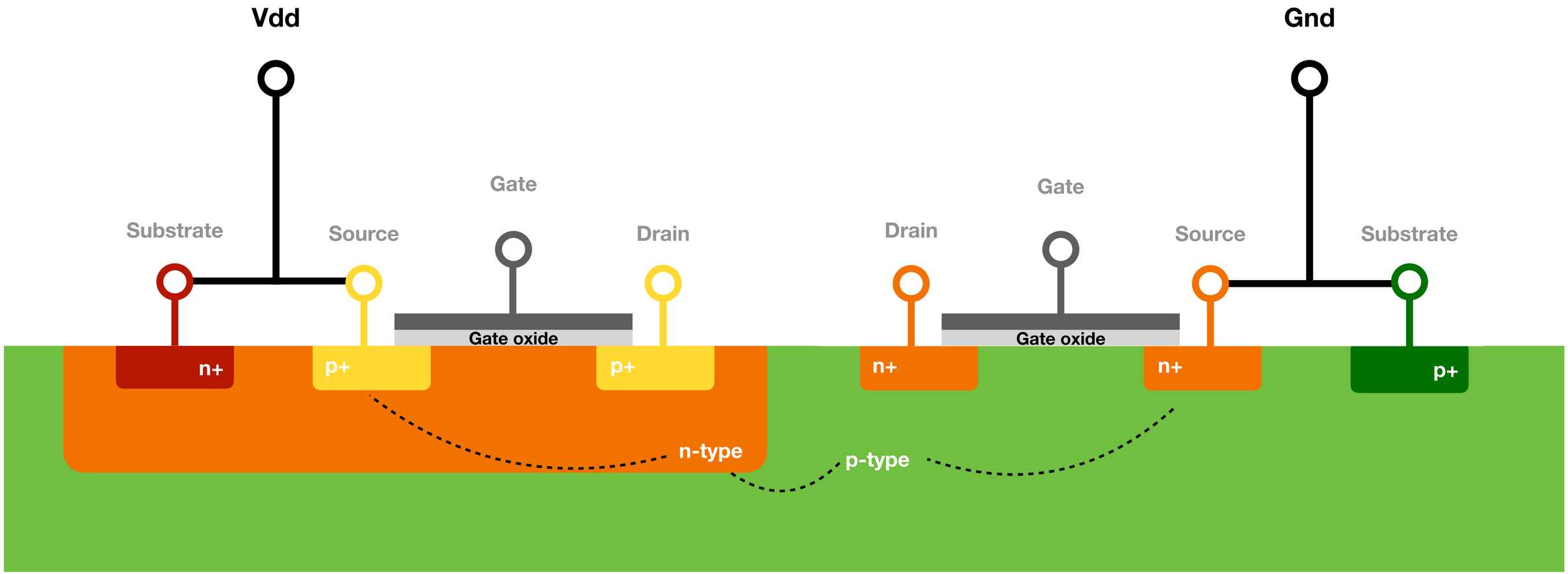


The addition of a gate voltage (or large charge deposit) can reduce the depletion region and lead to a current flow through the whole device

that will not stop while there is current flow

Latch-up in CMOS



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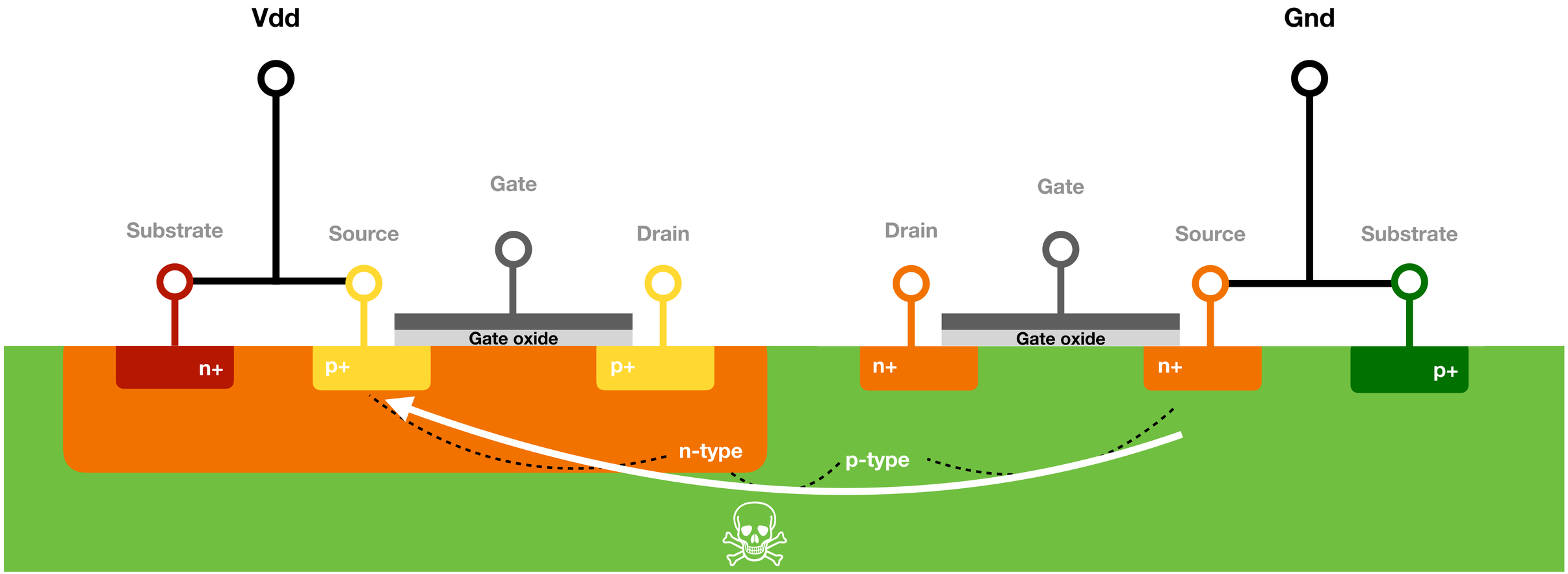


Silicon fabrication

Why silicon?

There is a simple reason as to why silicon is the dominant semiconductor used in electronics

- Silicon oxide

The ability to easily grow a native, stable, insulating oxide is what opens up the whole area to exploitation. Next steps are:

- Production of large, single-crystal wafers with low contaminants
- Doping, both n- and p-type
- Electrical contacts (particularly ohmic)

With many/most other semiconductors these are the challenges that need to be overcome before reliable detectors can be manufactured

Wafer production - the Czochralski method

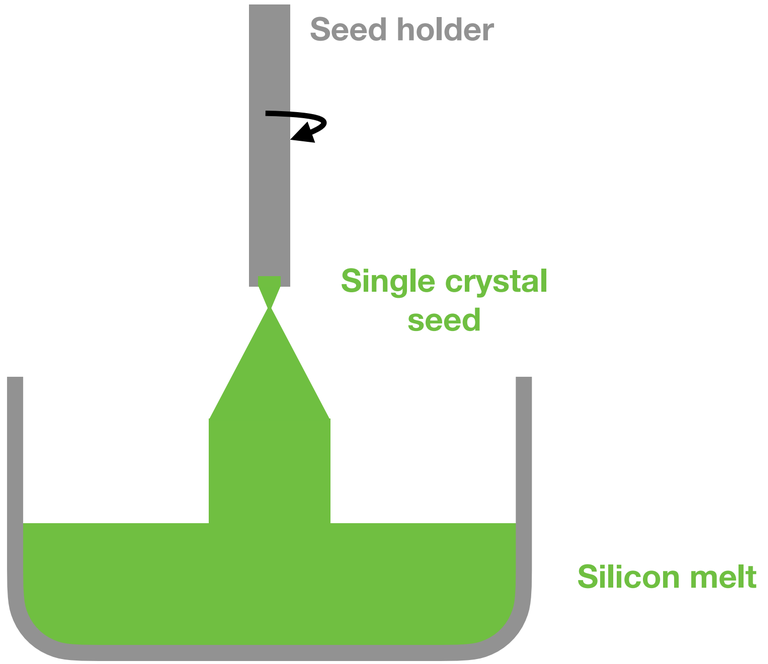
Wafer production still follows the method proposed in 1915 by Czochralski (discovered by accident)

- Very pure silica is placed in a crucible and dissolved to form a melt
- A single crystal seed is dipped into the melt and slowly extracted, while rotating
- The resulting ingot is a single crystal following the same orientation as the seed crystal

This happens at high temperature - 1425°C - and for large diameters

- Commercial processing now done on 12” wafers

Nonetheless, impurities from the crucible (such as O2) can be present at the level of 10^{18} cm^{-3}



Wafer production - Float Zone refinement

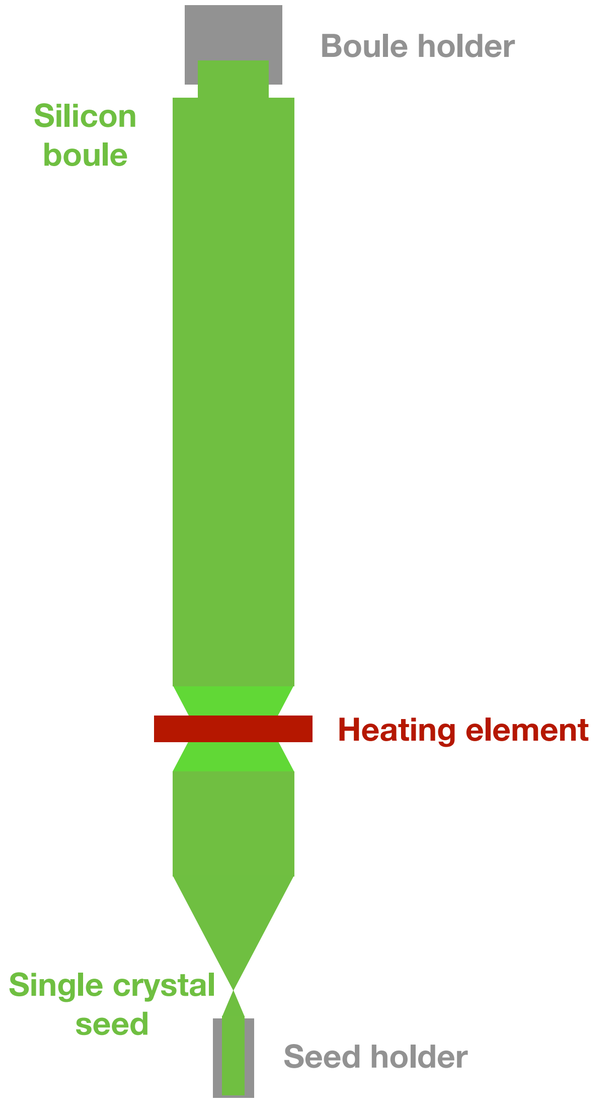
For much purer silicon wafers, float zone refinement can be used

The silicon ingot is effectively re-melted in a narrow band, which is scanned from one end to the other

- Contaminants remain in the melted region rather than crystallising into the now very-pure silicon lattice
- They are filtered all the way to the end of the ingot and then discarded

Produces high-resistivity wafers ideal for detectors

- $n_{eff} << 10^{13}$ cm^{-3}



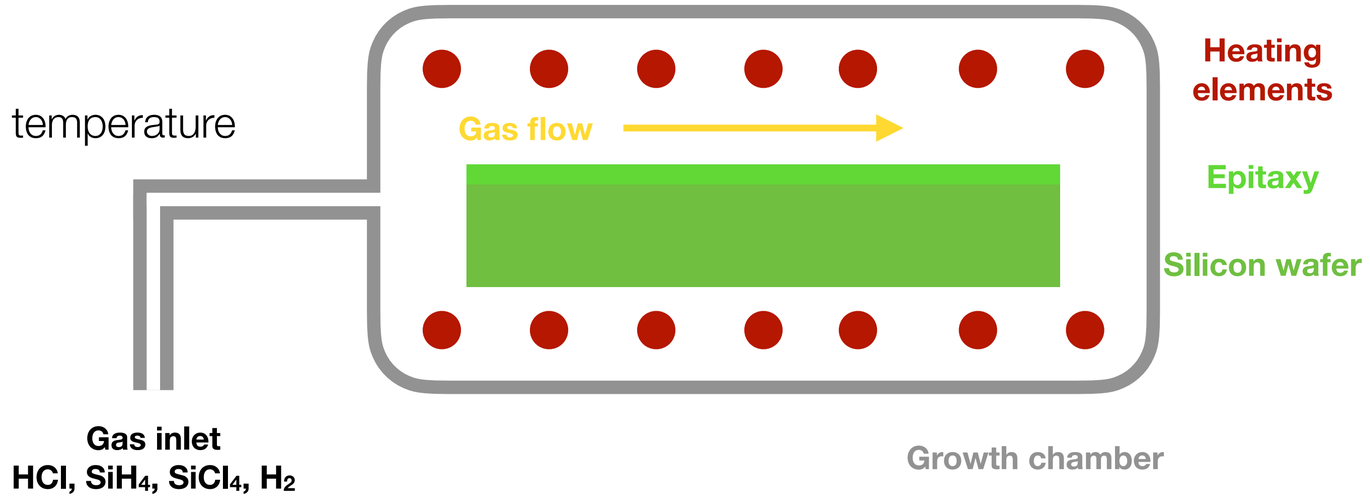
Epitaxial growth

Another method for obtaining a pure silicon crystal with high resistivity is to grow a dedicated pure layer on top of an existing silicon wafer

- This layer is referred to as an *epitaxial layer*

The wafers are placed in a chamber heated to high temperature (800 - 1150°C)

- Wafer surface must be atomically clean
- Gases containing silicon introduced into the chamber
- Growth of 10s of nm per minute

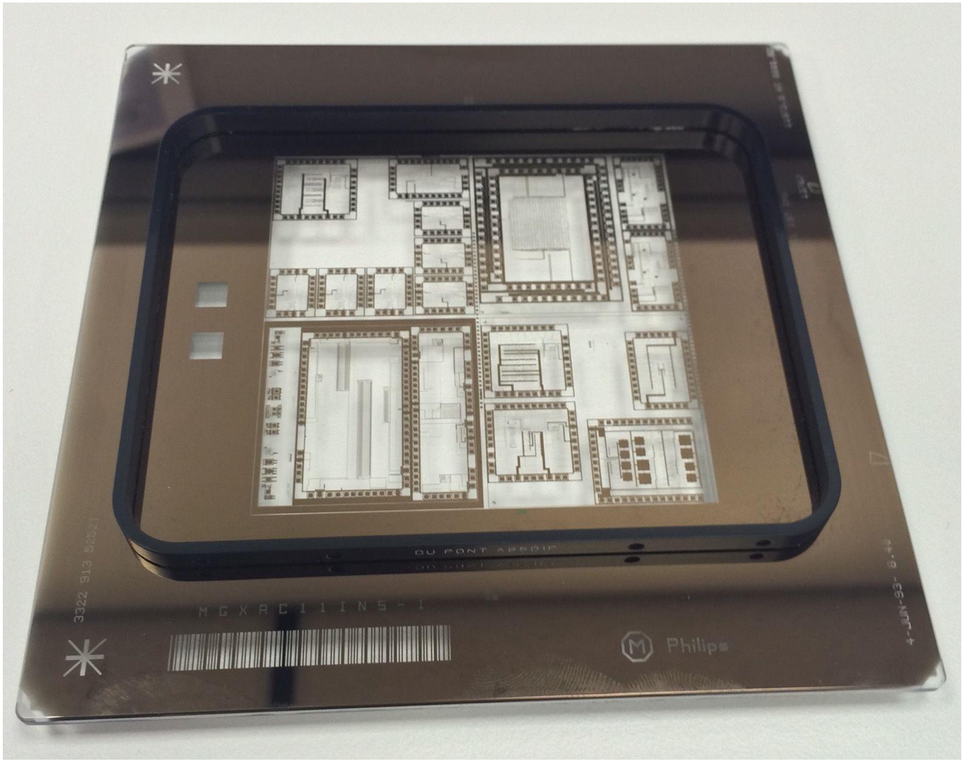


Photolithography

We want to be able to *pattern* our devices => deposit patterned masks

One of the most straightforward ways to do this is via photolithography

- A coating is applied to the full silicon wafer - called a *resist*
- A mask is produced containing the desired pattern
- The pattern is transferred to the resist either by placing the mask in contact and illuminating it, or by projecting light through the mask via a lens
- The resist will either harden or break down, depending on the material chosen

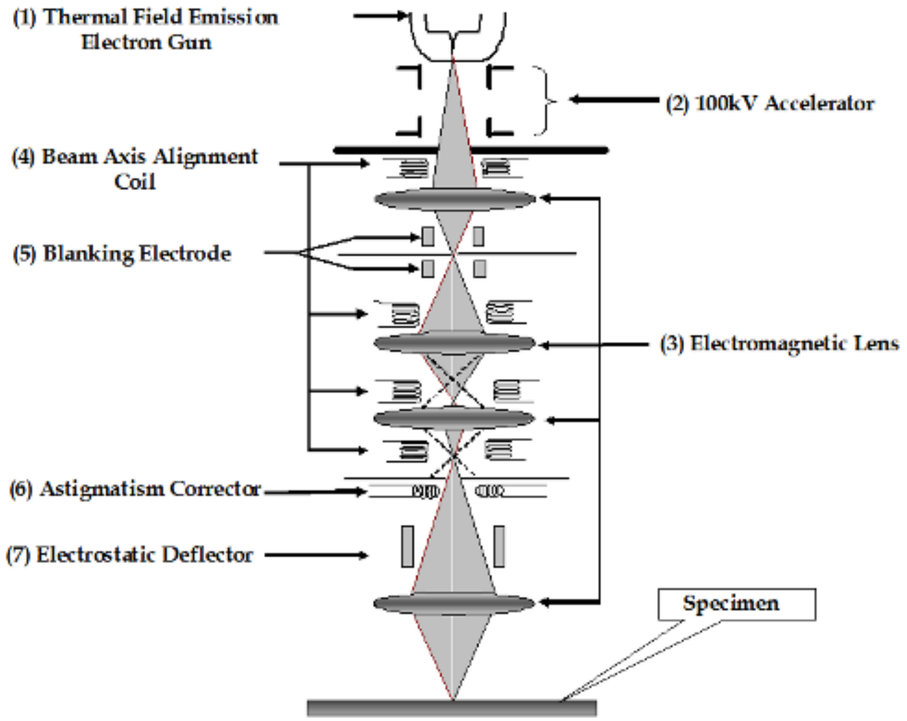


E-beam lithography

Photolithography depends on light and so starts to limit the feature size around the wavelengths used

- For much finer objects use a focussed beam of electrons, scanned across the surface in the desired pattern
- No mask, just direct scanning

Resolutions can be much much better - down to below 10 nm - but at the cost of limited throughput



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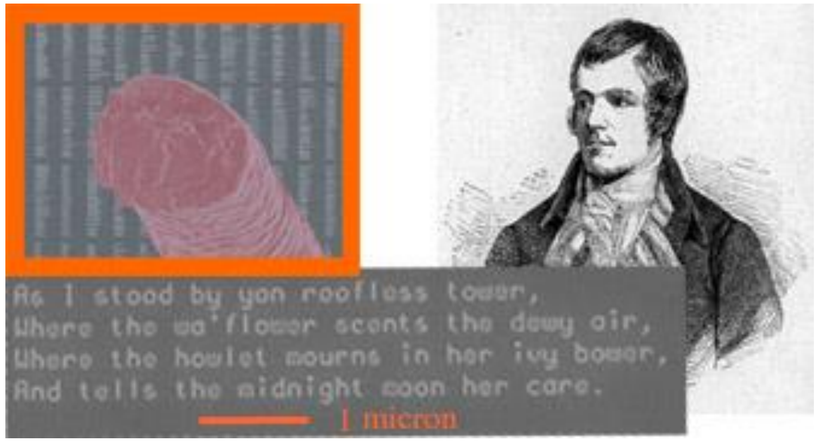
- For much finer objects use a focussed beam of electrons, scanned across the surface in the desired pattern
- No mask, just direct scanning

Resolutions can be much much better - down to below 10 nm - but at the cost of limited throughput



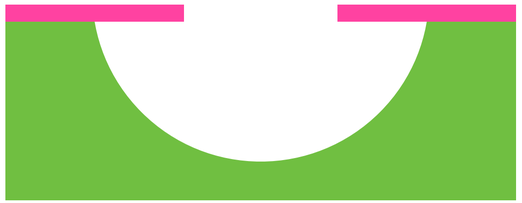
A book of the Complete Works of Robert Burns, Scotland's National Bard, has approximately 480 pages. To publicise the capability of the new Vistec VB6 UHR EWF electron beam lithography tool at the JWNC, we used it to write the Complete Works of Robert Burns on a small piece of silicon. Ten copies would fit on the head of a pin and this is likely to be the world's smallest copy of the works of Burns. The image shows pages of text alongside a human hair plus detailed text from the song "As I stood by yon roofless tower". Each character is approximately 150 nm

Etching

There are two kinds of etching, both with their own advantages/ disadvantages: **wet** and **dry**

Wet etching is relatively straightforward

- Immerse your wafer in something hideously corrosive/toxic/ carcinogenic until the bits that you don't want have been removed…
- Etching will be isotropic
- Not all materials have suitable chemistry for wet etching (NB. HF used for SiO_2)



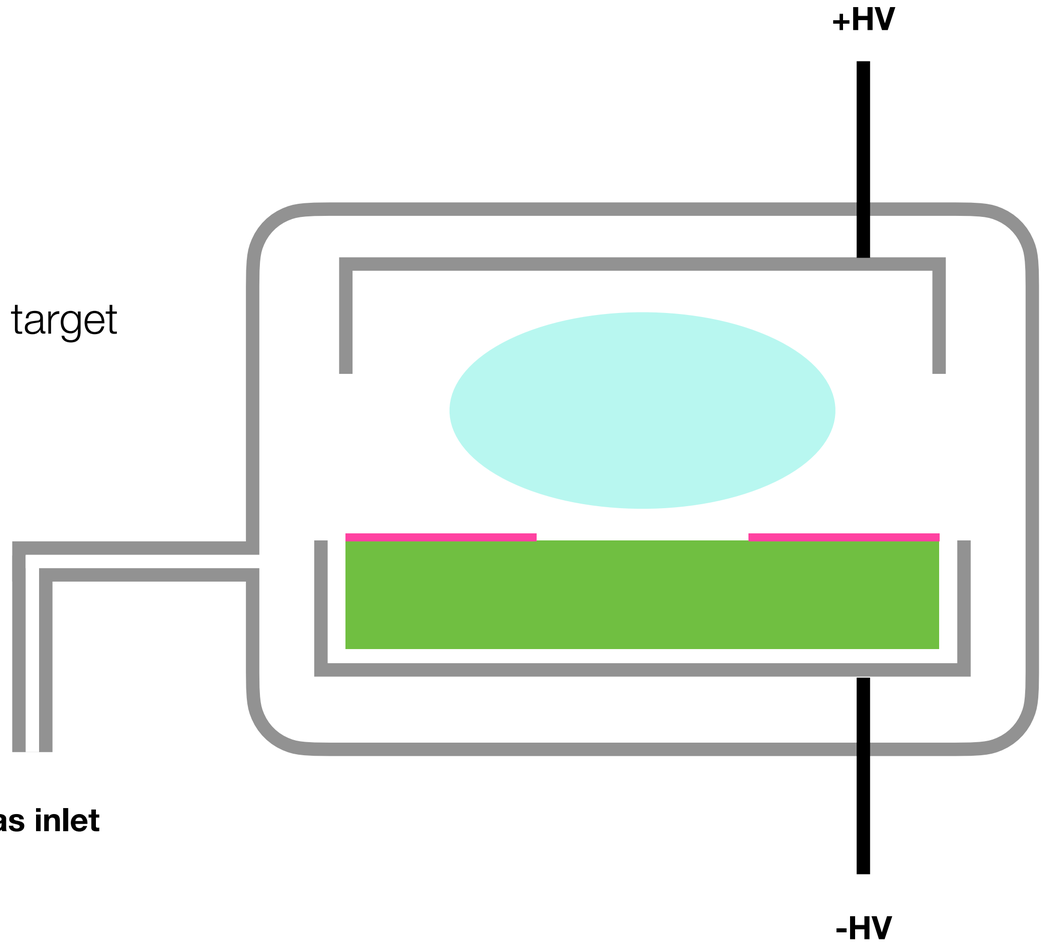
Wet etching
Isotropic

Dry etching
Anisotropic

Etching

Dry etching uses pressurised gas and a high voltage to generate a plasma

- Once ions are created they accelerate towards the target wafer
- A combination of reactant species and mechanical impacts etches anisotropically
- Reactive Ion Etching (RIE) a common technique
- Most materials can be dry etched
- Useful to achieve high aspect ratios



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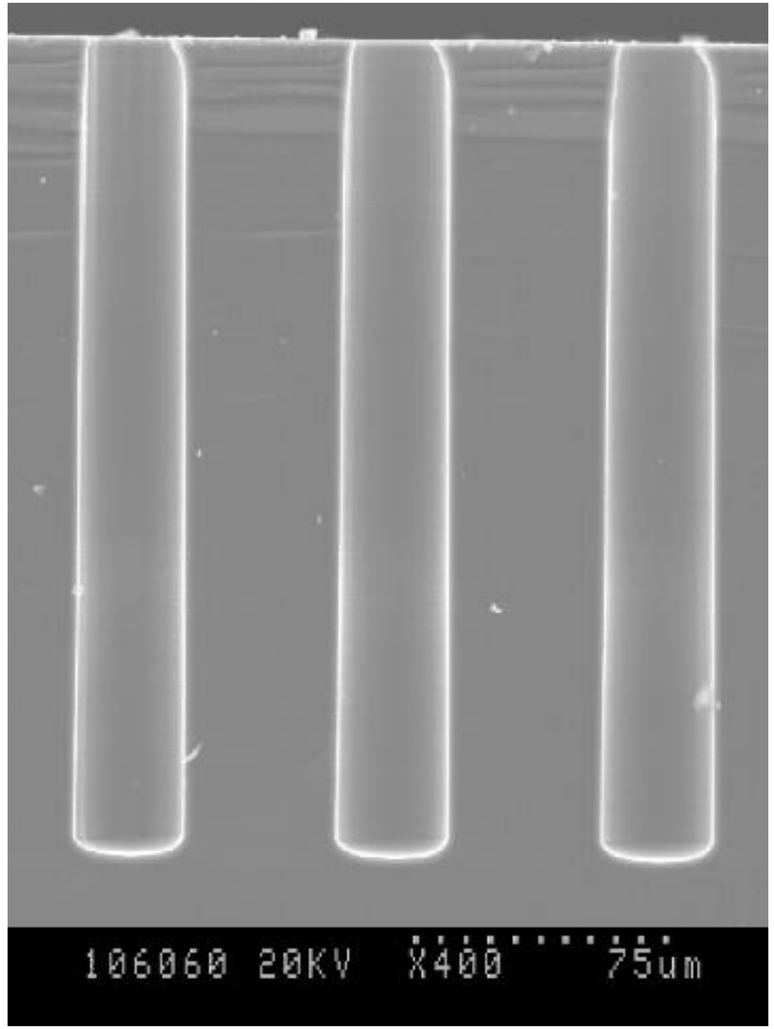
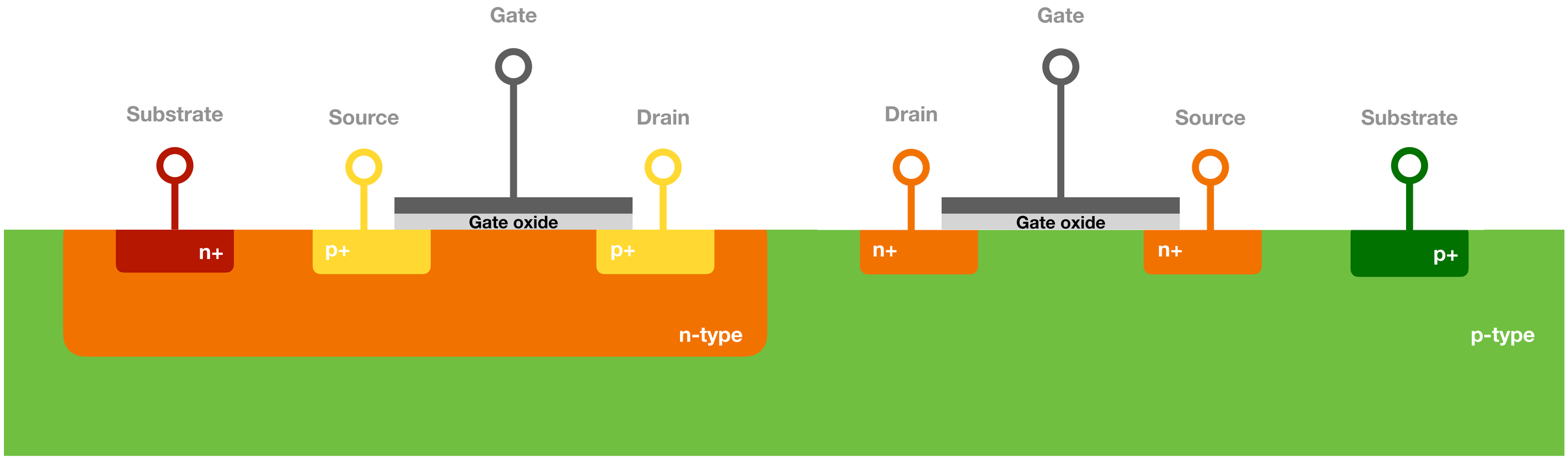


Oxidation

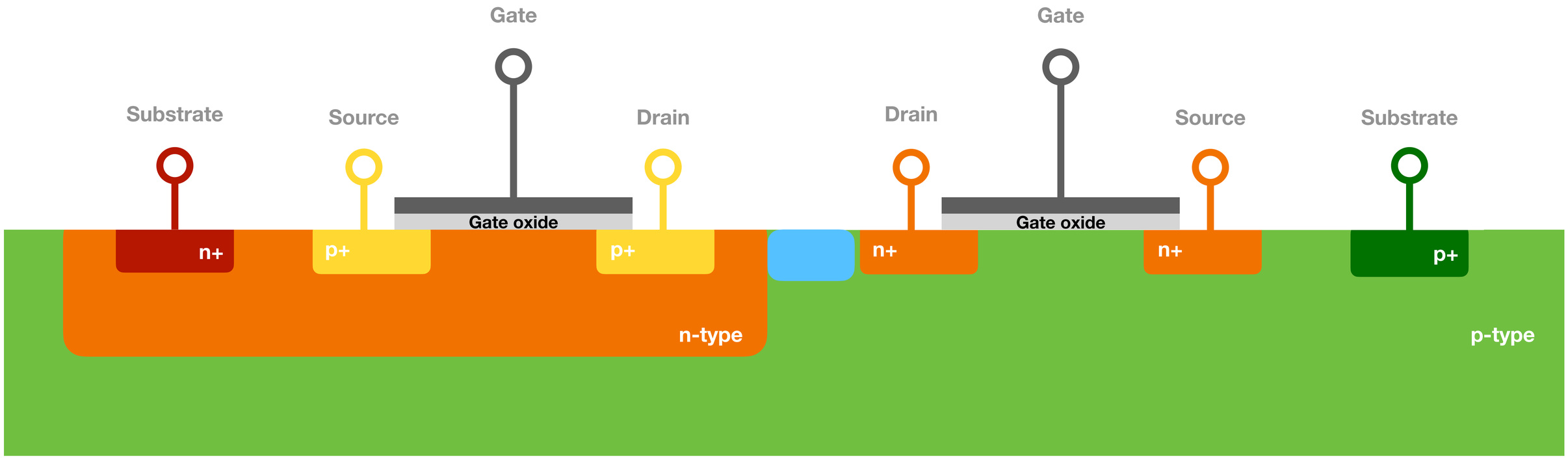
Oxidation of the silicon performs multiple roles

- A stable protection layer over the silicon
- An insulating layer for building vertical structures
- *An isolation layer between neighbouring transistors*

Oxidation for isolation



Oxidation for isolation



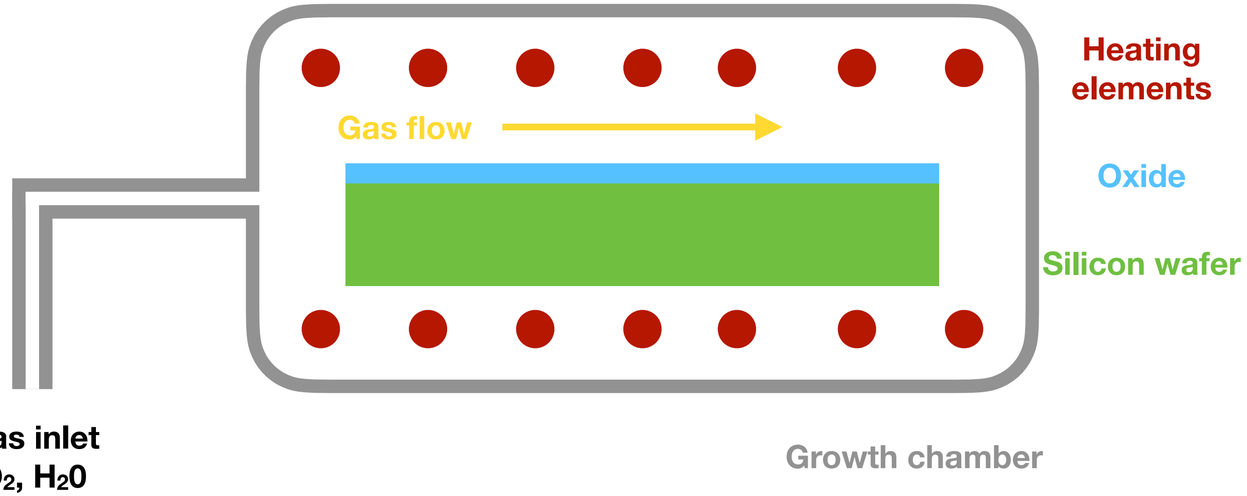
Oxidation - thermal growth

Heating wafers in a chamber and introducing gases is a versatile technique…

For thermal growth of oxide layers we can do this in two ways:

- **Dry oxidation.** Better quality oxide produced, but slow growth rate ~ 10 nm/hour
- **Wet oxidation.** Lower quality oxide, but 10x growth rate

However…

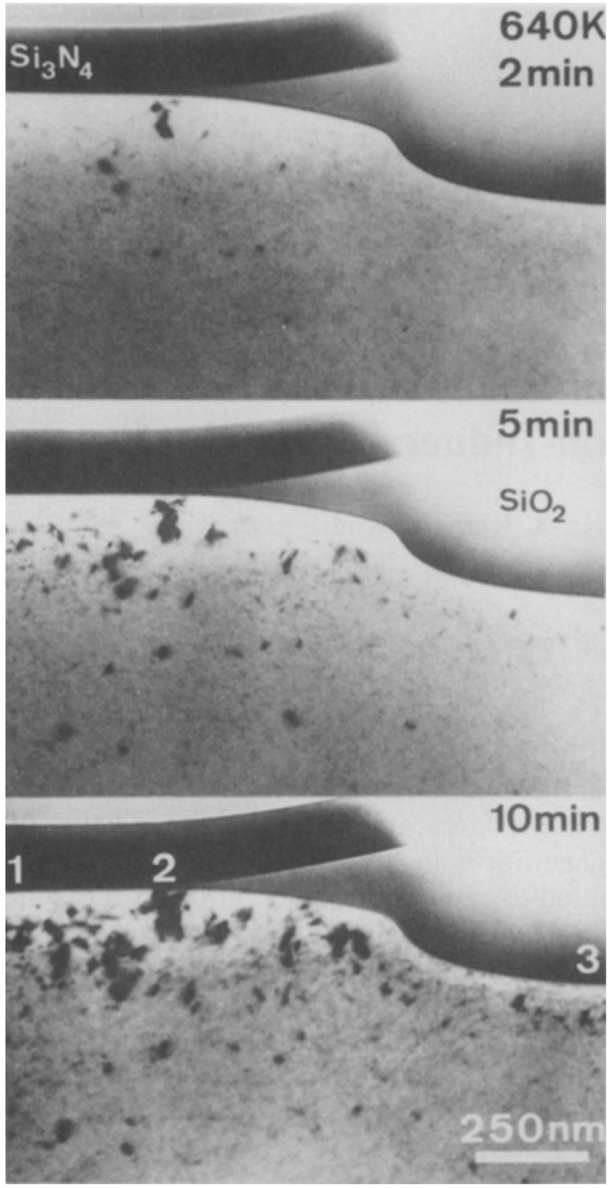


Oxidation - thermal growth

When trying to isolate wells from each other, these shallow trench isolations require filling a large volume with oxide

- The oxide will push up other layers that are on top, and start to wedge deeper along the silicon surface
- So called “bird’s beak”

Things aren’t as simple as we would like them to be…



Oxidation - shallow trench isolation (STI)

We start with a silicon wafer, with oxide and nitride layers grown on top

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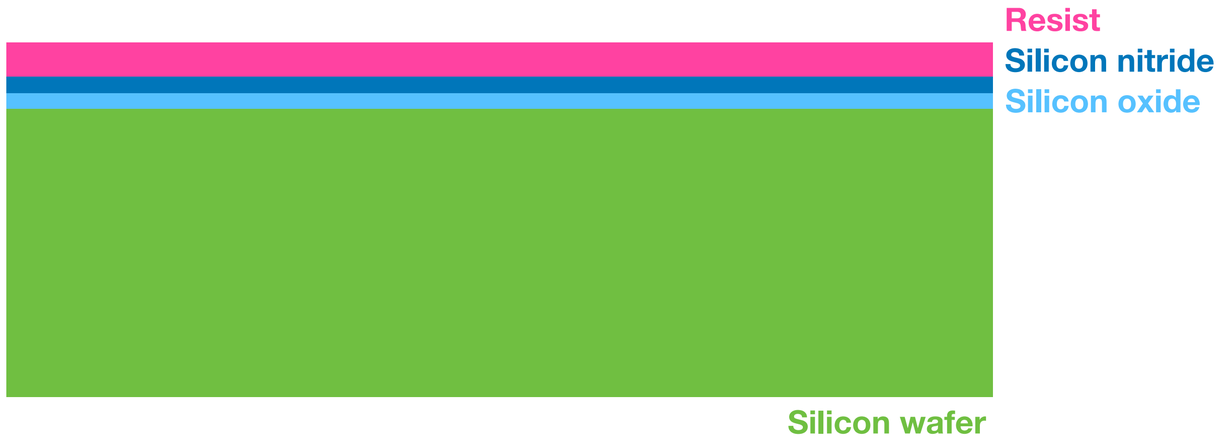

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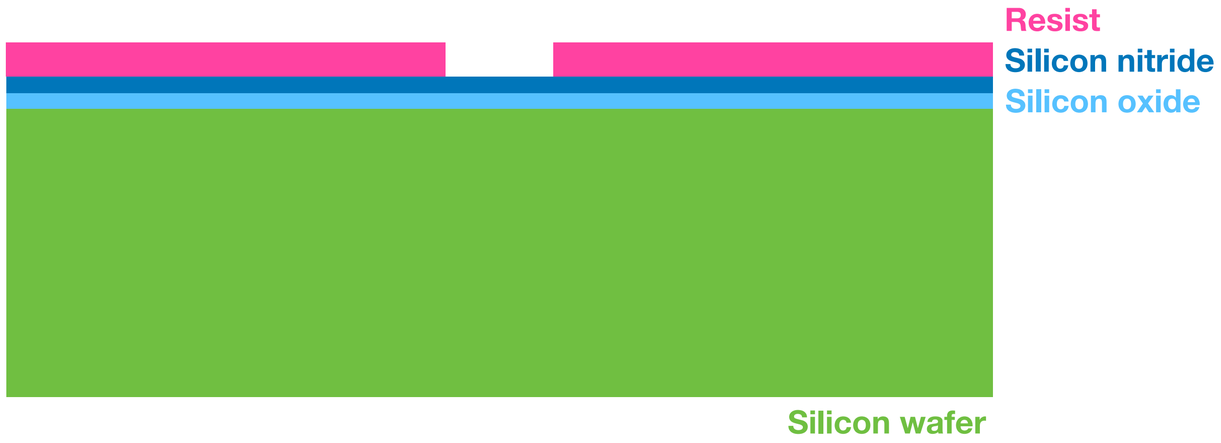

Oxidation - shallow trench isolation (STI)

We start with a silicon wafer, with oxide and nitride layers grown on top

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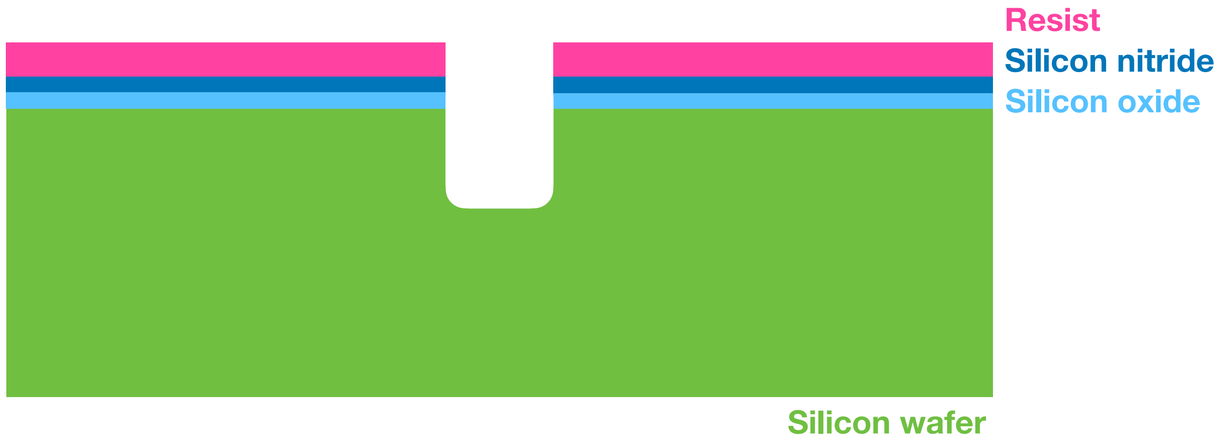

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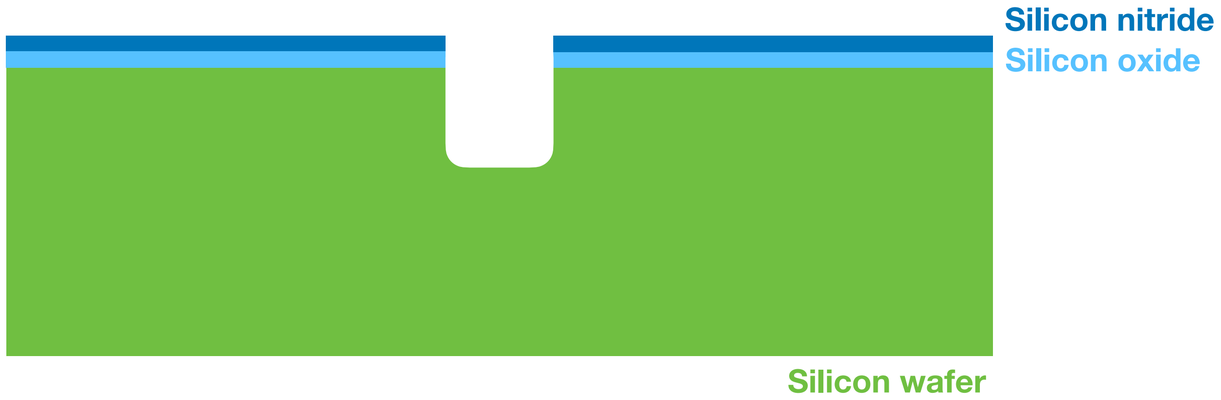
- The resist is removed



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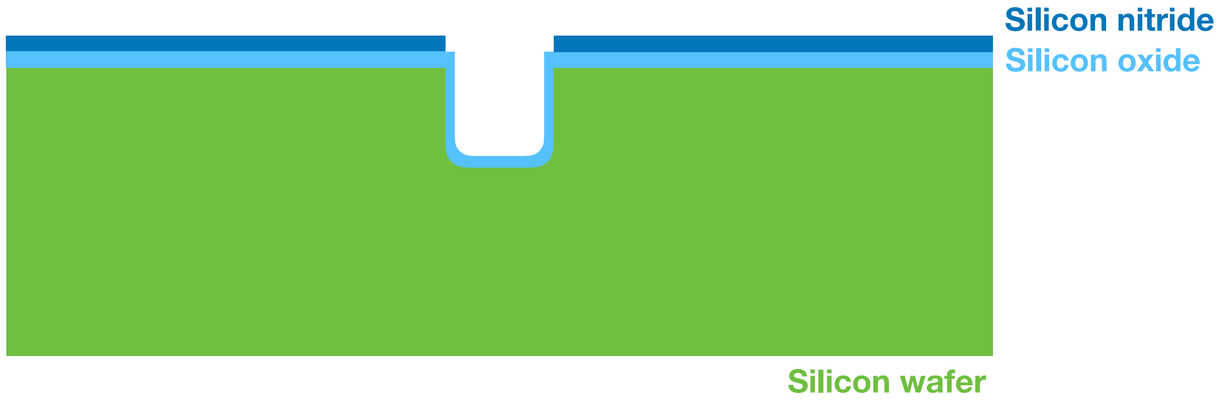

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- A resist is grown to provide the etching pattern
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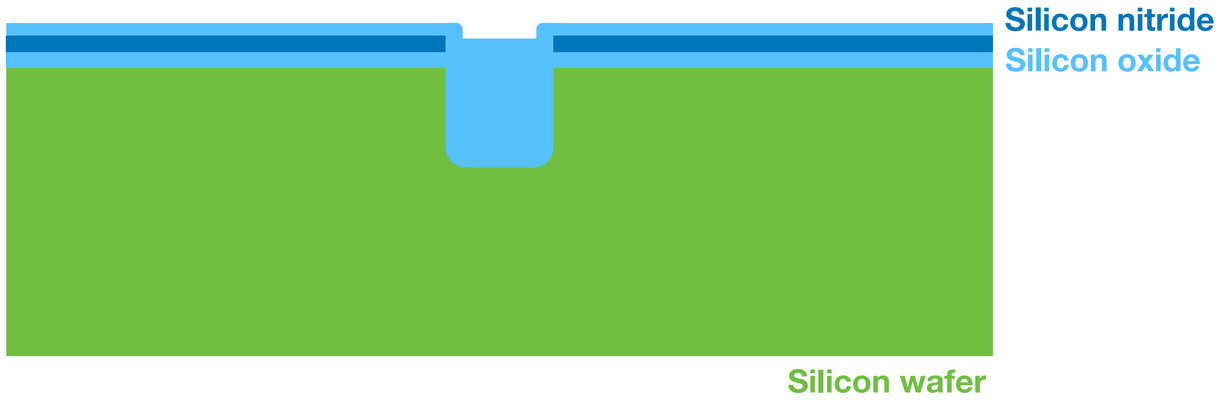
- A **thermal oxide** is grown
- **CVD** is used to deposit silicon oxide everywhere



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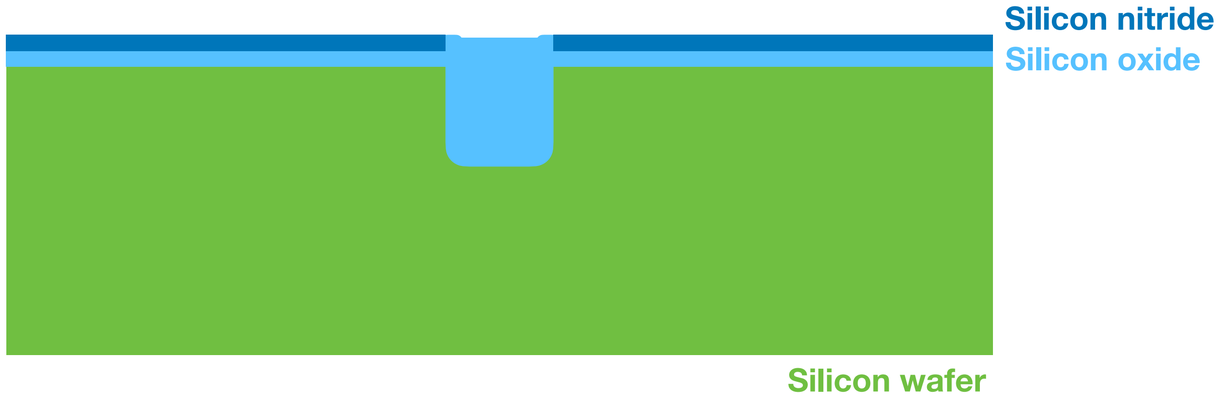

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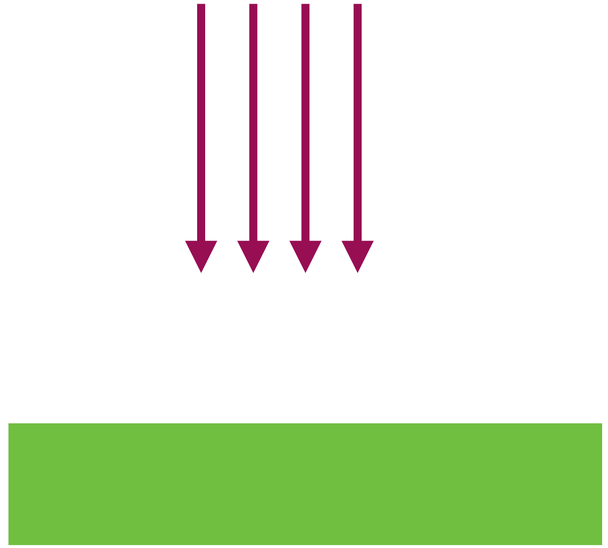
- The oxide is polished down
- The nitride is removed

Doping

There are a few methods to dope silicon wafers, from those during growth to gas diffusion in a chamber at high temperature

One particularly useful method is *ion implantation*

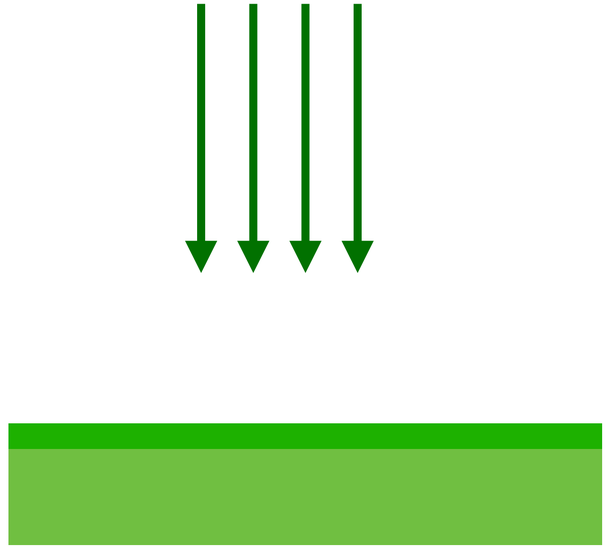
- A small particle accelerator is used to create and accelerate dopant ion species to max ~few MeV
- Spectrometer gives high purity beam
- Ions directed onto wafer surface BUT penetration affected by lattice structure



Doping - ion implantation

To avoid this, we can first *implant silicon*

- This creates an amorphous silicon region at the surface



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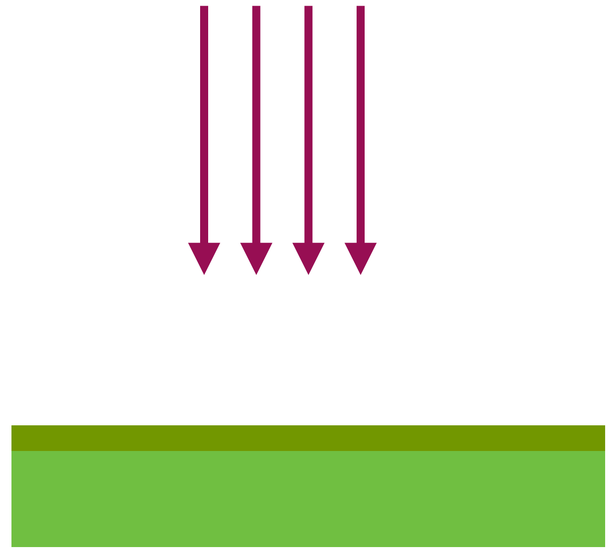
- We can then implant the ions that we want, without worrying about the crystal orientation



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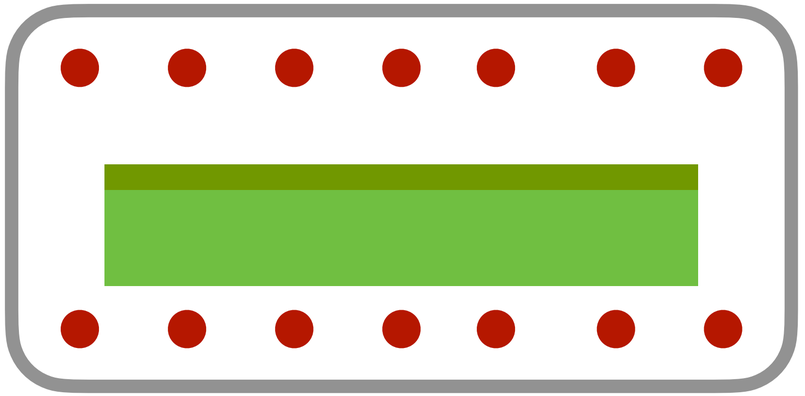

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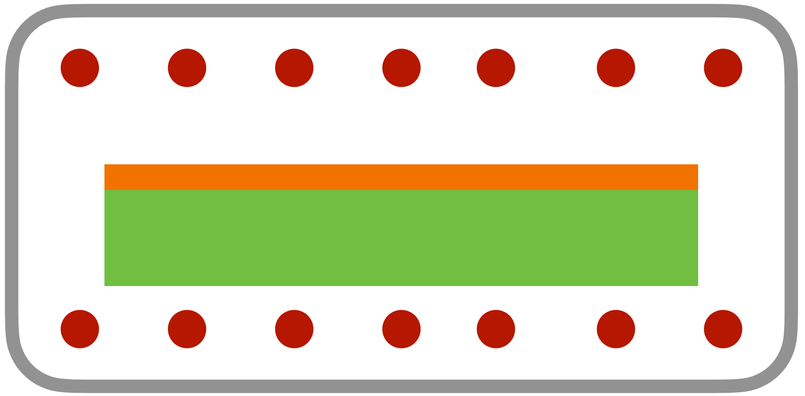
- High temperature also leads to dopant diffusion => limit time to < 20 seconds of 1000°C

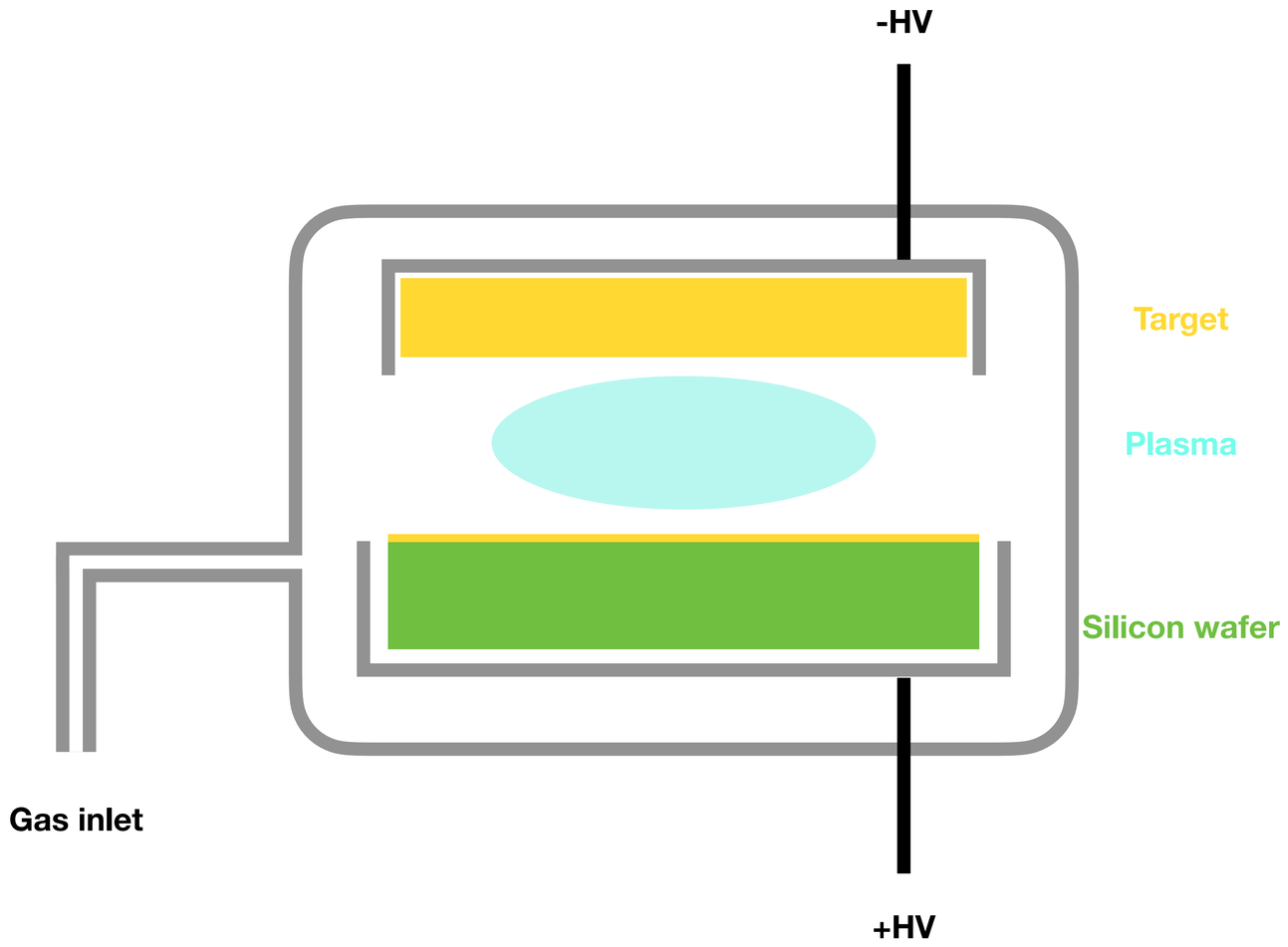


Metallisation

Metal layers can be deposited via CVD, as for other steps, but another common technique is *sputtering*

Sputtering works rather like the dry etch process, but in reverse

- Gas atoms are ionised into a plasma, before being accelerated towards the target metal
- Chunks of the metal are ejected from the impact, spraying all over the chamber



Detector fabrication steps

Just to demonstrate some of the steps involved in making a simple diode:

- Start with a silicon wafer

Detector fabrication steps

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Detector fabrication steps

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- Start with a silicon wafer
- Grow an oxide
- Spin on a resist

Detector fabrication steps

Just to demonstrate some of the steps involved in making a simple diode:

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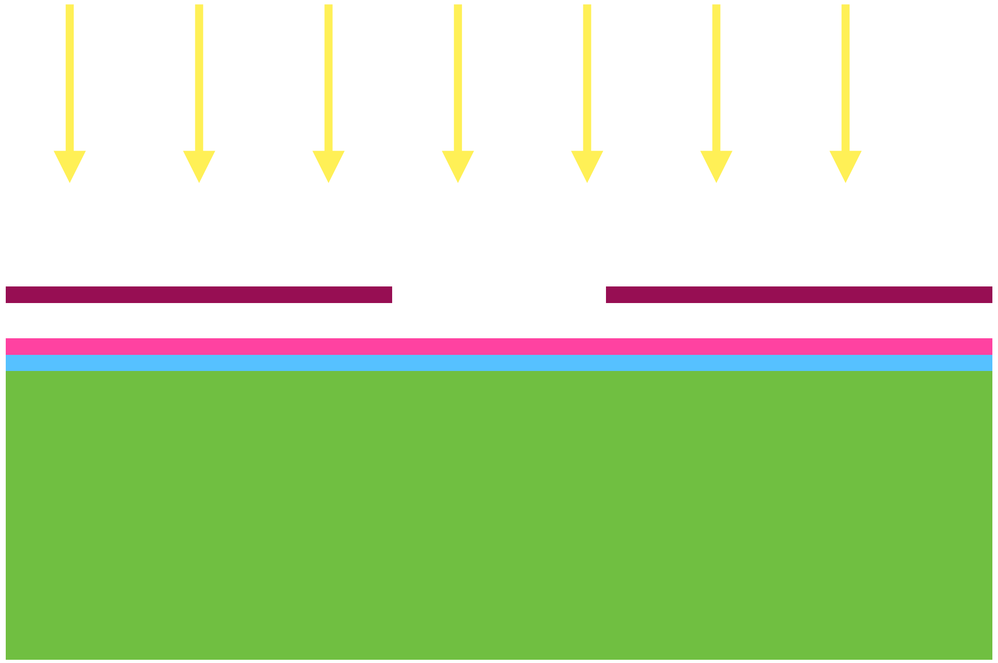
- Grow an oxide
- Spin on a resist
- Align the lithography mask



Detector fabrication steps

Just to demonstrate some of the steps involved in making a simple diode:

- Start with a silicon wafer
- Grow an oxide
- Spin on a resist
- Align the lithography mask
- Develop the resist

Detector fabrication steps

Just to demonstrate some of the steps involved in making a simple diode:

- Start with a silicon wafer
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- Spin on a resist
- Align the lithography mask
- Develop the resist
- Etch the oxide

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Just to demonstrate some of the steps involved in making a simple diode:

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- Develop the resist
- Etch the oxide
- Remove the resist

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- Remove the resist
- Dope the silicon

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- Spin on a resist
- Align the lithography mask
- Develop the resist
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- Remove the resist
- Dope the silicon
- Spin a new resist

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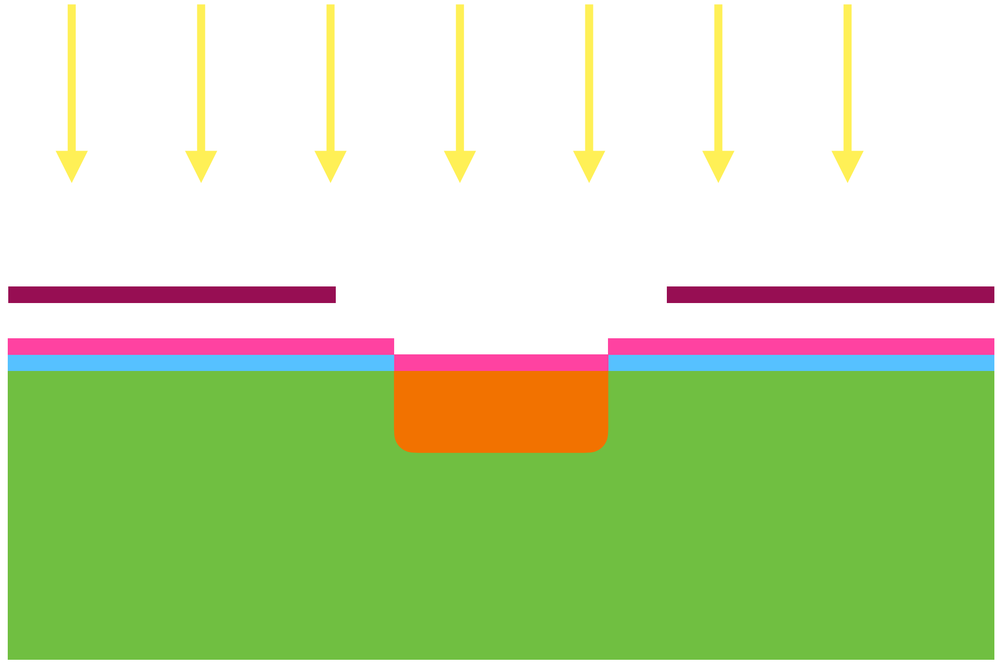
- Dope the silicon
- Spin a new resist
- Align a new mask



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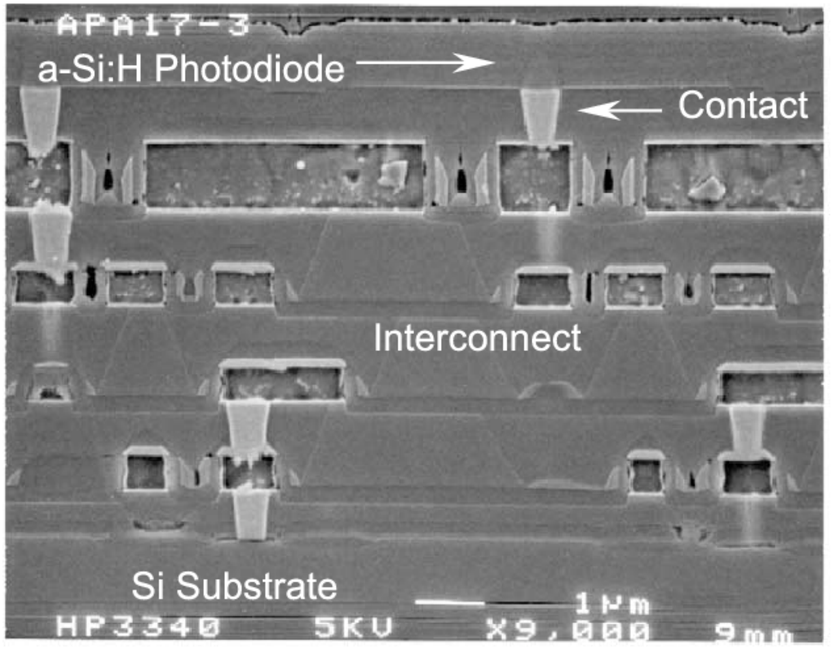
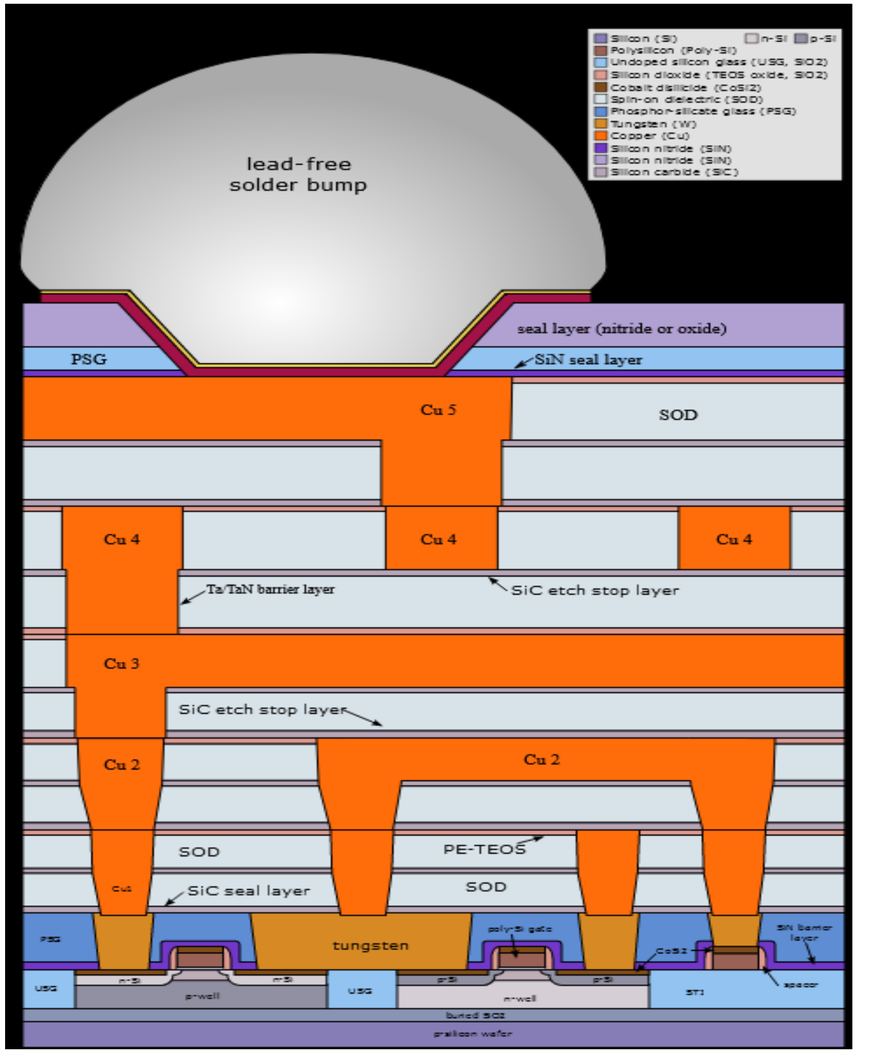
- Develop the resist
- Etch the oxide
- Remove the resist
- Dope the silicon
- Spin a new resist
- Align a new mask
- Develop the resist
- CVD with metal
- Remove the resist
- CVD the back side

CMOS cross-section



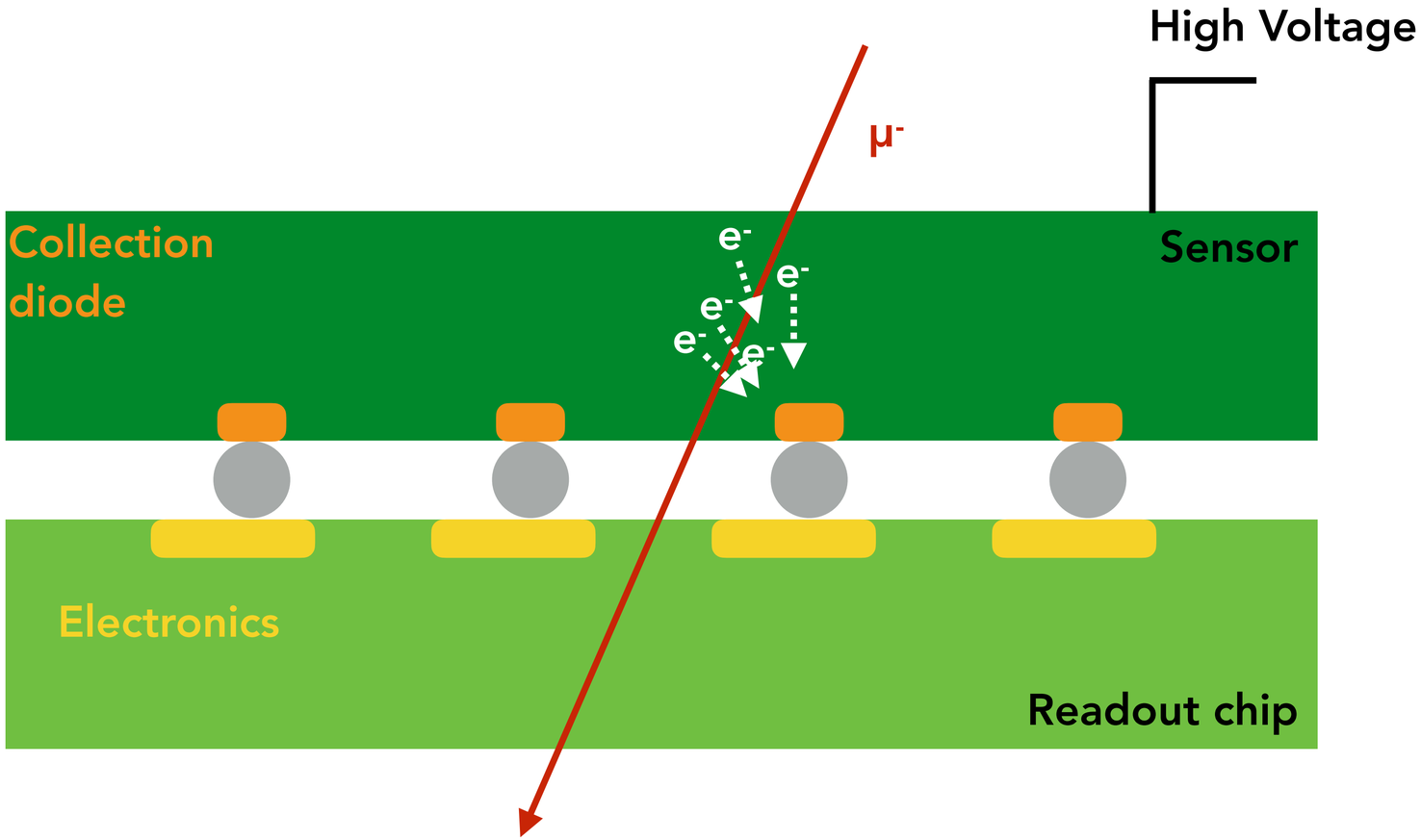


Silicon pixel detectors

Hybrid pixel detector - planar sensor

The technology of choice for most inner (vertex) detectors is still **hybrid pixel detectors**

- Here, the sensor containing our PN-junctions is connected channel by channel (which may be 50 μm in size) to a readout chip
- This decouples what happens on the sensor and in the electronics, and allows us to fully deplete the sensor



Hybrid pixel detector - planar sensor

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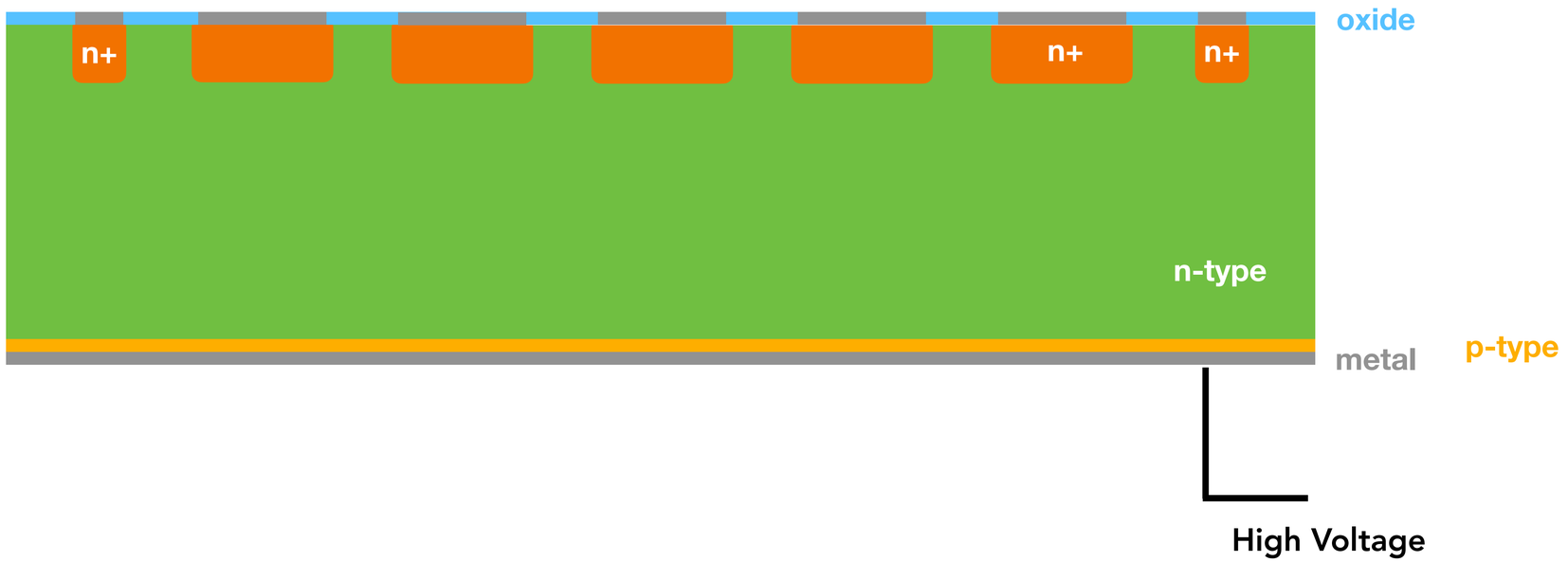
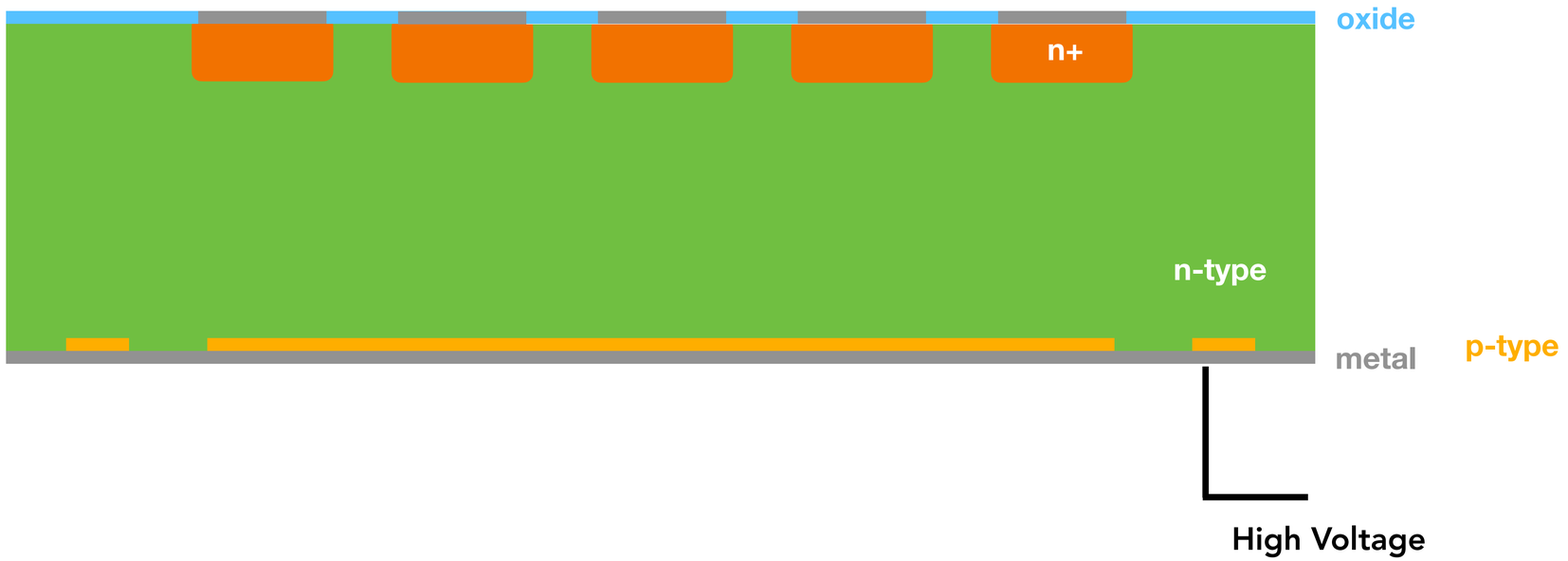


daniel.hynds@physics.ox.ac.uk

Hybrid pixel detector - planar sensor



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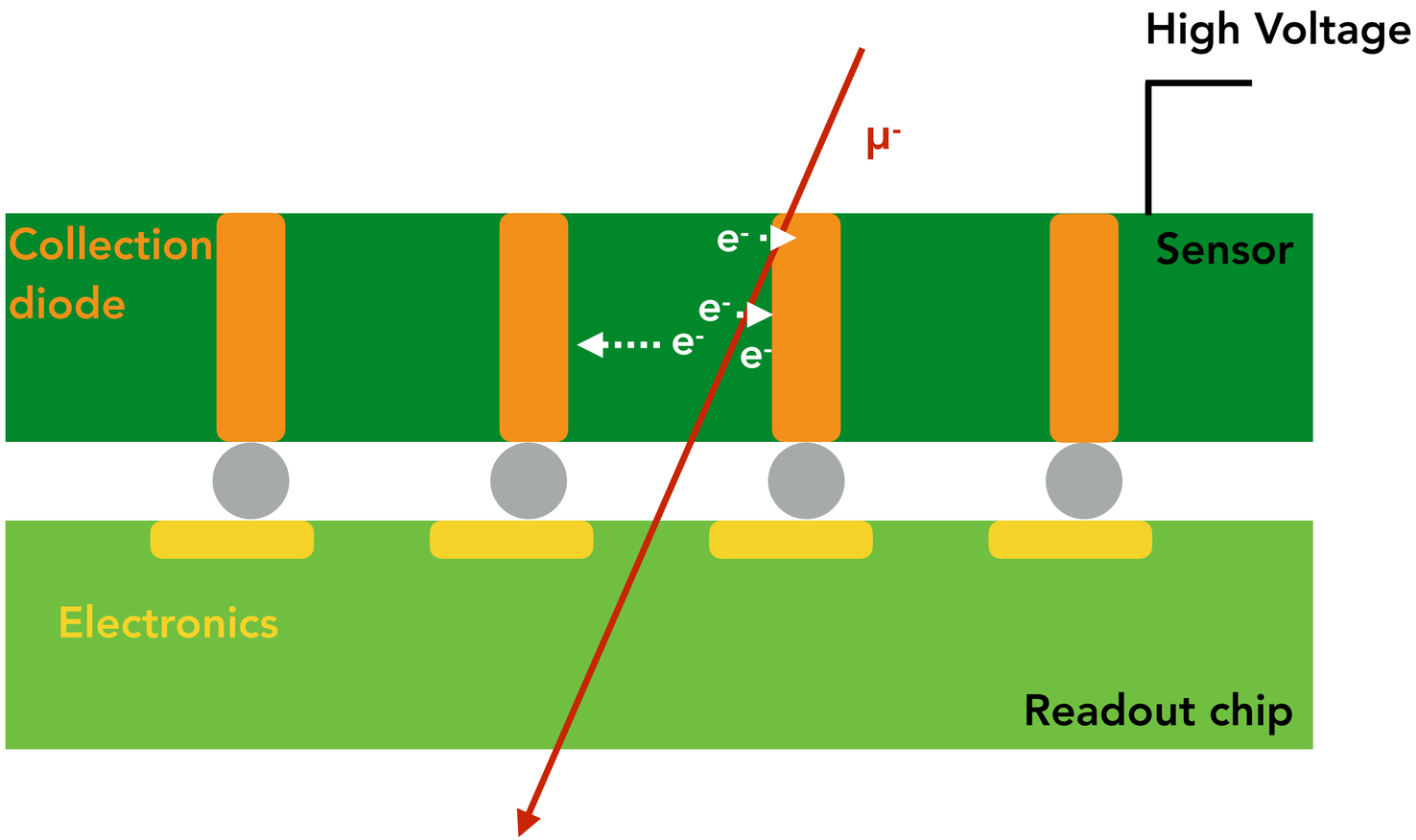
Hybrid pixel detector - planar sensor

Hybrid pixel detector - 3D sensor

Variations in the sensor layout do not affect the electronics, so we have a lot of freedom to change the sensor

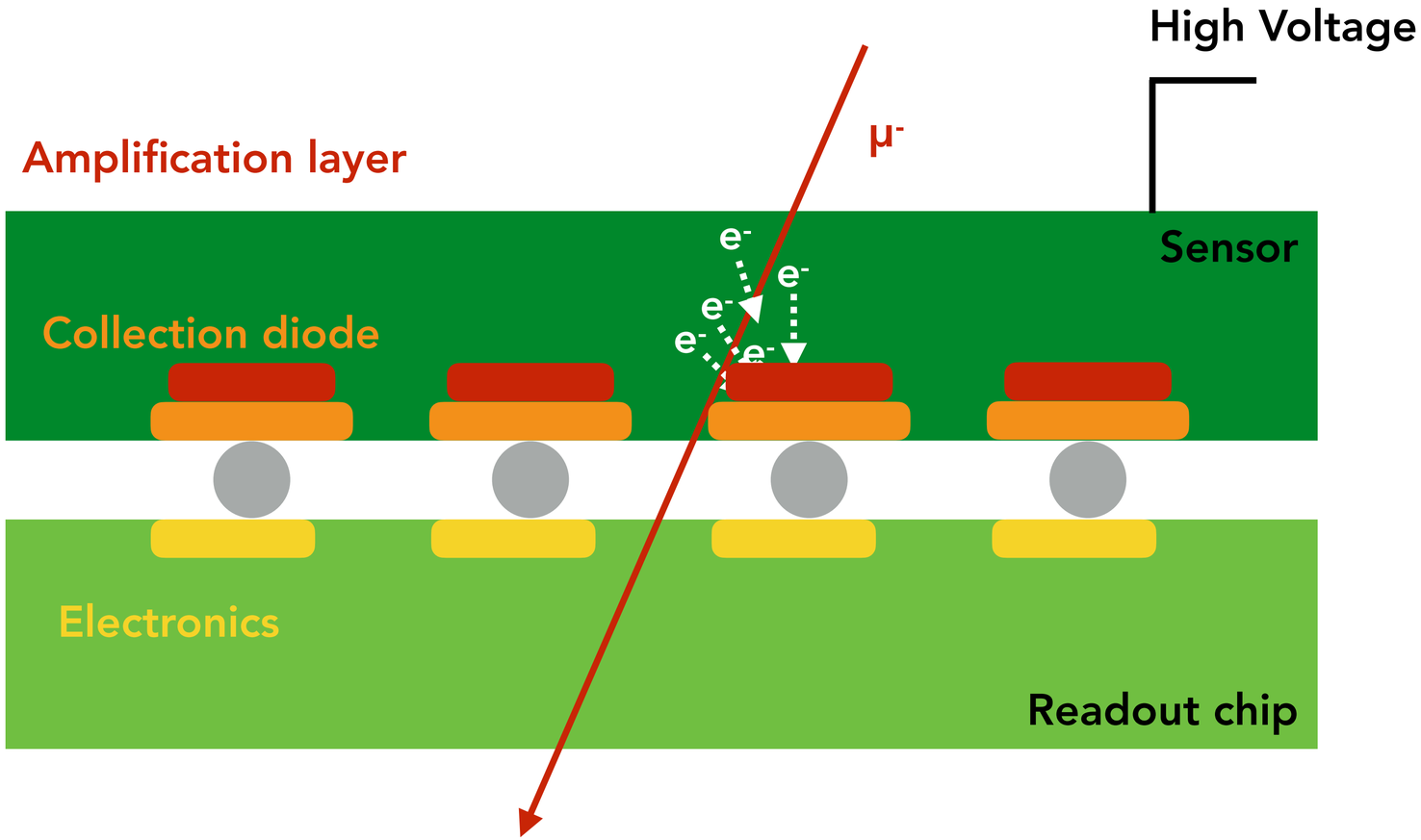
- For thick planar sensors, the charge has a long way to travel to be collected
- We could instead *etch* through the silicon and have a 3D structure, which reduces the collection path



Hybrid pixel detector - LGAD sensor

When thinking of signal speed or detecting small charge deposits, we have to do something a little more creative

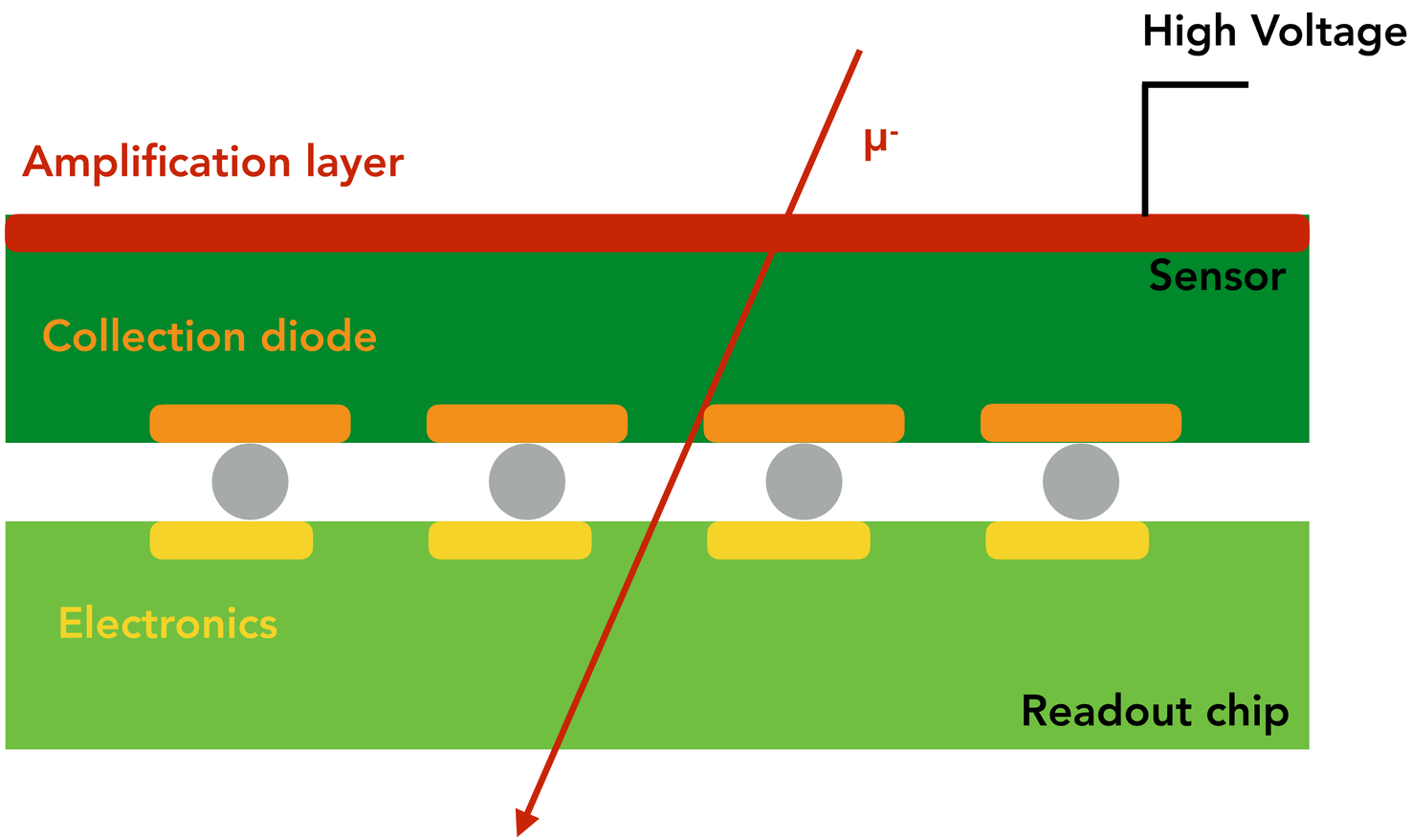
- If the electric field inside the silicon gets high enough, then we can accelerate our charge carriers enough that they cause *additional ionisation*
- This is achieved by some additional doped regions, to give us a **Low Gain Avalanche Diode (LGAD)**
- This can give us a gain of up to ~100 (though not between pixels!)



Hybrid pixel detector - iLGAD sensor

LGADs are still under very active investigation, and there are many proposed variants to allow segmentation without loss of gain

- One approach is to move the amplification layer to the back side of the sensor
- These so-called **inverted-LGADs** use the motion of both charge carriers to create a larger signal



Monolithic detector - MAPS

Hybrid pixel detectors give a lot of functionality in-pixel, and allow flexibility for the choice of sensor, but are relatively expensive devices

- If this is all being done in silicon, why not use the same piece? **Monolithic detectors**

Monolithic detector - MAPS

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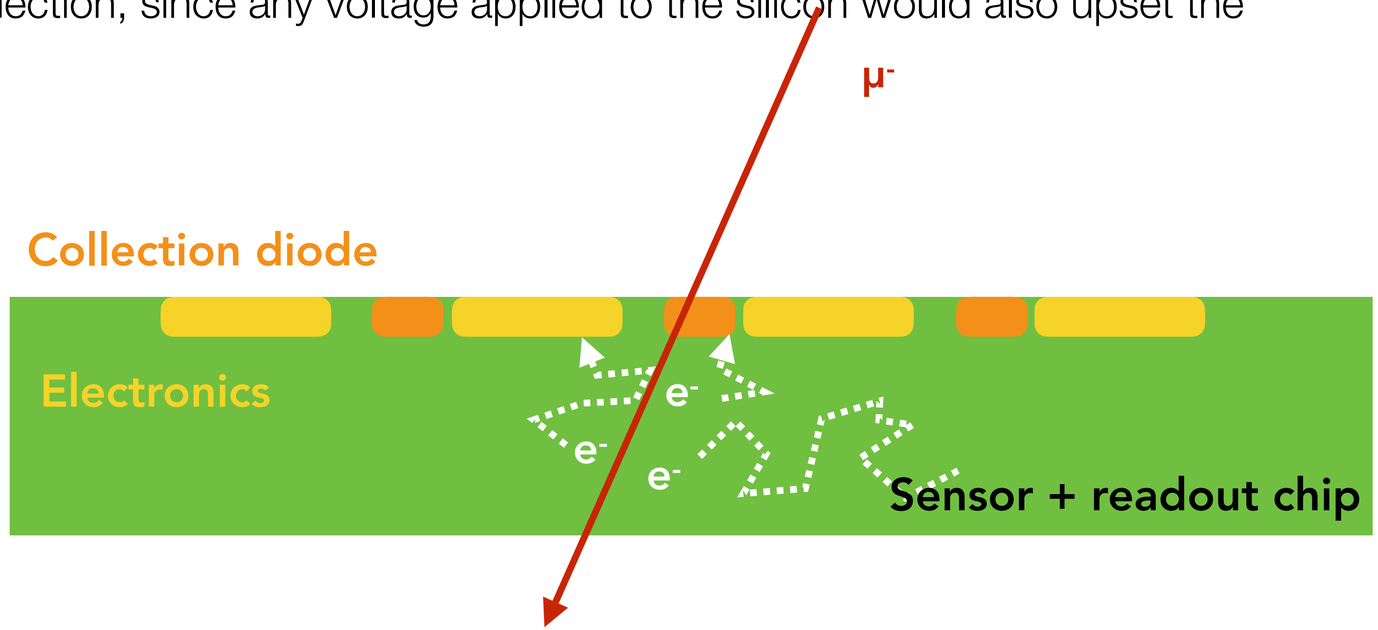
- If this is all being done in silicon, why not use the same piece? **Monolithic detectors**

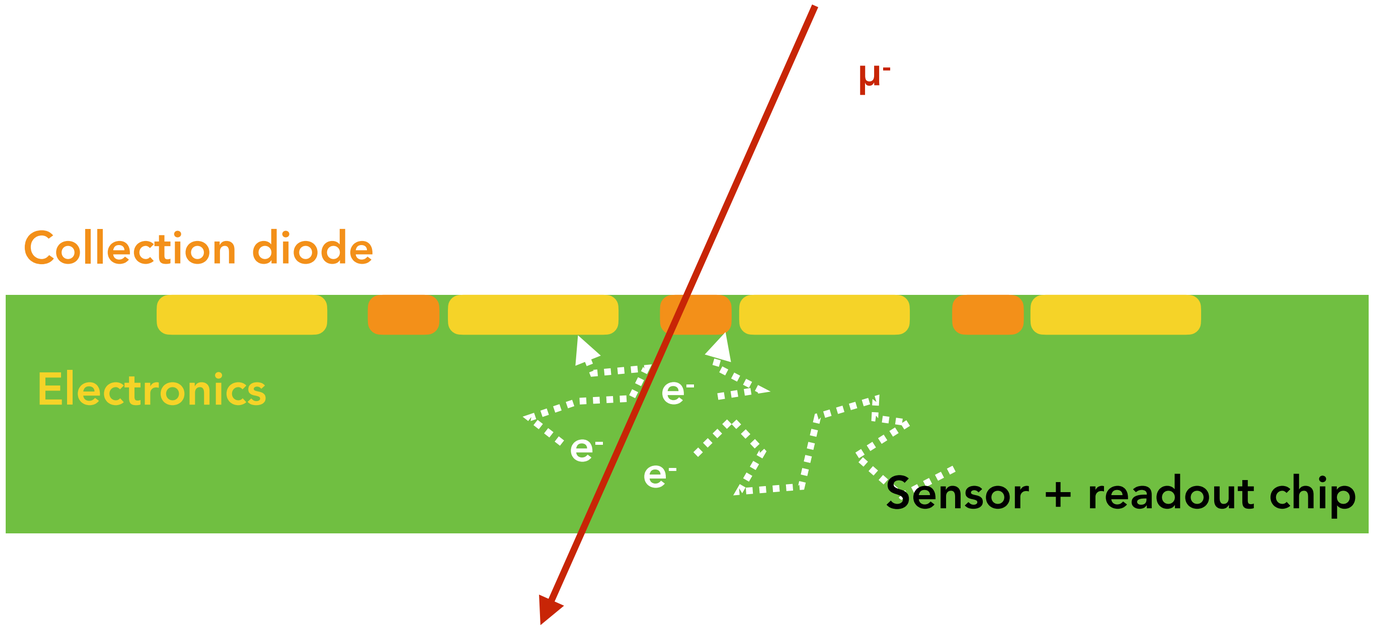
Historically these suffered from slow charge collection, since any voltage applied to the silicon would also upset the electronics

- Small built-in depletion region
- Most charge collected by diffusion
- **Monolithic Active Pixel Sensors (MAPS)**



Monolithic detector - HR CMOS

In the last 10 years, monolithic devices have evolved substantially, taking advantage of new processes within the microelectronics industry



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Monolithic detector - HR CMOS

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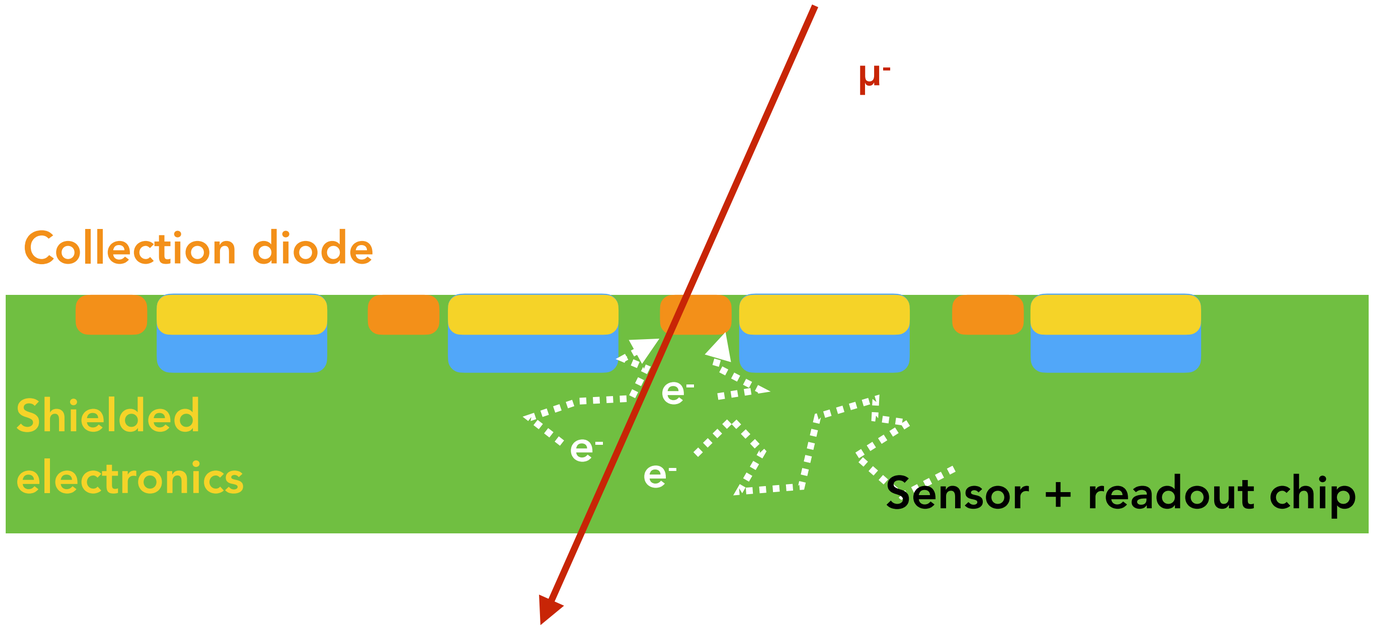
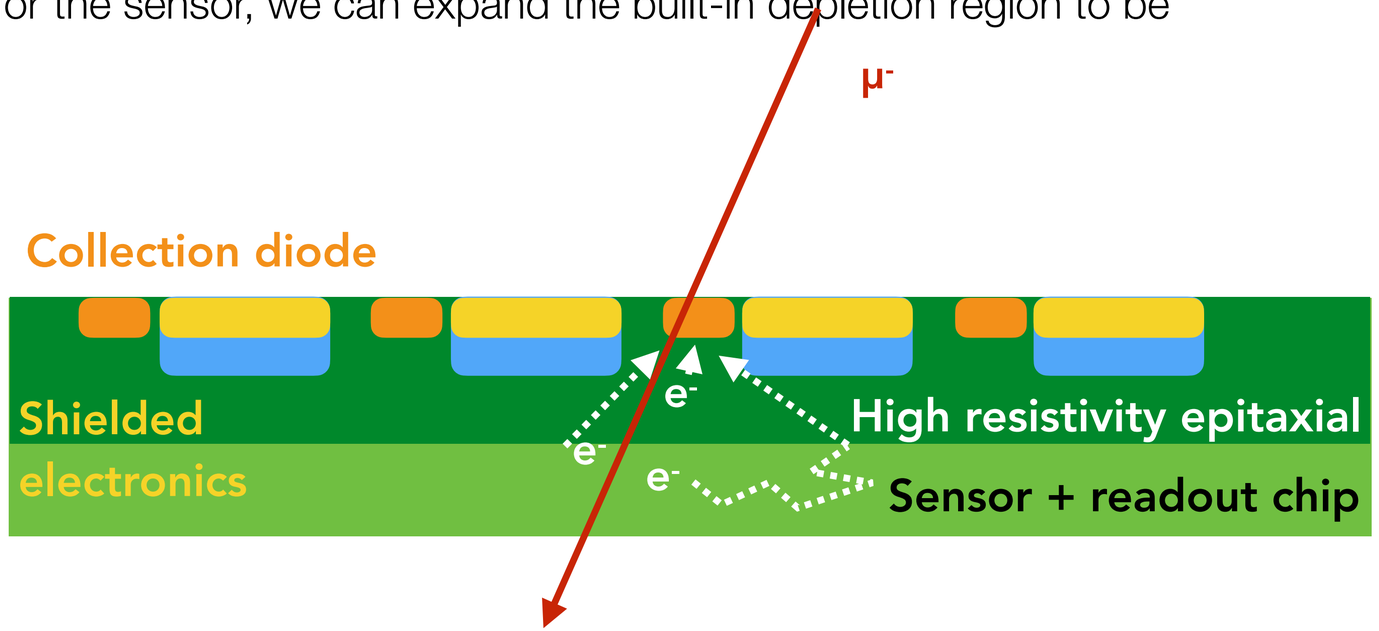
- By shielding our electronics, we can now prevent competition for charge collection between the electronics wells and the collection node



Monolithic detector - HR CMOS

In the last 10 years, monolithic devices have evolved substantially, taking advantage of new processes within the microelectronics industry

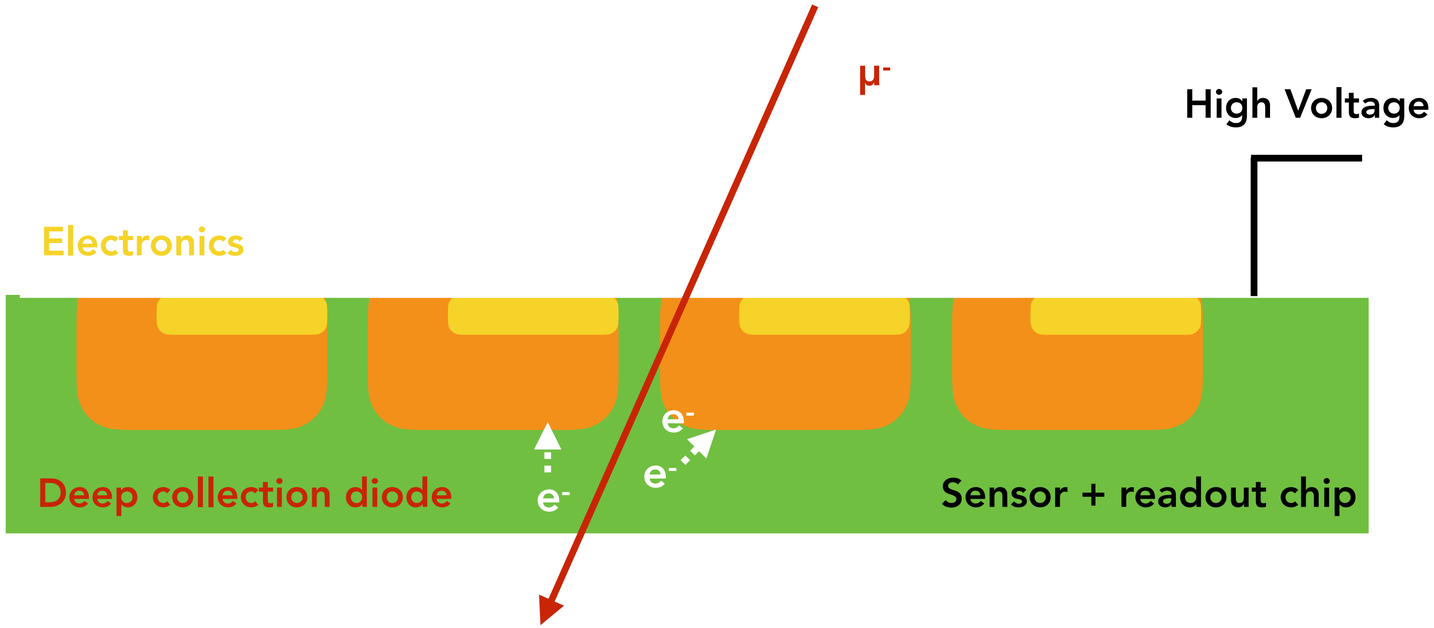
- By shielding our electronics, we can now prevent competition for charge collection between the electronics wells and the collection node
- By using a high-resistivity epitaxial layer for the sensor, we can expand the built-in depletion region to be substantial in size (10 - 15 μm)
- These are termed **High Resistivity CMOS** detectors



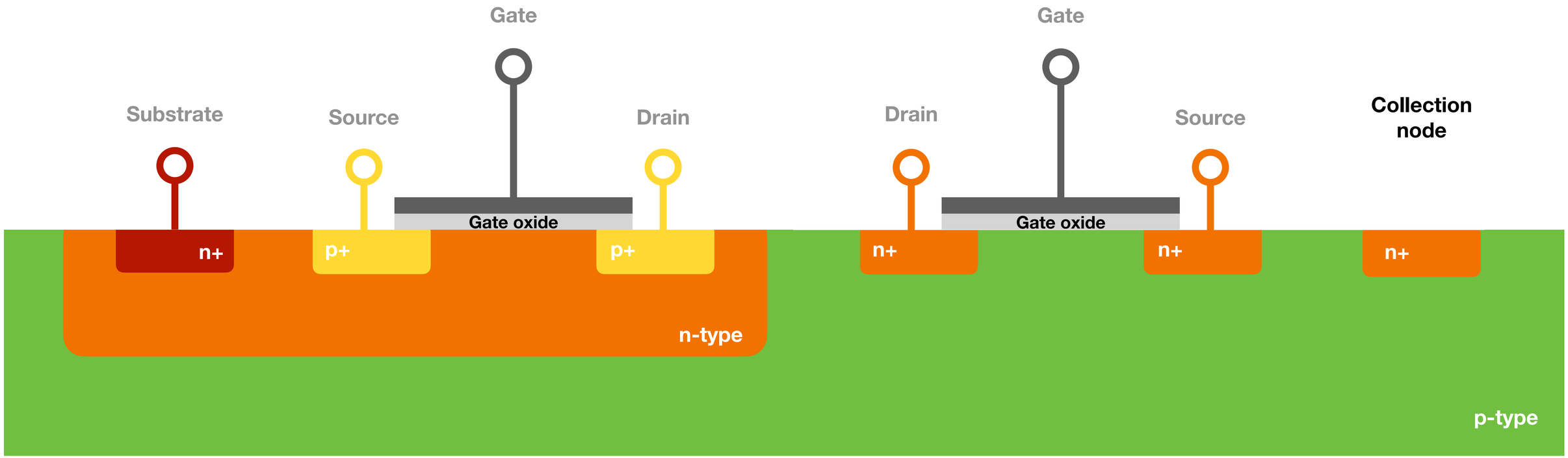
Monolithic detector - HV CMOS

An alternative approach is to tackle the other issue: applying a reverse bias voltage while protecting the electronics

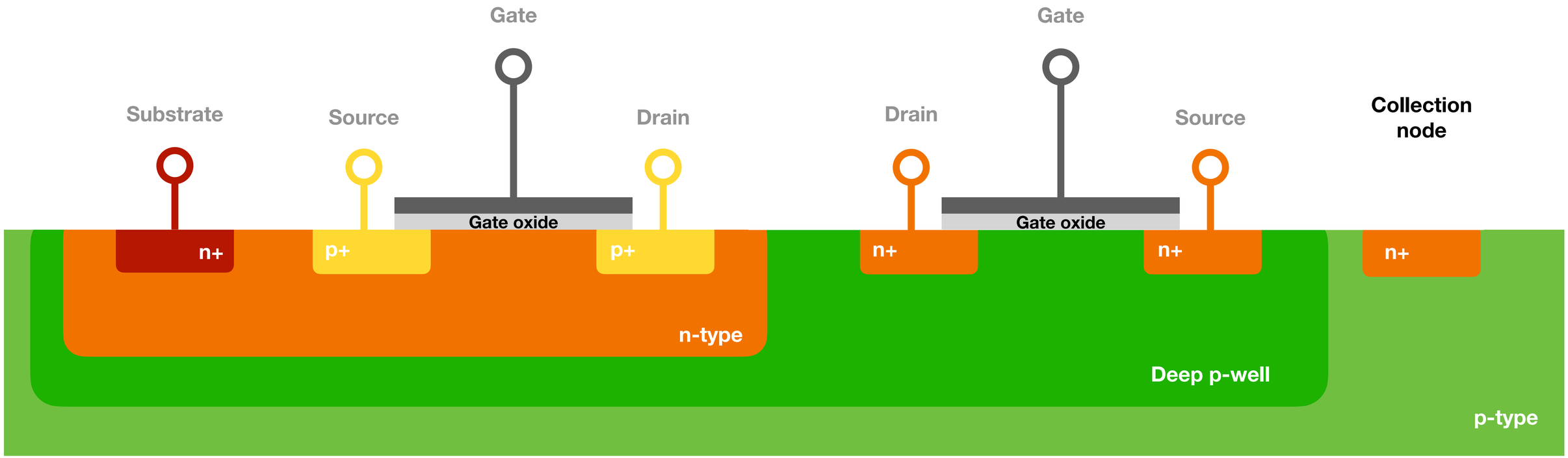
- Many companies have developed deep n-wells to function at high voltages
- We turn our simple collection node into one of these deep n-wells and “hide” all of the electronics inside
- Imaginatively termed **High Voltage CMOS**



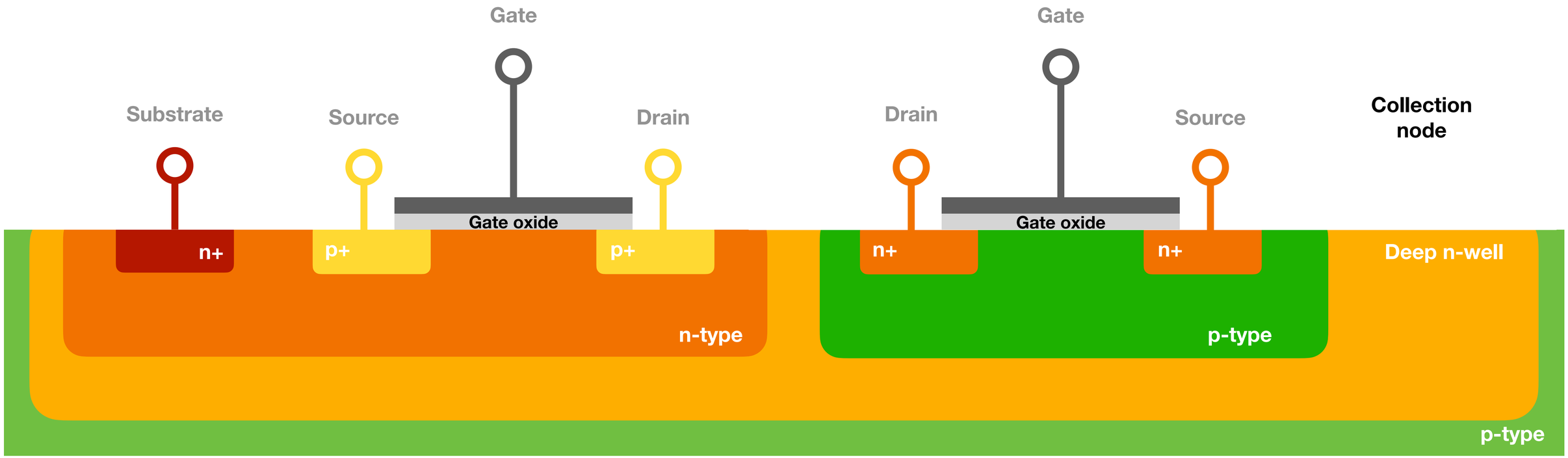
MAPS detectors - classic



HR-CMOS


Gate
Gate
Substrate
Source
Drain
Drain
Source
Collection node
Gate oxide
Gate oxide
n+
p+
p+
n+
n+
n+
n-type
Deep p-well
p-type

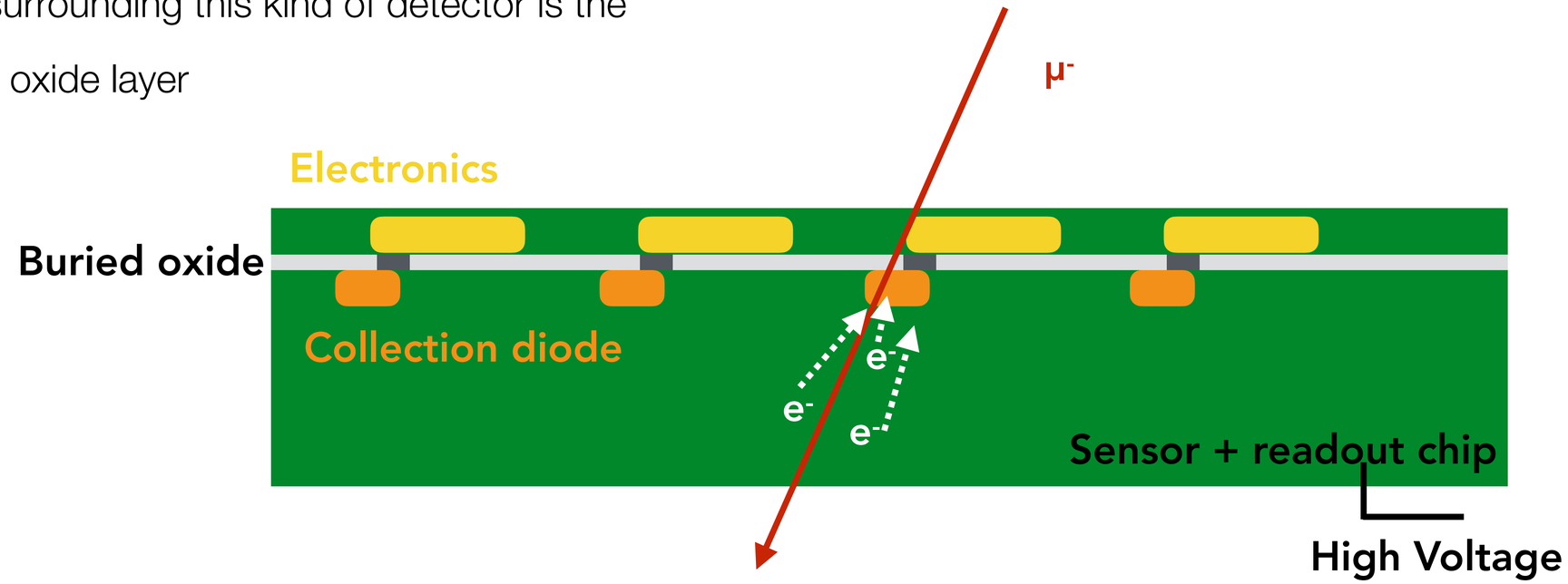
HV-CMOS


Gate
Gate
Substrate
Source
Drain
Drain
Source
Collection node
Gate oxide
Gate oxide
n+
p+
p+
n+
n+
Deep n-well
n-type
p-type
p-type

Monolithic detector - SOI

Another experimental (but not widely used) approach to solving this problem is to “separate” the silicon containing the collection node from the silicon containing the electronics

- An oxide layer is implanted in order to act as an insulating barrier, with vias connecting the electronics
- Such sensors are called **Silicon on Insulators**
- One of the main issues surrounding this kind of detector is the build-up of charge in the oxide layer



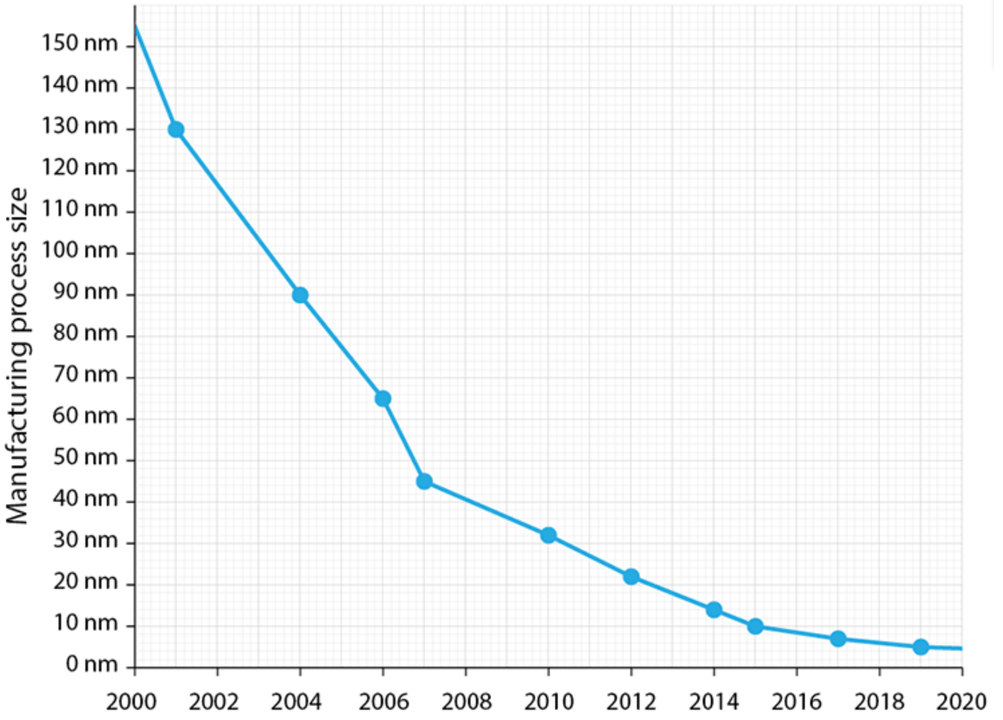
Technology nodes

Microelectronics industry moves much faster (and has much more money) than we do…

- Devices on the market just now with **4 nm** feature size
- In particle physics we are preparing to install the first readout electronics with 65 nm in 2027

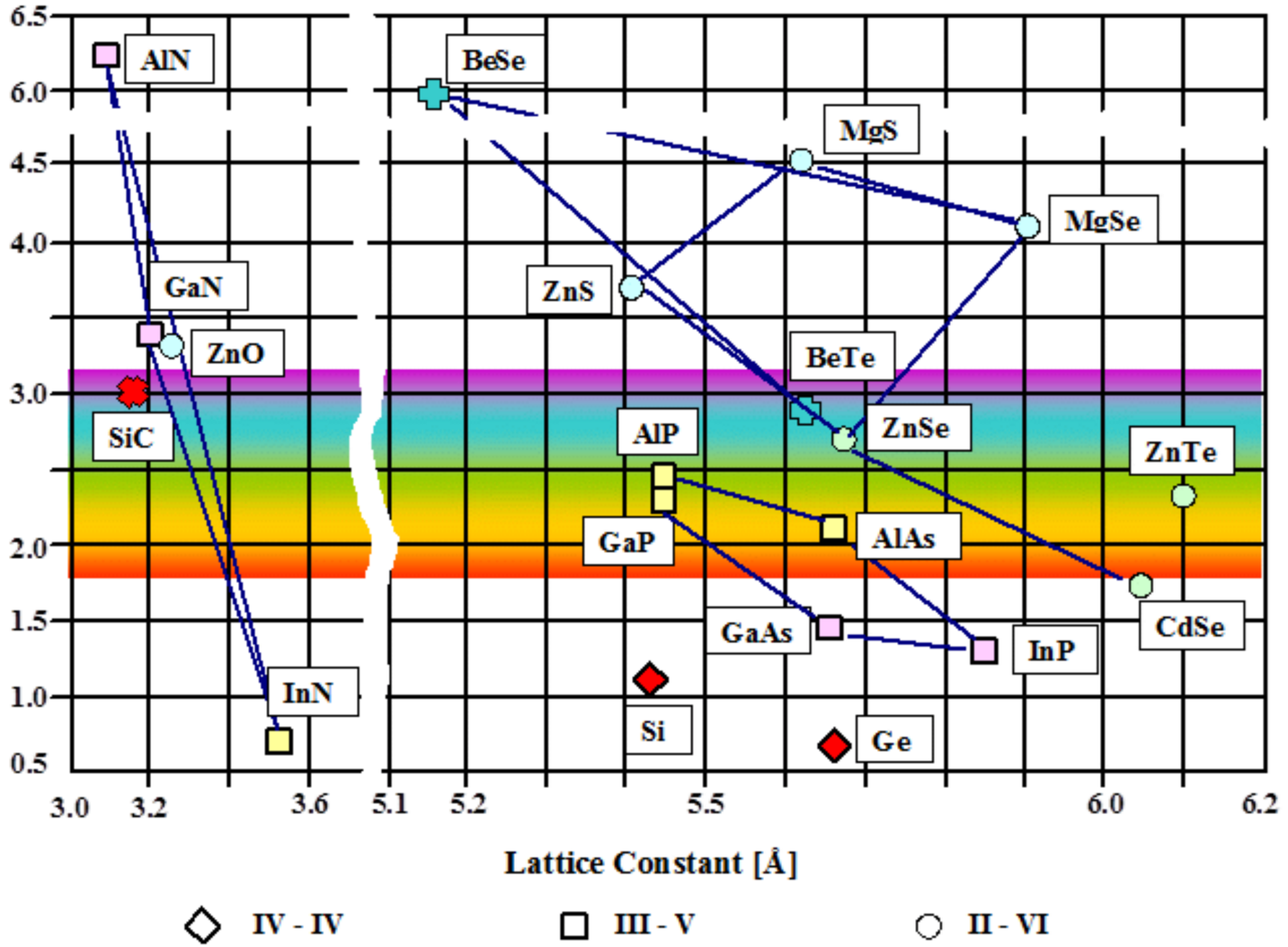
Some trends have helped us - smaller devices and thinner oxides give better inherent TID tolerance

- However, below 28 nm transistor layout changes drastically (FinFETs) - performance TBD



Non-silicon pixel detectors

Non-silicon sensors



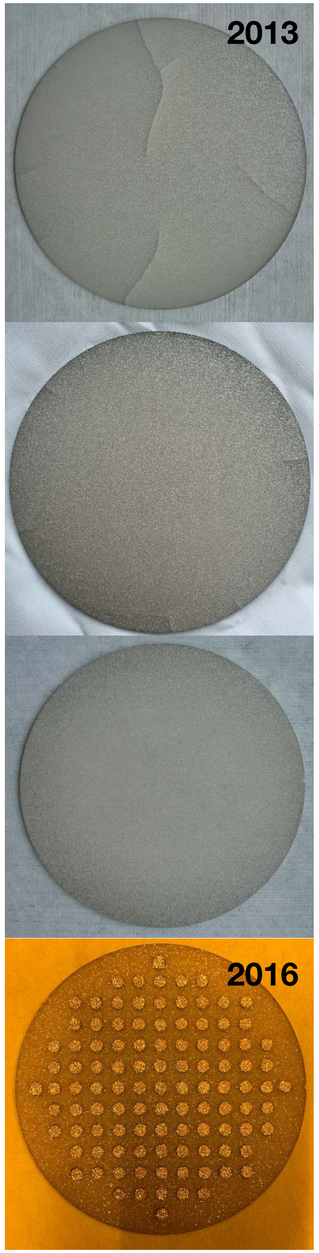
Non-silicon sensors: Diamond

Diamond detectors have been waiting for silicon to give up for several years now

- Analogous crystal structure but band gap of ~5.5 eV
- Low leakage current but also lower signal for equivalent energy loss

One of the major challenges is crystal quality

- Limited vendors of wafers, difficulty and cost involved in single crystal manufacture
- Typically polycrystalline, suffering charge loss



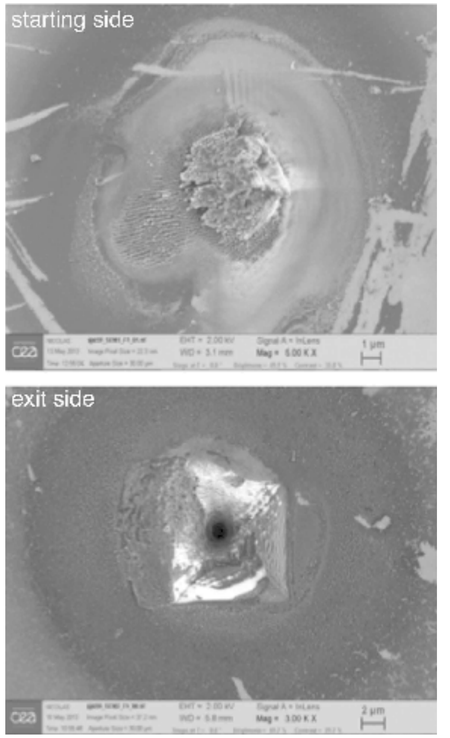
Non-silicon sensors: 3D Diamond

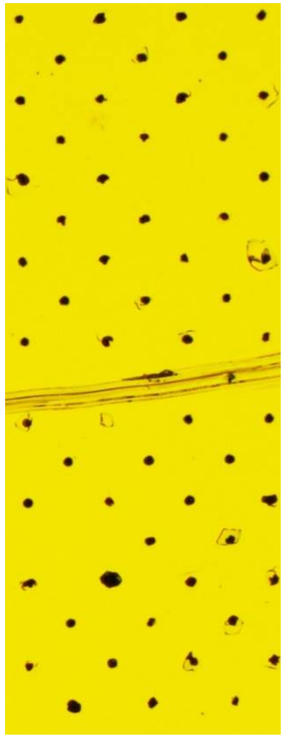
An interesting development in the last 5-10 years: 3D diamond!

- Since one of the main issues is carrier lifetime (crystal quality) reduce the path length significantly by extending the collection nodes through the sensor bulk
- No need to etch - scan a focussed laser through the depth to generate a graphitic contact

One of the disadvantages of this at present is the scanning required to create columns

- Only performed at one or two places
- Attempts ongoing to parallelise column growth



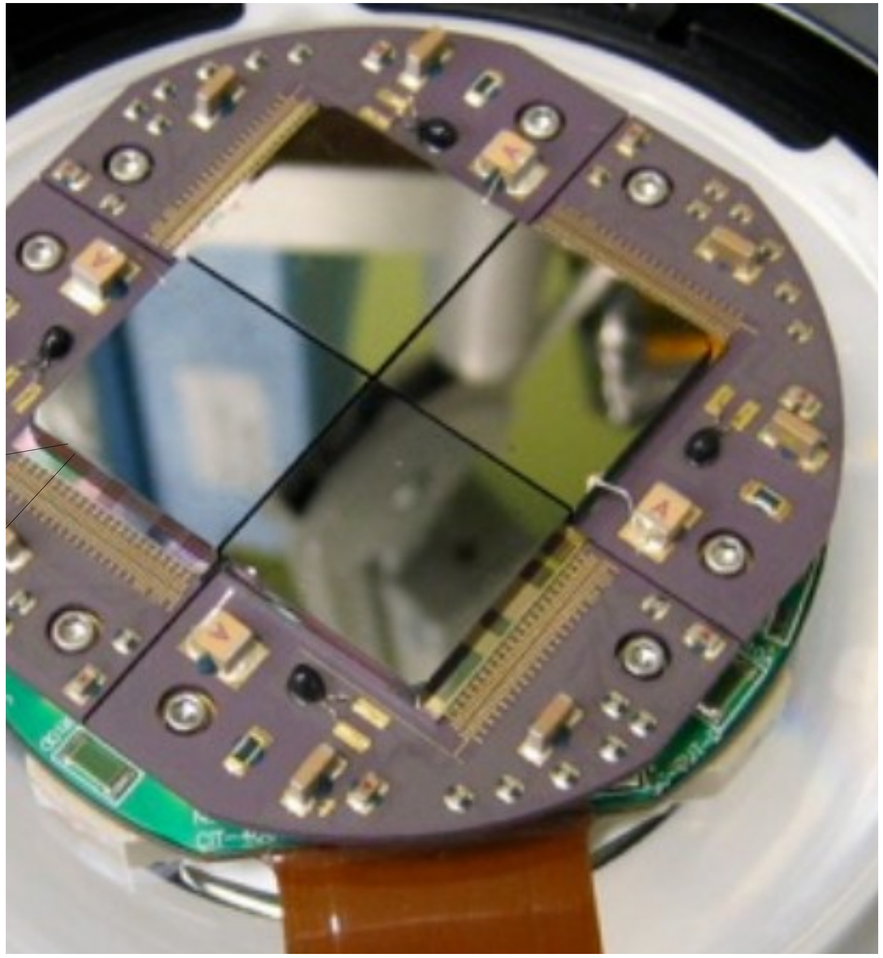


Hole diameter ~6µm

Non-silicon sensors: GaAs and CdZnTe

Both GaAs and CZT have been used as sensors for x-ray detection for many years now

- Wafer quality still an issue - grain boundaries give regions of the sensor with low charge collection efficiency
- Fabrication tricky - chemistry required for good metallic contacts
- Nonetheless, CdZnTe featured in satellite-mounted x-ray camera (NuSTAR)
- Improvements leading to energy resolution of ~1% at 662 keV



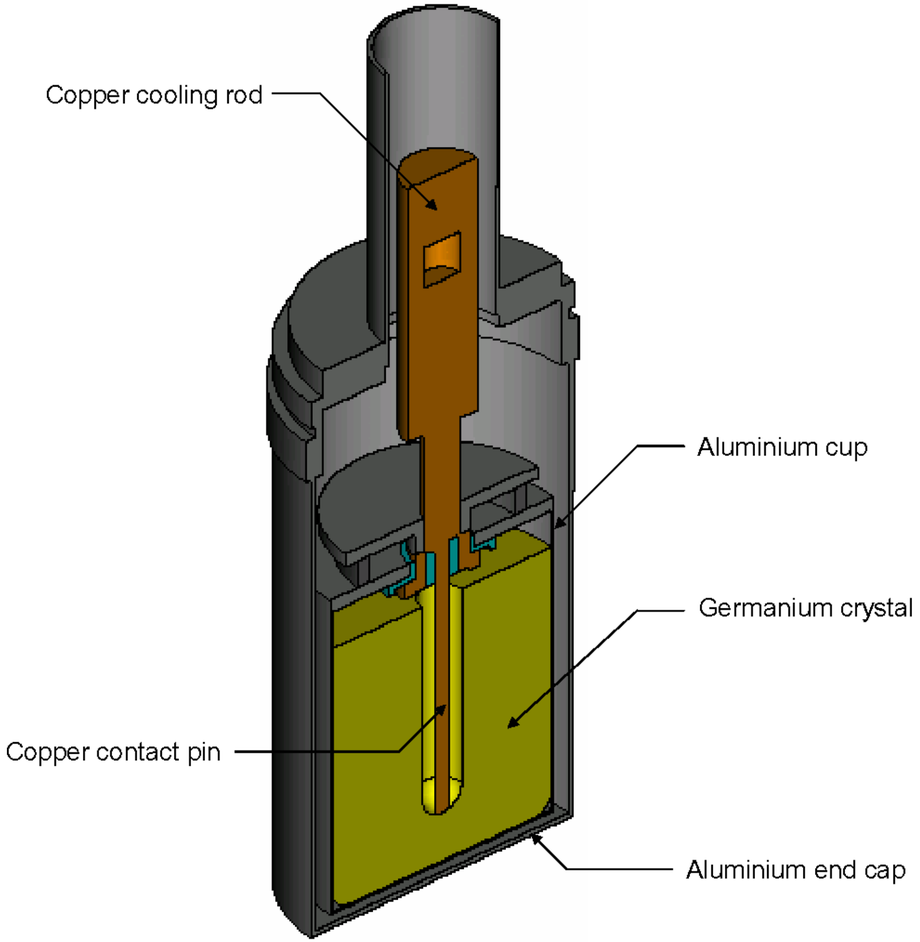
Non-silicon sensors: Ge

Germanium detectors have long been used for particle detection

- Reasonable purity single crystals can now be manufactured (though at some cost)
- Applications in x-ray and gamma spectroscopy

The main issue with Germanium is fundamental: the bandgap!

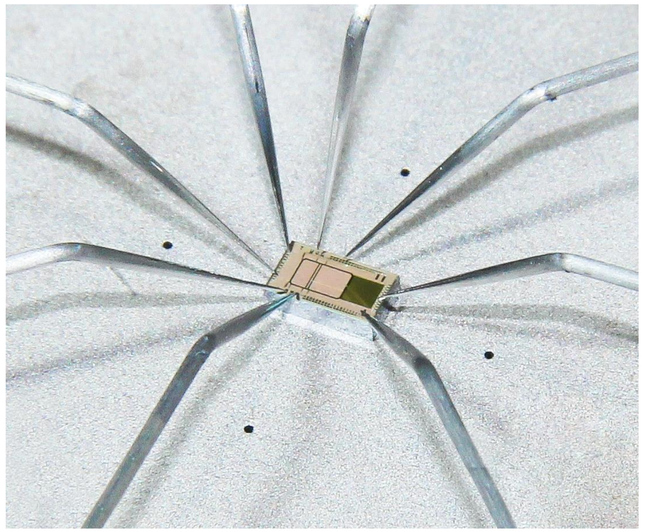
- Small bandgap means large leakage currents at room temperature
- Typical operation at cryogenic (liquid nitrogen) levels

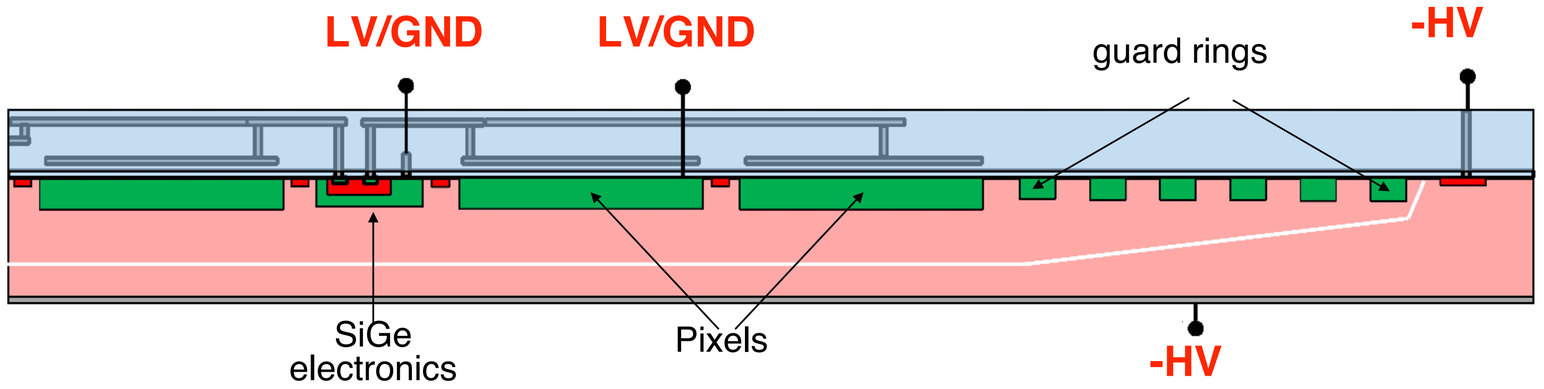


Non-silicon sensors: Ge

More recent appearance of Ge in particle physics detectors is part of industry available BiCMOS processes

- Ge deposited in a small region and used to manufacture very fast timing circuitry
- This currently sits outside of the pixel volume (so inactive area) but an interesting development





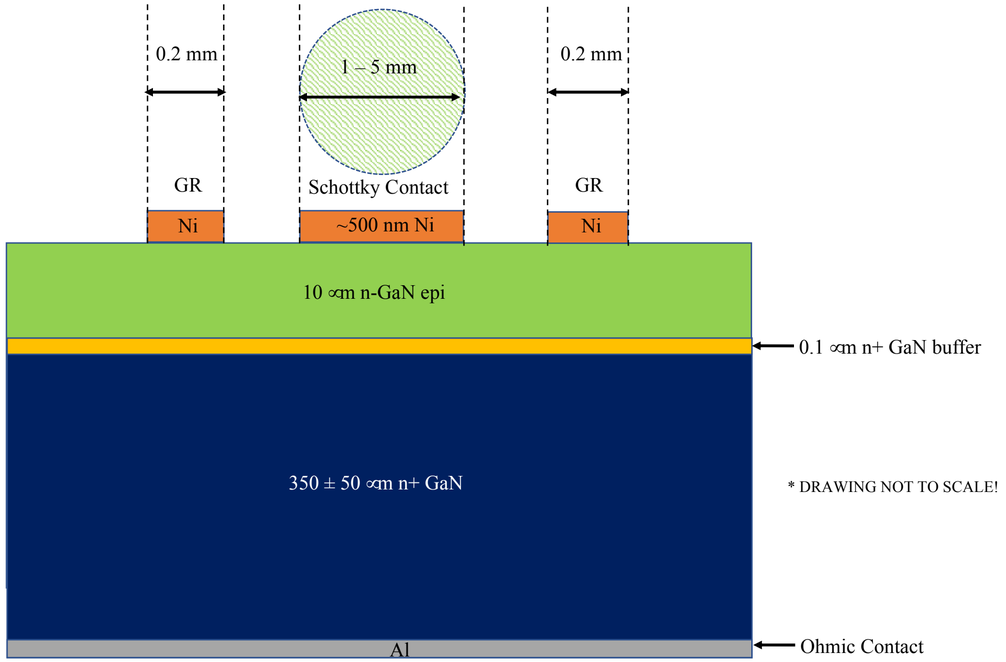
Non-silicon sensors: GaN

More recent addition to materials being considered due to high lattice displacement energy threshold

- Should show much less NIEL damage than silicon

Already large usage of GaN devices in high power electronics, appearance of wafers with high quality epitaxial

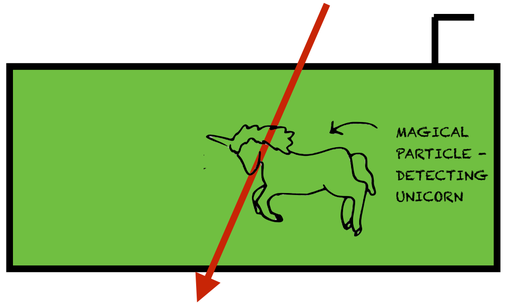
- Note that these are 2” wafers…



Summary

What kind of detector to choose?

Unfortunately there is no quick answer other than:

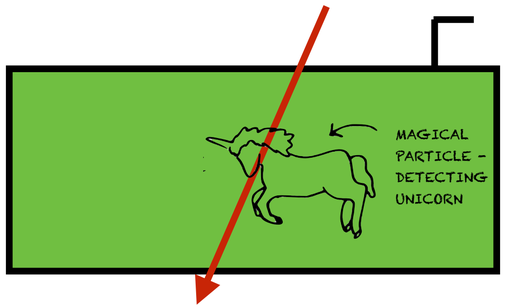


Some broad statements can guide:

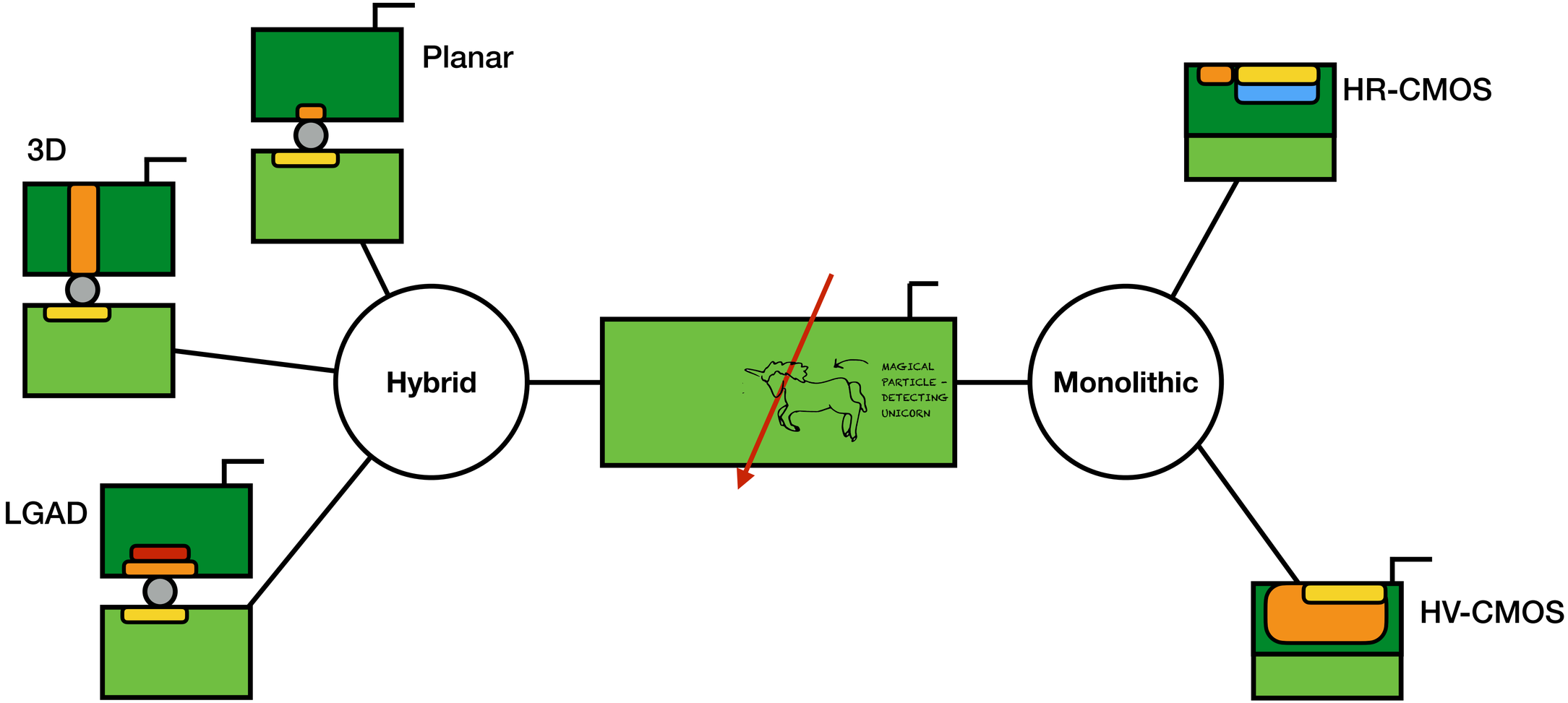
- Hybrid pixel detectors are necessary if you need high-Z sensors (X-rays, gamma rays)
- Monolithic detectors are typically cheaper than hybrid
- Built-in amplification if you have low signal or need very fast timing

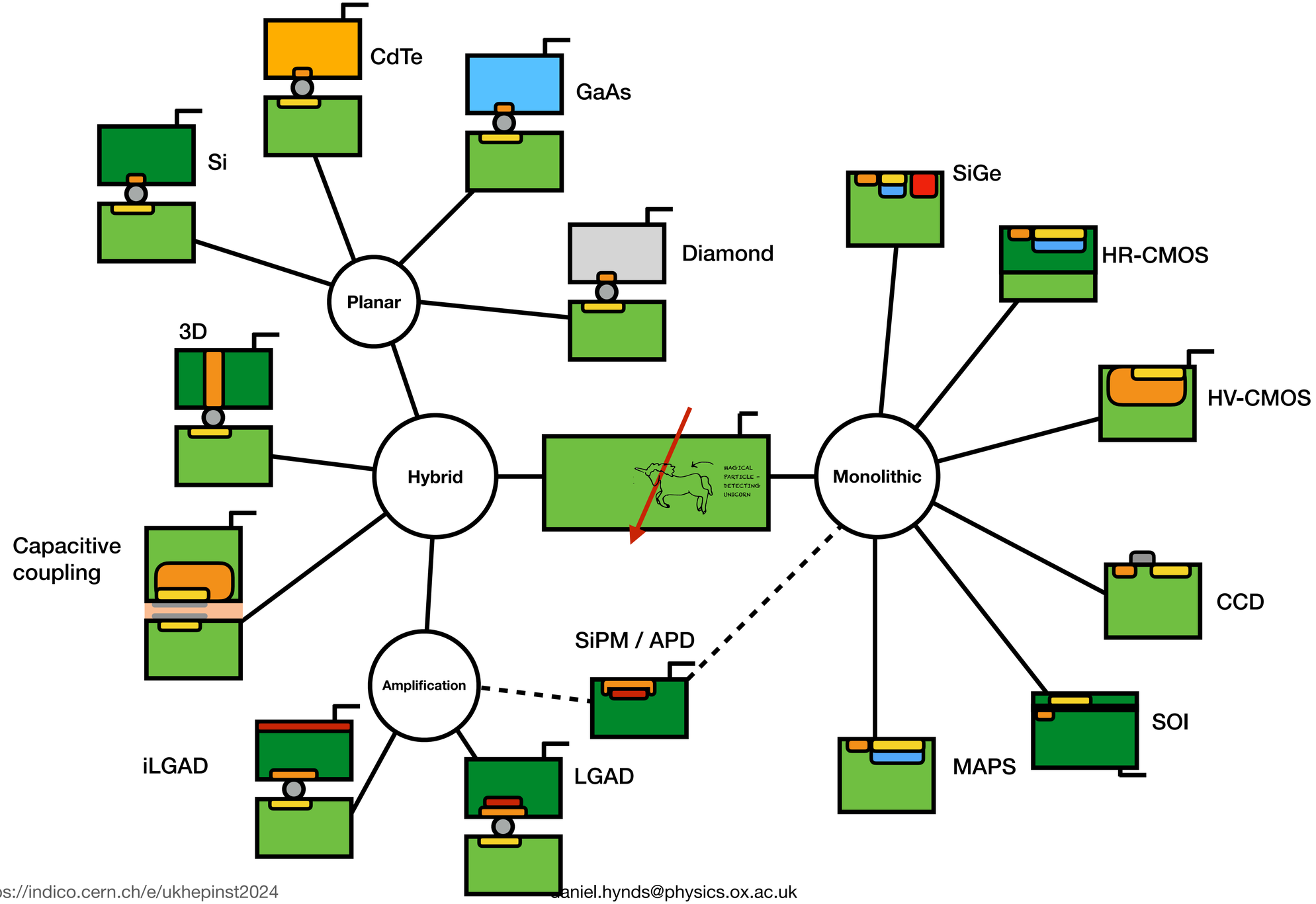
But the details will very much depend on the application

The silicon zoo



The silicon zoo





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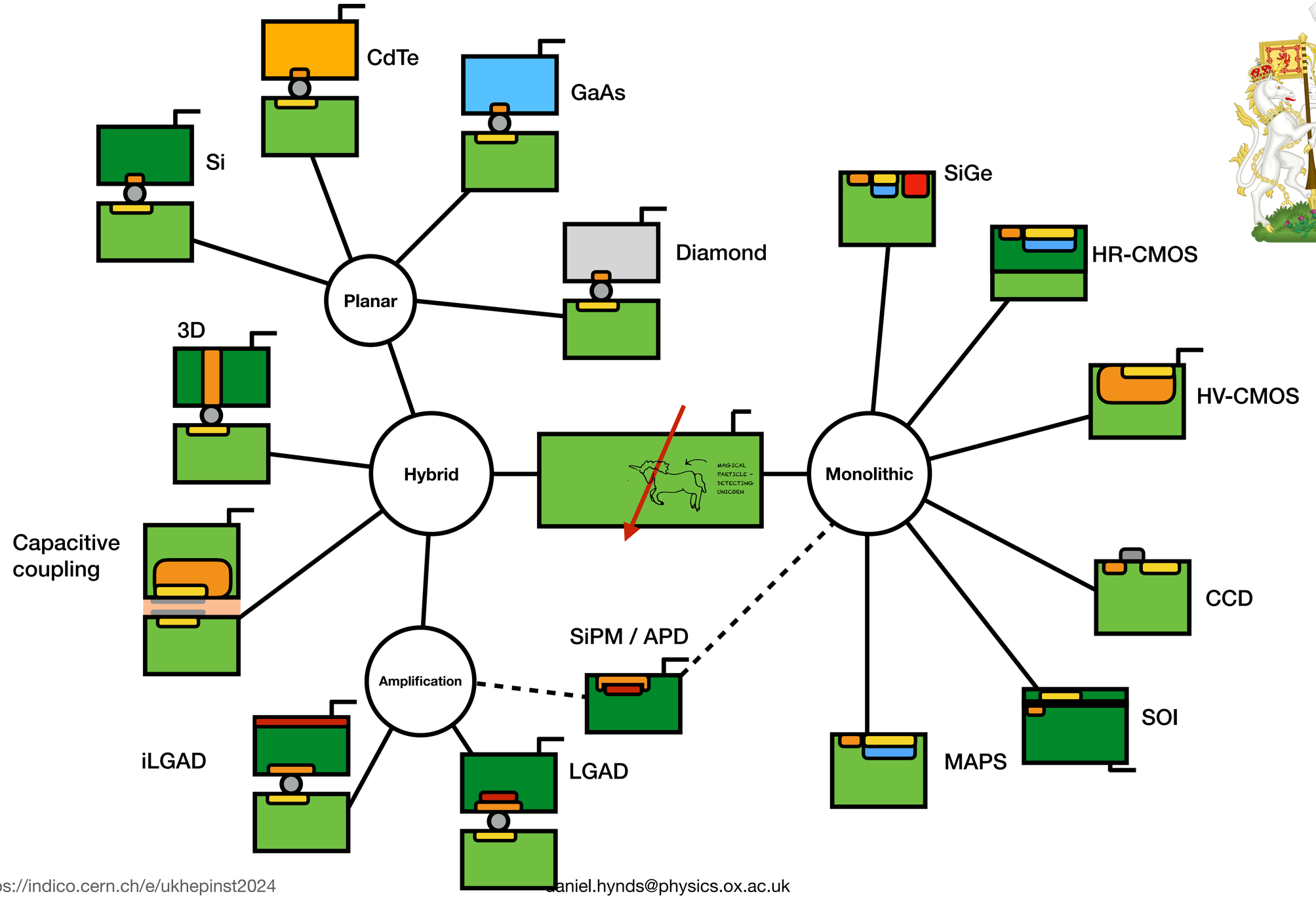

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To finish

Eventually, I started to realize that science could explain how EVERYTHING worked.

There was no longer any need for my magical unicorns. Science killed my unicorns.

$$e = 1 - \frac{1}{(V_1/V_2)^{\gamma-1}}$$

$$\Delta S_{UNIVERSE} > 0$$

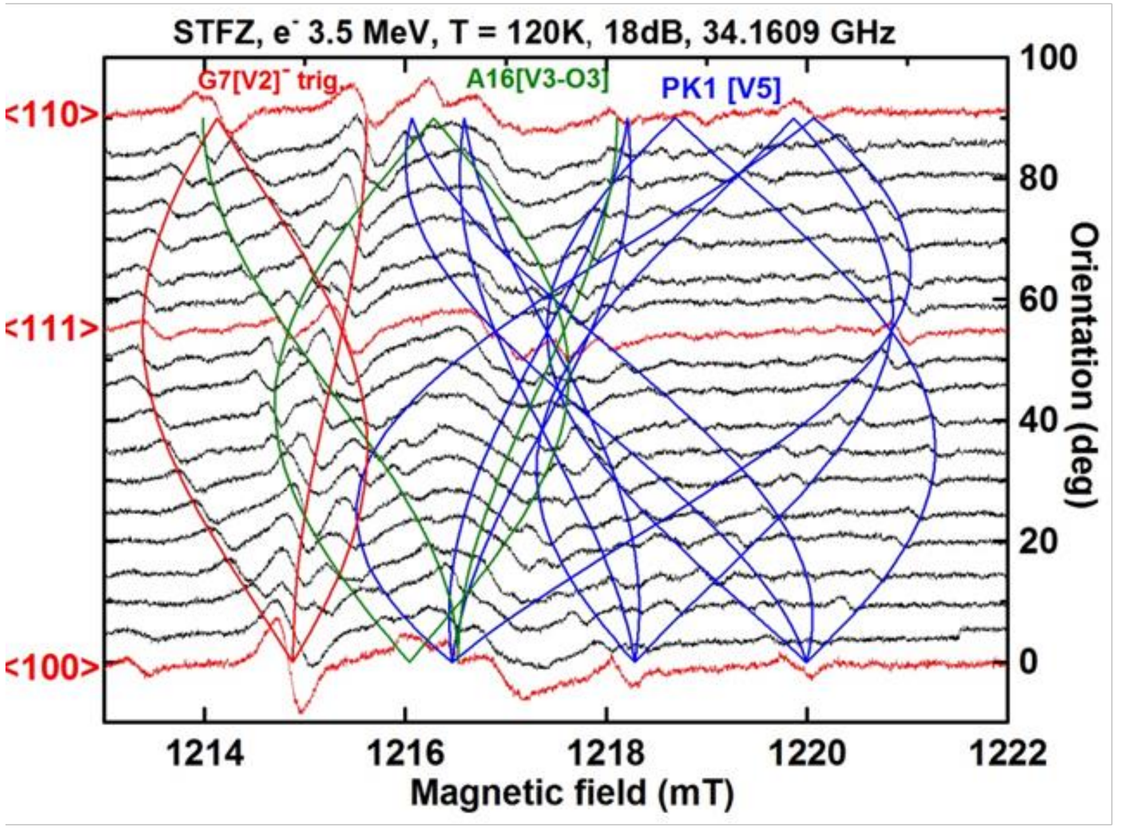
$$\Sigma F_y = T - mg = ma_y$$

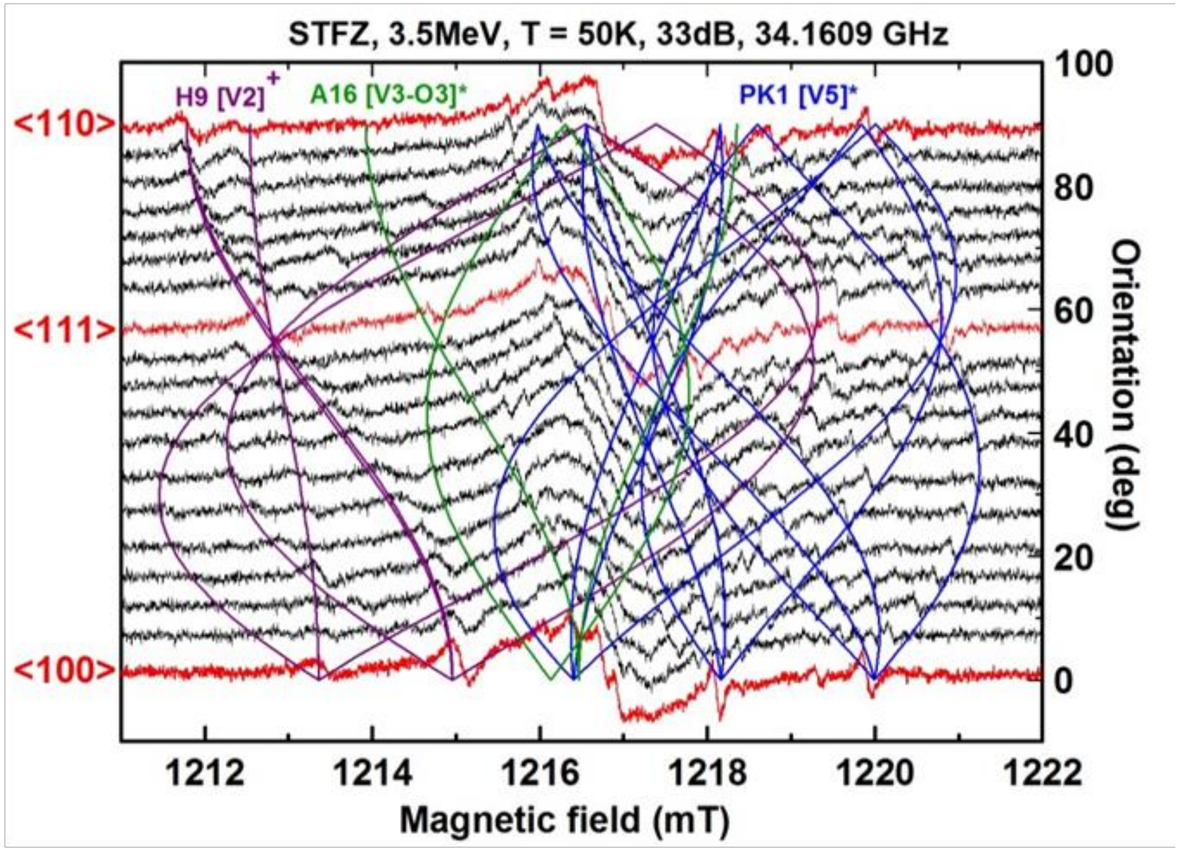
$$\nabla \times E = -\frac{\partial B}{\partial t}$$

To finish

The physical mechanisms underlying the response of advanced CMOS microelectronics are now relatively well known in broad outline, but they may never be known in full detail. The models for interface trap production, and for the oxide hole trap, both date from the 1980s, although some of the confirming experiments were done in the 1990's. But what the models tell us is that the overall response is extremely complicated. There are multiple processes involved, with complicated time dependences, and different field dependences, and different temperature dependences. How all the pieces fit together will always be a complicated story. Anytime the manufacturing processes change, trench oxides replacing planar isolation structures, or new dielectrics entering production, etc., many of the details of the response will have to be worked out again. Considering how often new manufacturing techniques are introduced, there is little chance the community will ever run out of things to do.

Variation of ESR spectra with measuring temperature (120K) and (50 K).





Thank you!