

Norwegian contributions to ITk Pixels



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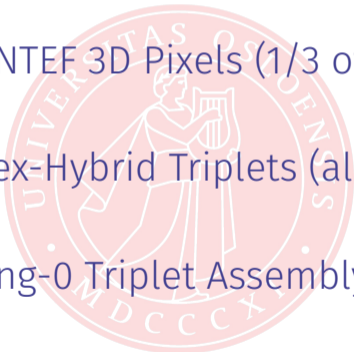
¹University of Oslo ²University of Bergen

ITk Visit to Norway — 2024-06-25



Outline

- 1 Funding and Project Structure
- 2 SINTEF 3D Pixels (1/3 of the Innermost layer)
- 3 Flex-Hybrid Triplets (all three designs)
- 4 Ring-0 Triplet Assembly and Testing



NorLHC I/II WP2

Project structure and funding

NorLHC / WP2 - 2018-22

In-kind:

- Local infrastructures at the University groups in Bergen and Oslo
- Module prototyping, testing and validateion
- Sensor qualification and pre-production

Common:

- Pixel ASIC
- Hybridization /flip-chip

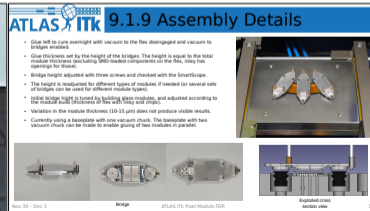
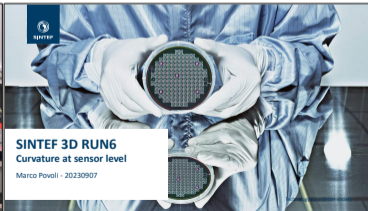
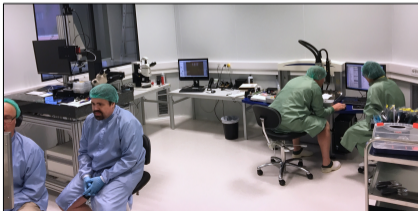
NorLHC-II / WP2 - 2023-27

In-kind:

- Sensor production
- Flex-PCB production
- Site qualifications
- Module assembly (Oslo)
- Module testing (Bergen)

Common:

- On-detector services
- Common items



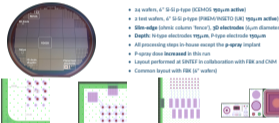
SINTEF 3D Pixel Sensors

Recent history of 3D technology at SINTEF

YEAR	Project	Wafer type	Active thickness [nm]	Electrode diameter [µm]	Remarks
2006	Run-1	4" SiC	230	35	N-type, low mechanical yield
2008	Run-2	4" SiC	230	35	SiO ₂ pass (rough)
2010	Run-3	4" SiC	230	35	Low yield (2 out of 28 wafers ok)
2018	Run-4*	6" Si-Si	50 & 100	8	Very good yield (E-14 layout)
2019	Run-5*	6" Si-Si	150	6	OK yield (POSS A/B) with active edge
2021	Run-6*	6" Si-Si	150	6	Completed Feb. 2021, ATLAS pre-production, (POSS A/B with common layout with FBK, slim-edge termination)


*funded by Norwegian ATLAS R&D

Fabricated wafers
Pixel layout - 50µm x 50µm - 1E configuration



- 24 wafers, 6" Si-Si p-type (ICD405 90µm active)
- 2 test wafers, 6" Si-Si p-type (P82M/NGTO [LX] 100µm active)
- Slim-edge (inter-column "finest"): 3D electrodes (5µm diameter)
- Depth: N-type electrodes 10µm, P-type electrode 100µm
- All processing steps in-house except the p-spray implant
- P-spray dose increased in this run
- Layout performed at SINTEF in collaboration with FBK and CNR
- Common layout with FBK (6" wafers)

3D RUN6 - Fabrication process

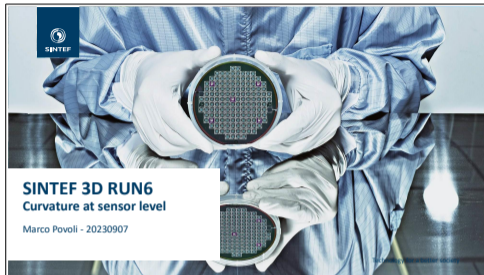


1. P-spray/implantation + oxidation
2. Etching mask for CRK (aluminium)
3. CRK of π -columns
4. Phosphorus doping and poly filling
5. Planarize doping
6. Repeat steps 3-6 for p -columns (SiO₂)
7. Contact opening
8. Temporary metal deposition and patterning
9. TEMP METAL MEASUREMENTS
10. Temporary metal removal and cleaning
11. Final metal deposition, patterning and sintering
12. Passivation deposition and patterning
13. Final baking if necessary

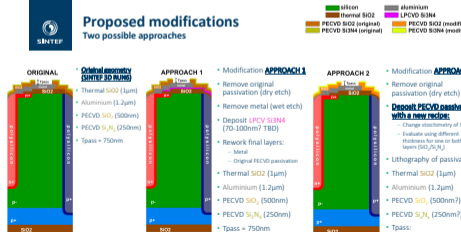
→ 40 main steps / to months of net processing

Production Runs

- First wafers from Run-6 was delivered to ATLAS beginning of 2022. Up to **70 %** good die per wafer.
- Residual stress imbalance has caused some doubts and delays in downstream processing, successful mitigation under way.
- Runs 7 & 8 are currently in progress, ETA end 2024



Proposed modifications
Two possible approaches



ORIGINAL (Original geometry SINTEF 3D RUN6)

- Thermal SiO₂ (1µm)
- Aluminium (1.2µm)
- PECVD SiO₂ (500nm)
- PECVD Si₃N₄ (250nm)
- Tpass = 750nm

APPROACH 1

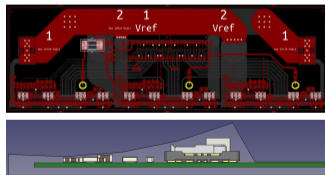
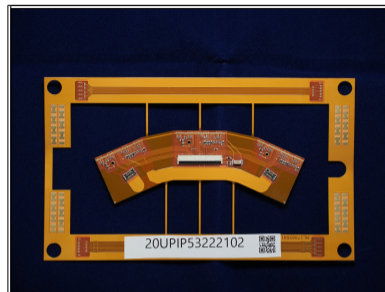
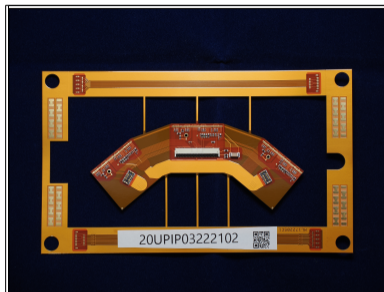
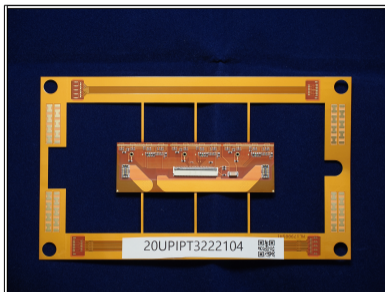
- Modification **APPROACH 1**
- Remove original passivation (dry etch)
- Remove metal (wet etch)
- Deposit LPCVD Si₃N₄ (70-100nm? TBD)
- Rework final layers:
 - Metal
 - Original PECVD passivation
- Thermal SiO₂ (1µm)
- Aluminium (1.2µm)
- PECVD SiO₂ (500nm)
- PECVD Si₃N₄ (250nm)
- Tpass = 750nm

APPROACH 2

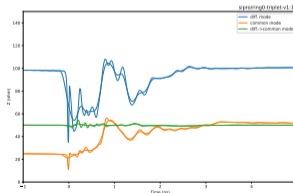
- Modification **APPROACH 2**
- Remove original passivation (dry etch)
- Deposit PECVD passivation with a new recipe:
 - Change stoichiometry of Si₃N₄
 - Evaluate using different thickness for one or both layers (SiO₂, Si₃N₄)
- Lithography of passivation
- Thermal SiO₂ (1µm)
- Aluminium (1.2µm)
- PECVD SiO₂ (500nm?)
- PECVD Si₃N₄ (250nm?)
- Tpass:
 - TARGET = 750nm
 - Might require different thickness

M. Povoli et al. TREDI 2022

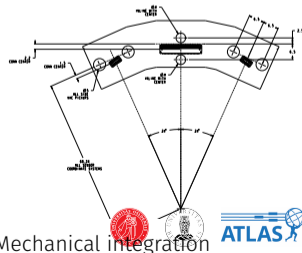
Triplet Flex-Hybrid Design and Manufacture



Detector envelope



Signal integrity



Mechanical integration

Precision Assembly

Triplet Assembly

Pick and place (Zevac Onyx32)

- Survey the triplet face-down in jig with cut-outs (inlay)
- Glue application by stamping at each chip location
- Bare modules picked and surveyed using custom tool (bridge)
- Each module held in place below bridge during glue cure

