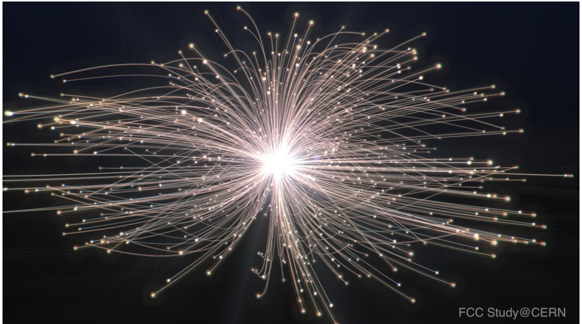
Performance of the IDEA vertex detector in fullsim and ultra-light vertex detector concept

FCC Detector Concept meeting

Armin Ilg

University of Zürich

03.06.2024



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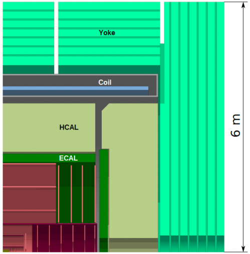
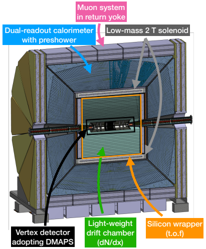
FUTURE CIRCULAR COLLIDER

FCC-ee detector *concepts*



CLD: CLIC-Like Detector [1, 2].

- ILC → CLIC → FCC-ee (→ μCol)
- Si vertexing and tracking
- Highly-granular ECAL and HCAL, CALICE-like
- Solenoid coil outside calorimeter system



IDEA: Innovative Detector for e^+e^- Accelerators [3, 4].

- Si vertexing
- Drift chamber (down to 1.6% X/X0, $\mathrm{d}N_{\mathrm{ion.}}/\mathrm{d}x$)
- Si wrapper with timing
- Dual-readout calorimeter with preshower
- Solenoid coil inside calorimeter system

ALLEGRO: A Lepton coLLider Experiment with highly GRanular calorimetry Read-Out (M. Aleksa).

- Si vertexing and drift chamber
- Highly granular noble liquid ECAL, Pb/W+LAr or W+LKr
- ECAL and solenoid coil in same cryostat
- CALICE-like or TileCal-like HCAL

FCC-ee detector *concepts*

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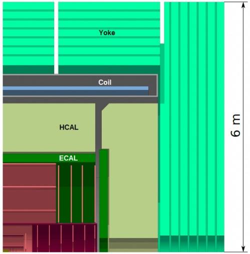

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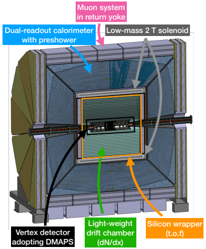

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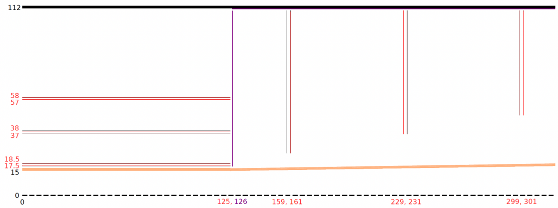
FCC-ee vertex detector layouts

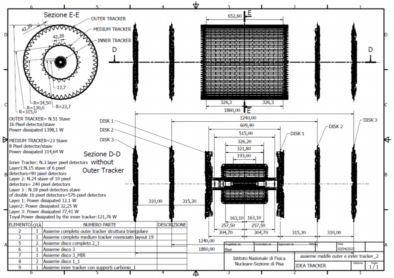
CLD → Rescaled CLICDet vertex detector



arXiv:1911.12230

- $r_{\text{min}} = 13\,\text{mm}$, vertex system until $r = 112\,\text{mm}$, $z = 300\,\text{mm}$
- Three double-layer barrel layers and disks
- No engineering studies since CLICDet developments

IDEA → New vertex detector layout



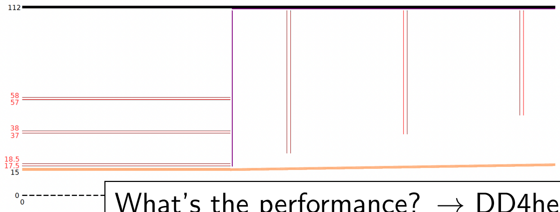
F. Palla , see talk at FCC US week at BNL

- $r_{\text{min}} = 13.7\,\text{mm}$, vertex system until $r = 315\,\text{mm}$, $z = 930\,\text{mm}$
- Three single-layer barrel layers
- Two outer barrel layers and three disks
- Engineered design, integrated into MDI

FCC-ee vertex detector layouts

University of Zurich[UZH]

CLD → Rescaled CLICDet vertex detector



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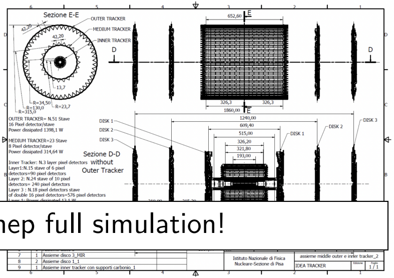

What's the performance? → DD4hep/Key4hep full simulation!

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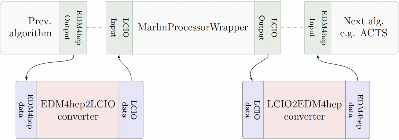
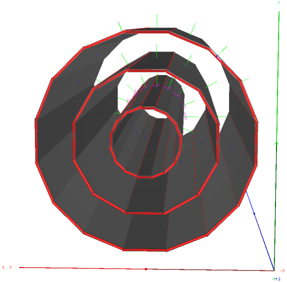
Detector model in k4geo

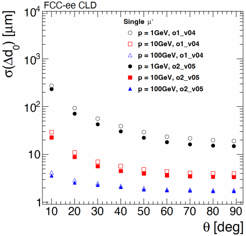
- Linear collider reconstruction (iLCSoft/CLICPerformance)
- Can generate EDM4hep output using k4MarlinWrapper



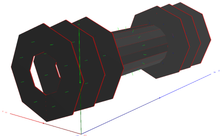
Access to all LC tools: PandoraPFA, LCFI+, etc.



CLD vertex barrel

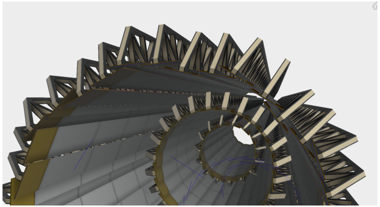


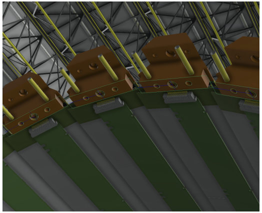
Updated CLD vertex (G. Sadowski, 7th FCC Physics Workshop)

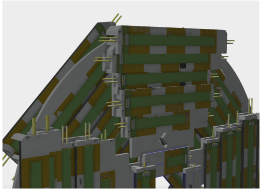


CLD endcap and vertex barrel

Vertex detector by INFN Pisa (more details in F. Palla's talk at 2nd FCC US Workshop), support tube by INFN-LNF, holding lumical, vertex and beam pipe (more on MDI in M. Boscolo's talk)

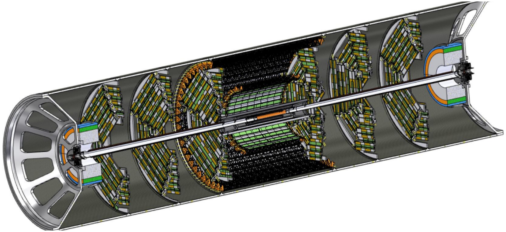






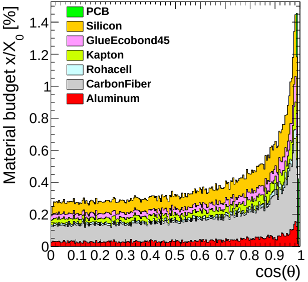
Vertex outer barrel and vertex disks using quad ATLASPix3 DMAPS with $150 \times 50\,\mu\text{m}^2$ pixels, water-cooled

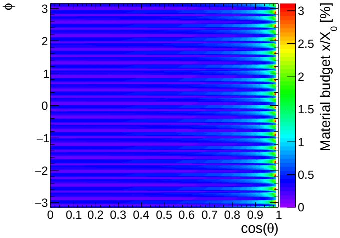
Vertex inner barrel consisting of staves of dual ARCADIA DMAPS, with pixels of $25{\times}25\,\mu\text{m}^2$ ($\sim 3\,\mu\text{m}$ single point resolution), air-cooled



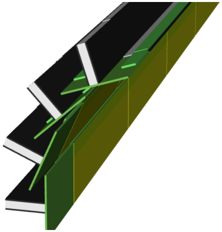
Vertex inner barrel

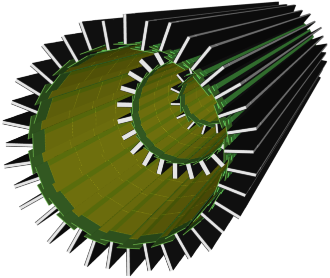
- $r_{\text{min}} = 13.7\,\text{mm}$, 2 mm to beam pipe (can we go closer?)
- Correct material stack, flexes, end-of-stave hybrid, insensitive sensor areas (2 mm)
- Proxy volume for stave holding structure
- Support structure CAD model can be imported (more details in backup), service cones missing
- Material budget in line with 0.3% per layer at $\cos(\theta) = 0$ (CDR assumption)





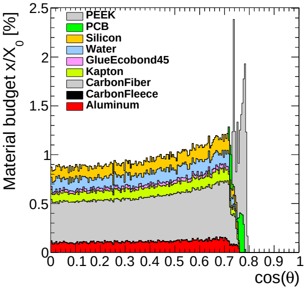
First layer

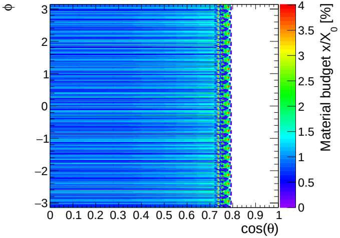




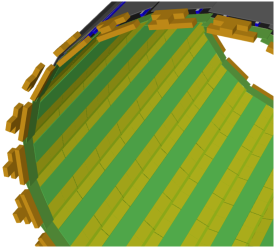
Vertex inner barrel, without support

- Correct material stack, correct description of ATLASPix3 insensitive peripheries
- Proxy volumes for truss structure and cooling pipes
- Proxy volume for end-of-stave holder (orange, material budget contribution optimised with F. Palla)
  - → Still significant contribution

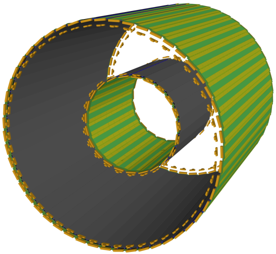




Complete outer barrel



Middle tracker



Complete vertex outer barrel system

Vertex disks

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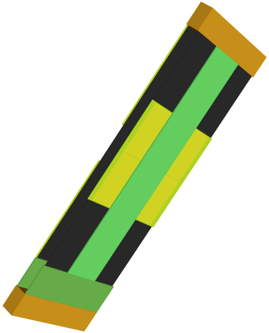
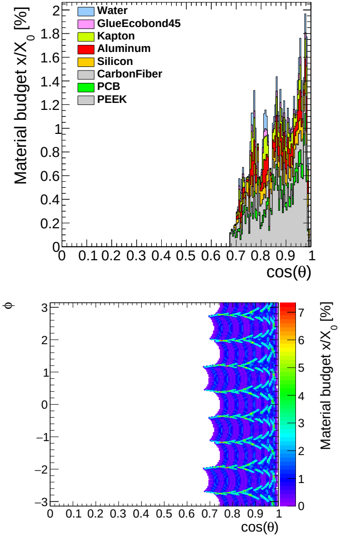
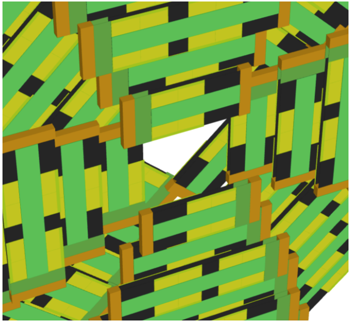
- Correct placement of all modules in r and z
- Missing vertex disk global support
- Very uneven x/X_0 distribution



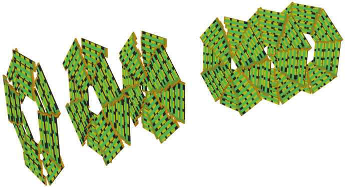
One short stave



Disk 0



Disk 0 zoom-in



Complete vertex disks system

Complete system

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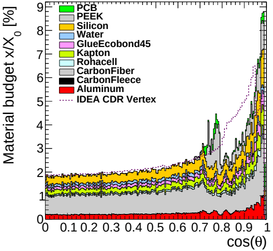
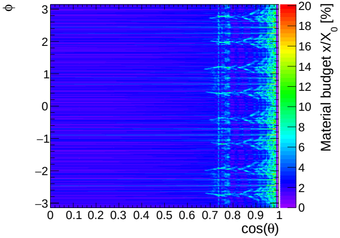
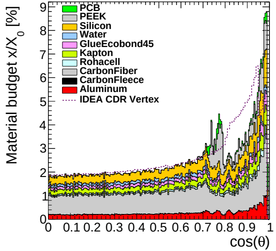


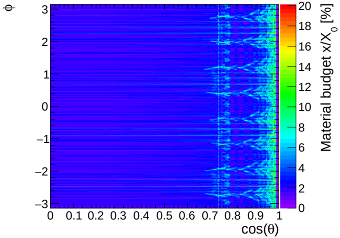


Complete vertex system

- Material budget comparable with CDR estimate
- Will make the updated version available soon
- Plan to include last missing volumes using DDCAD
- Look at all material budget evaluations as a lower limit, there's always gonna be more added! (e.g off-detector cabling)
- No drift chamber tracking available yet $\rightarrow$ instead use CLD and iLCSoft reconstruction

Complete system





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- Look at all material budget evaluations as a lower limit, there's always gonna be more added! (e.g off-detector cabling)
- No drift chamber tracking available yet → instead use CLD and iLCSoft reconstruction
  - Frankenstein approach: Remove CLD vertex detector (and a couple of Inner Tracker layers and disks) and instead insert IDEA vertex, run CLD full simulation
  - Let's have a first look!

CLD with IDEA vertex detector

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Necessary changes

- Removing first Inner Tracker barrel layer ($r = 127\,\text{mm}$)
- Removing first and second Inner Tracker disks ($r = 79.5$ and $123.5\,\text{mm}$)
- Increase conformal tracking max. distance (CT_MAX_DIST)
- *MinClustersOnTrack* from 4 to 3 in conformal tracking in vertex barrel and disks

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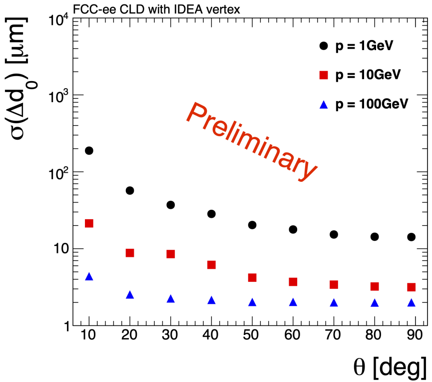
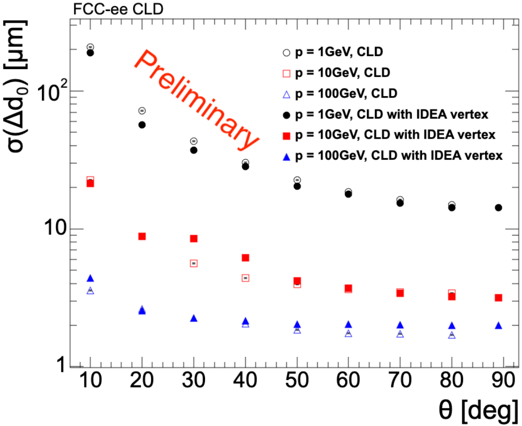


Nota bene

- No silicon wrapper
- Assume spatial resolution of $3\,\mu$m for vertex inner barrel (same as CLD), and $14\,\mu\text{m} \times 43\,\mu$m for outer barrel and disks (CLD: vertex endcap: $3\,\mu$m, inner tracker endcap: $5\,\mu$m or $7 \times 90\,\mu$m)

Comparison between CLD and IDEA vertex



IDEA vertex better at lower momenta, CLD vertex better at high momenta
→ Makes sense as CLD uses double layers (with double the material budget)

Note: $\theta = 89^\circ$ points missing for CLD

Other, preliminary, results in backup

Sensor-only vertex detector

DMAPS in 65 nm TPSCo process

- More logic per cm^2
- Lower power consumption $\rightarrow$ Air cooling
- Enables 12" wafers $\rightarrow$ Wafer-scale bent sensors!

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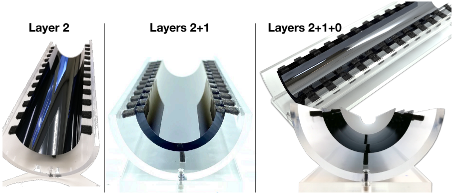
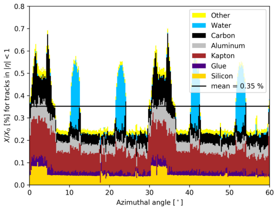
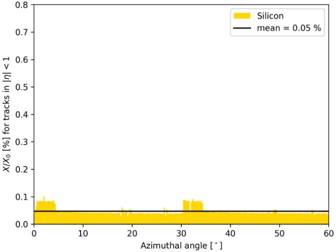
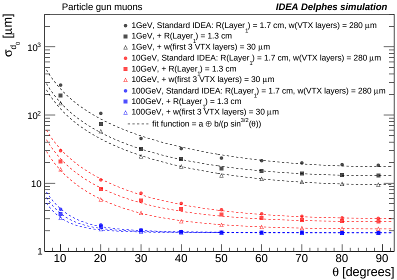


Layer assembly concept for ALICE ITS3 [5]





Material budget in ALICE ITS2 (left, [6]) and silicon only (M. Mager)



L. Freitag (BSc. thesis [7])

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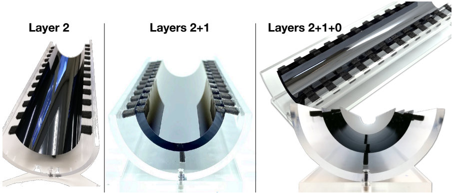

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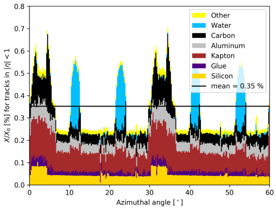

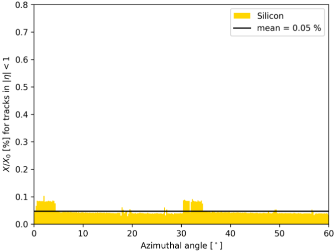

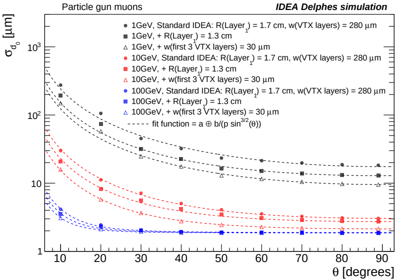

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L. Freitag (BSc. thesis [7])

How can such a vertex detector be realised at FCC-ee? → See also here

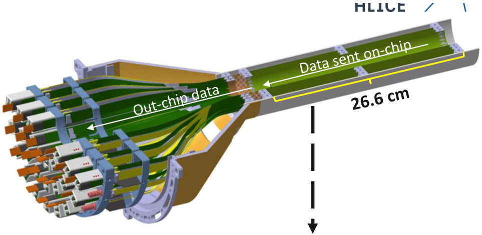
ALICE ITS3 layout

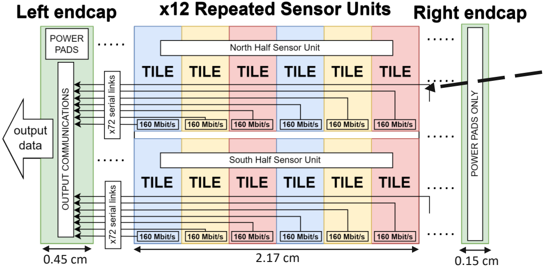
University of Zurich[UZH]

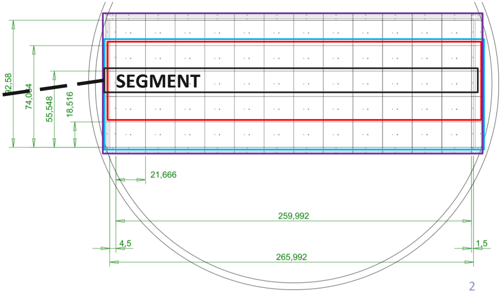
ITS3
- Wafer-scale Monolithic Active Pixel Sensors (**MAPS**)
- Cylindrical sensors of radii 18/24/30 mm

Architecture requirements (**Stitching**)
- Dies divided into 3,4 or 5 **Segments**
  - **2 endcaps** on the edges
  - **12 Repeated Sensor Units** (RSU)
    - *12 tiles per RSU*

Data transfer on-chip to the left edge (26.6 cm)

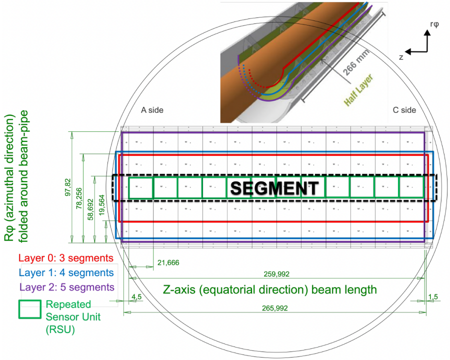






M. Rodriguez @ TWEPP 2023

- First layer at smaller radius, from 18 to 13.7 mm
  - → Mechanically okay, electrically to be demonstrated
  - → First layer to use just two segments to reach smaller radius
- ITS3 readout only in one direction → We want to measure forward-backward asymmetries extremely precisely
  - → Read and power from both sides where possible
- ITS3 doesn't care too much about forward coverage → We do. down to $\theta = 140\,\text{mrad}$
  - → Need to find solution for 3rd and 4th layer! → Multiple wafer-scale sensors in a row in z
  - → Ensure flexes, cables, etc. are not in front of lumical
- ITS3 doesn't care too much about hermeticity → We do.
  - → Cannot overlap multiple staves/ladders as in ATLAS/CMS
  - → Evaluate impact of only $\sim 95\%$ coverage per layer (chip service region and gap between sensors)
  - → Increase number of layers from 3 to 4 to ensure at least three hits

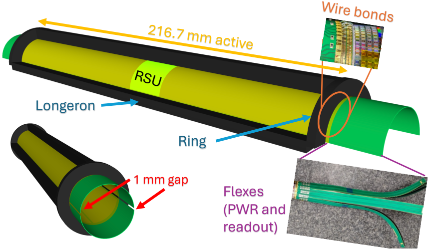


Layer 1 and 2

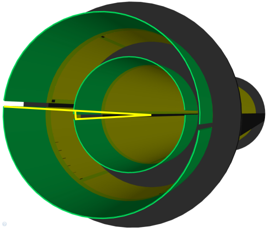
- Coverage down to 125 mrad (155 mrad) for layer 1 (layer 2)
- Gap of 1.25 mm between half-barrels, layer 2 rotated in ϕ to avoid overlap with layer 1
- Readout and power from both sides

Layer 3 and 4

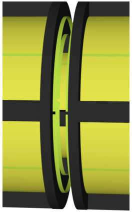
- Two sensors per side, readout only on sides, power on sides and center (power wire)
- Asymmetric design: 8 (10) RSUs on +z (-z) side for layer 3, inverted for layer 4, to cover gap at $z = 0$ (not yet in DD4hep model)



Layer 1 layout



Layer 1+2



$z =$ region with layer 3 and 4, without asymmetric design

First material budget evaluation (preliminary!)

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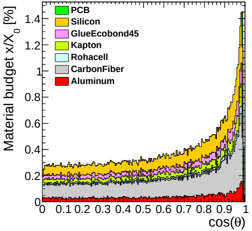
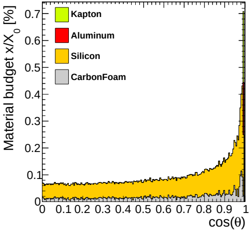
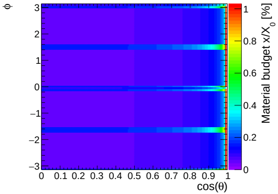
Layer 1 (classic vertex)



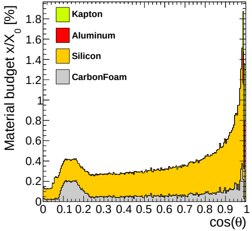
Ultra-light layer 1



Ultra-light layer 1 ($cos(\theta)$ vs. ϕ)



Ultra-light layer 1–4



Material budget reduction of ~ 5, uniform distribution in ϕ except for longeron locations

Incoherent pair production in vertex detector

The problem is incoherent pair production in first vertex layer

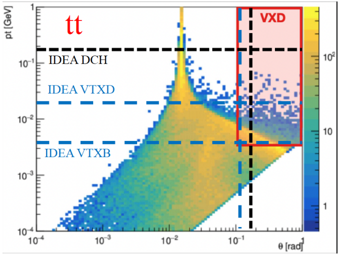
Table 2: Number of pairs produced per bunch crossing (BX) at the four working points, and maximum occupancy measured in the barrel and endcaps of the vertex detector and tracker (respectively VXDB, VXDE, TRKB, TRKE).

		Z	WW	ZH	$t\bar{t}$
1	Pairs/BX	1300	1800	2700	3300
10^{-6}	O_{max}(VXDB)	70	280	410	1150
10^{-6}	O_{max}(VXDE)	23	95	140	220
10^{-6}	O_{max}(TRKB)	9	20	38	40
10^{-6}	O_{max}(TRKE)	110	150	230	290

In 2019, in CLD vertex, a maximal occupancy of 70×10^{-6} per bunch crossing was found using GuineaPig simulation

- Assuming cluster size of 5, safety factor of 3
- $25 \times 25\,\mu m^2$ pixels

→ Doesn't seem like a lot, but assuming bunch spacing of 20 ns at Z pole, results in $560\,MHz/cm^2$



A. Ciarma

Incoherent pair production in vertex detector

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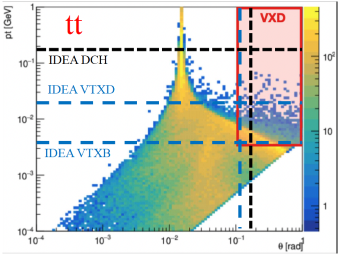
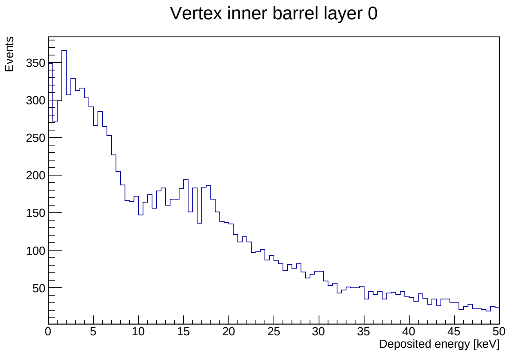


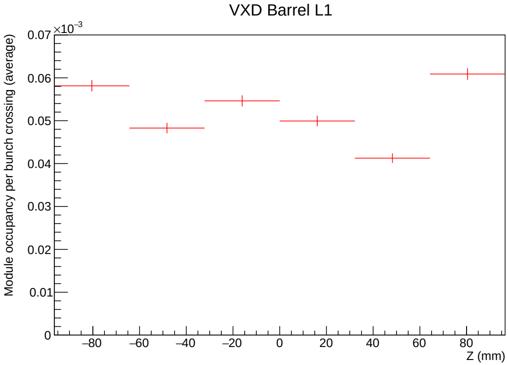
A. Ciarma

What is the situation in IDEA vertex detector?

Occupancies in IDEA vertex detector

- First layer at $r = 13.7\,\mathrm{mm}$
- Cut at $1.8\,\mathrm{keV}$, equivalent to 500 electrons
- GuineaPig files from A. Ciarma with incoherent pair production from 100 bunch crossings





Data rate in IDEA vertex detector

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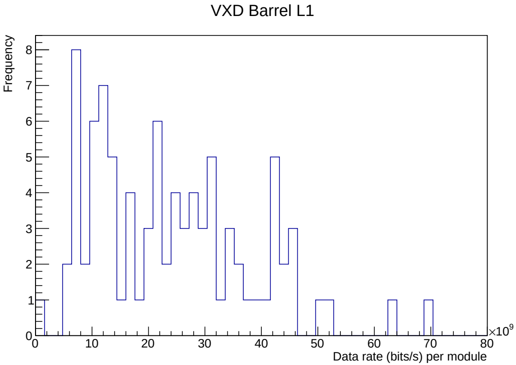
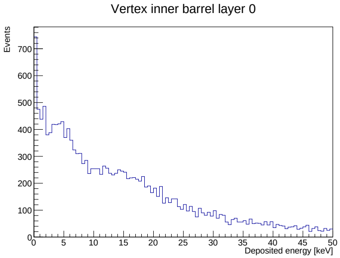
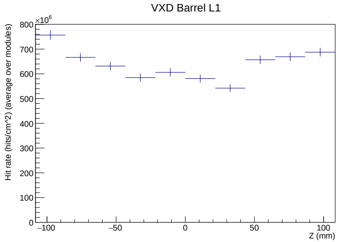
- Without trigger: Assume 32 bits transferred per pixel (10+8 needed for ARCADIA)

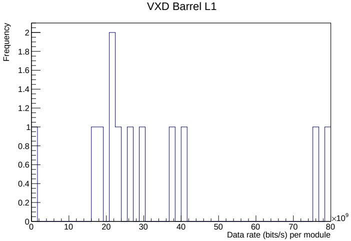


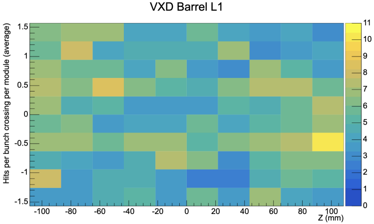
- Need more stats to get better estimate on maximal occupancy and data rates (will rerun with 4000 BCs using V23 lattice) → Update for FCC Week
- Recall safety factor of 3, cluster size of 5
  - → Triggerless readout seems neither impossible nor straightforward
  - → Interplay with sensor development: Large charge sharing to improve resolution or low charge sharing to reduce readout rate?

Occupancies in ultra-light IDEA vertex detector









- More occupancy in very forward region (coverage down to 125 mrad)
- Recall that 1 RSU is around twice the size of 1 ARCADIA module

→ Again need for higher statistics

Conclusions

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IDEA vertex

- Reasonable d_0 performance of IDEA vertex using CLD detector and reconstruction
- Some additions such as cones for air cooling and cables needed, but outside of acceptance

Ultra-light vertex detector concept

- Conceptual design, adapted from ALICE ITS3 to FCC-ee
- Compromise hermeticity (or radius of first hit) with reduced material budget
- Need to add new sensitive surface to DD4hep (cylinder segment) to estimate vertexing performance using CLD reconstruction

Incoherent pair production background in IDEA vertex

- Comparable results to previous estimation in CLD vertex
- Further studies needed
  - → What is the impact of an increased threshold on physics?
  - → Can part of the background be cut away on-detector e.g. using cluster size? (need silicon digitisation with clustering algorithm in Key4hep)

Thanks!

[1] N. Bacchetta, et al., *CLD – A Detector Concept for the FCC-ee*, arXiv:1911.12230 [physics.ins-det].

[2] D. Dannheim, et al., *CERN Yellow Reports: Monographs, Vol 1 (2019): Detector Technologies for CLIC*, tech. rep., 2019.

[3] IDEA Collaboration, G. F. Tassielli, *A proposal of a drift chamber for the IDEA experiment for a future e^+e^- collider*, in *Proceedings of 40th International Conference on High Energy physics — PoS(ICHEP2020)*. Sissa Medialab, Feb., 2021.

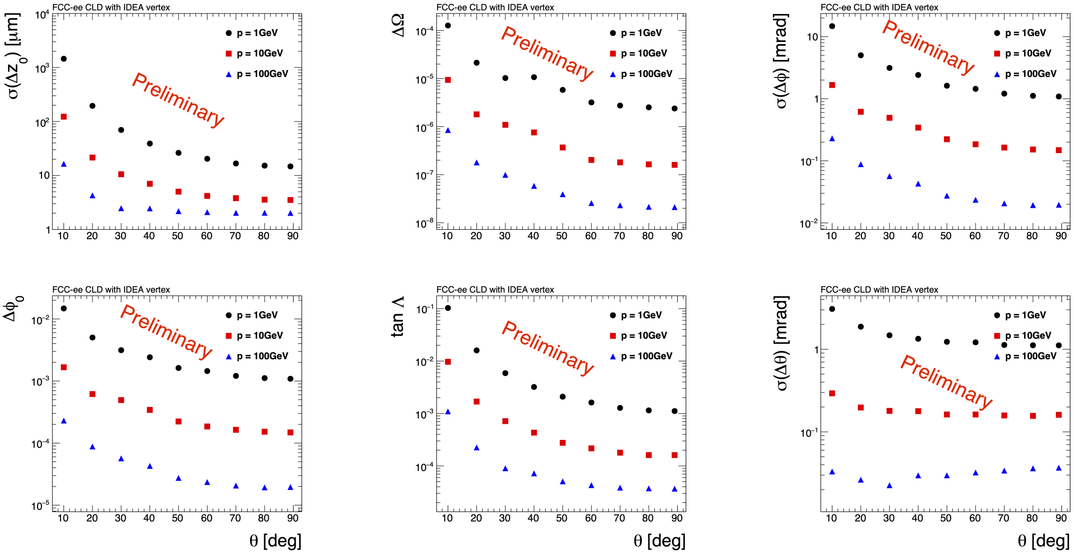
[4] FCC Collaboration, *FCC-ee: The Lepton Collider*, The European Physical Journal Special Topics **228** (2019) 261–623.

[5] M. Mager, *On the "bendable" ALPIDE-inspired MAPS in 65 nm technology*, 11, 2021. https://indico.ihep.ac.cn/event/14938/session/6/contribution/196. 2021 International Workshop on High Energy Circular Electron Positron Collider.

[6] F. Reidt, *Upgrading the Inner Tracking System and the Time Projection Chamber of ALICE*, Nuclear Physics A **1005** (2021) 121793.

[7] L. Freitag, *Benefits of Minimizing the Vertex Detector Material Budget at the FCC-ee*, 2023. http://cds.cern.ch/record/2851362. BSc thesis, presented 01 Feb 2023.

Further performance plots



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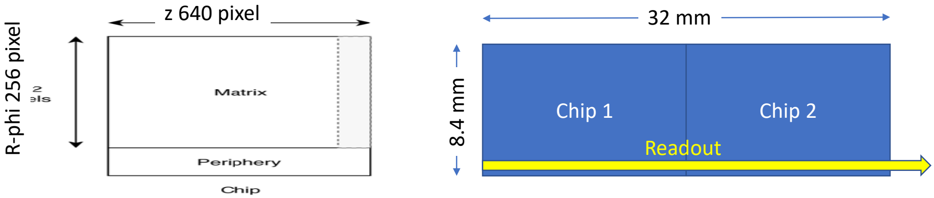
Istituto Nazionale di Fisica Nucleare

Module concept inspired by ARCADIA INFN R&D

- Depleted Monolithic Active Pixel Detectors (DMAPS) sensor and back-side processing already tested on silicon
- Pixel size 25x25 μm^2, 50 μm thick
- Active area 640 pixel (16 mm) in z and 256 pixels (6.4 mm) in $r - \varphi$
- Chip periphery plus an inactive zone: total of 2 mm in $r - \varphi$
- Chips are side-abuttable in z

Composed of 2 pixelated parts: total of 8.4 mm $(r - \varphi)$ × 32 mm (z)

- Power budget not established yet: assume (reasonably) $50\ \mathrm{mW/cm^2}$



F. Palla , see talk at FCC US week at BNL

Outer tracker module

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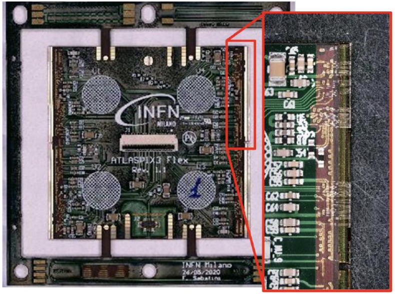
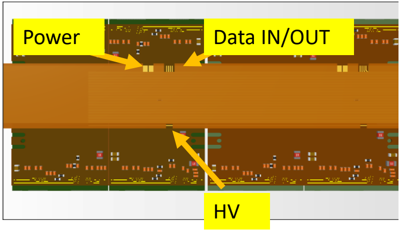
- Based on ATLASPIX3 R&D
  - DMAPS
  - 50 x 150 μm^2
  - Up to 1.28 Gb/s downlink
  - TSI 180 nm process
  - 132 columns of 372 pixels

  - Active (total) length (r-phi x z)
    - 18.6 (21) mm x 19.8 (20.2) mm
  - Module is made of 2x2 chips – total length:
    - size 42.2 mm x 40.6 mm

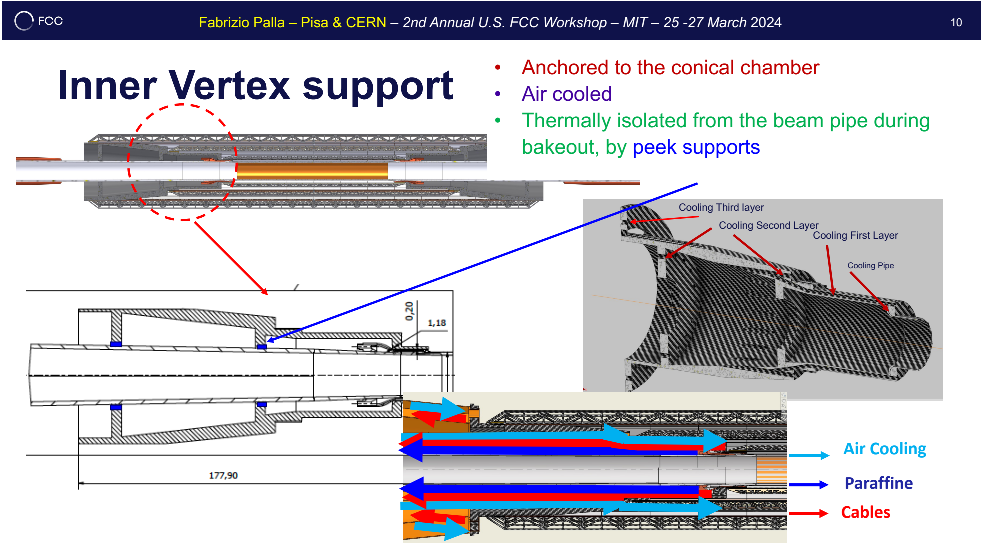
  - Power budget not established yet:
    assume $100\ \mathrm{mW/cm^2}$



o Nazionale di Fisica Nucleare



F. Palla , see talk at FCC US week at BNL



F. Palla, 2nd FCC US Workshop

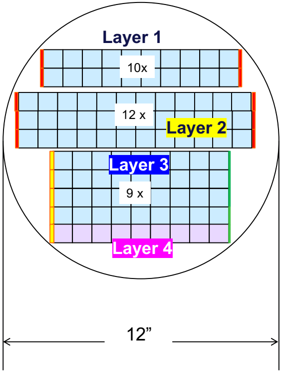
Data rates issues *(see F. Bedeschi talk at 7th FCC Workshop)*

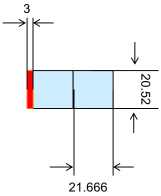
- **Largest data rates occur at the Z energy**
- **Expected data rates per BX/module [cluster size 5]**
  - From machine backgrounds (Incoherent pair creation – safety factor of 3) ~ 19 hits/BX/module
  - From collisions (200 kHz) ~ average ~<1 hit/BX/module
- **Inner layer ~400 MHz/cm^2 → ~25 Gb/s per module**
  - might be reduced if cluster size is only 2 – as measured for many MAPS
  - *ALICE3 hit rate ~100 MHz/cm^2 (pixel size 10μm x 10μm)*
  - 2nd layer ~10x less data volume
- **Triggered readout**: for 200 kHz the data bandwidth per module, rate is only 150 Mb/s
  - Impact on physics?

- **All these depend on pixel pitch, thickness, R/O architecture, bias voltage.**
  - For a review see M. Winter talk at March 11 meeting

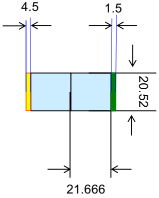
F. Palla, 2nd FCC US Workshop

Same reticle for all layers





Layer 1&2



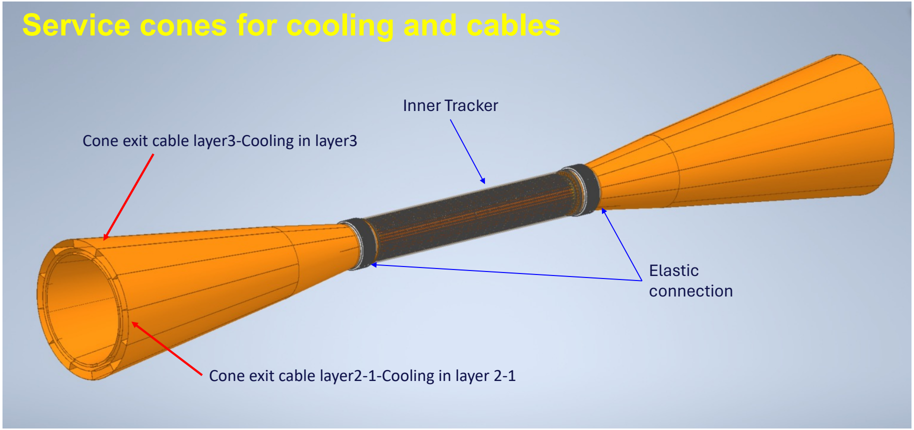
Layer 3&4

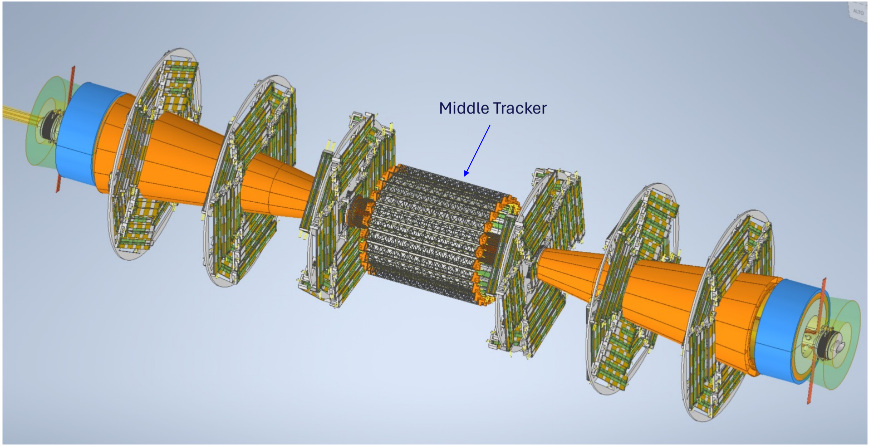
Layer	Radius (mm)
1	13.7
2	20.23
3	26.76
4	33.3

	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Power dissipation in ITS3
(not necessarily the same for FCC-ee)

- RSU~ 50 mW/cm^2 (depends on Temp.)
- LEC ~ 700 mW/cm^2


Service cones for cooling and cables
Inner Tracker
Cone exit cable layer3-Cooling in layer3
Elastic connection
Cone exit cable layer2-1-Cooling in layer 2-1


Middle Tracker

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- First layer at smaller radius, from 18 to 13.7 mm
  - → Mechanically okay, electrically to be demonstrated
  - → First layer to use just two segments to reach smaller radius
    - Assuming same RSU size (= reticle size of CMOS process of given silicon foundry) of $19.564 \times 21.666\,\text{mm}^2$ (in $r - \phi \times z$) then radius would be 12.77 mm.
    - Can consider more complex approach using *edge* reticle pieces to reach any desired radius for the first layer
  - → Assume perfect reticle size in $r - \phi$ of 21.02 mm to get to $r = 13.7$ mm for the first layer

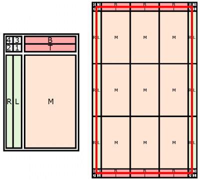
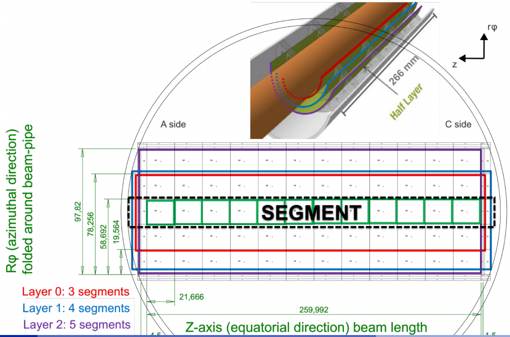
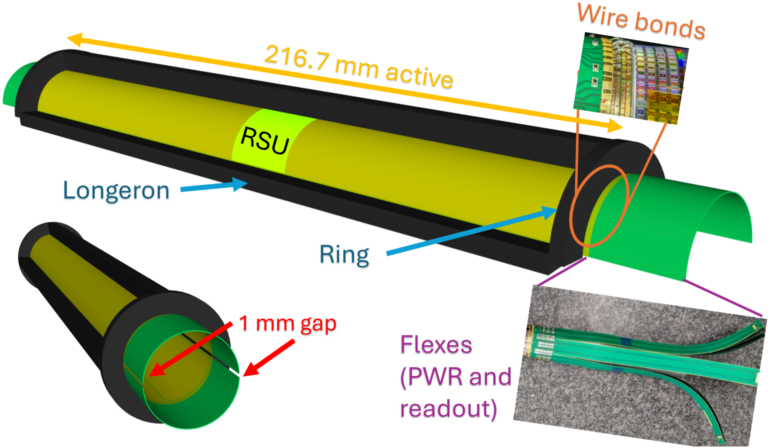


Figure 3.32: Principles of stitching. Left: design reticle with sub-frames (M, B, T, R, L, 1-4. Right: exposures on the wafer and resulting circuits (not to scale).



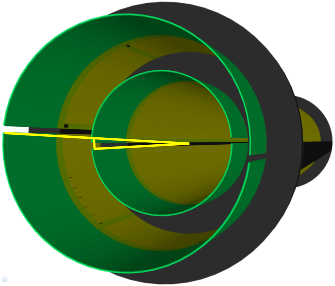
Layer 1

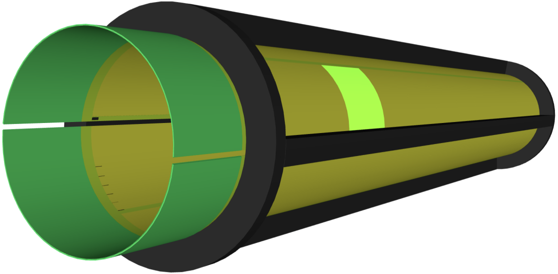
- 10 RSUs and 2 ECs long, $\theta_{\text{min}} = 125.8\,\text{mrad}$, $|cos(\theta)| < 0.992$ (106.35 mrad assuming 20 mm flex)
- Two half-barrels two segments wide each, 1 mm gap, readout and power from both sides



Layer 2

- 12 RSUs long (limit given 12 inch wafer size), at $r = 20.39\,\text{mm}$
- Coverage down to $\theta_{\text{min}} = 155.58\,\text{mrad}$, $|cos(\theta)| < 0.991$
- Rotated in ϕ by 8° to avoid overlap with layer 1
- Could slightly twist sensor to minimise gaps in coverage e.g. at $z = 0$, in-between RSUs





Layer 3

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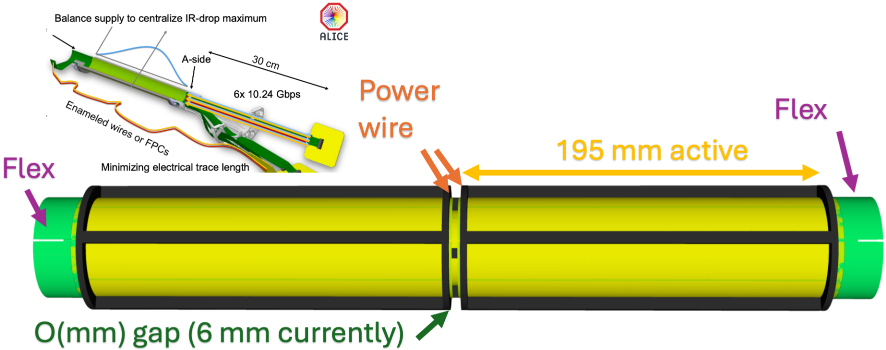
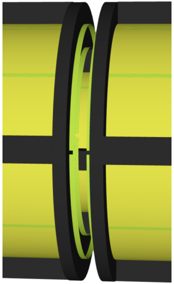
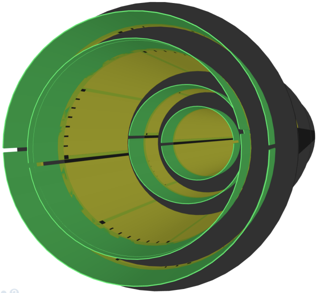
- $r = 27.08\,\text{mm}$, two sensors per side, with 9 RSUs each
- Coverage down to $\theta_{\text{min}} = 135.93\,\text{mrad}$, $|cos(\theta)| < 0.991$
- Readout on sides, power on sides and center (power wire)



Layer 4

- Same length as layer 3, sensors are five RSUs wide, at $r = 33.77\,\text{mm}$
  - Simpler mechanical assembly given same length of layer 3 and 4 (sacrificing forward coverage)
- Coverage down to $\theta_{\text{min}} = 168.94\,\text{mrad}$, $|cos(\theta)| < 0.986$
- Gap at $z = 0$ could be mitigated by having asymmetric design with sensors with 10 and 8 RSUs on the $z > 0$ and $z < 0$ sides respectively





The common software vision: Key4hep

Key4hep is a huge ecosystem of software packages adopted by all future collider projects, complete workflow from generator to analysis

- Event data model: EDM4hep for exchange among framework components
  - Podio as underlying tool, for different collision environments
  - Including truth information
- Data processing framework: Gaudi
- Geometry description: DD4hep, ability to include CAD files
- Package manager: Spack: `source /cvmfs/sw.hsf.org/Key4hep/setup.sh`