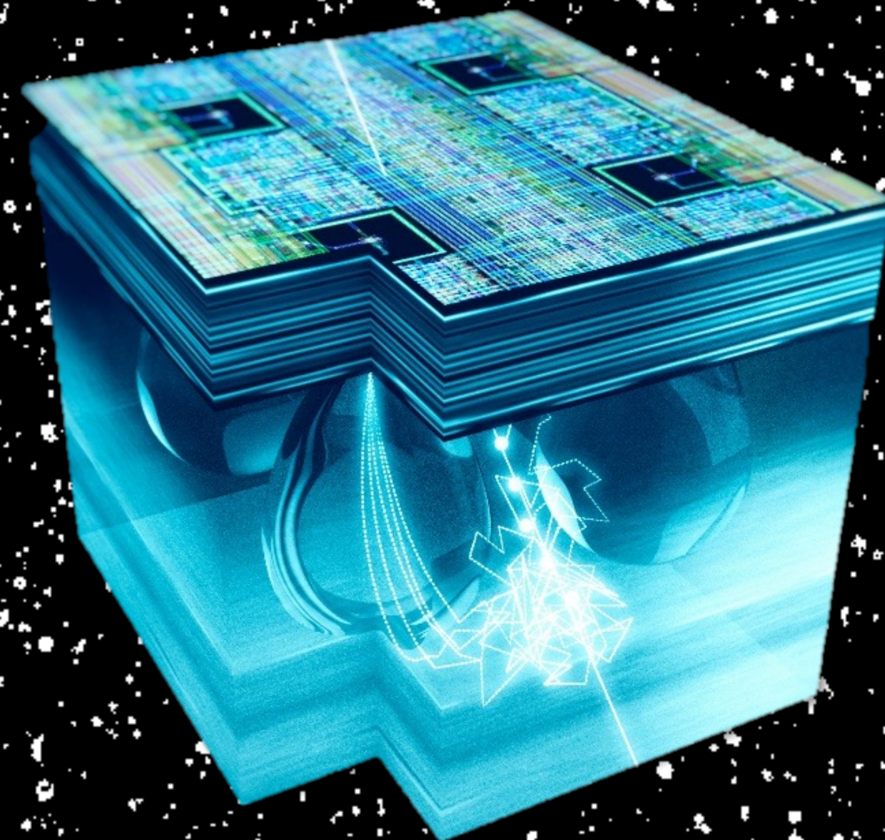
Evolution of MAPS technologies (for HEP !)



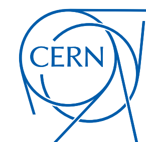
ALPIDE prototype: 200 MeV protons at PSI

Walter Snoeys

Many thanks to colleagues from CERN, the ALICE ITS2 and ITS3 upgrade, ATLAS Itk, WP1.2, …

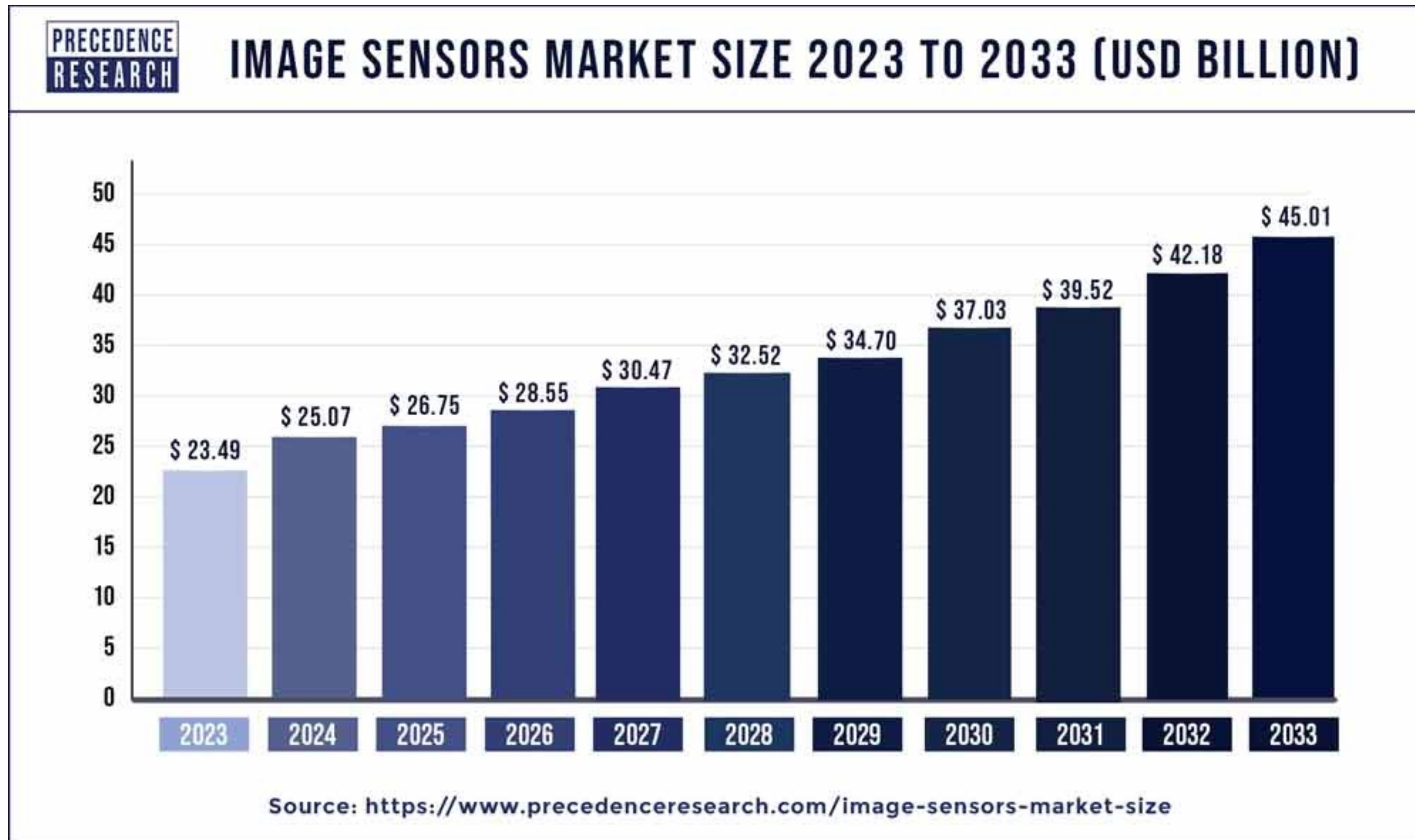
FCC-EE, CERN, July 1st 2024

walter.snoeys@cern.ch



Imaging technology market

- 23.9B USD in 2023, expected to reach 45B USD by 2033
- Global Semiconductor market valued at 611.35B USD in 2023, projected to grow from 681.05B in 2024 to 2062.59B by 2032 (Fortune Business Insights), driven by Artificial Intelligence, IoT, …



CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

… and now CMOS MAPS make their way in High Energy Physics !

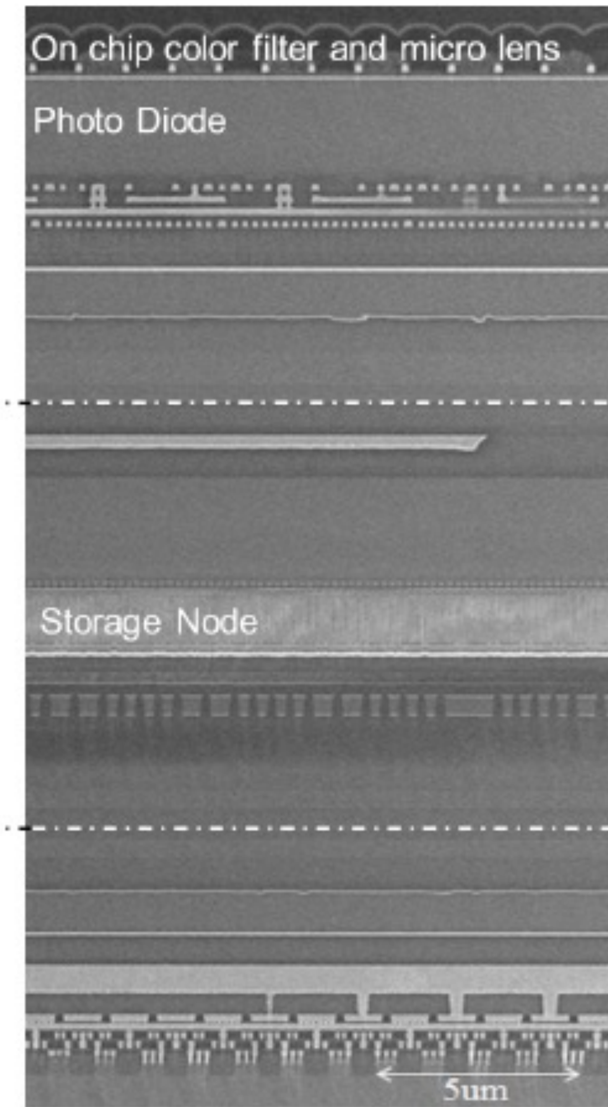
Hybrid still in majority in presently installed systems

Wafer stacking now offered by several foundries !

Top part (BI-CIS process technology)

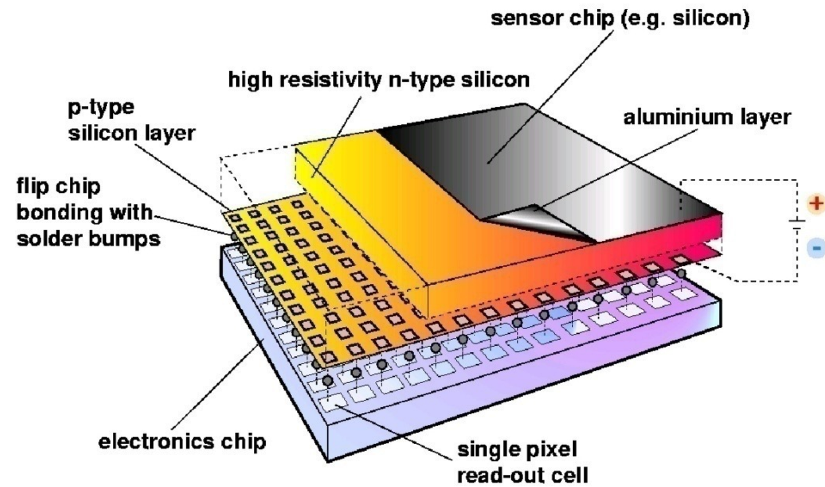
Middle part (DRAM process technology)

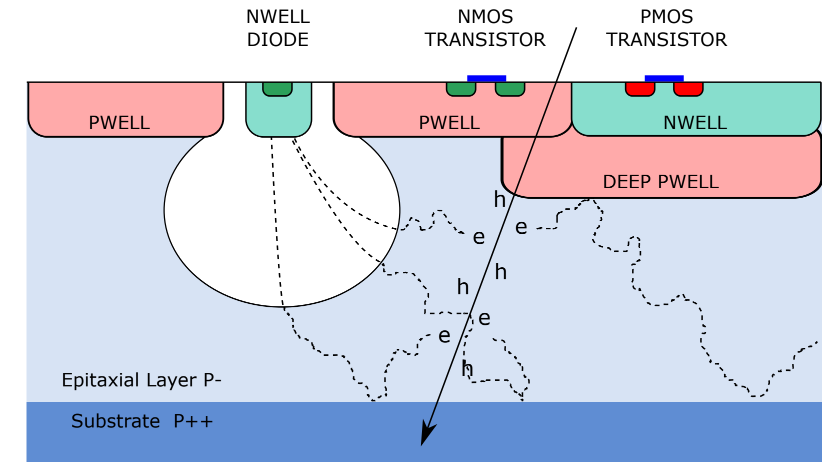
Bottom part (Logic process technology)



Sony, ISSCC 2017

Hybrid vs Monolithic





Hybrid

- Large majority of presently installed systems
- 100 % fill factor easily obtained
- Sensor and ASIC can be optimized separately
- Spin-off from HEP developments:

  for example spectral photon counting chips in this workshop

Monolithic

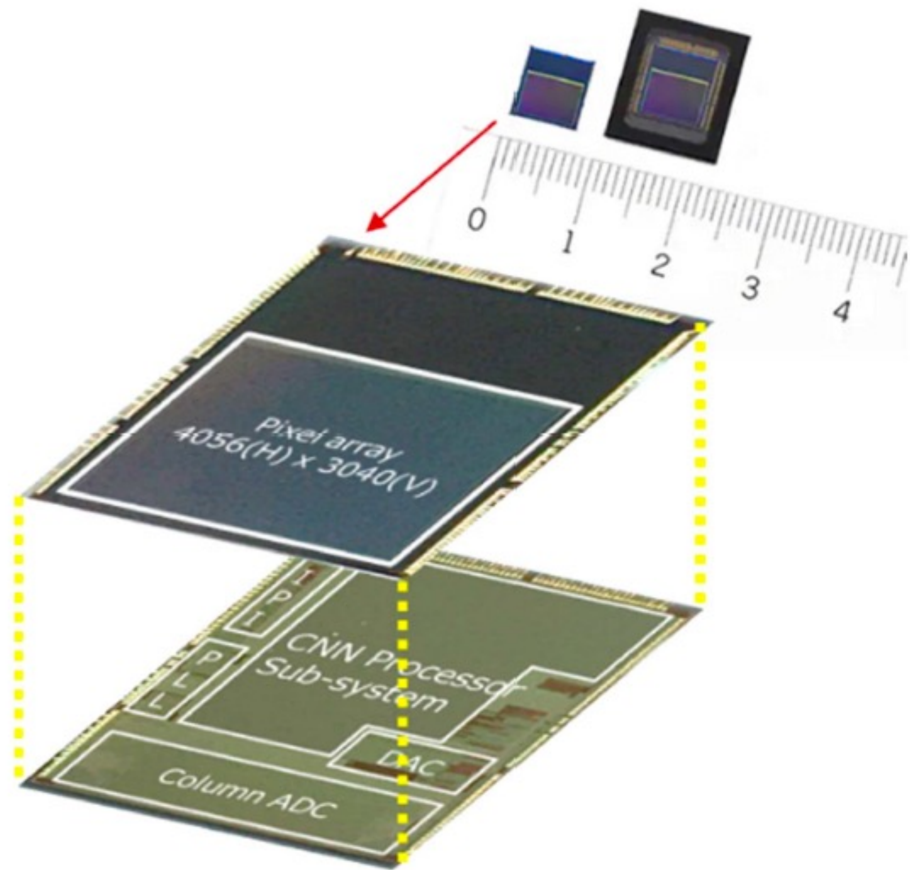
- Easier integration, lower cost
- Potentially better power-performance ratio and strong impact on material budget

Motivation for intense R&D since more than 30 years

- Trend towards more standard technologies

New technologies (TSV's, microbumps, wafer stacking…) make the distinction between hybrid and monotlithic more vague.

Sony: Intelligent Vision Sensor and Edge Computing Envisage the Future



Fabrication Process		Top chip 65nm / Bottom chip 22nm
Chip size		7.558mm(H) x 8.206mm(V)
Number of effective pixels		4056(H) x 3040(V)
Image size		Diagonal 7.857 mm
Pixel size		1.55μm(H) x 1.55μm(V)
Supply voltage		Pixel and Analog 2.6V/Interface 1.7V/Logic 0.8V
Input clock		12~27MHz
Output I/F	Option1	MIPI(CSI-2) 4 lane DPHY 2.1Gbps/lane
	Option2	SPI 35Mbps
DSP	Number of MACs	2304MACs
	Peak Power efficiency	4.97TOPS/W
	Processor Clock	262.5MHz
Sensor Readout time	12.3M[4056(H)x3040(V)]	16.52msec
	3.1M [2028(H)x1520(V)]	5.52msec
Power consumption	12.3M[4056(H)x3040(V)] 30fps	278.8mW
	3.1M [2028(H)x1520(V)] 120fps	379.1mW
Image output format	Sensor	Bayer RAW
	Input tensor	RGB or YUV

Fig. 1 A photo of the intelligent vision sensor in stacked architecture with a pixel chip and a logic chip.

- Stacked device with neural network for image recognition
- Discusses different architectures of Neural Networks for this application, outperforms traditional imagers for image recognition.

Omnivision: A 2.2 µm 2-Layer Stacked HDR Voltage Domain Global Shutter CMOS Image Sensor with Dual Conversion gain and 1.2 e- FPN (IEDM 2023 40.2)

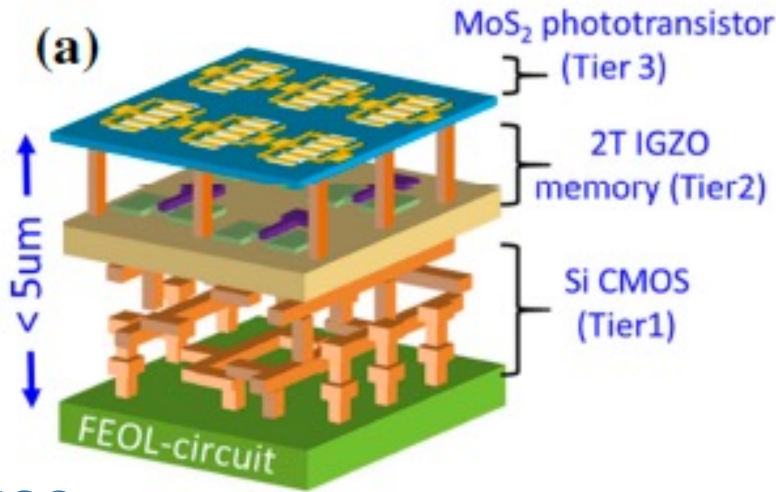
	This work	IISW 2023 [4]	IEDM 2019 [3]	IEDM 2022 [5]	ISSCC 2019 [6]	ISSCC 2020 [7]	IISW 2019 [8]
Pixel pitch	2.2 µm	3.45 µm	2.2 µm	1.8 µm	2.7 µm	2.3 µm	4.0 µm
C-mode / V-mode	V-mode	V-mode	V-mode	V-mode	V-mode	V-mode	V-mode
Resolution	1280x400	5M	1280x1024	1280x1024	1080x1280	1280x800	-
Number of storage Capacitors per pitch	4	4	2	2	2	2	4
Frame Rate	60fps	60 fps	120 fps	120 fps	120 fps	120 fps	-
FWC	11k e- @ LCG	20k e- @ LCG	12k e- @ LCG	14k e- @LCG	10k e-	12k e- @LCG	40k e- @LCG
Effective Shutter efficiency @940nm	>100dB	>100dB	>100dB	130dB	86dB	85dB	140dB
RN	3.8 e- @ HCG	2.7 e- @ DCG	3.1 e- @ HCG	1.8 e- @ HCG	3.5 e-	2.1 e- @HCG	5 e- @ HCG
FPN	1.2 e- @ HCG	1.4 e- @ DCG	1.7 e-	-	-	-	4.2 e- @ HCG
QE @940nm	38%	41%	38%	-	36%	42%	-
DR	85dB	90dB	71.74dB	77.8dB	110dB	75dB	102dB
SNR Tran	24dB	26dB	-	-	-	-	-

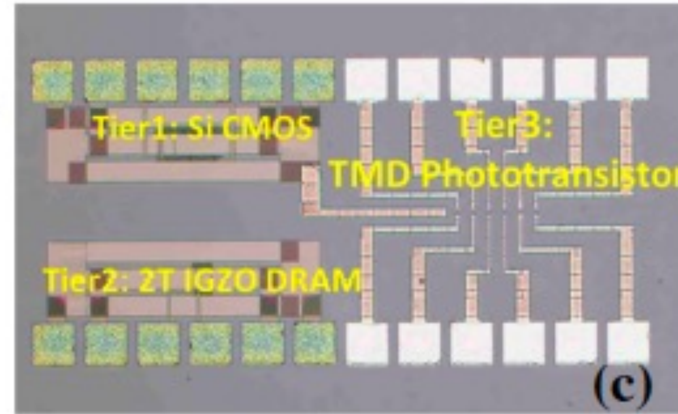
- Very small pixel for High Dynamic Range
- Sensor wafer and readout wafer

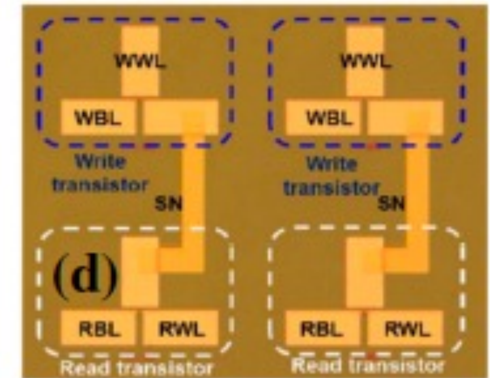
TSMC: 3D Monolithically Integrated Device of Si CMOS Logic, IGZO DRAM-like, and 2D MoS_2 Phototransistor for Smart Image Sensing 33.2

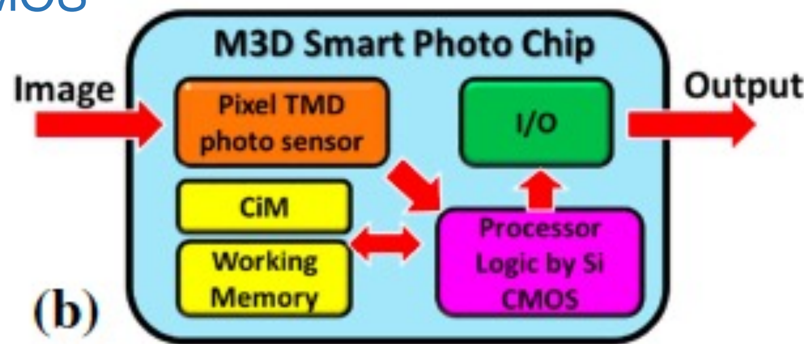
IEDM 2023

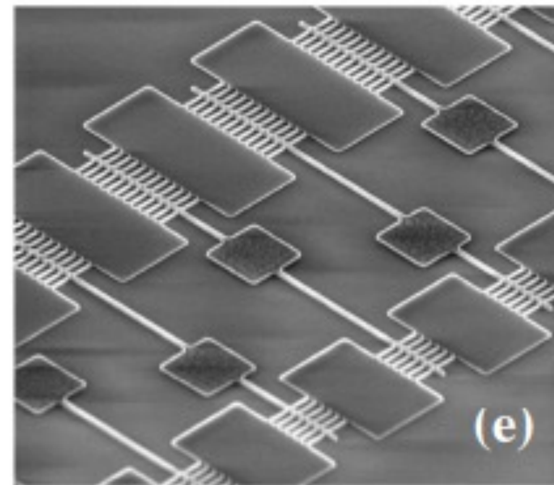
- 3 tiers
- Finfet in CMOS











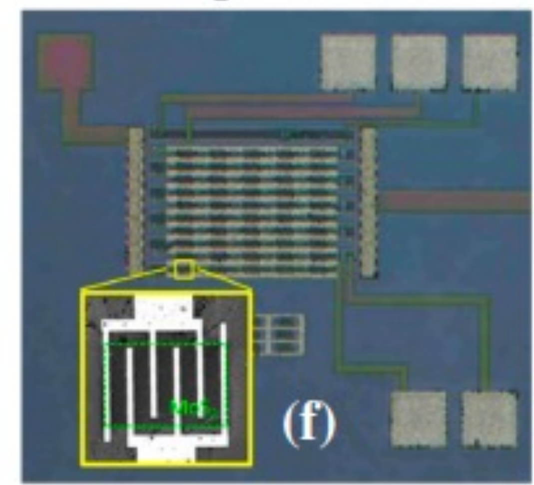
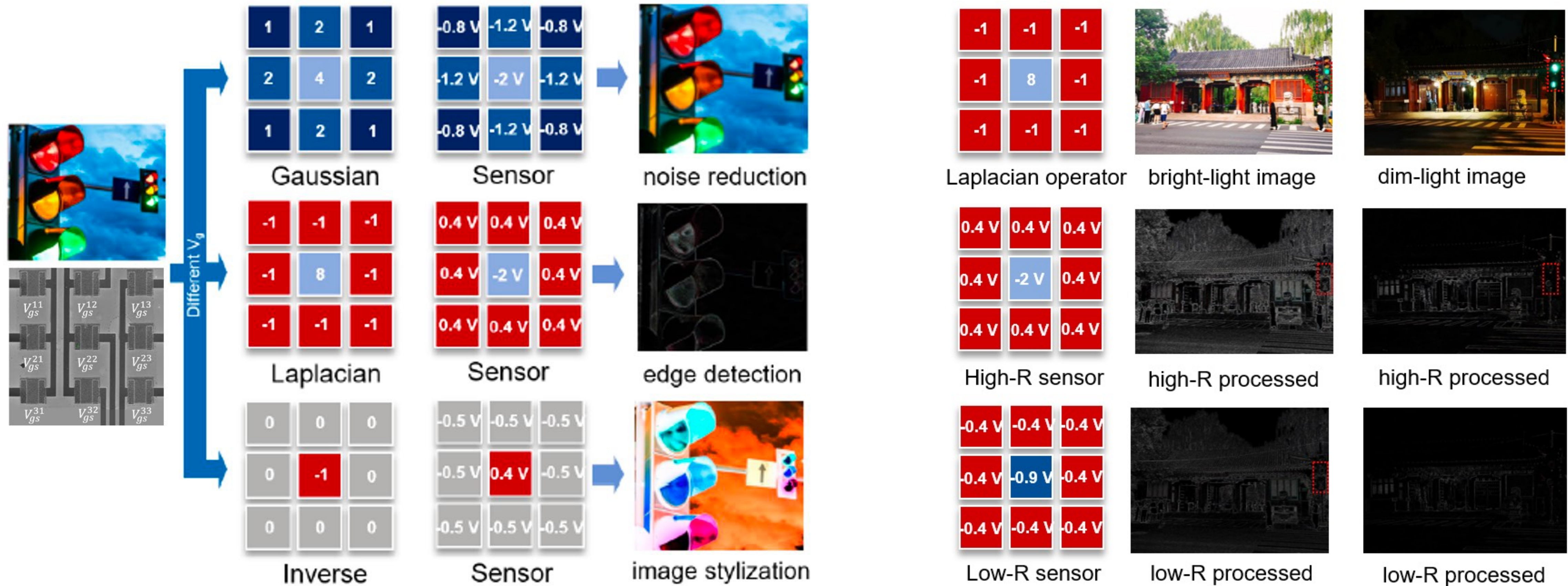


Fig 1. Illustration of a three-tier monolithic 3D image sensor enabled by low thermal budget sequential process and its data flow for smar image sensor application, as shown in (a) and (b), respectively. (c) Top view of the three-tier devices. (d) the bottom 20nm technology nod multi-fin FinFET circuit, (e) the middle 2T0C IGZO DRAM-like, and (f) the top monolayer MoS_2 phototransistor array with 5x5 cells.

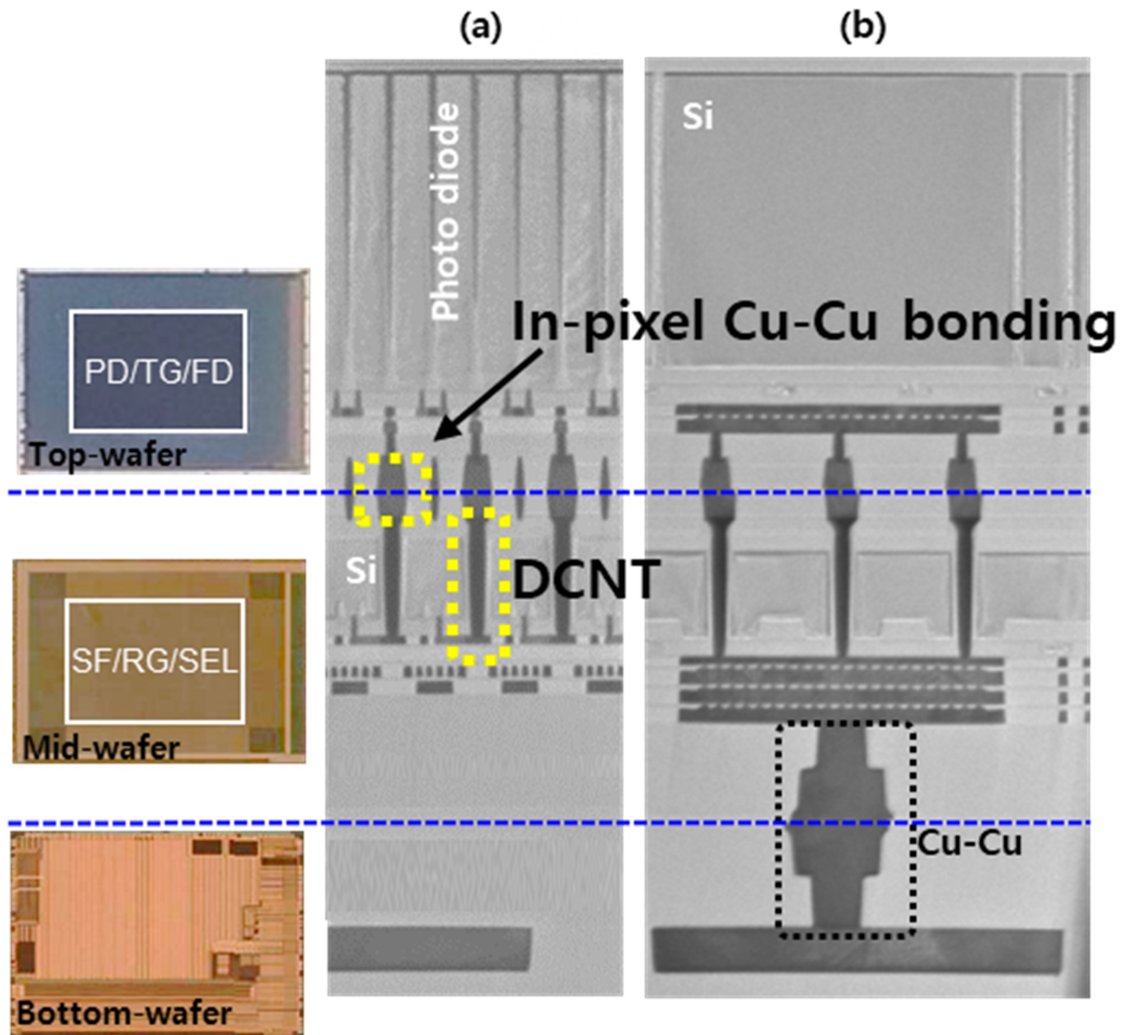
Peking University: Ultrasensitive Retinomorphic Dim-light Vision with In-Sensor Convolutional Processing Based on Reconfigurable Perovskite Bi_2O_2Se Heterotransistors 33.3

IEDM 2023



- Can modulate the photo-responsitivity with voltage, and can use this for convolution operations and in-sensor compute, for applications like noise-reduction, edge detection and other purposes.

Samsung: A 0.5 µm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-pixel Cu-Cu Bonding 40.1 IEDM 2023



- Top tier Photo diode and Transmission Gate
- Middle tier in-pixel transistors
- Bottom Analog and digital CMOS

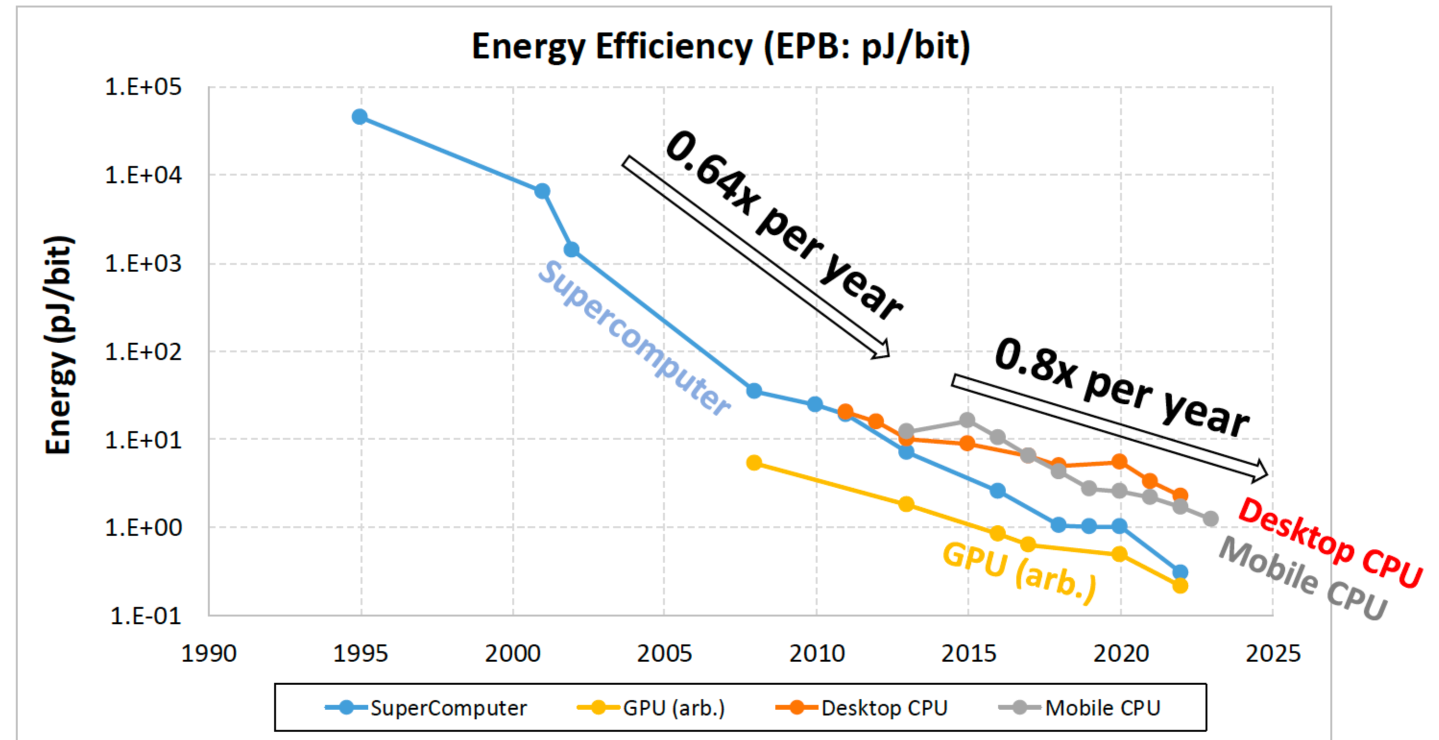
- (a) Pixel array (b) periphery

Wafer stacking and Artificial Intelligence more and more widespread in commercial imaging !

CMOS Imaging technologies vs mainstream technologies

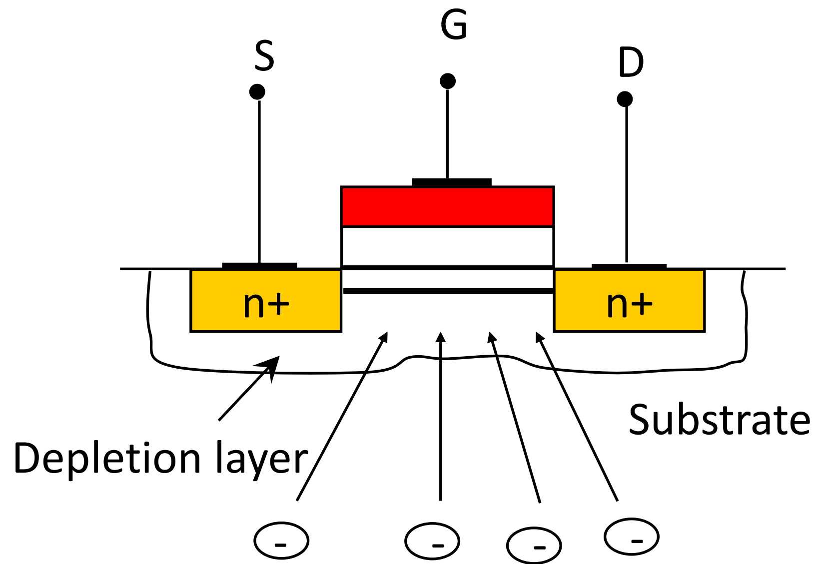
- Wafer stacking well established in commercial imaging sensors
- Artificial Intelligence enters for enhanced performance and in sensor compute

- How about mainstream technologies ? (we do not necessarily need an imaging technology…)
  - Pushed by computing needs for artificial intelligence.
  - Computing enhancement power limited
  - Needs addressed by:
    - Transistors
    - On-chip interconnect
    - Heterogeneous integration
    - In-memory compute



Jie Deng Qualcomm
IEDM 2023

Transistor: traditional



G
S
D
n+
n+
Depletion layer
Substrate

Linear region (low VDS)

For a sufficiently positive gate voltage, electrons are attracted to the SiO2-Si interface => conductive layer (channel) is formed (P-substrate gets inverted locally). The channel which links source and drain, forms a resistor between the two. Current increases with increasing VDS.

Saturation region (high VDS)

Significant current flow and resistive drop in the channel. Electrons near the drain are insufficiently attracted by the gate, and the channel gets pinched off. Beyond that point increasing VDS does/should not change current significantly.

However, for very small gate length and conventional transistors, drain-induced barrier lowering has to be avoided, or coupling of the drain voltage into the channel-region near the source.

In Finfet and Gate All Around this effect is much better suppressed.

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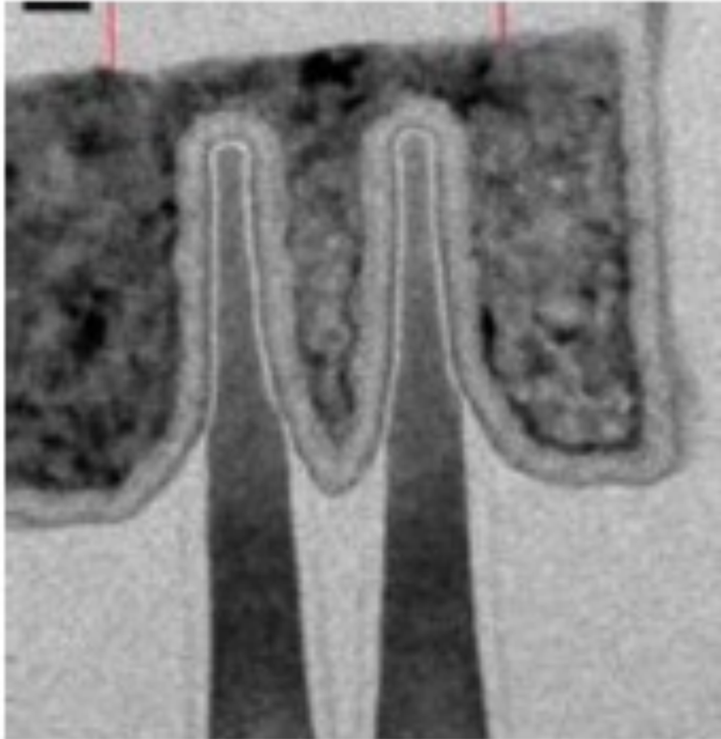
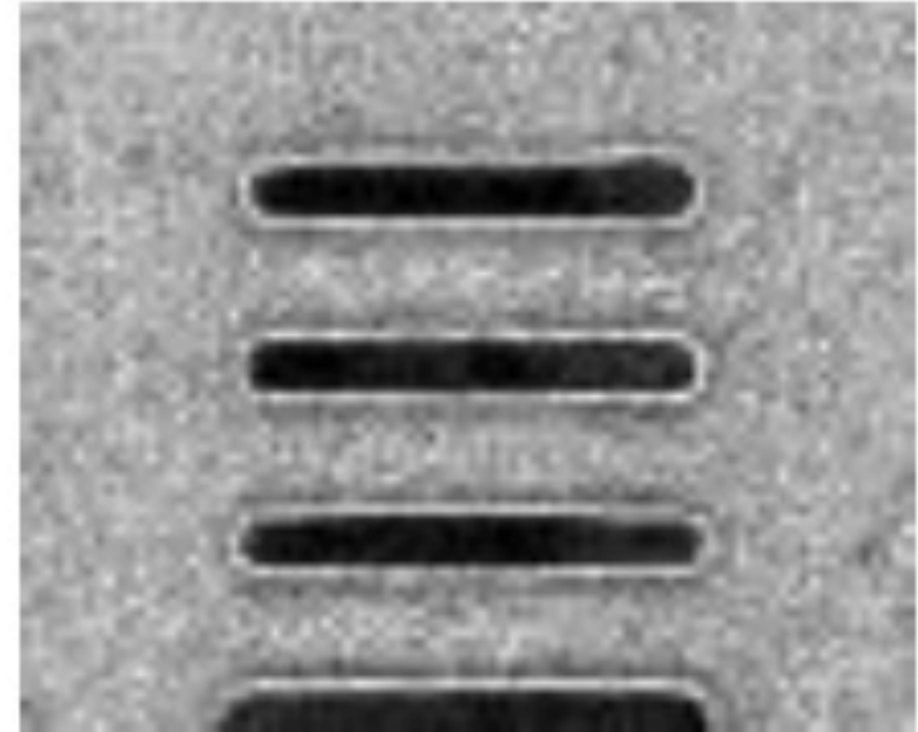
Transistor: Finfet and Gate All Around Transistor



Finfet: INTEL

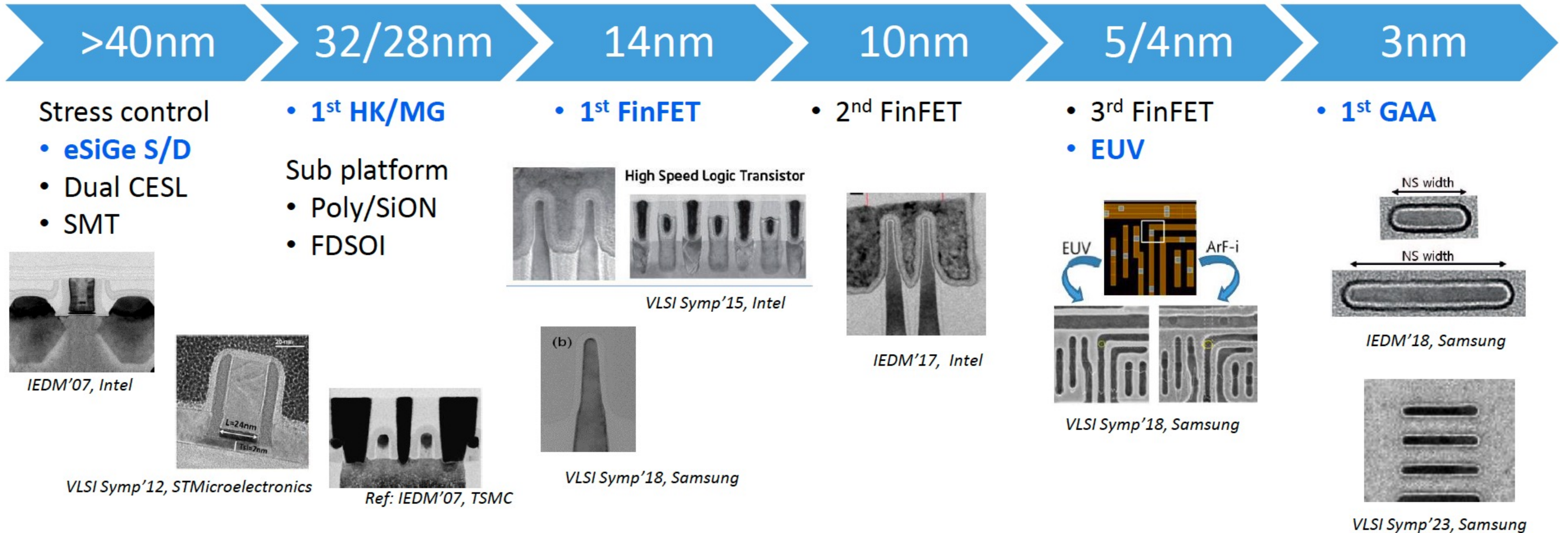


Gate All Around : SAMSUNG

In Finfet and Gate All Around bulk volume suppressed, much better electrostatics, much lower Drain Induced Barrier Lowering (DIBL). GAA superior to Finfet.

Transistor : more revolutionary innovation steps than in interconnect

- Performance and Power improvement with Area Scaling continues through innovation in Structure/Process/Material/Equipment, etc.



IEDM'07, Intel

VLSI Symp'12, STMicroelectronics

Ref: IEDM'07, TSMC

VLSI Symp'15, Intel

VLSI Symp'18, Samsung

IEDM'17, Intel

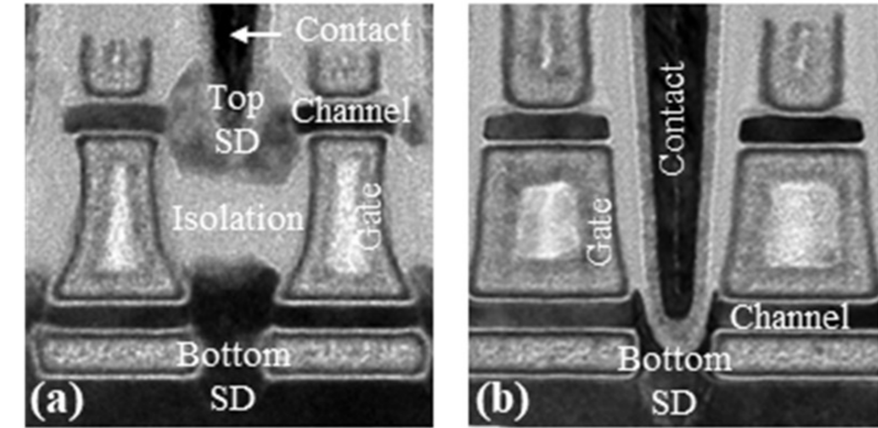
VLSI Symp'18, Samsung

IEDM'18, Samsung

VLSI Symp'23, Samsung

Transistor: Finfet is running out of steam, replaced by Gate All Around

- Gate All Around (GAA) faster, more current drive, and more uniform
- All major players are moving to GAA, eg IEDM 2023
- Even moving to stacked nanosheet and PMOS and NMOS



Samsung 29.4
Stacked NMOS and PMOS

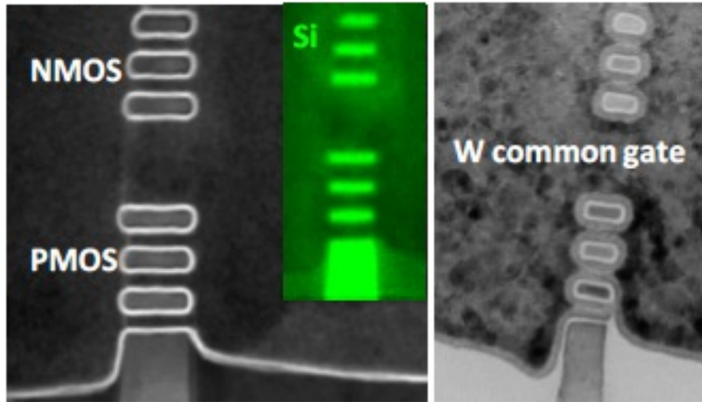
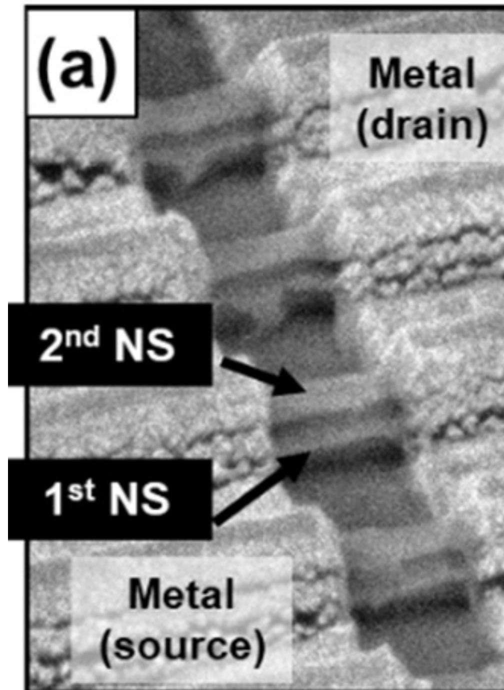


Fig. 5. TEM micrograph shows CFET device after ribbon release on the left demonstrating capable process despite high aspect ratio. TEM micrograph on the right is captured after common-gate fill and polish, showing that the gates of top n-MOS and bottom p-MOS are connected.

Intel 29.2



TSMC 2.1
Channel width 50 nm

	(001) GAA Si NS	(110) GAA Si NS
LC (L_g = 80 nm)		
SC (L_g = 15 nm)		

IBM research 2.5

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Intel: Process innovations for future technology nodes with back side power delivery network and 3D device stacking. 19.1 IEDM 2023

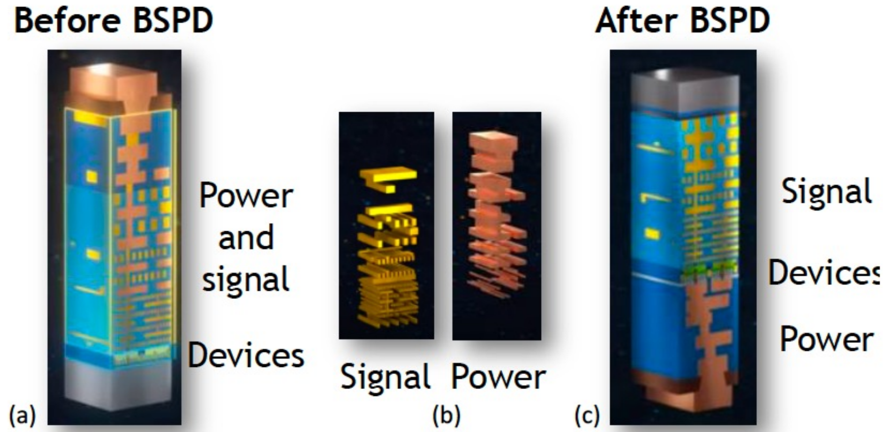


Fig. 1. Schematic diagram showing device layer and interconnect stacks. (a) Case without BSPD. (b) Illustration of usage of wires for signaling and ower delivery. (c) Case with BSPD.

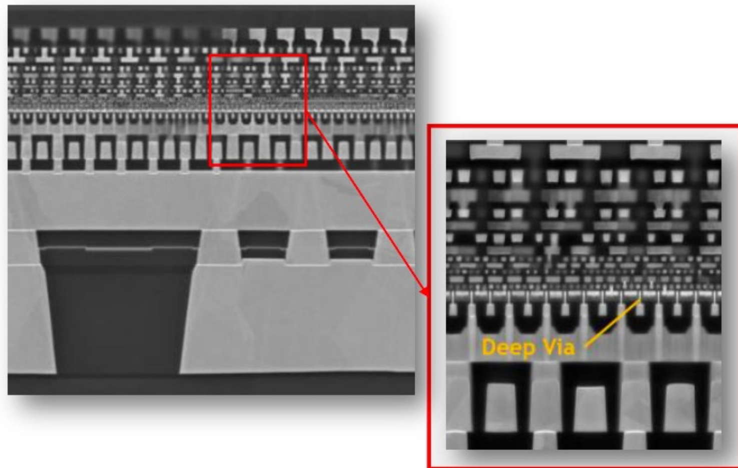


Fig. 2. Cross sectional image of Intel 4 + PowerVia process [1].

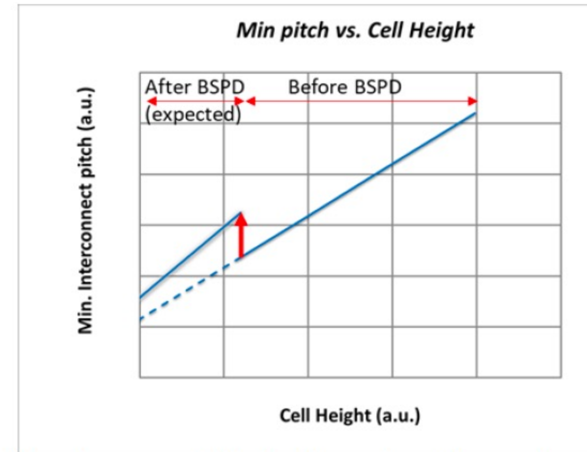


Fig. 5. Relation between Cell Height and minimum interconnect pitch, showing the expected effect of implementation of BSPD in future technologies.

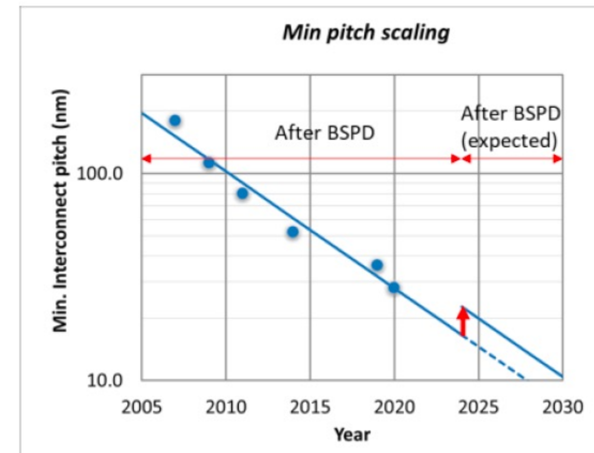
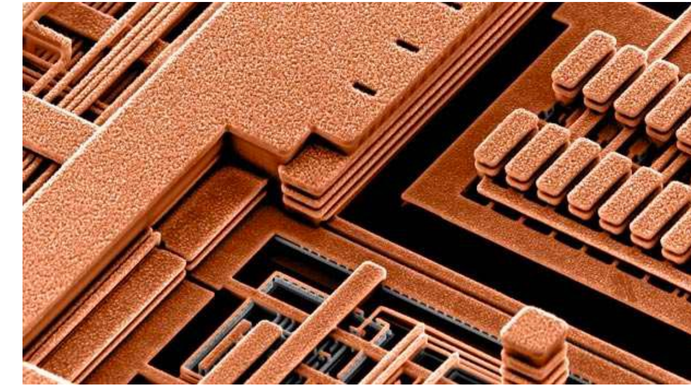


Fig. 6. Historical evolution of the minimum interconnect pitch with time, extended to include expected effect of deployment of BSPD.

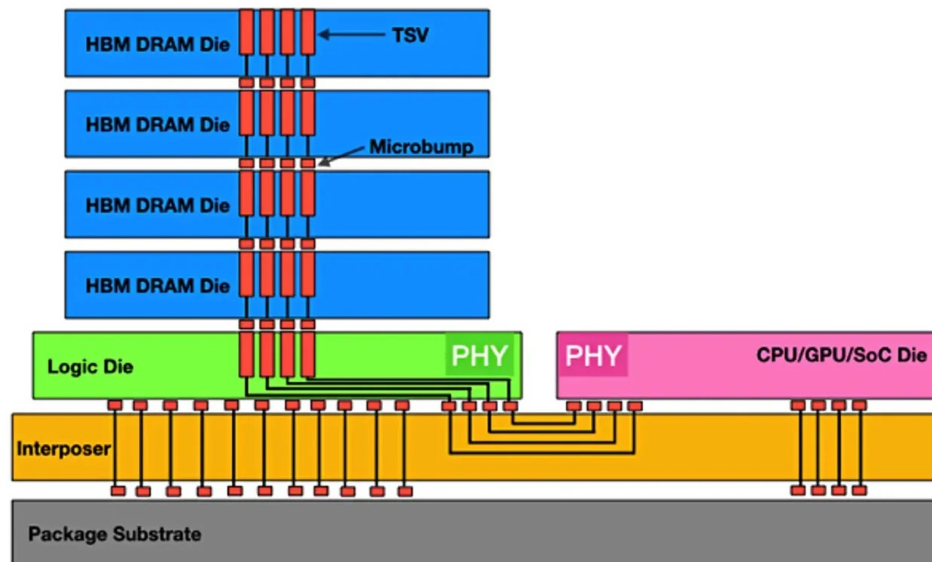


D. Edelstein et al. IEDM 1997

- One shot improvement after Cu introduced by IBM in 1997
- Lower cost, less scaling for same performance, more flexibility …
- Expect ultimately also to route signals on the back side…

Heterogenous integration

- Transistor cost scaling (0.7x) per generation down to 28 nm, and then much flatter from one generation to the other.
- In addition, memory, logic and analog scale differently (logic size scales, but this is much less the case for analog (almost constant area) and memory
- Cost benefit from density scaling therefore diminishes pushing for alternate design strategies enabled by 2.5 and 3D integration, wafer stacking, chiplets, etc.

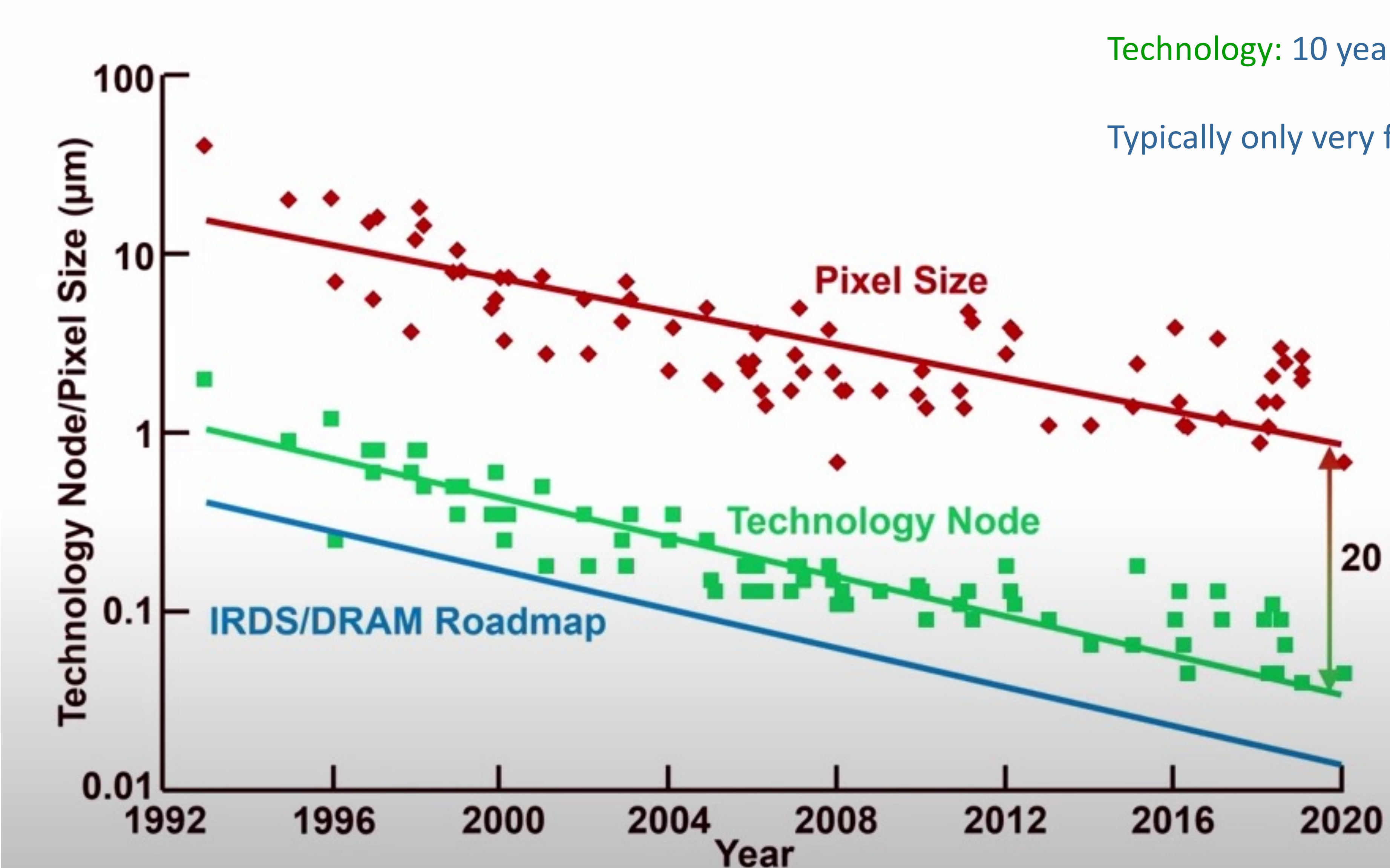


HBM High Bandwidth Memory

Source: semiengineering

Mainstream goes 2.5, 3D, potentially also very relevant for HEP !

Evolution of pixel size and technology node for standard visible imaging:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel

Albert Theuwissen, ISSCC 2021

General requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1…0.3
HL-LHC 3ab^{-1}	5	1.5
FCC HH	10-350	3-100

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

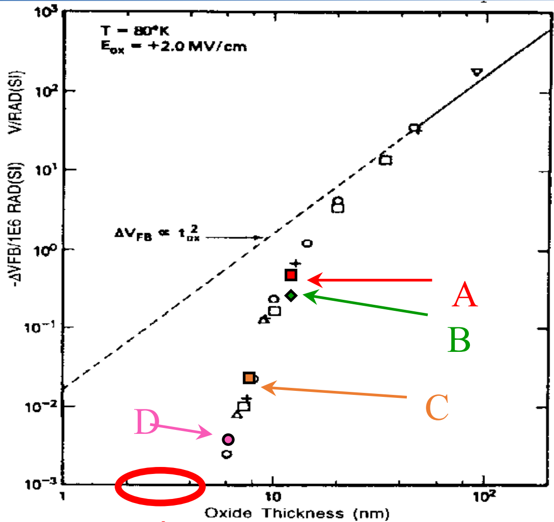
Time resolution

- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

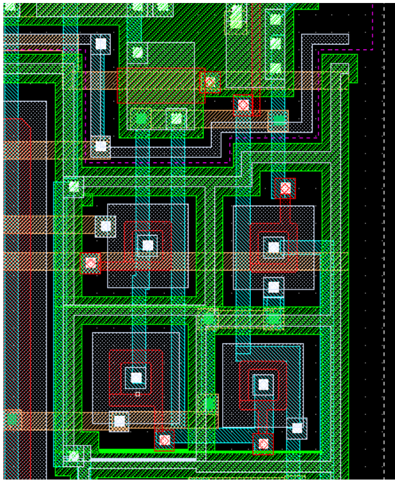
Larger and larger areas

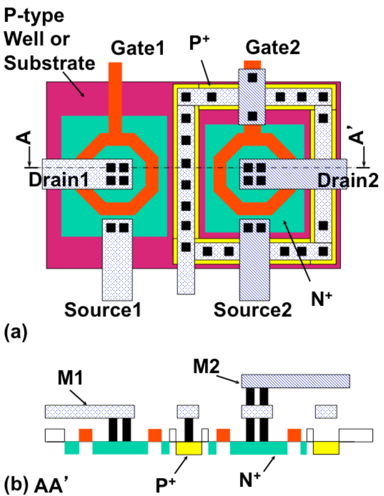
- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

Circuit radiation tolerance: like standard CMOS

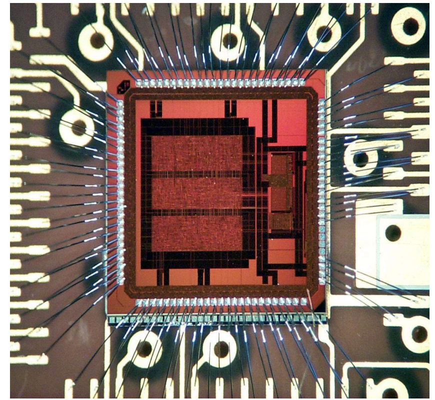


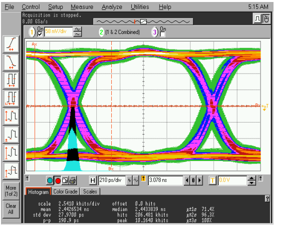
After N.S. Saks et al, IEEE TNS, Vol. NS-31 (1984) 1249





G. Anelli et al., IEEE TNS-46 (6) (1999) 1690





P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

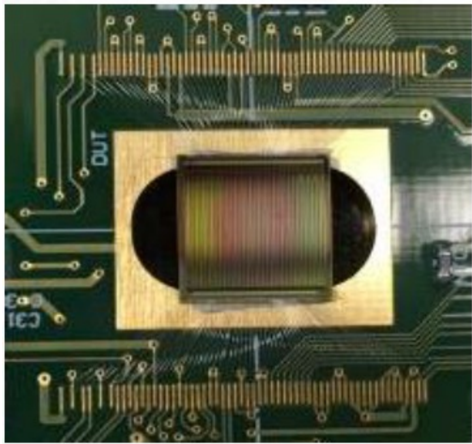
Total ionizing dose:

- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate e.g. from spacers, new gate dielectrics, **requires extensive measurement campaigns** F. Faccio et al. IEEE TNS-65 (1) 164, 2018,

Single event effects:

- Single Event Upset : triple redundancy with majority voting (now special scripts S. Kulis)
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies => **need attention in the design**

Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)



Efficiency non-irradiated **after 1.14 E15 n_{eq}/cm^2**

Vertical position (mm): 3, 2, 1, 0, −1, −2, −3

Horizontal position (mm): −1.0 −0.5 0.0 0.5 1.0 | −1.0 −0.5 0.0 0.5 1.0

Hit efficiency (%): 100.0, 97.5, 95.0, 92.5, 90.0, 87.5, 85.0, 82.5, 80.0, 77.5, 75.0

T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

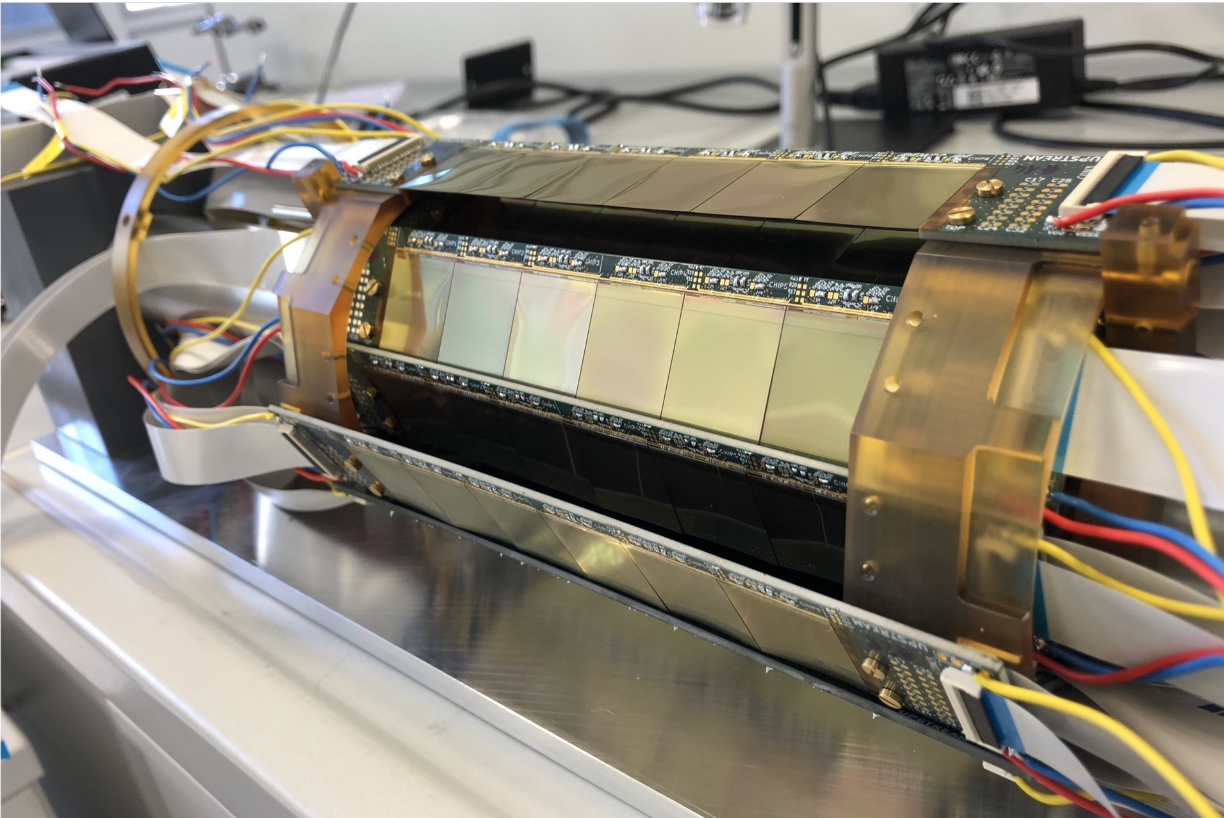
Courtesy N. Wermes

Other developments in same technology:

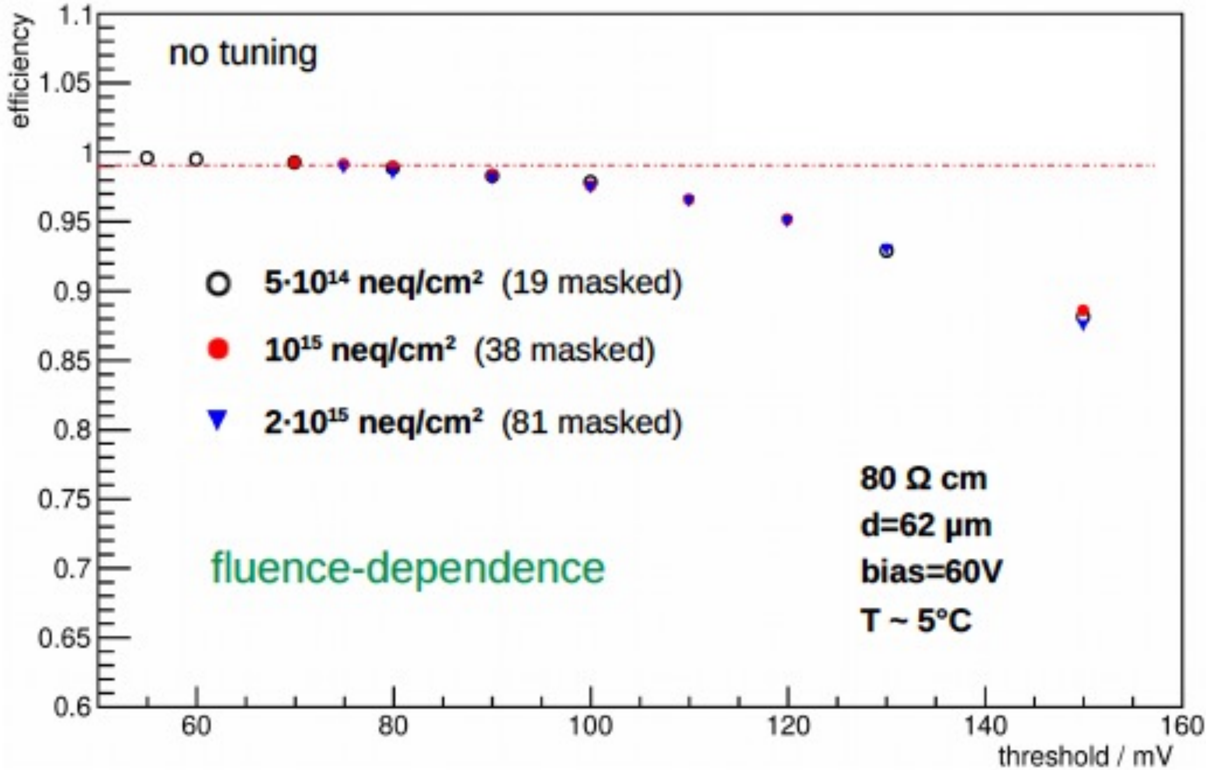
CACTUS Y. Degerli et al. doi:10.1088/1748-0221/15/06/P06011, VCI 2022, NIM A 1039 (2022) 167022

RD-50 E. Vilella et al. doi:10.22323/1.373.0019

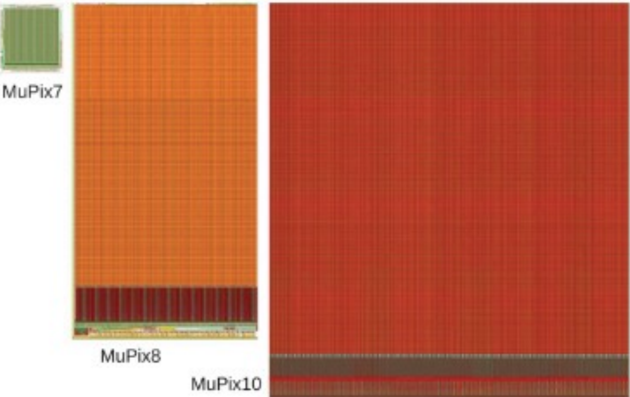
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)



MuPix vertex detector prototype

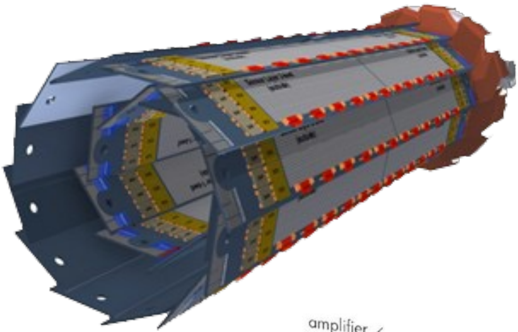


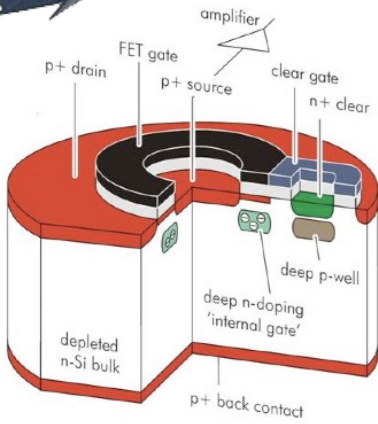
Courtesy I.Peric and A. Schoening



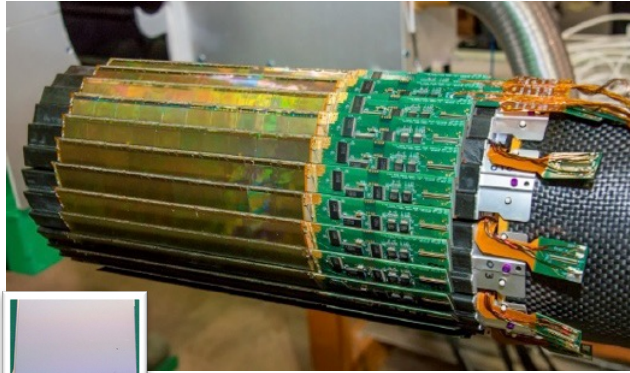
AMS/TSI 180nm, also used for ATLASPIX

Monolithic sensors in HEP move into mainstream technology



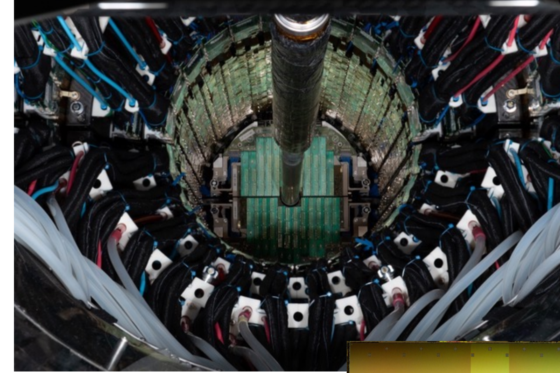


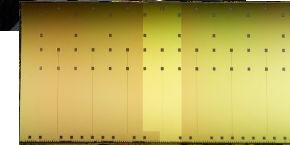
DEPFET in Belle



MIMOSA28 (ULTIMATE) in STAR
IPHC Strasbourg
First MAPS system in HEP
Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout





ALPIDE in ALICE
First MAPS in HEP with sparse readout similar to hybrid sensors
Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode
LF Monopix, MuPix,…
Extreme radiation tolerance and timing uniformity, but large capacitance

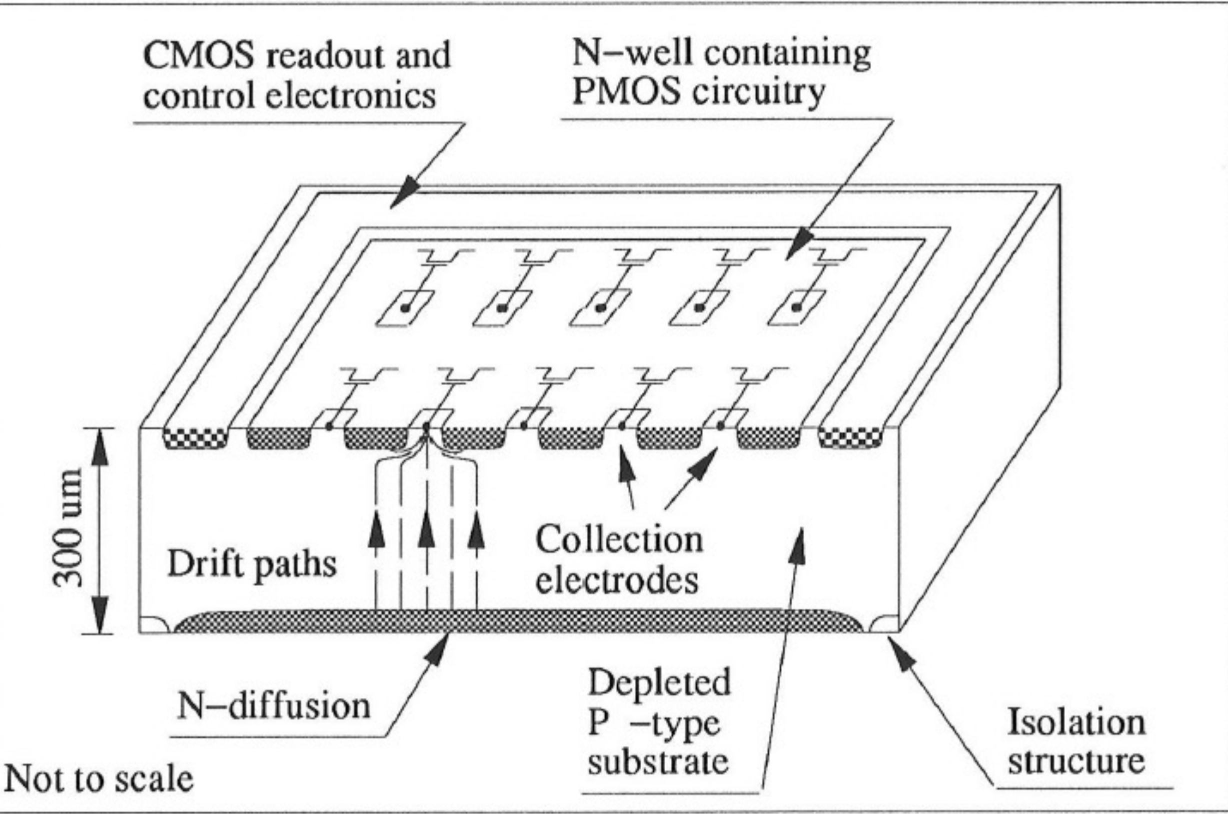
Small collection electrode
ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, …

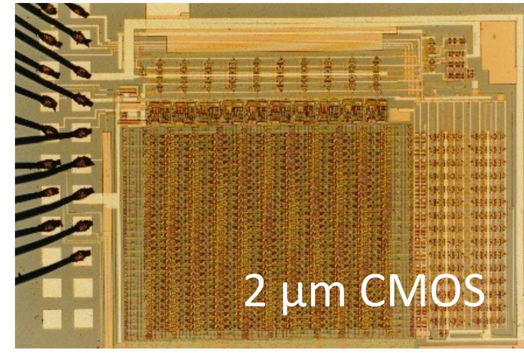
- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

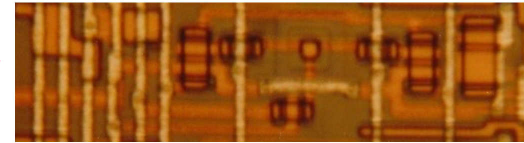
Commercial deep submicron CMOS technology evolved "naturally" towards

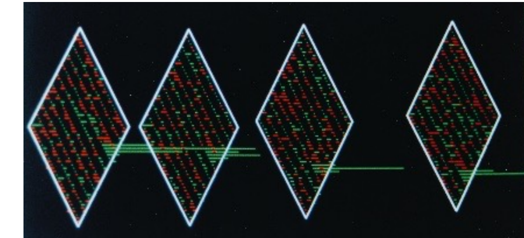
- Very high tolerance to ionizing radiation (some caveats, cfr G. Borghello, F. Faccio et al.)
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

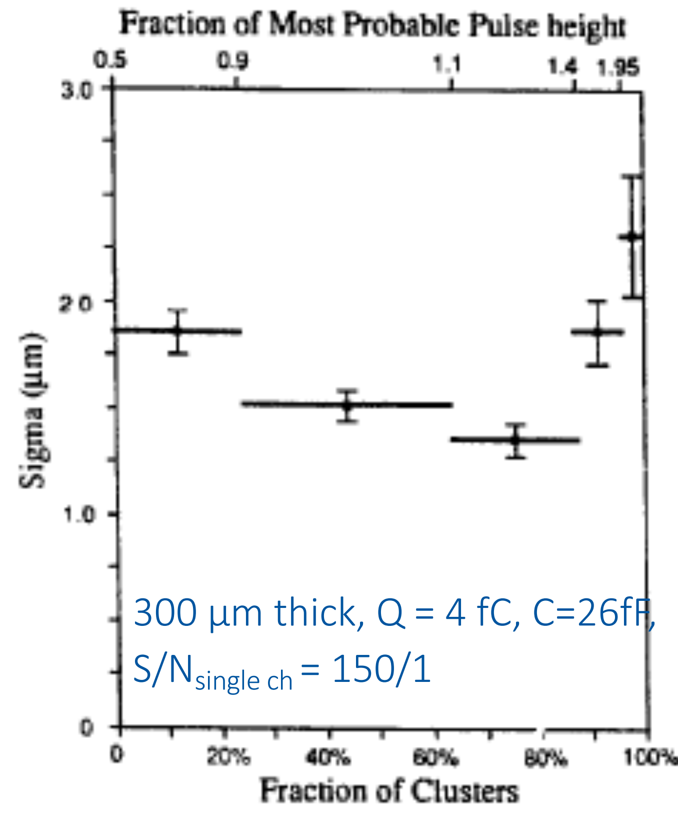
A monolithic detector for high energy physics (PhD thesis 1992), CMOS with double sided processing
Stanford University 1987-1992, and the University of Hawaii



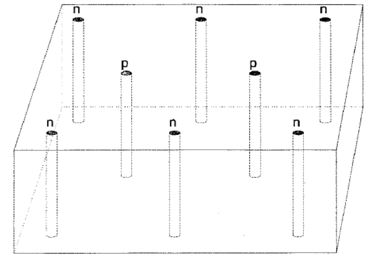








- Separation of junction from small collection electrode
- Better than 2 µm position resolution even at 34 µm pitch due to good S/N
- Improved back side trench isolation led to sensors with 3D electrodes (S.Parker, J. Segal)

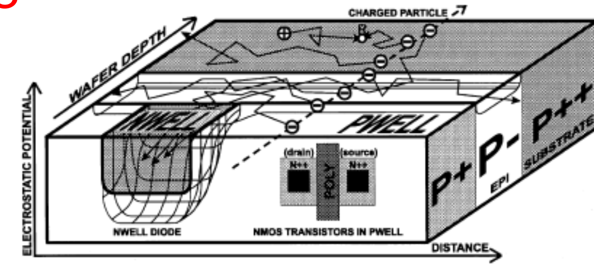


C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

KEY ENABLERS: Mimosa series – IPHC Strasbourg - Move to standard CMOS

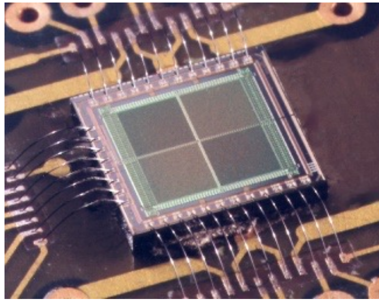
A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



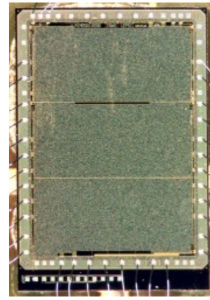
NIM A 458 (2001) 677-689

Mimosa1 – 1999
AMS 0.6 μm



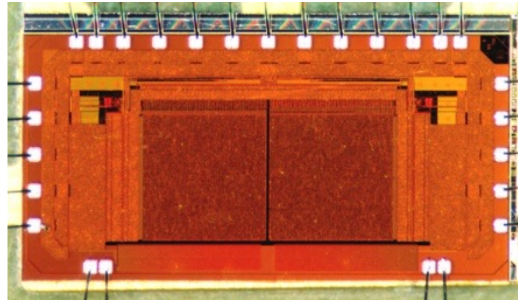
20μm pixel

Mimosa2 – 2000
MIETEC 0.35 μm



20μm pixel

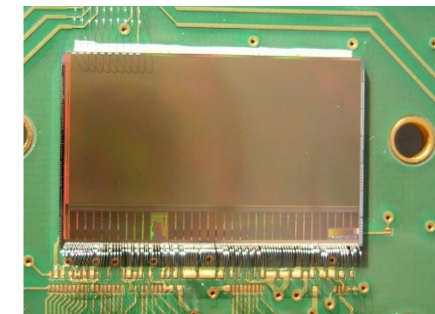
Mimosa3 – 2001
IBM 0.25 μm



8μm pixel

....

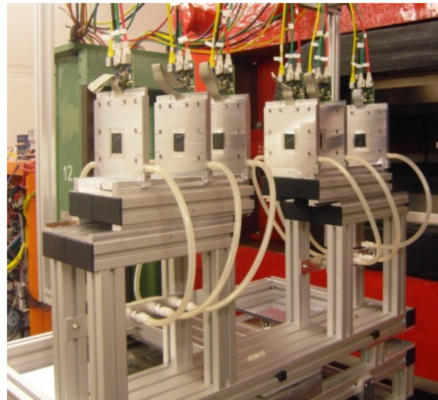
Mimosa26 – 2008
AMS 0.35 μm



18.4 μm pixel

....

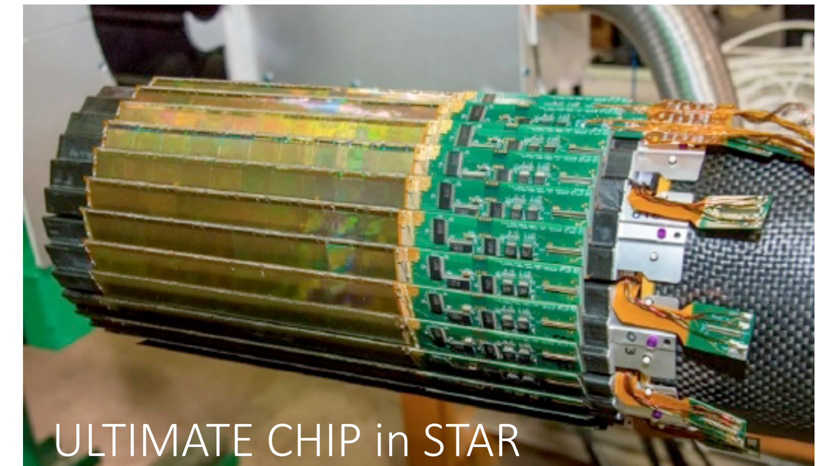
Mimosa26 – 2008 in the EUDET Telescope,



Rolling shutter readout

First MAPS with integrated zero-suppressed readout, used for several applications, also EUDET telescope

First use of MAPS in HEP



KEY ENABLERS: The INMAPS process: STFC development, in collaboration with TowerJazz: a game changer

Additional deep p-well implant allows full CMOS in the pixel and 100 % fill factor

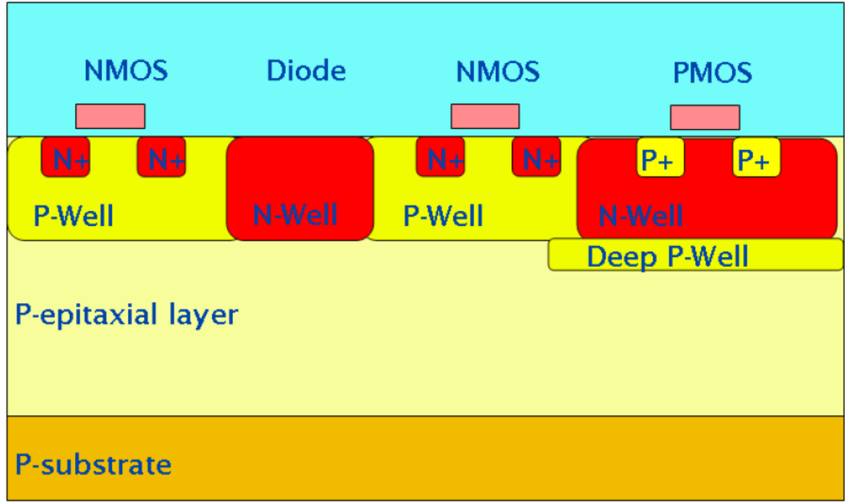
Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels

Jamie Alexander Ballin [2], Jamie Phillip Crooks [1], Paul Dominic Dauncey [2], Anne-Marie Magnan [2], Yoshinari Mikami [3,**], Owen Daniel Miller [1,3], Matthew Noy [2], Vladimir Rajovic [3,***], Marcel Stanitzki [1], Konstantin Stefanov [1], Renato Turchetta [1,*], Mike Tyndel [1], Enrico Giulio Villani [1], Nigel Keith Watson [3], John Allan Wilson [3]

[1] Rutherford Appleton Laboratory, Science and Technology Facilities Council (STFC), Harwell Science and Innovation Campus, Didcot, OX11 0QX, U.K

[2] Department of Physics, Blackett Laboratory, Imperial College London, London, SW7 2AZ, U.K

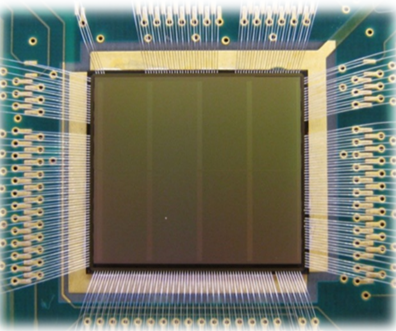
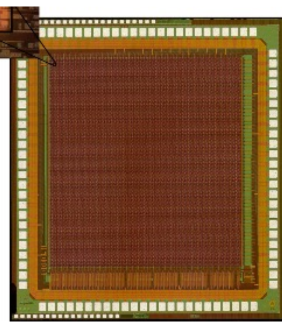
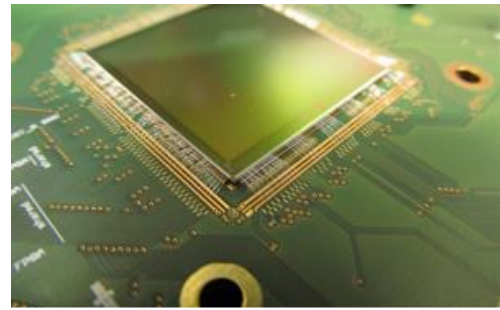
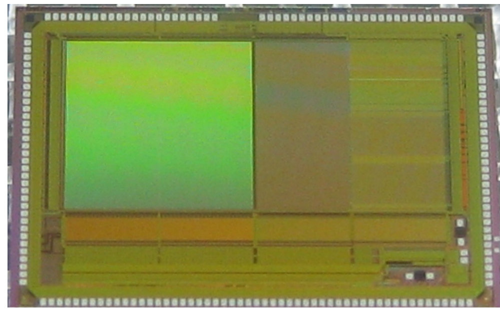
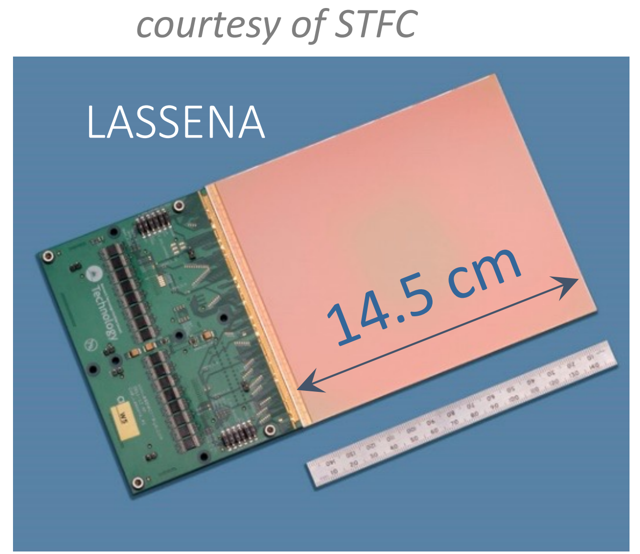
[3] School of Physics and Astronomy, University of Birmingham, Birmingham, B15 2TT, U.K



Sensors 2008 (8) 5336, DOI:10.3390/s8095336

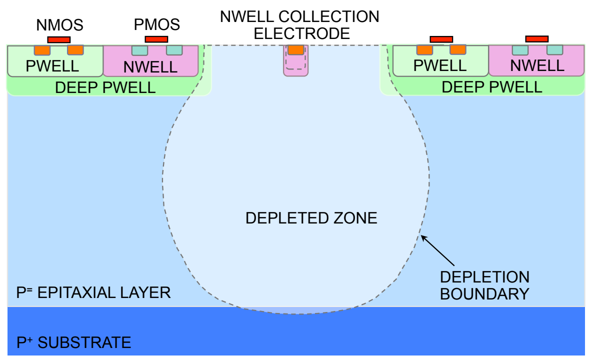
New generation of CMOS sensors for scientific applications in TowerJazz CIS 180nm

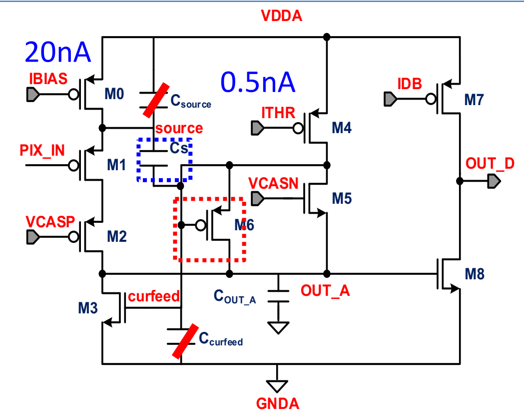
courtesy of STFC

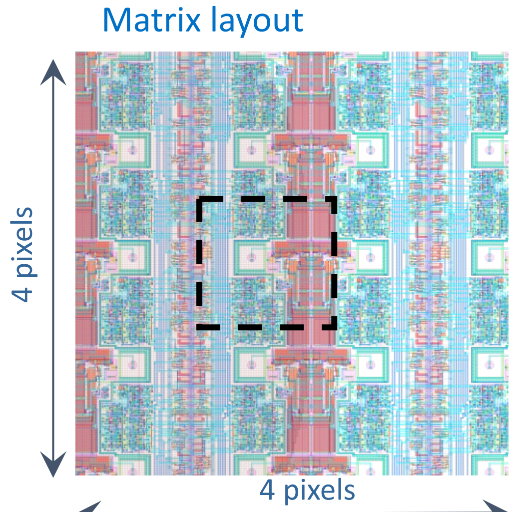
TPAC ILC ECAL (CALICE)	DECAL Calorimetry	PIMMS TOF mass spectroscopy	CHERWELL Calorimetry/Tracking	
				
50μm pixel	50μm pixel	70μm pixel	48 μm x 96 μm pixel	50μm pixel, waferscale

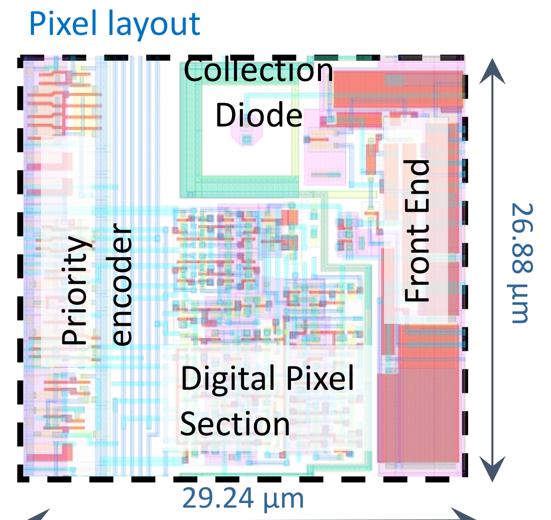
Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

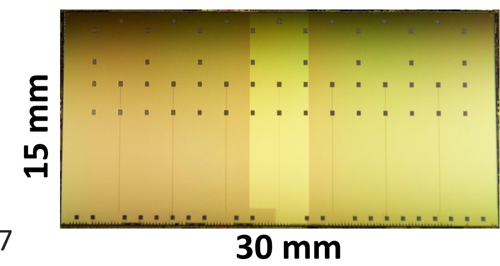
ALPIDE chip in ALICE ITS2

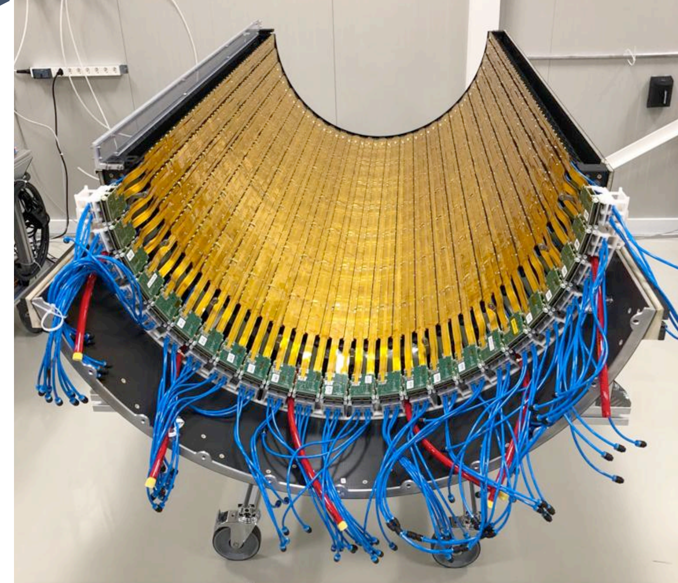






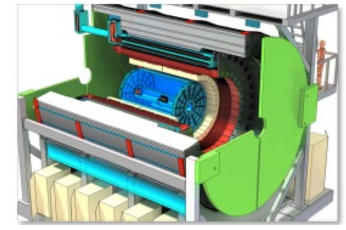




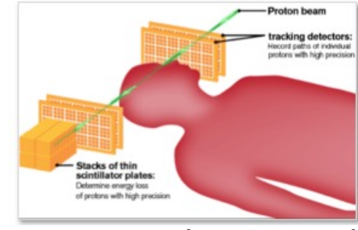


Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m^2 sensitive area

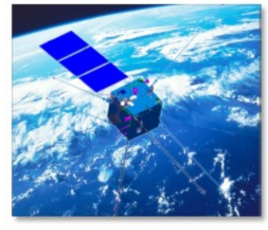
- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 µm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm^2 and 10 m^2 in the experiment not ideal -> stitching would have been of interest
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications



sPHENIX



Proton CT (tracking)



CSES – HEPD2

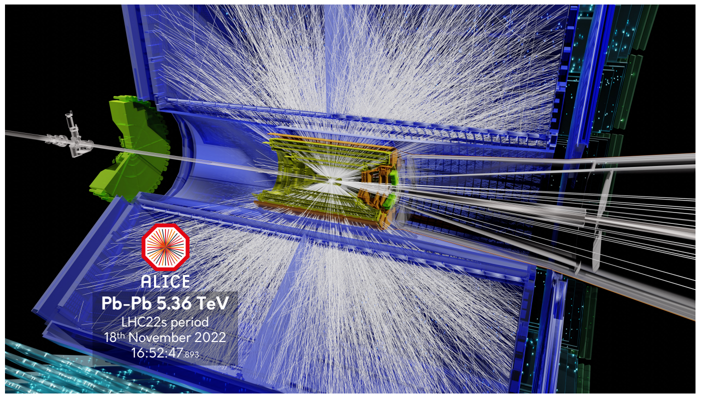
Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

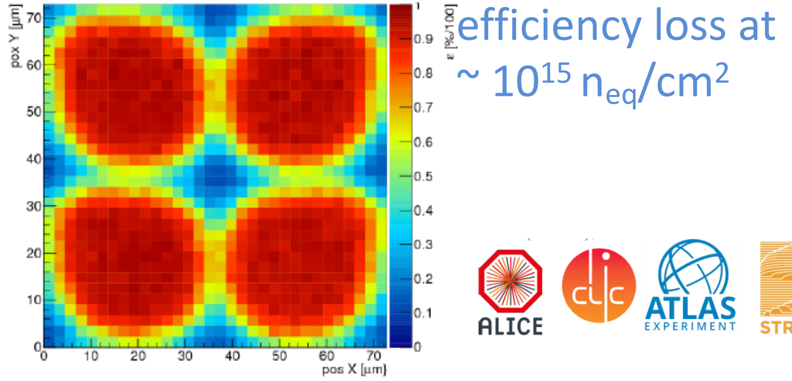
Pixel optimization for better margin: move junction away from the collection electrode for full depletion:
Better time resolution, radiation hardness and … efficiency, especially for thin sensors

in 180 nm

See also presentation of F. Reidt

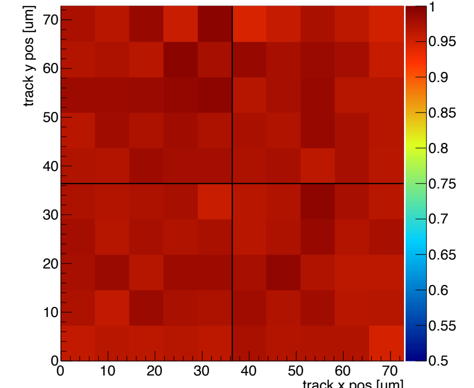


ALPIDE and ITS2 in ALICE (10 m²)

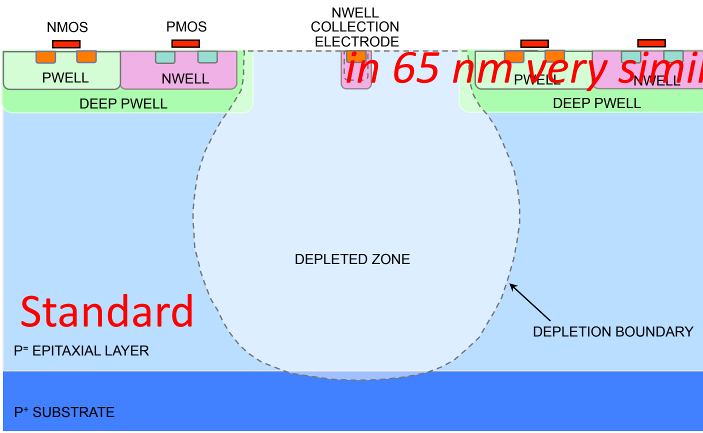


E. Schioppa et al, VCI 2019

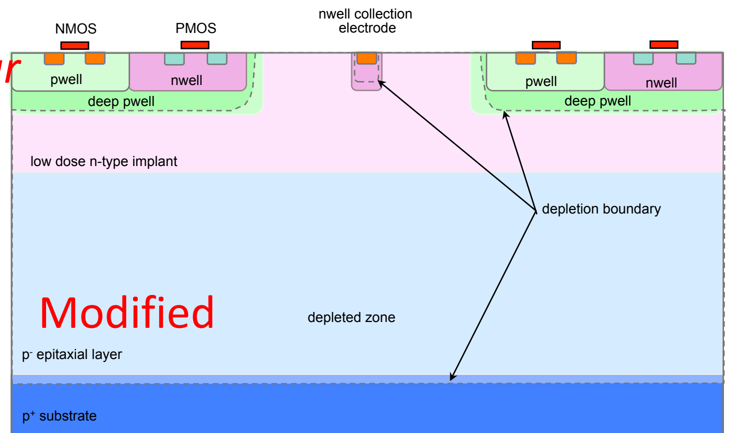
efficiency loss at ~ 10^{15} n_{eq}/cm^2



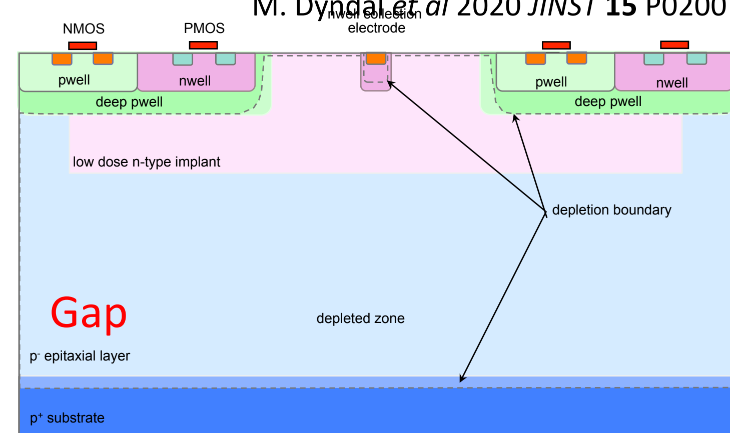
H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200



in 65 nm very similar

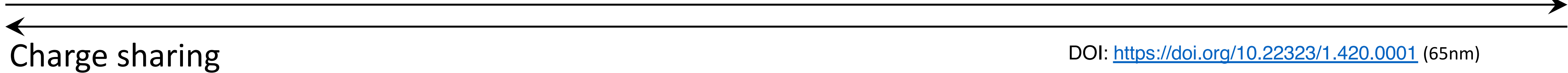


M. Munker et al. https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed



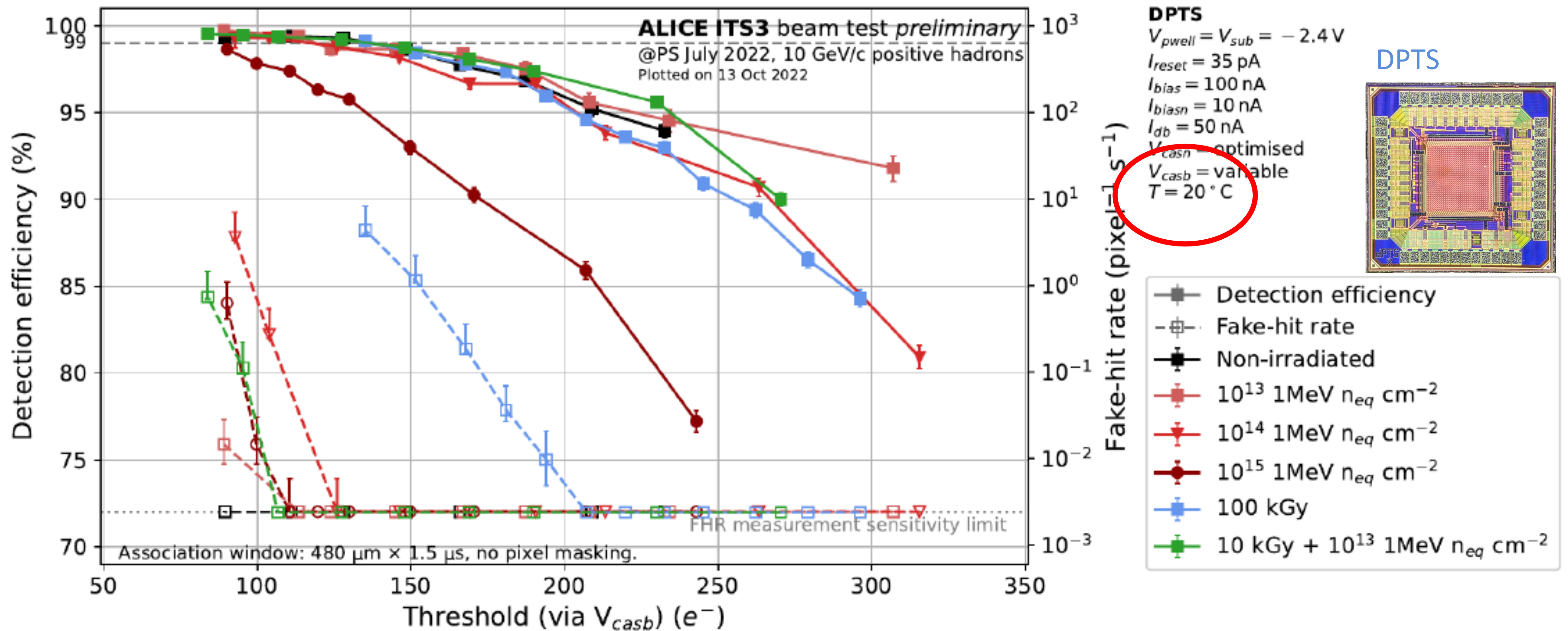
Charge sharing

DOI: https://doi.org/10.22323/1.420.0001 (65nm)

65 nm very similar, profited significantly from 10 years experience in 180 nm

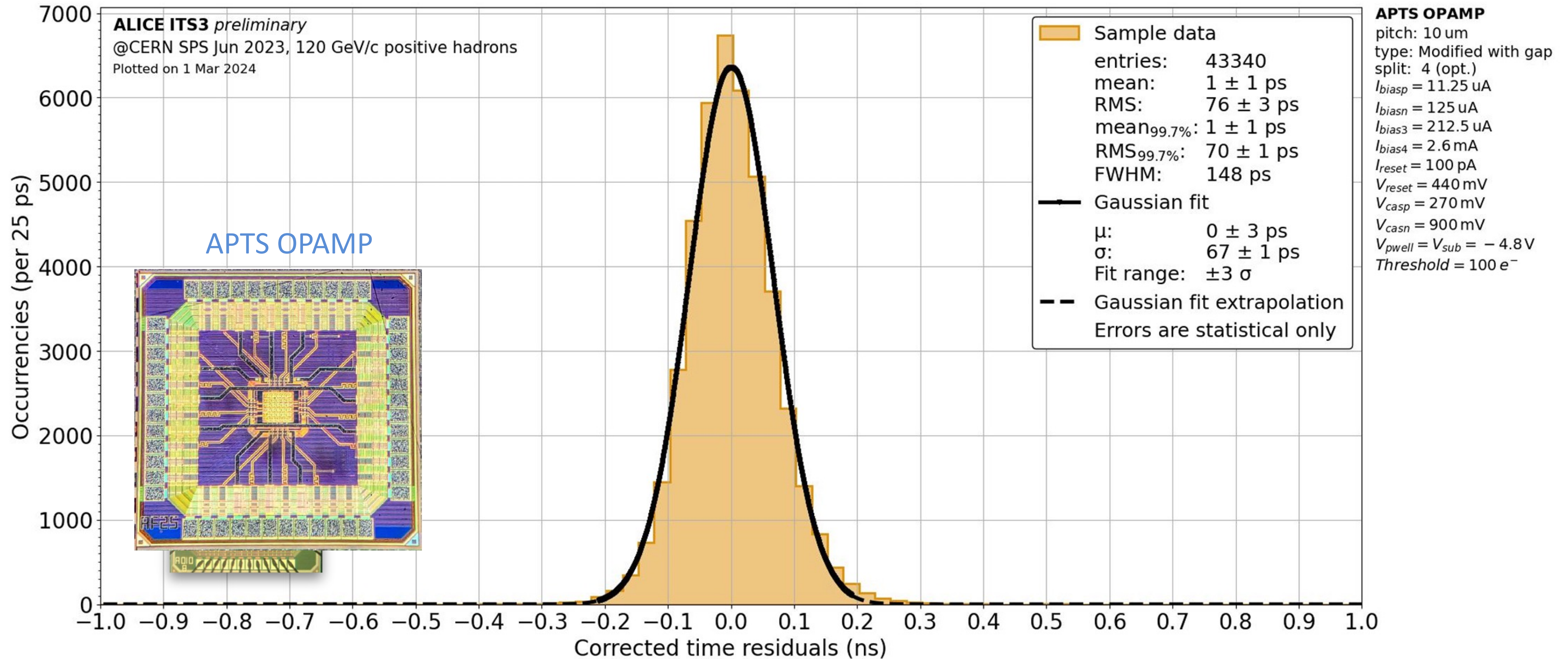
EP R&D WP1.2 with a very significant contribution from ALICE ITS3 team (large measurement team 40-50 people)

~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature doi: 10.1016/j.nima.2023.168589



- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 μm^2 pixel (DPTS) including sensor optimization
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- KEY ACHIEVEMENT: 65nm ISC qualified for HEP, many features not yet explored (wafer stacking, special imaging devices…)

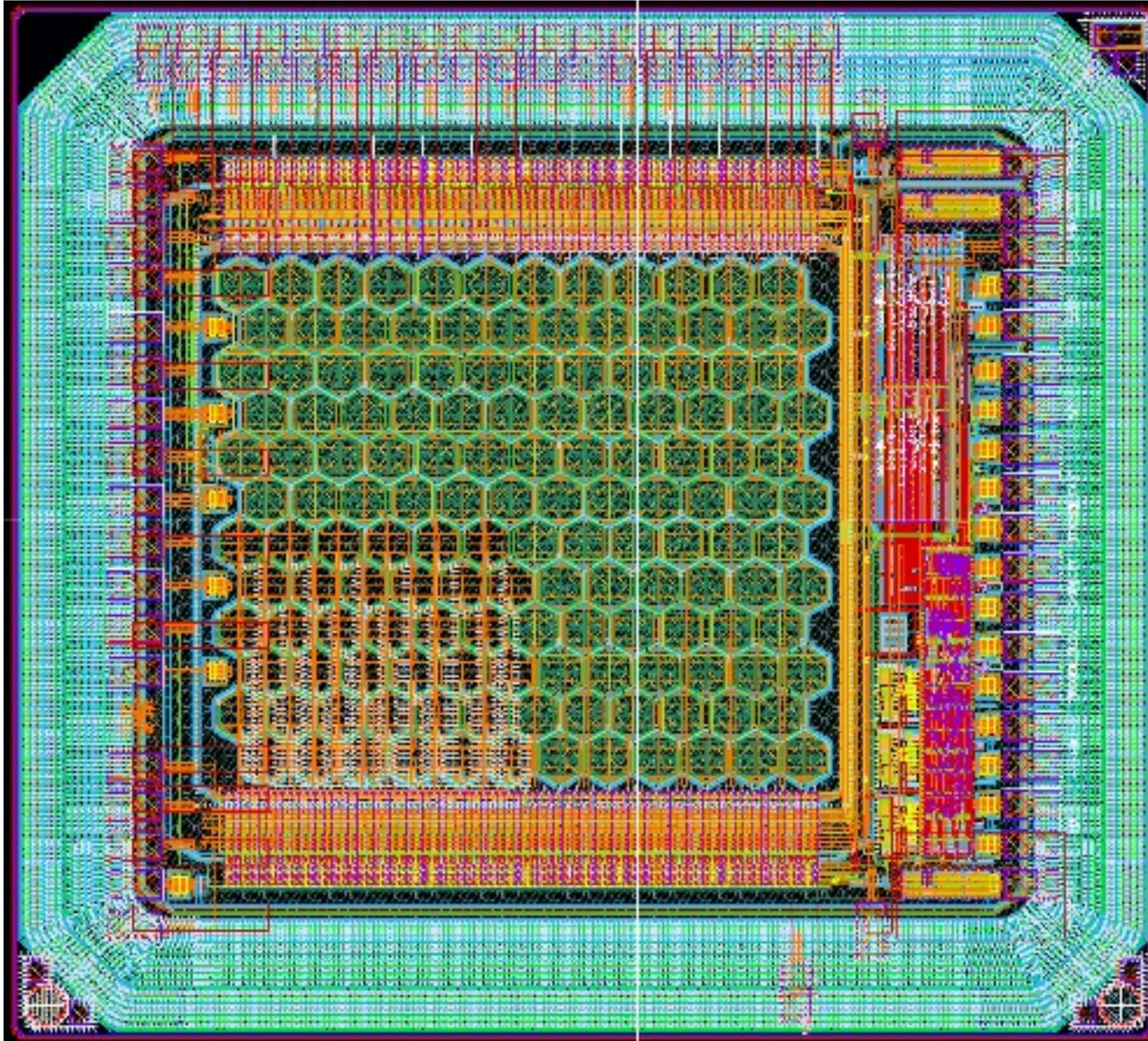
Sensor timing



Bong-Hwi, U. Savino et al. ULITIMA 2023, L. Aglietta, 16th Pisa conference on advanced detectors.

(180nm FASTPIX ~100 ps with time walk and cluster size correction, J. Braach et al. doi:10.48550/arXiv.2306.05938)

MONOLITH: SiGe BiCMOS development



- Heterojunction Bipolar Transistor (HBT) gives cut-off frequencies otherwise only reached in more advanced CMOS technologies
- Large collection electrode hexagonal pixel arrangement
- Prototype without gain:
  - Full efficiency
  - ~ 20 ps time resolution without gain layer
  - Radiation tolerance 10^{16} n_{eq}/cm^2, also for the HBT !

Courtesy G. Iacobucci

DRD7.6a

Strategic Goal

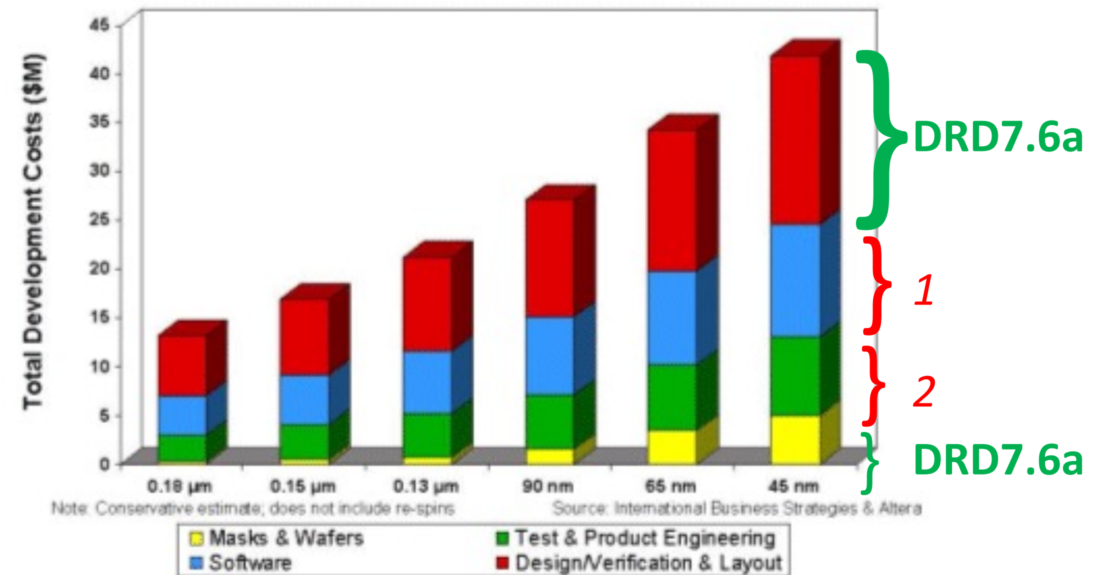
- Provide efficient and affordable access to imaging technologies to projects, DRDs like DRD3, and experiments
- Share and reduce development costs & time
- Requires concentration of resources

Performance Targets

- Shared PDKs, IPs and access to runs
- Chip submissions and test results

Supported Technologies

- TPSCO 65nm
- Tower Semiconductor 180nm
- LFoundry 110nm (see M. Rolo's presentation)



https://www.design-reuse.com/articles/12360/fpgas-and-structured-asics-low-risk-soc-for-the-masses.html

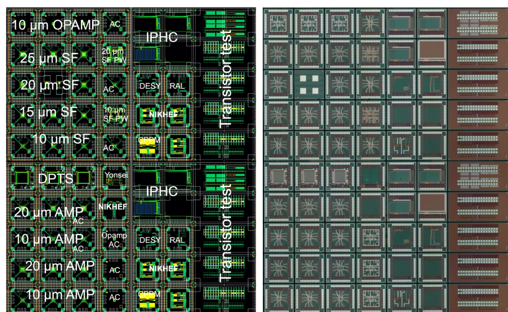
Resources for 1: Software & 2: Test setups not included within DRD7.6a

TPSCo 65 nm (MLR1, ER1 and ER2)

Last EP R&D report: https://cds.cern.ch/record/2891650
ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

MLR1: Dec 2020: 1.5 x 1.5 mm² test chips

qualification of TPSCo 65 nm for HEP

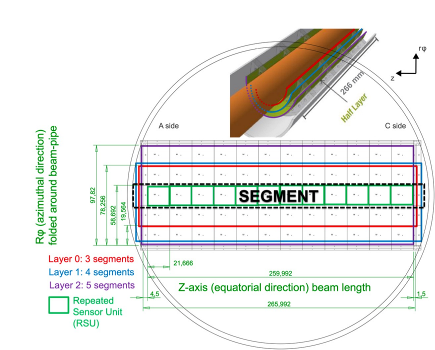


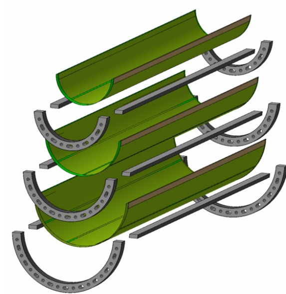
- Fully efficient at RT before and after 10^{15} n_{eq}/cm^2
- Sensor time resolution ~ 70 ps (10 µm pitch)
- Investigating path to tolerance to higher irradiation levels and lower input capacitance

(C. Lemoine *et al* 2024 *JINST* **19** C02033)

ER2: MOSAIX: Fall 2024:

First full prototype for ALICE ITS3





See presentation G. Aglieri Rinella, F. Reidt

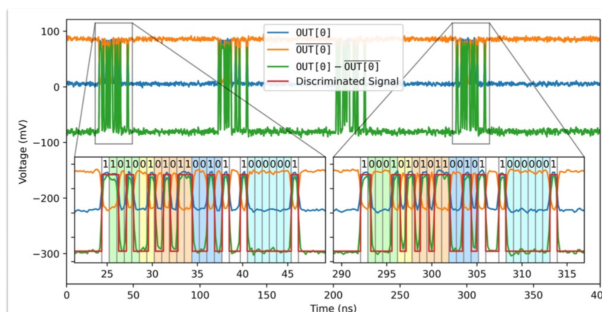
ER1: Dec 2022:

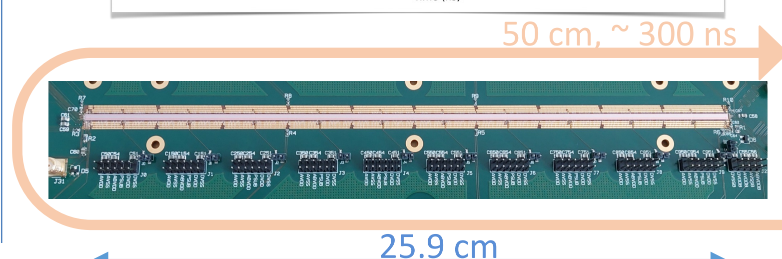
Learning about stitching

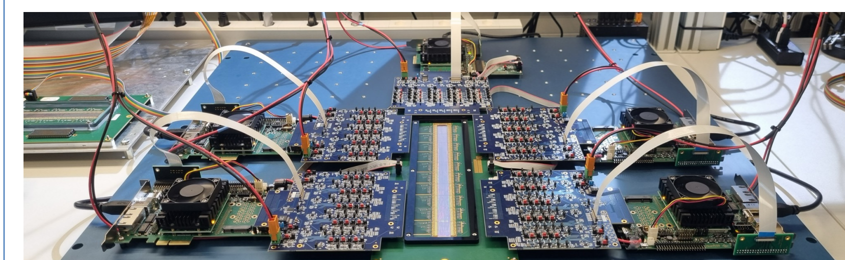
Two stitched sensors with 10 repeated units:
Both functional, learnings to be included in ER2

MOST (25.9 cm x 0.25 cm):

- 18 µm pitch, very densely designed pixel matrix
- Global power distribution + conservatively designed highly granular power switches to switch off faulty parts
- Asynchronous, hit-driven readout, low power consumption + timing information
- Pulsing signal and output signals at the end of the chip, round trip more than 50 cm, ~ 300 ns, with ~800 repeaters, all 256 signal lines functional



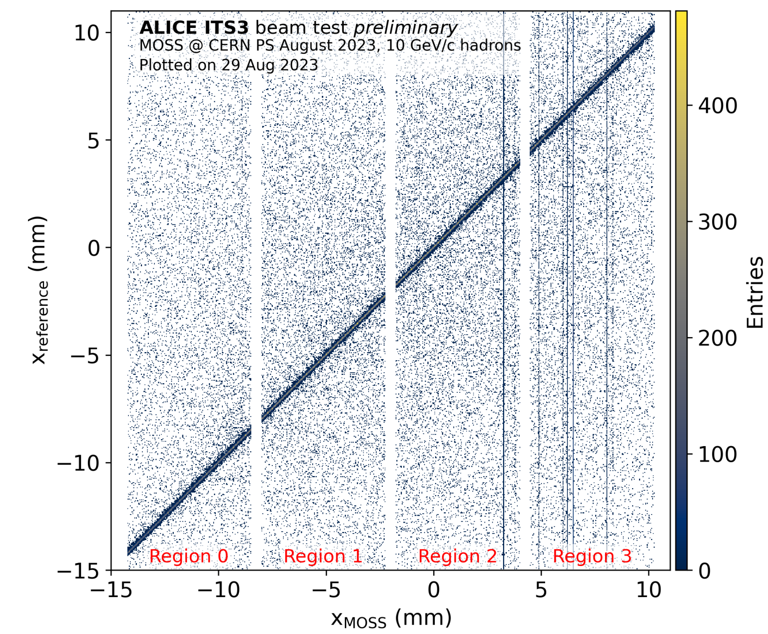




MOSS (25.9 cm x 1.4 cm):

- Top half 22.5 µm pitch, bottom half 18 µm pitch
- Each half powered completely independently with 4 conservatively designed submatrices -> many power domains
- Synchronous readout

Hit x-coordinate correlation between MOSS and reference ALPIDE telescope



CONCLUSIONS and OUTLOOK

- After years of R&D monolithic sensors for HEP move to CMOS MAPS with complex in-pixel circuitry in mainstream CMOS technology, but requirements for HEP are not completely identical to those for visible light imaging, and some technology flexibility can still be beneficial.

- Circuit radiation tolerance as for standard CMOS, which naturally evolved towards significant tolerance with some caveats.

- 10 years of experience with 180 nm enabled fast qualification of the 65 nm technology for HEP and the exploration of wafer-scale sensors for ITS3, opening perspectives for other projects like ALICE3 and FCC-EE. Some foundry flexibility has allowed greatly improved sensor timing, radiation tolerance and operating margin based on general principles applicable to different technologies.

- Large collection electrode sensors provide extreme radiation tolerance and more uniform sensor timing but exhibit large input capacitance.

- Decreasing technology feature size or special imaging sensor features can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing.

- 3D wafer stacking now allows the connection of a readout wafer to a detector wafer, and deliver the fully finished diced assemblies to the customer. This reduces the distinction with hybrid sensors, but provides opportunities well beyond with multiple connections within each pixel and stacking of even more than two wafers.

- Unprecedented integration in electronics systems and advanced semiconductor technologies continues to be driven by the computation needs of AI and will also benefit HEP detector systems. Stitching and wafer stacking brings pixel pitches around 10 um within reach. The circuitry on a monolithic sensor allows the mitigation of local, otherwise fatal defects for large, even wafer-scale sensors.

- Some selected technologies are now qualified for HEP and supported through DRD7. It will be important to explore new ones, probably finer linewidth, but the effort for that Is large and our community will need to concentrate resources on a few.

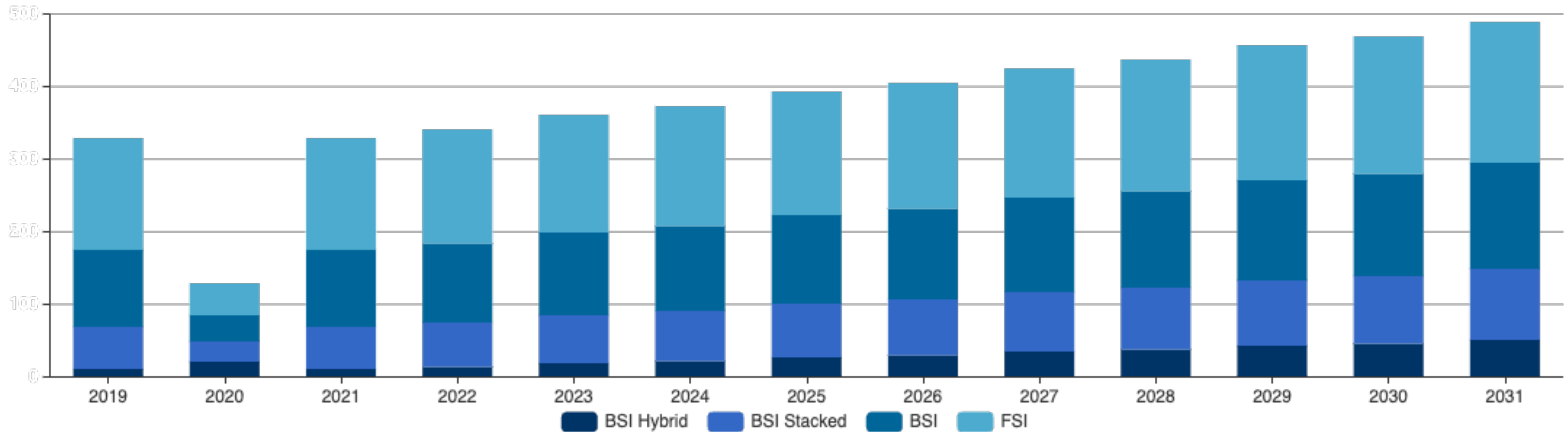
- CMOS monolithic sensors will become widely applied in HEP, in tracking, calorimetry and timing detectors. Non-negligible MAPS production volumes within HEP should allow our community to impact not only the quality of its own measurements, but also society in general, with access to the most advanced technologies.

THANK YOU !

Backup

CMOS Imaging technology market by category

- 23.9B USD in 2023, expected to reach 45B USD by 2033



Source: cognitivemarketresearch.com