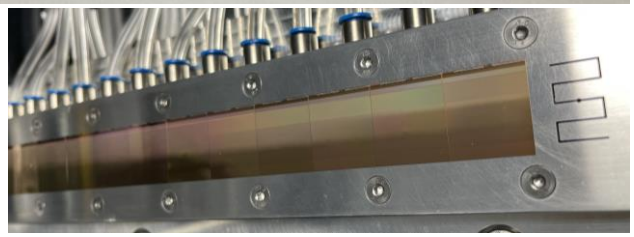
Mu3e Outer Pixel Construction Experience

UNIVERSITY OF OXFORD

Oxford is currently building one hundred and fifty 18 chip helium cooled 50µm MAPS instrumented ladders for Mu3e experiment.

- The ladders comprise robotically placed MuPix11 HV-CMOS ASIC, two layer Al Kapton data and power flex with SP-TAB bond interconnects and vias, 25µm carbon mechanical support.
- Each ladder is 400mm long, has a ~0.1%X/X_0, provides 10ns timestamping, 100µm pixel size, and a data driven readout architecture.
- The low mass, tightly coupled mechanical and electrical ladder design is a good prototype for what is required for FCC vertex structures.



We would like to present:

- Mu3e ladder design and performance
- Ladder mechanical qualification
- Ladder construction process, including:
  - 50µm thick ASIC testing procedures and difficulties
  - Ladder construction and handling tooling
  - Robotic ASIC placement with minimal gaps
  - SP-TAB boding development and process control
  - Carbon fibre support gluing
- Plans for a 1200mm long Mu3e phase 2 ladder and reduced mass carbon fibre supports