

VERTEX DETECTOR DESIGN AND INTEGRATION

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Maps Detector Technologies for the FCC ee Vertex Detector

2-3 July 2024

Outline

Progress on the layout

- Mechanical model for inner vertex and supports
- Lighter supports for Middle and Outer vertex

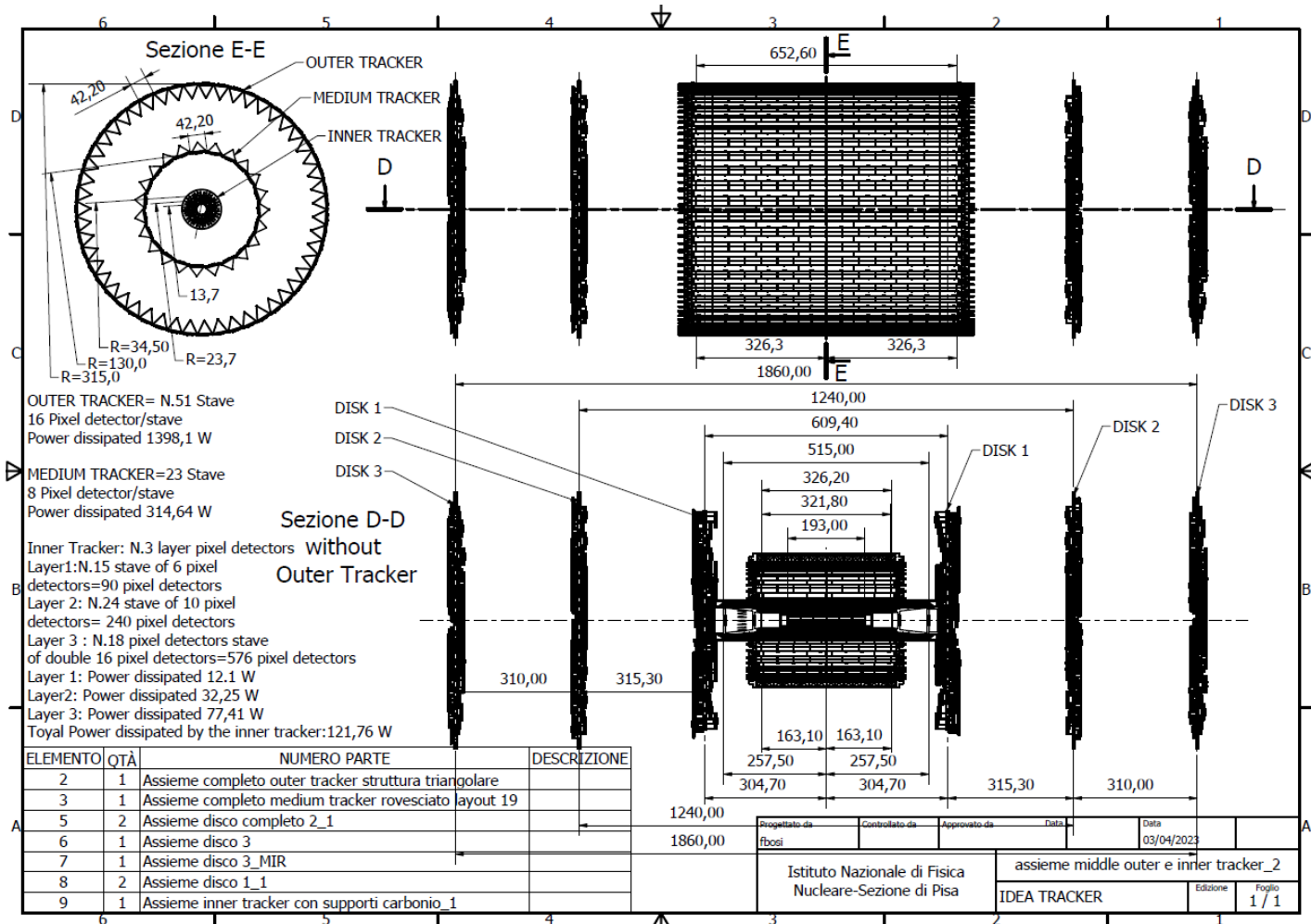
Ongoing efforts

- Integration of air cooling structures
- Curved sensors layout studies

Conclusions

See also Armin Ilg talk on Tuesday PED session

Mid-term feasibility study vertex detector layout

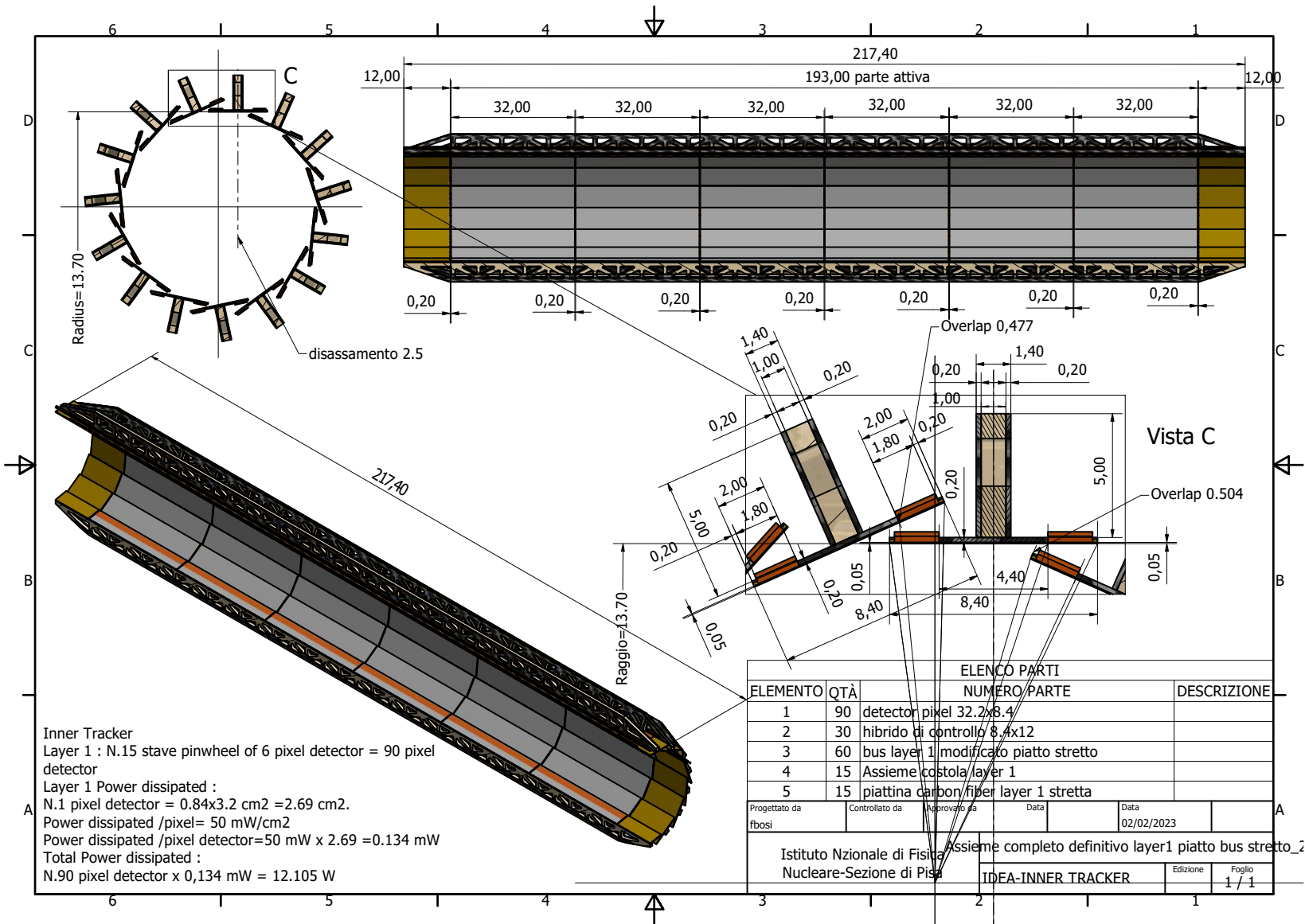


Outer vertex tracker:
ATLASPix3 based

- Modules of $50 \times 150 \mu\text{m}^2$ pixel size
- Intermediate barrel at 13 cm radius
 - Outer barrel at 31.5 cm radius
 - 3 disks per side

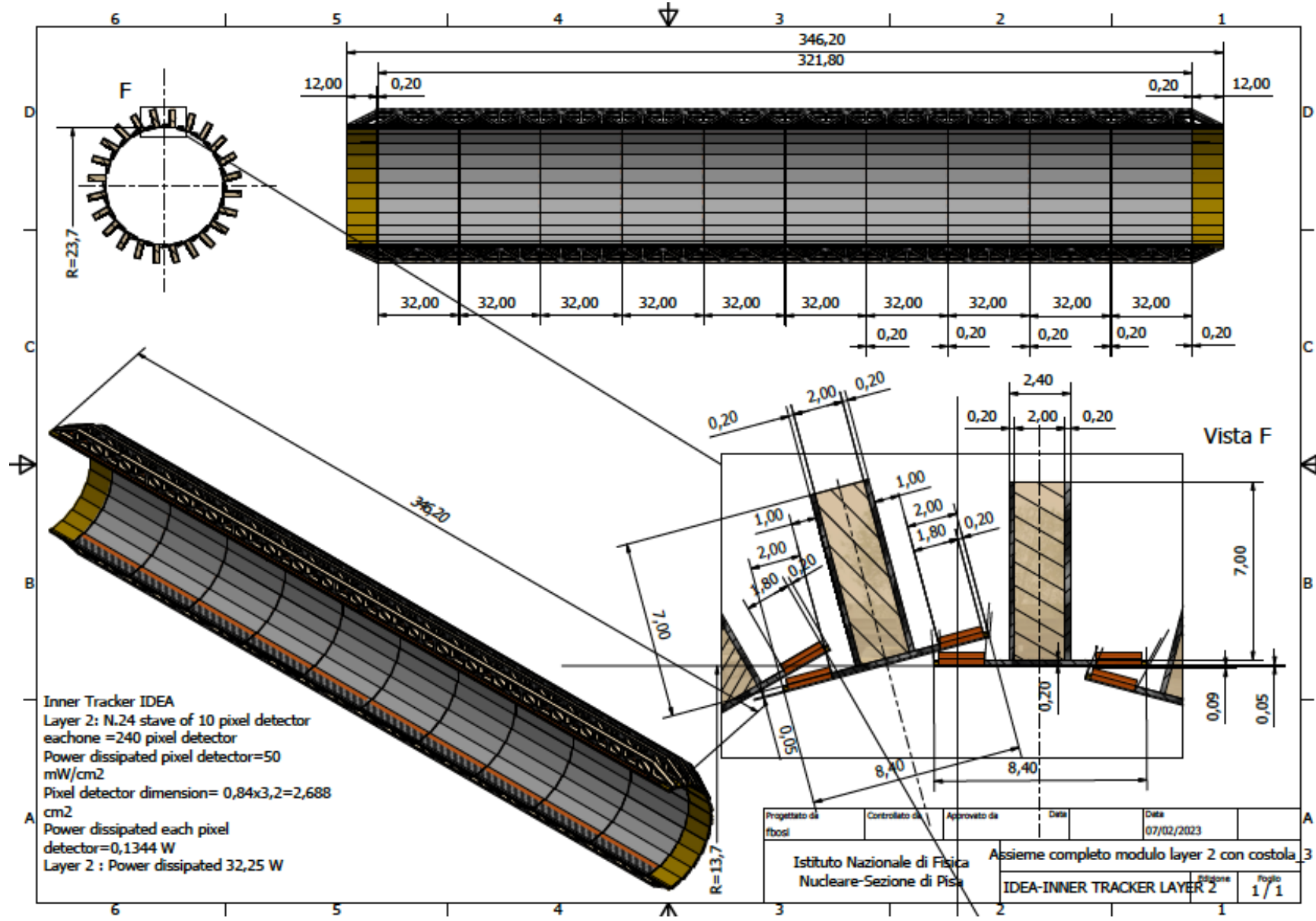
Inner Vertex detector:
ARCADIA based

- Modules of $25 \times 25 \mu\text{m}^2$ pixel size
- 3 barrel layers at
- 13.7, 23.7 and 34/35.6 mm radius



Inner Tracker
 Layer 1 : N.15 stave pinwheel of 6 pixel detector = 90 pixel detector
 Layer 1 Power dissipated :
 N.1 pixel detector = 0.84x3.2 cm2 = 2.69 cm2.
 Power dissipated /pixel= 50 mW/cm2
 Power dissipated /pixel detector=50 mW x 2.69 =0.134 mW
 Total Power dissipated :
 N.90 pixel detector x 0,134 mW = 12.105 W

Layer 1
 15 overlapping staves of 6 modules each
 Overlap to allow alignment ~500 μm
 Pinwheel geometry: all modules at the same (smallest) radius
 Power budget ~12 W
 Total weight ~22 grams
 Total thickness 0.25% X_0
 Silicon: 0.053% X_0
 Power and readout bus: 0.056% X_0



Inner Tracker IDEA
 Layer 2: N.24 stave of 10 pixel detector
 eachone =240 pixel detector
 Power dissipated pixel detector=50
 mW/cm²
 Pixel detector dimension= 0,84x3,2=2,688
 cm²
 Power dissipated each pixel
 detector=0,1344 W
 Layer 2 : Power dissipated 32,25 W

Layer 2
 24 overlapping staves of 10
 modules each

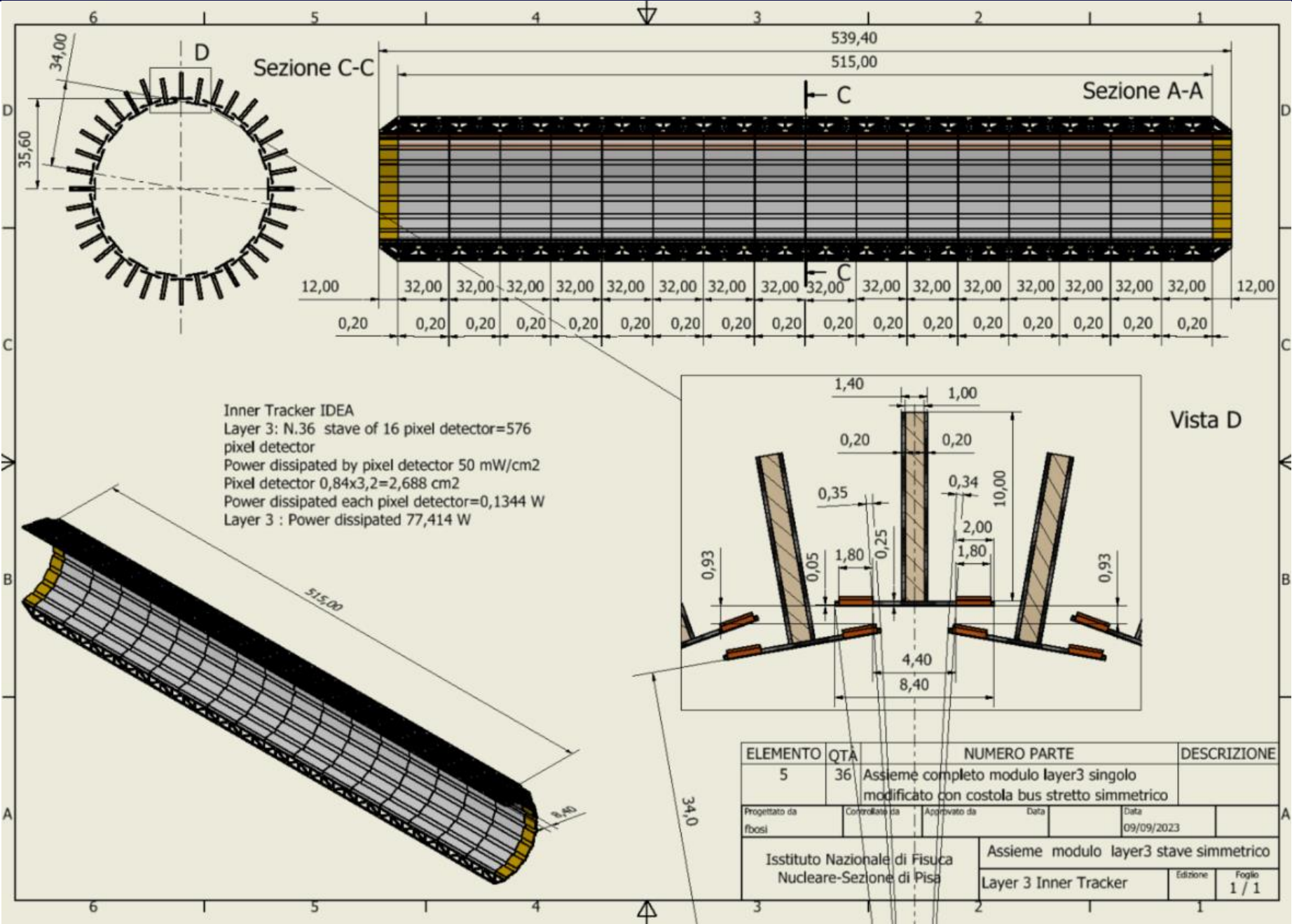
Pinwheel geometry
 Counter-rotated wrt layer 1 to
 mitigate charge-asymmetry
 effects in track reconstruction

Power budget
 ~32 W

Total weight ~63 grams

Total thickness 0.25% X₀

Progettato da fbosi	Controllato da	Approvato da	Data 07/02/2023
Istituto Nazionale di Fisica Nucleare-Sezione di Pisa			
Asieme completo modulo layer 2 con costola			
IDEA-INNER TRACKER LAYER 2		Edizione 1/1	Foglio 1/1



Layer 3
 36 staves of 16 modules each

Lampshade geometry.
 Charge symmetric track reconstruction

Total weight ~150 grams

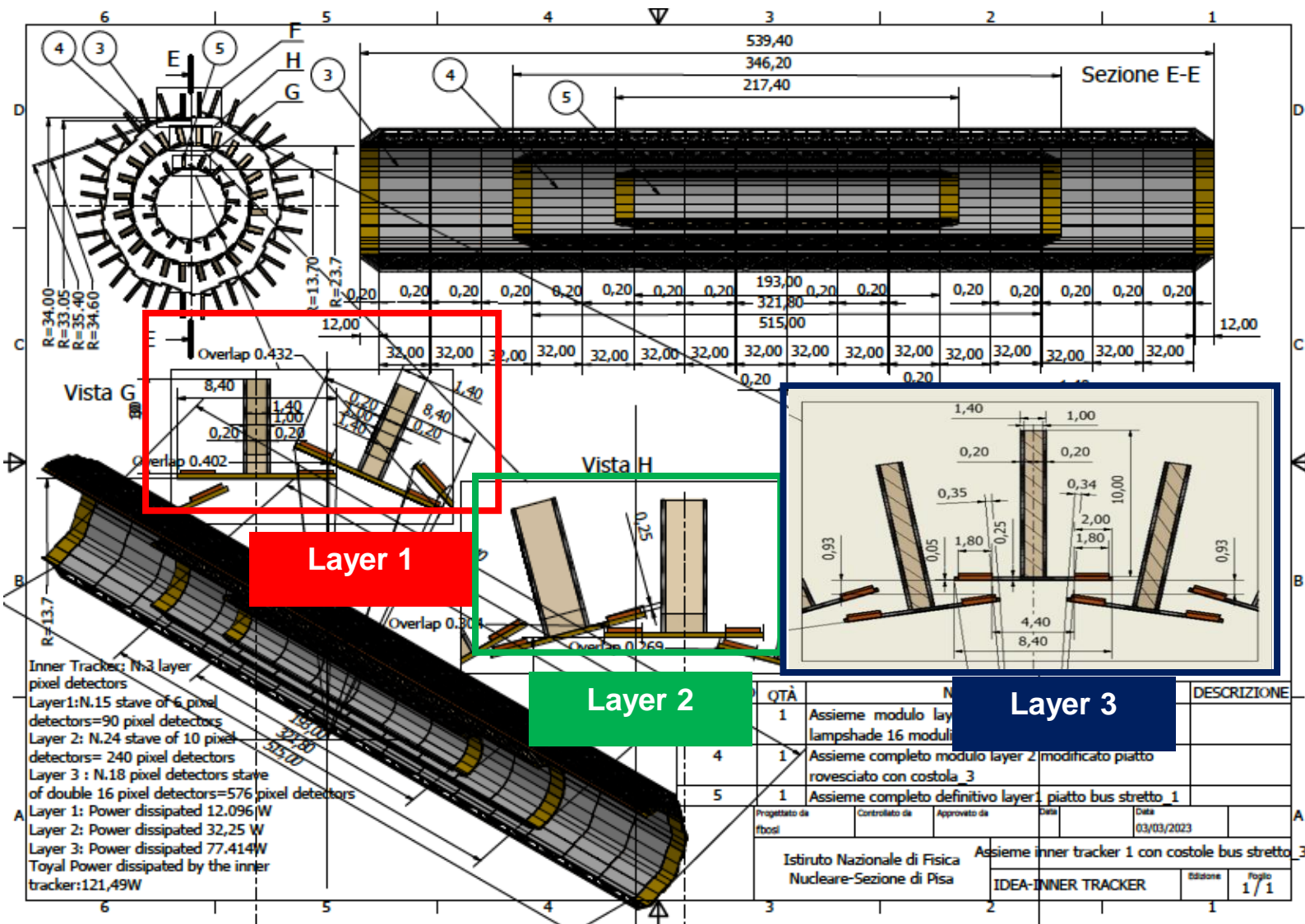
Total thickness 0.25% X_0

Power budget
 ~77 W

Overall Inner Vertex



Symmetric beam to avoid bend stress

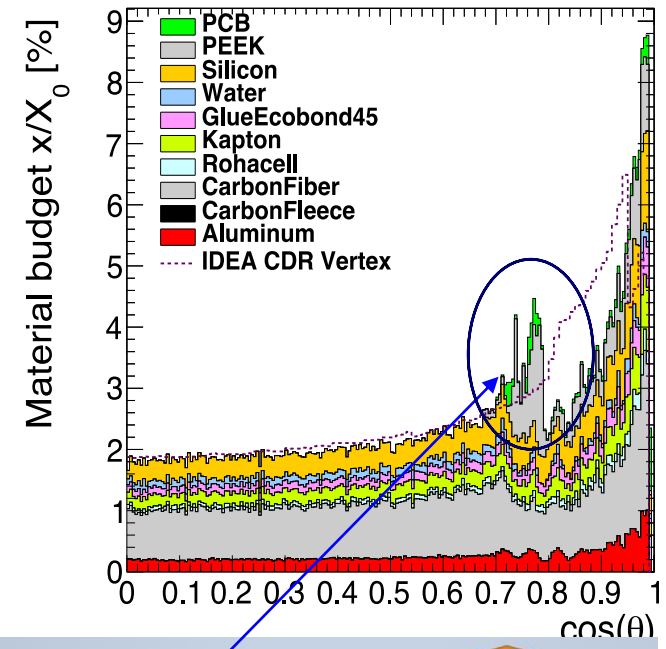
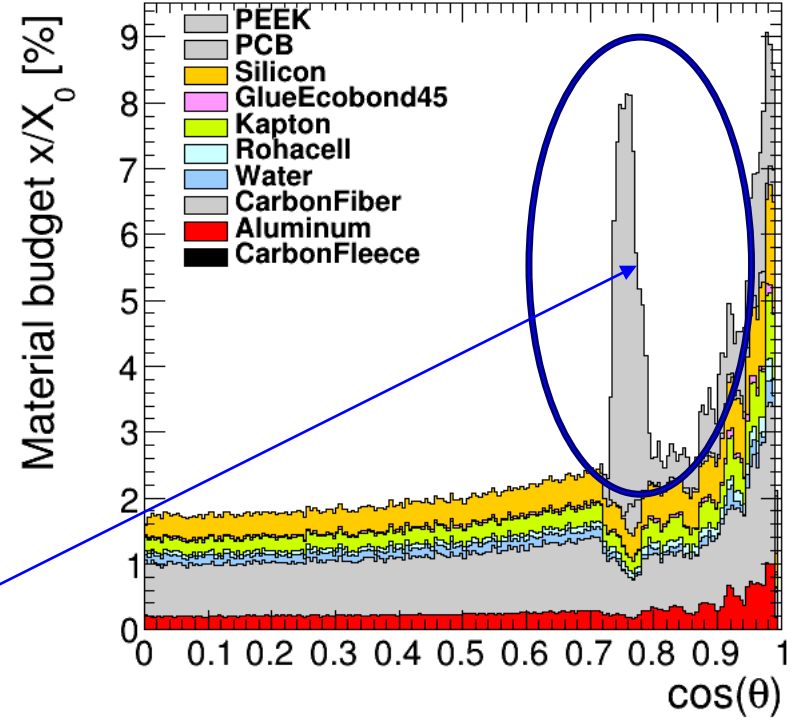
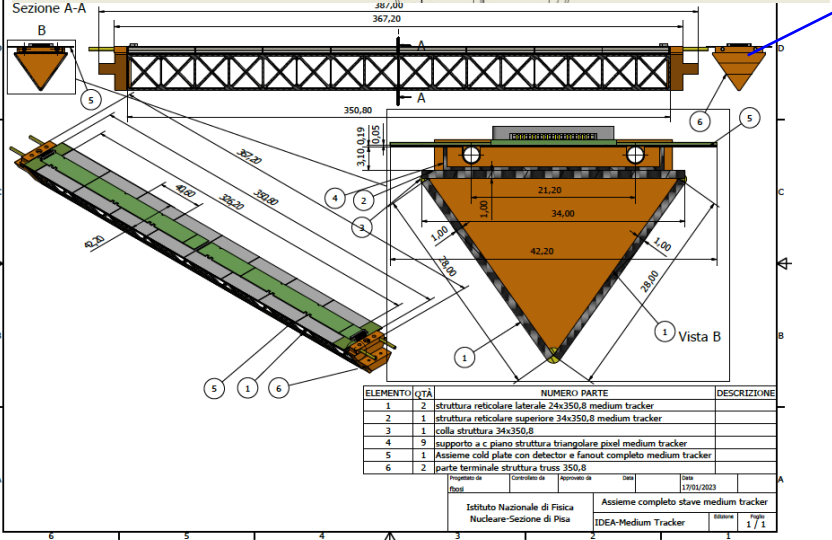
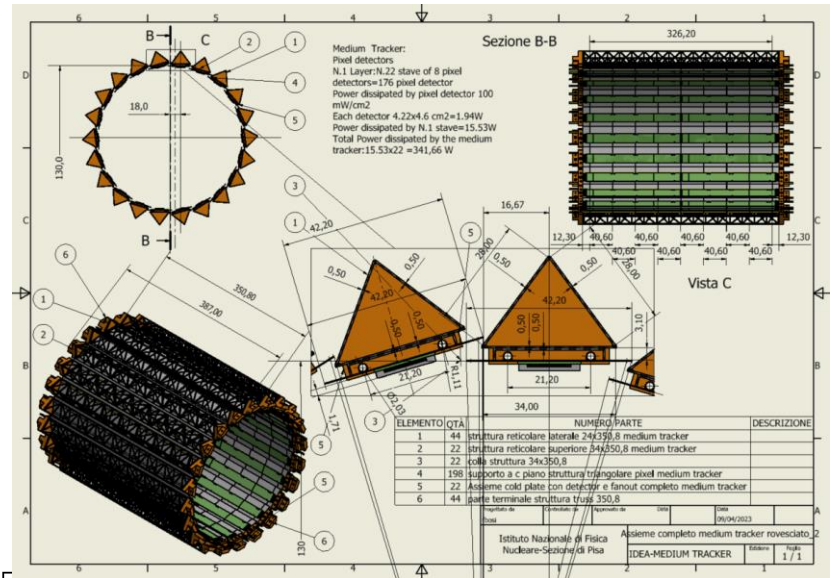


- Layer 1**
- Overlap to allow alignment ~500 μm
 - Pinwheel geometry
 - Total weight ~22 grams
 - Power 12 Watt

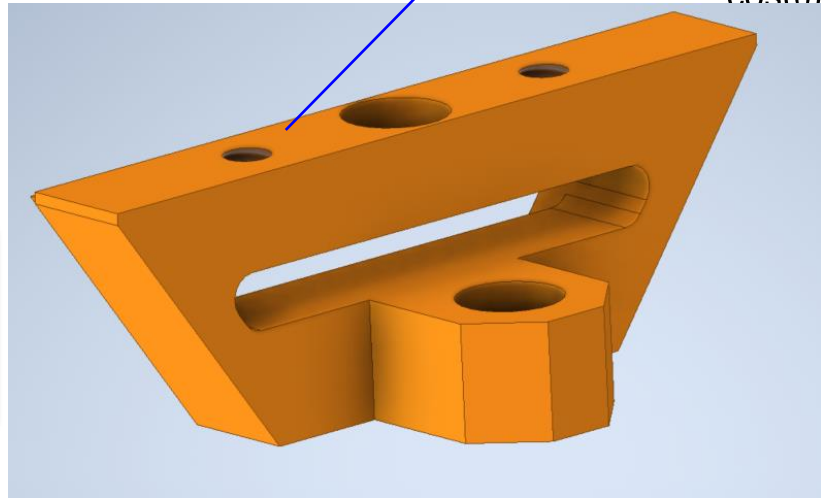
- Layer 2**
- Pinwheel geometry
 - Counter-rotated wrt layer 1
 - Total weight ~63 grams
 - Power 32 Watt

- Layer 3**
- Lampshade geometry.
 - Total weight ~150 grams
 - Power 77 Watt

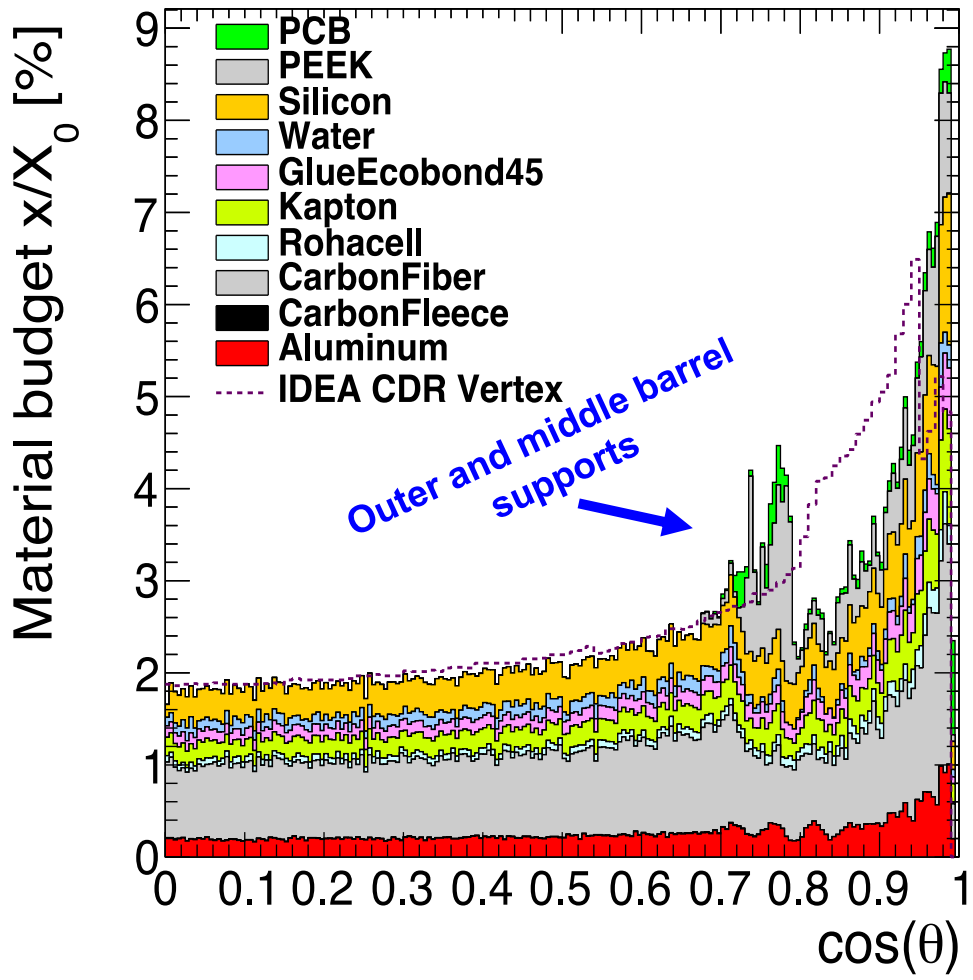
Middle/outer vertex supports optimisation



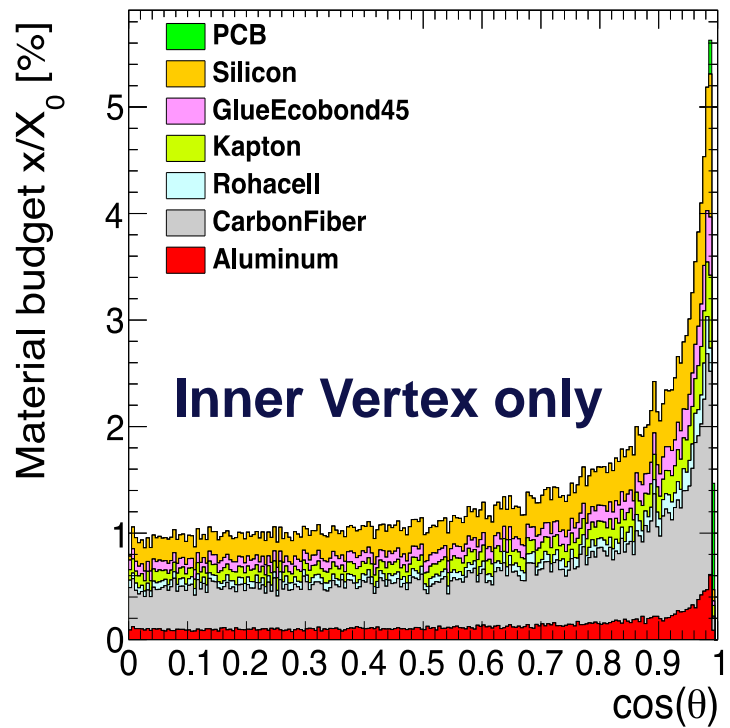
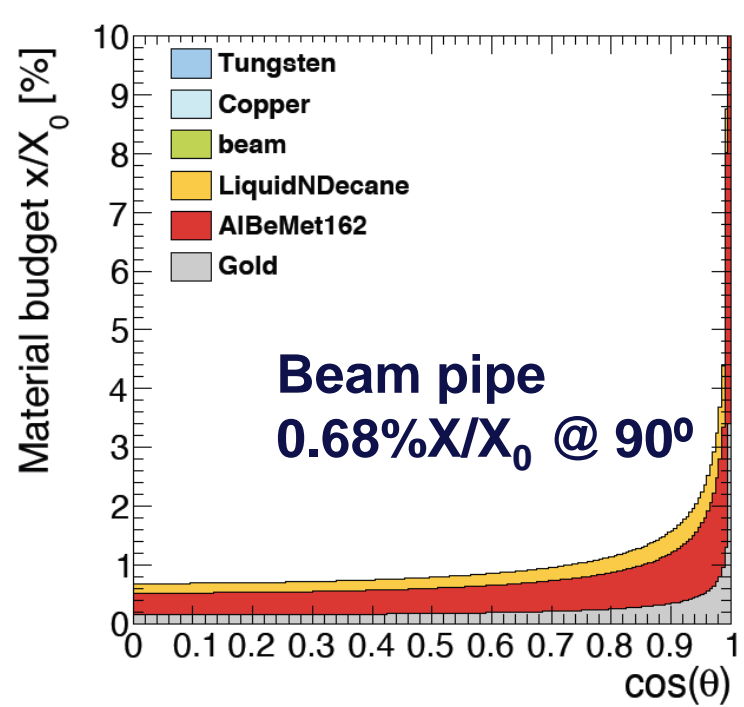
Shaped to minimize material at the end of the stave



Simulated material budget

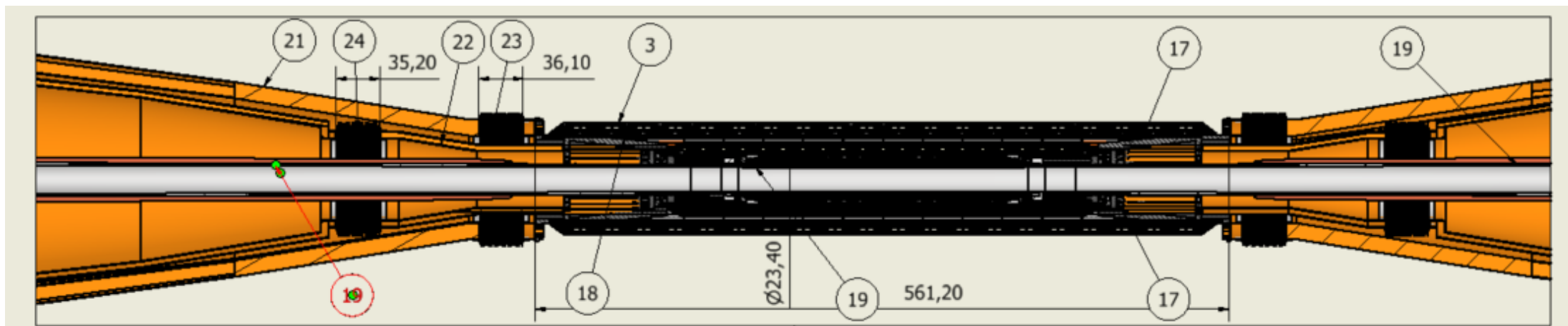
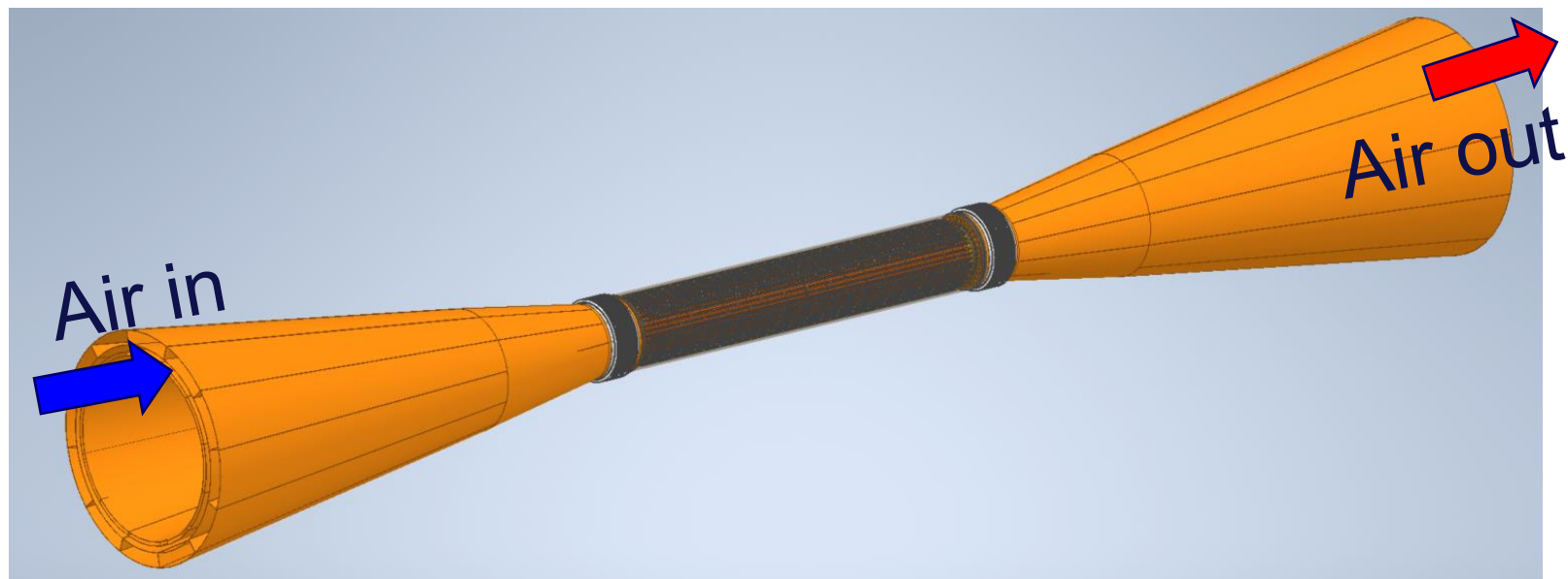


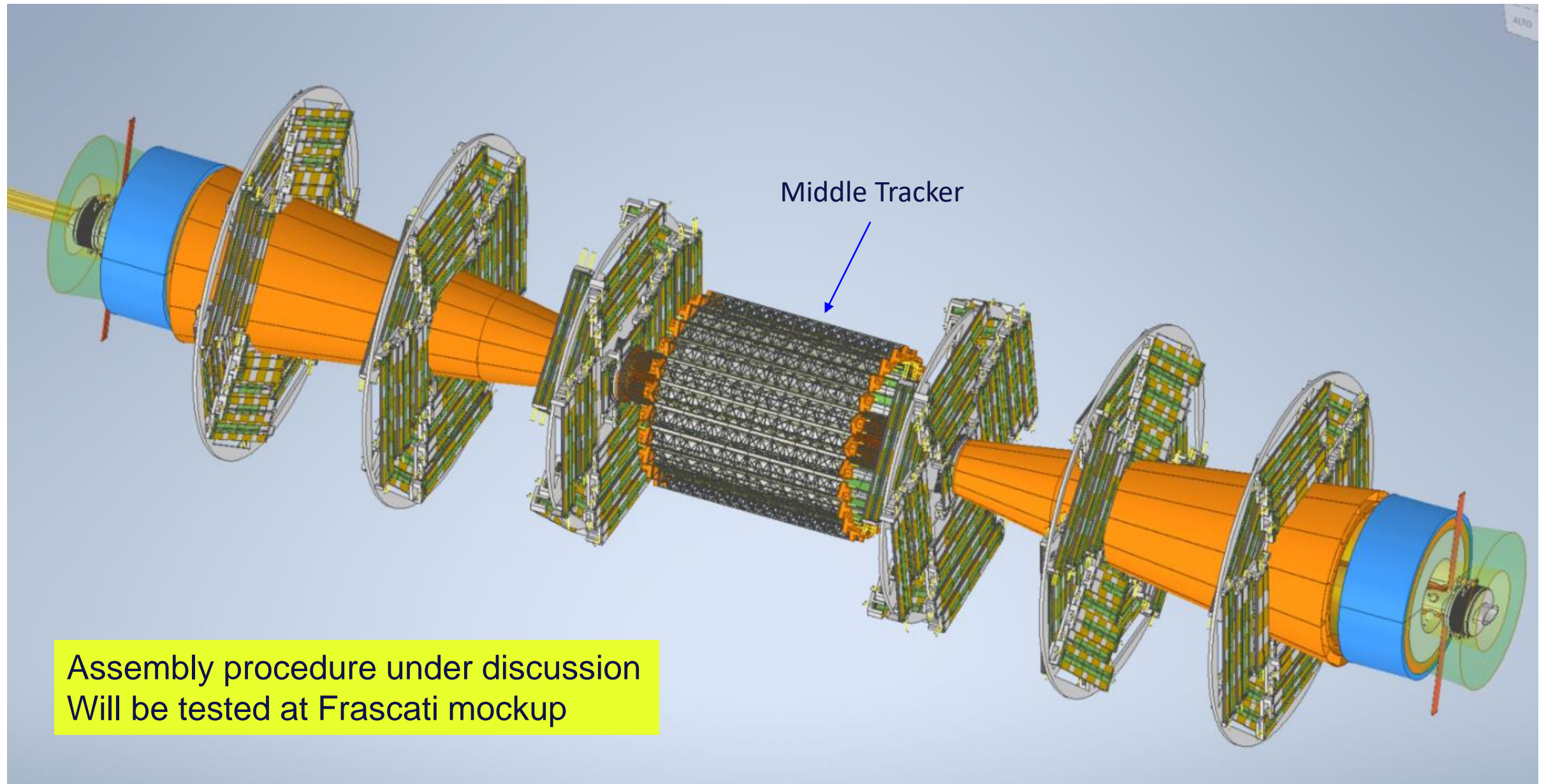
In agreement with CAD estimates
 Smaller X/X_0 wrt IDEA CDR estimates even including power and readout cables in the sensitive region
 Silicon only ~15% of the total



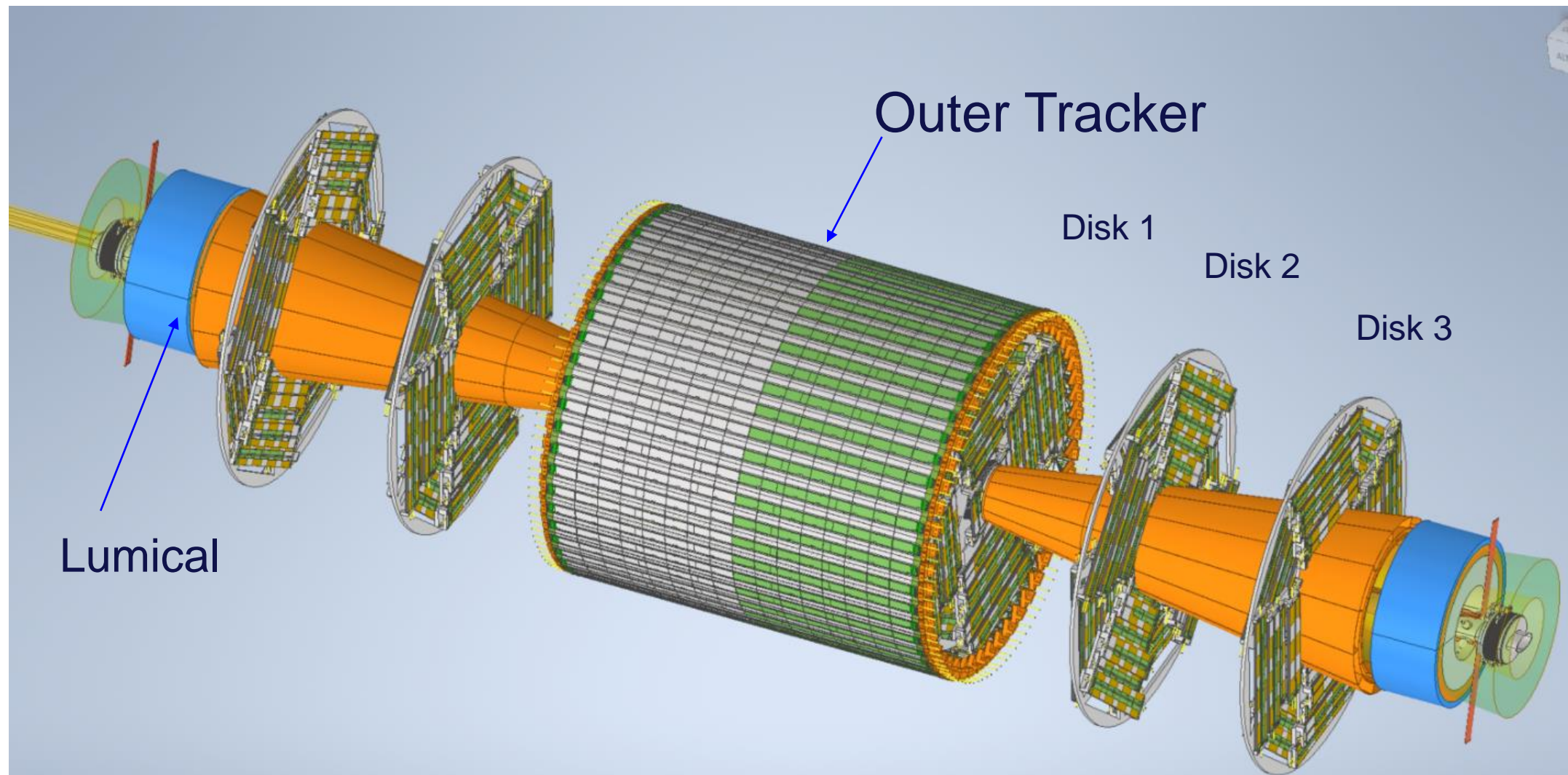
Air cooling + Cables cones

Elastically joined with bellows to the inner vertex to avoid stress.

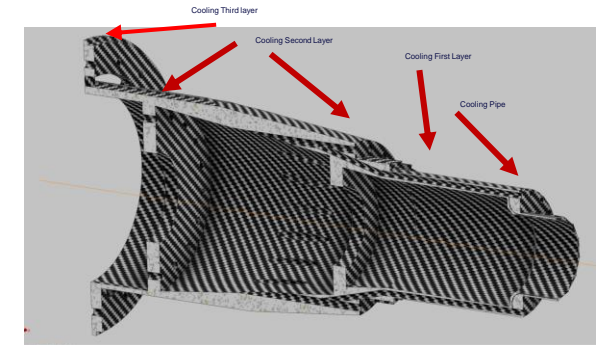
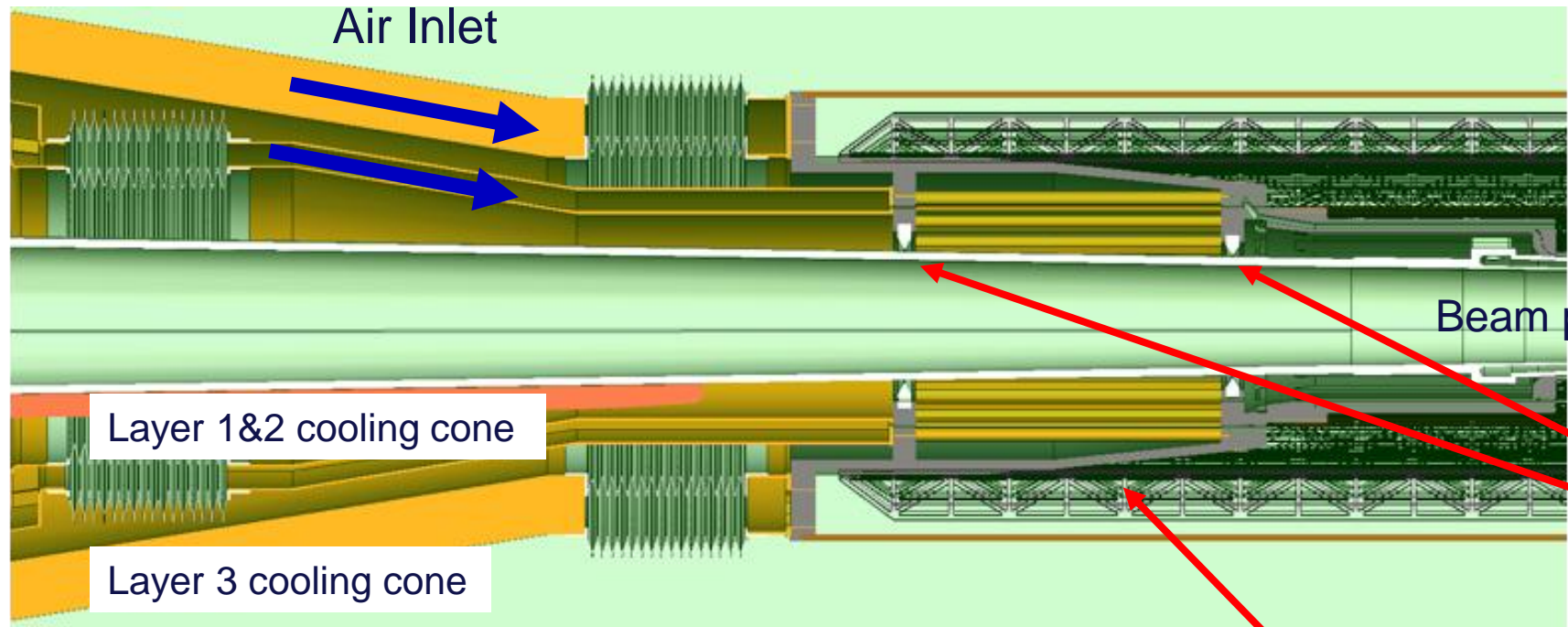




Total tracker



Inner vertex support and Carbon Fiber cooling cones



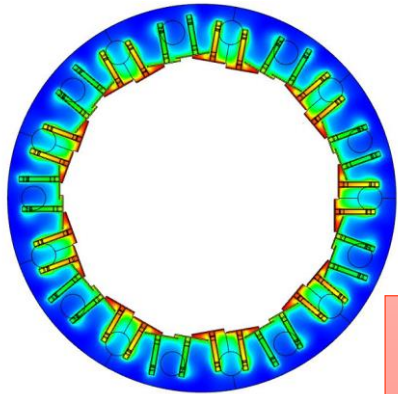
Beam pipe cooling manifold

Peek Support

Support cone

- Anchored to the conical chamber
- Air cooled
- Thermally isolated from the beam pipe during bakeout (150 °C), by peek supports

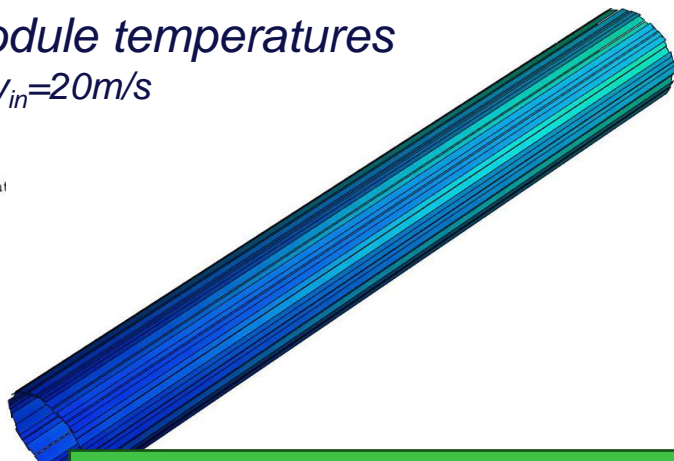
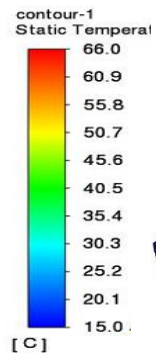
Air cooling simulations



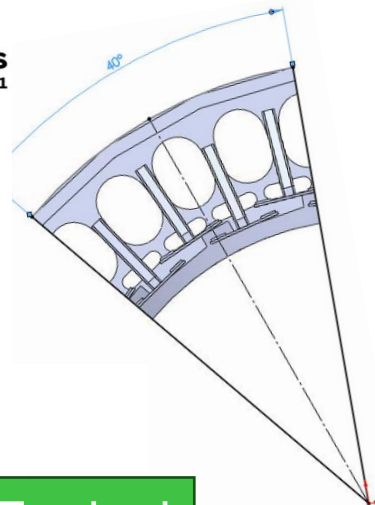
Layer 3 – largest power dissipation: 77 W

Optimization of flow rate
Compare Air with Helium
Max $\Delta T < 10^{\circ}\text{C}$ achievable

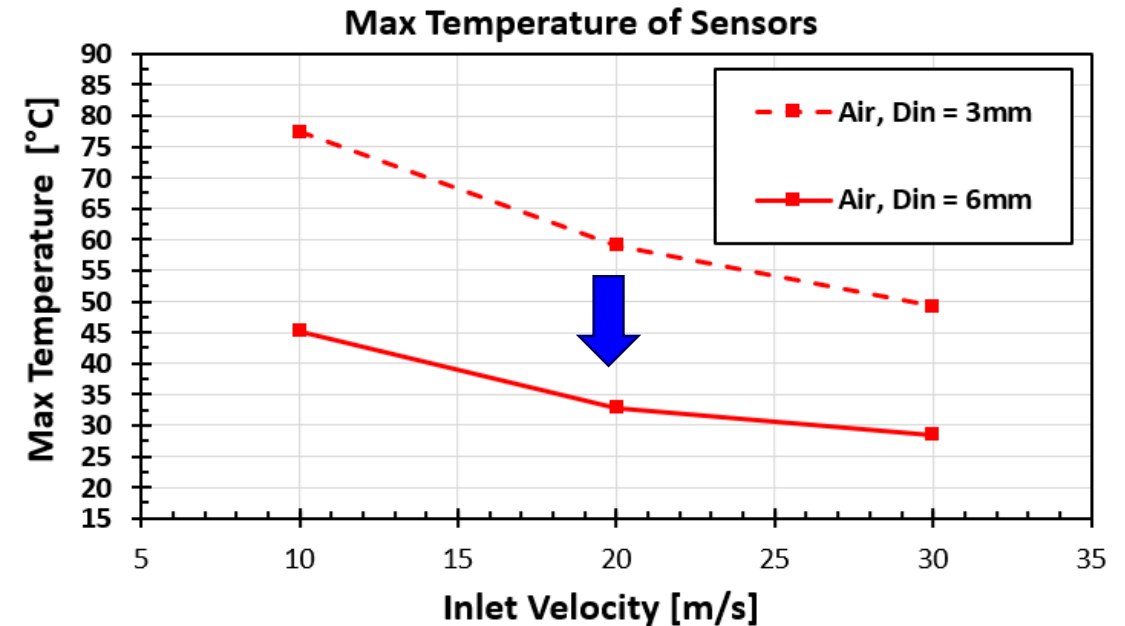
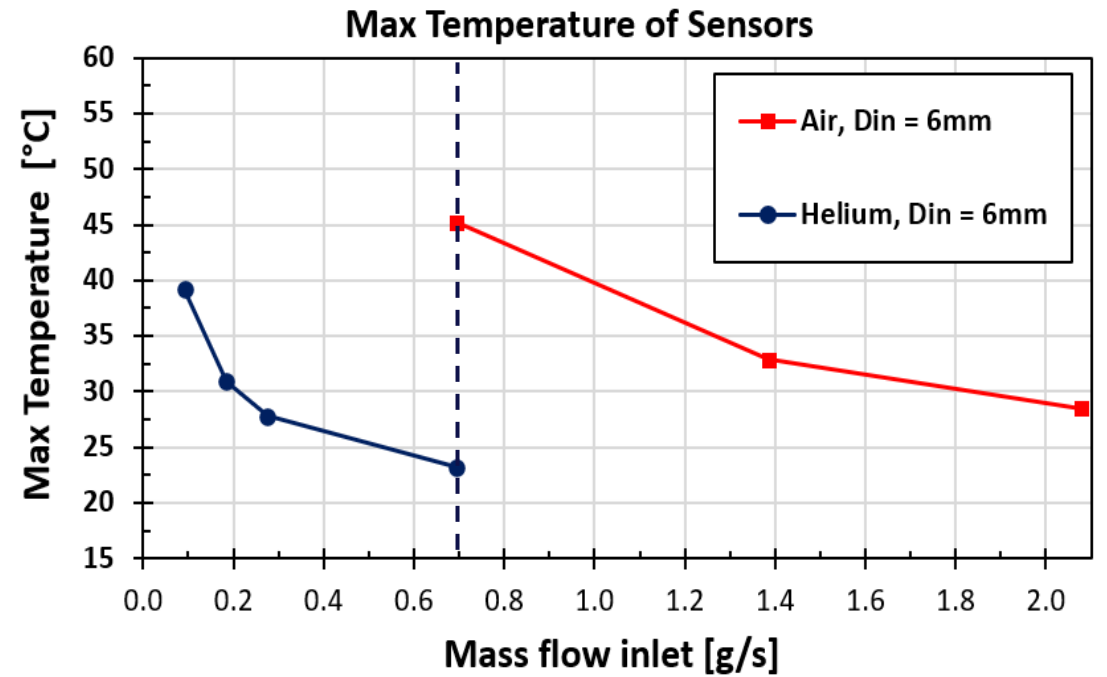
Module temperatures
@ $v_{in}=20\text{m/s}$



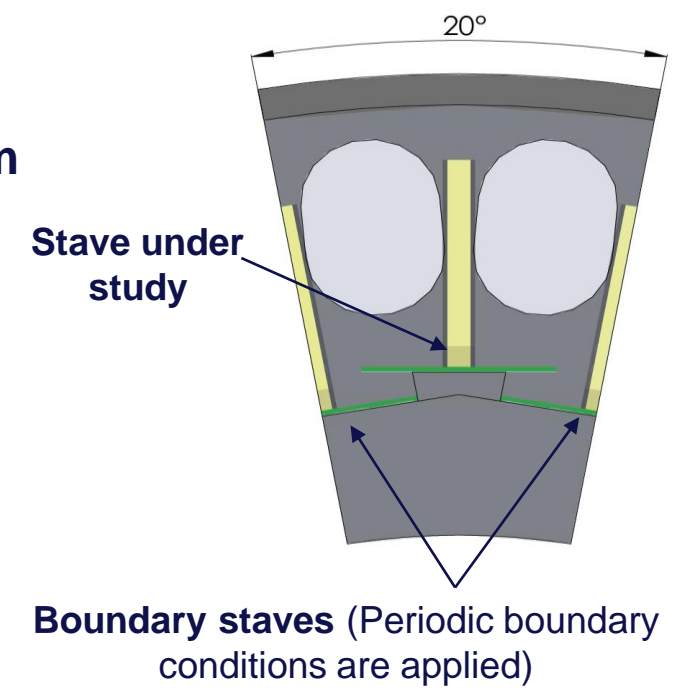
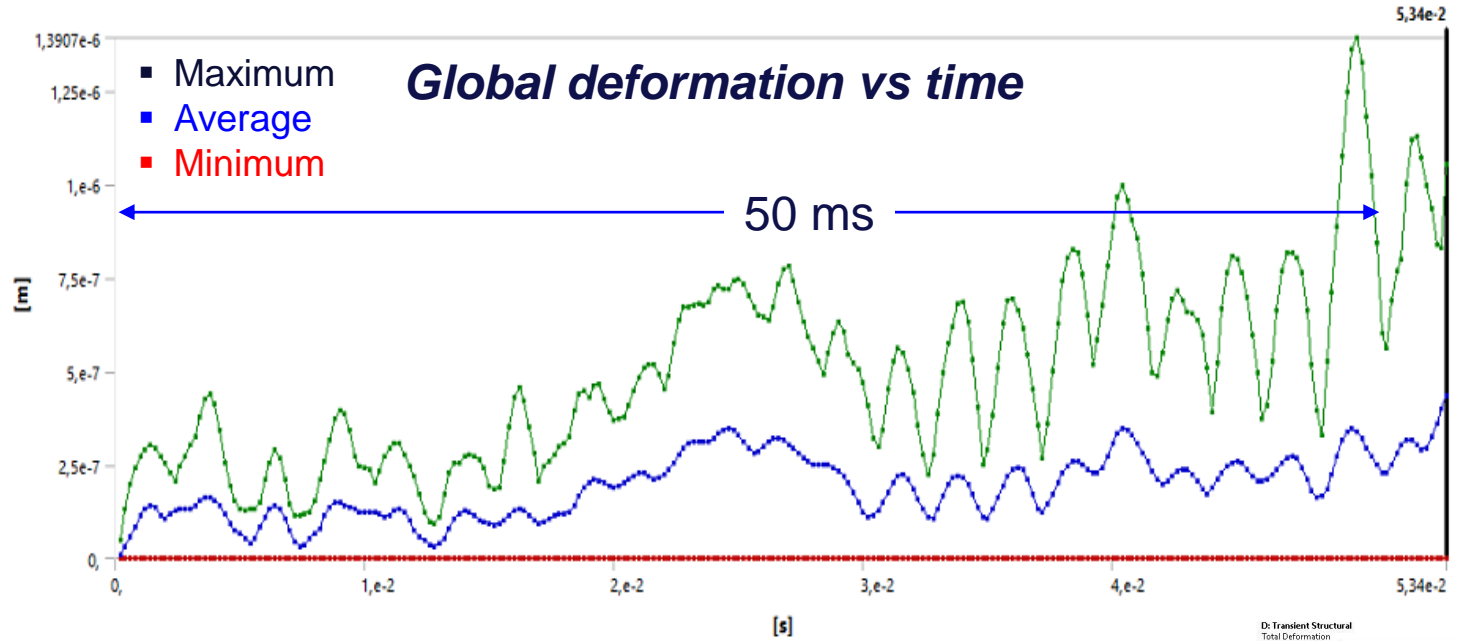
Ansys
2023 R1



See presentation of Cristiano Turrioni



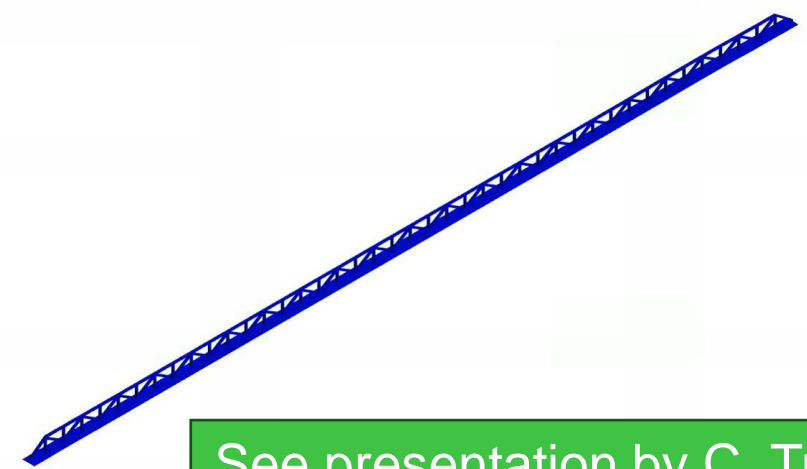
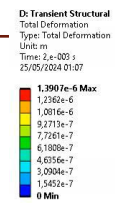
Transient mechanical analysis



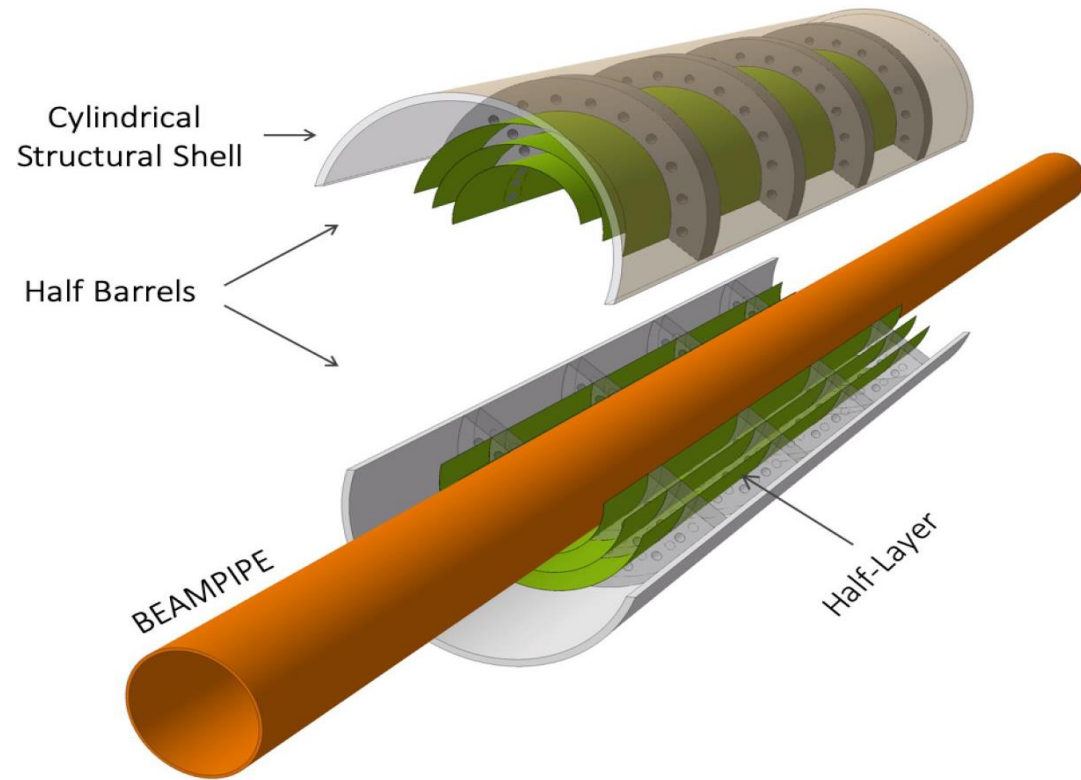
Maximum displacement ~ 1.5 μm @ $v_{in} = 10$ m/s due to first flapping mode – can be easily mitigated by redesign the supporting cone envelope.

More simulations ongoing changing boundary conditions.

A test setup will be made in Pisa and Perugia to validate the simulation



See presentation by C. Turrioni et al

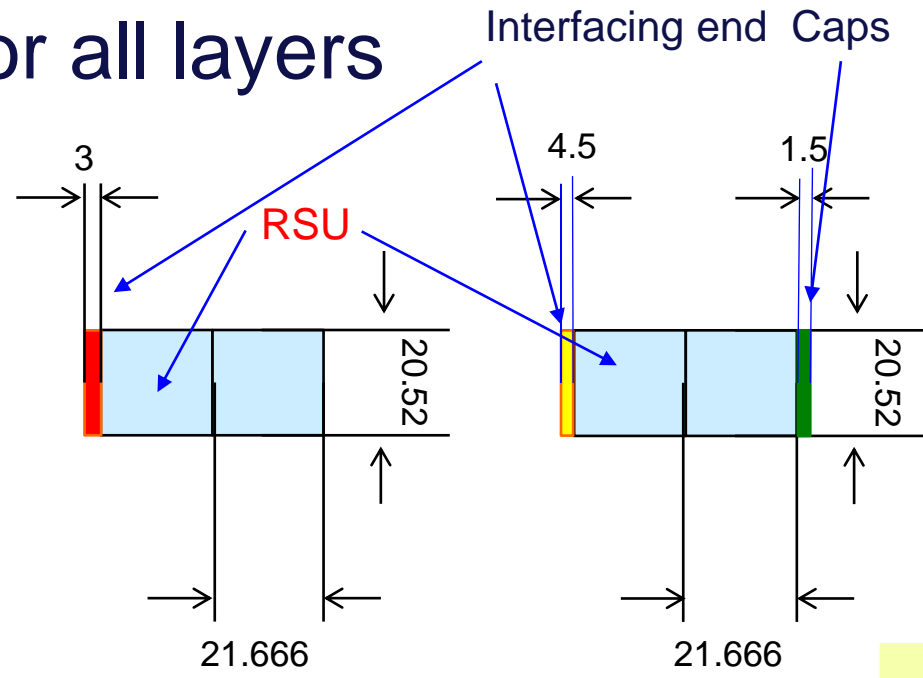
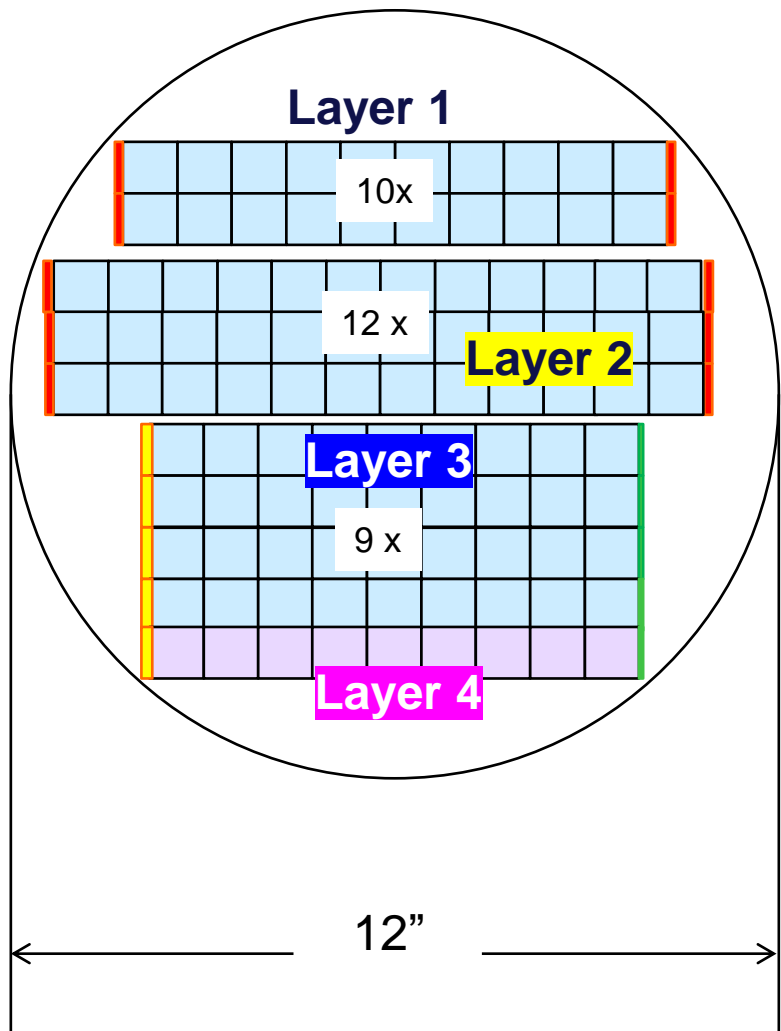


Lightweight layout using an ALICE ITS3 inspired design

(~0.05 % X/X_0 material budget per layer – 5 times less than the Mid-Term one)

After fruitful discussions with C. Gargiulo, A. Junique, G. Aglieri Rinella, W. Snoeys

Same reticle for all layers



Layer	Radius (mm)
1	13.7
2	20.23
3	26.76
4	33.3

Layer 1&2

Layer 3&4

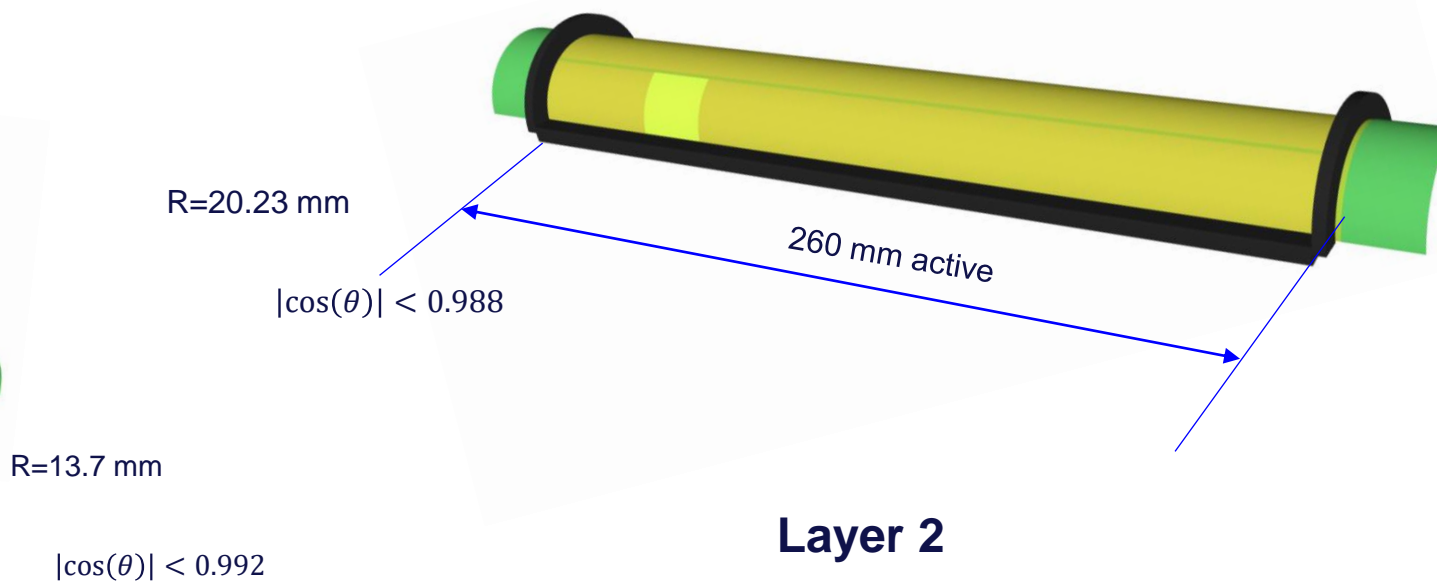
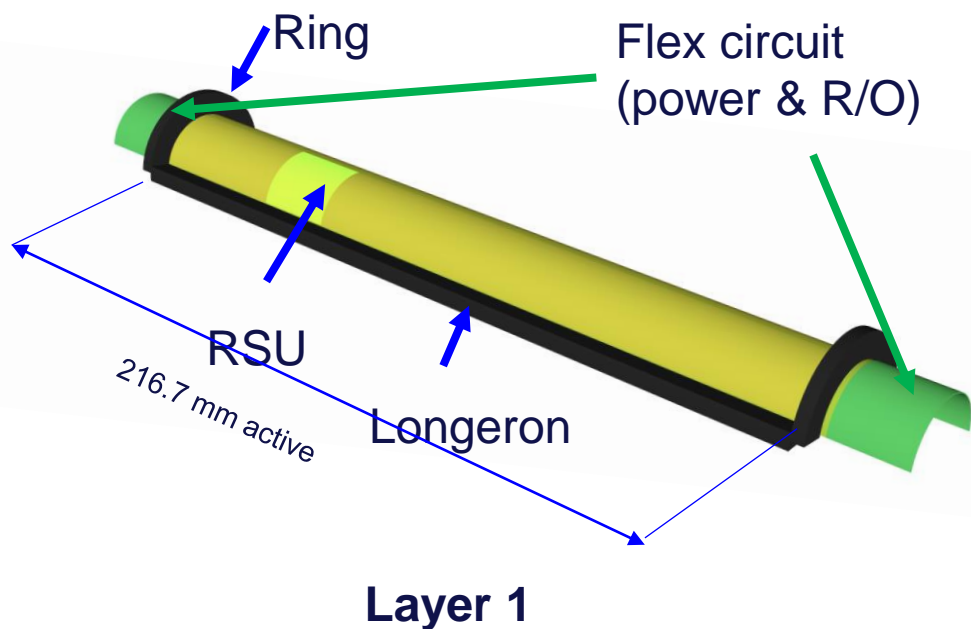
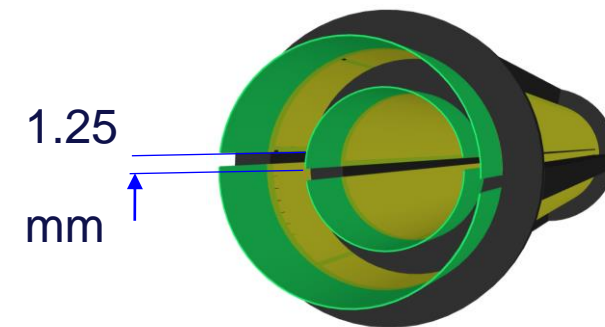
	Power density [mW cm ⁻²]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Power dissipation in ITS3 (not necessarily the same for FCC-ee)

- RSU ~ 50 mW/cm² (depends on Temp.)
- LEC ~ 700 mW/cm²

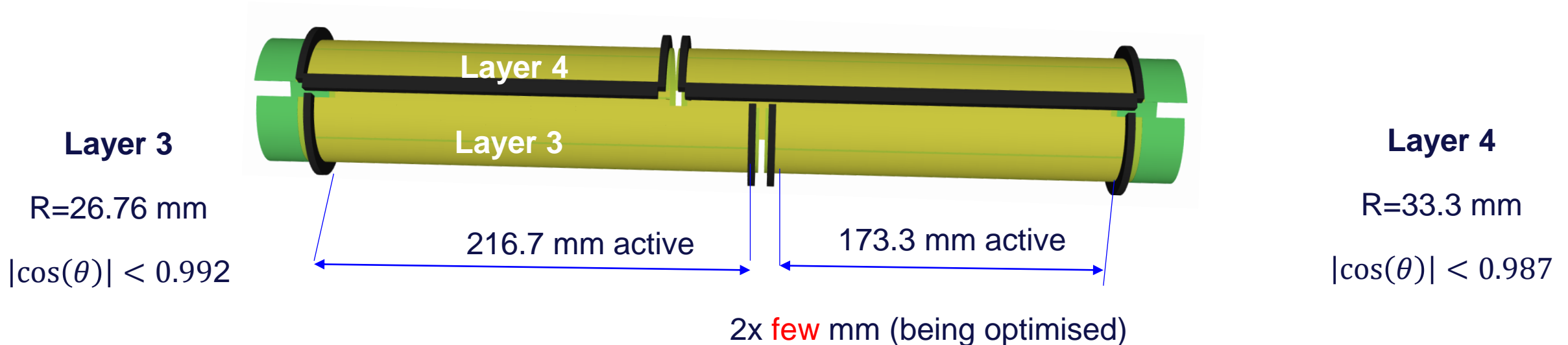
Layers 1 & 2

- Single stitched wafer
 - Readout and power from both sides (reduces transmission off-detector and limits power dissipation in the endcaps)
- Leaves ~1.25 mm* insensitive gap in R-phi, to account for assembly tolerances

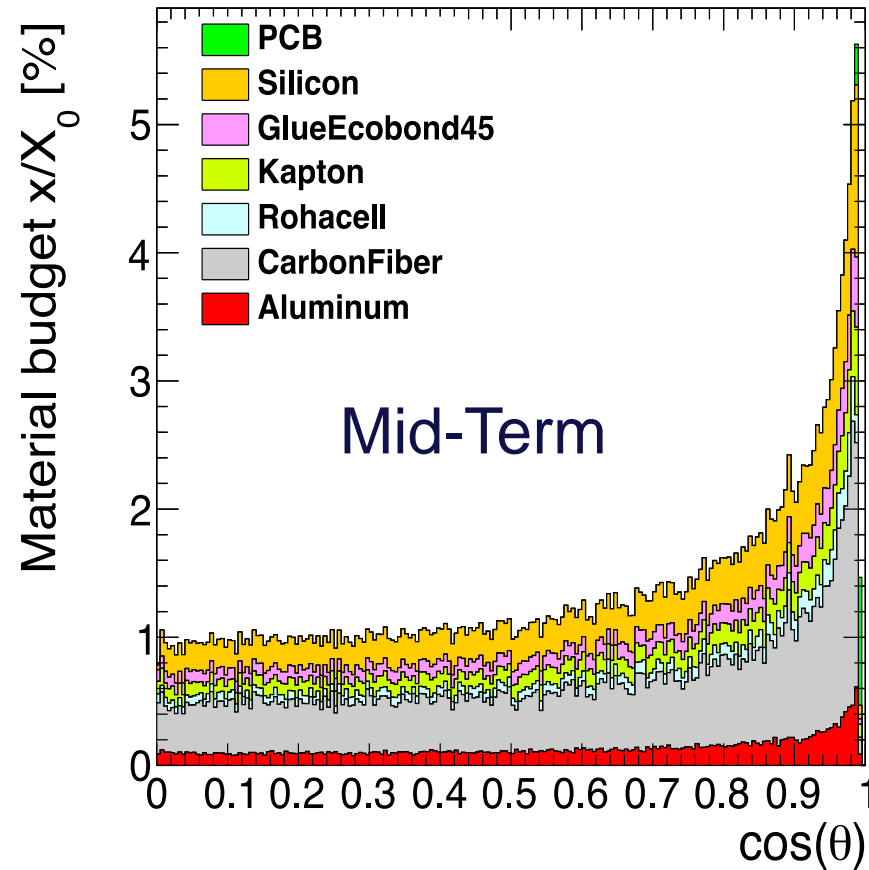
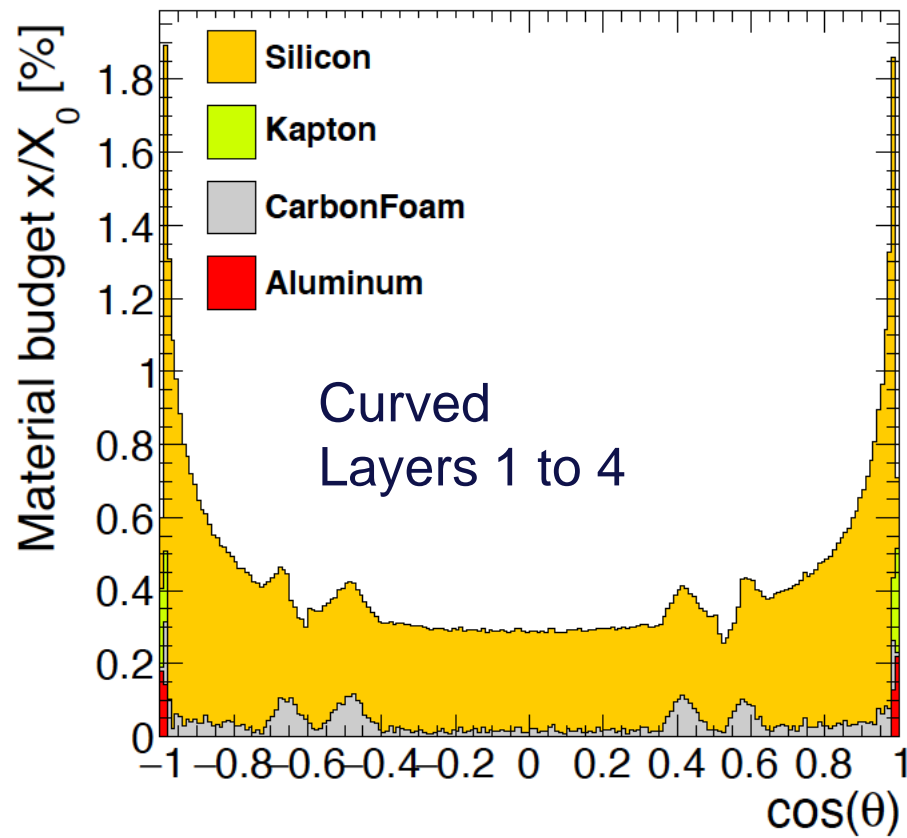


Layers 3 & 4

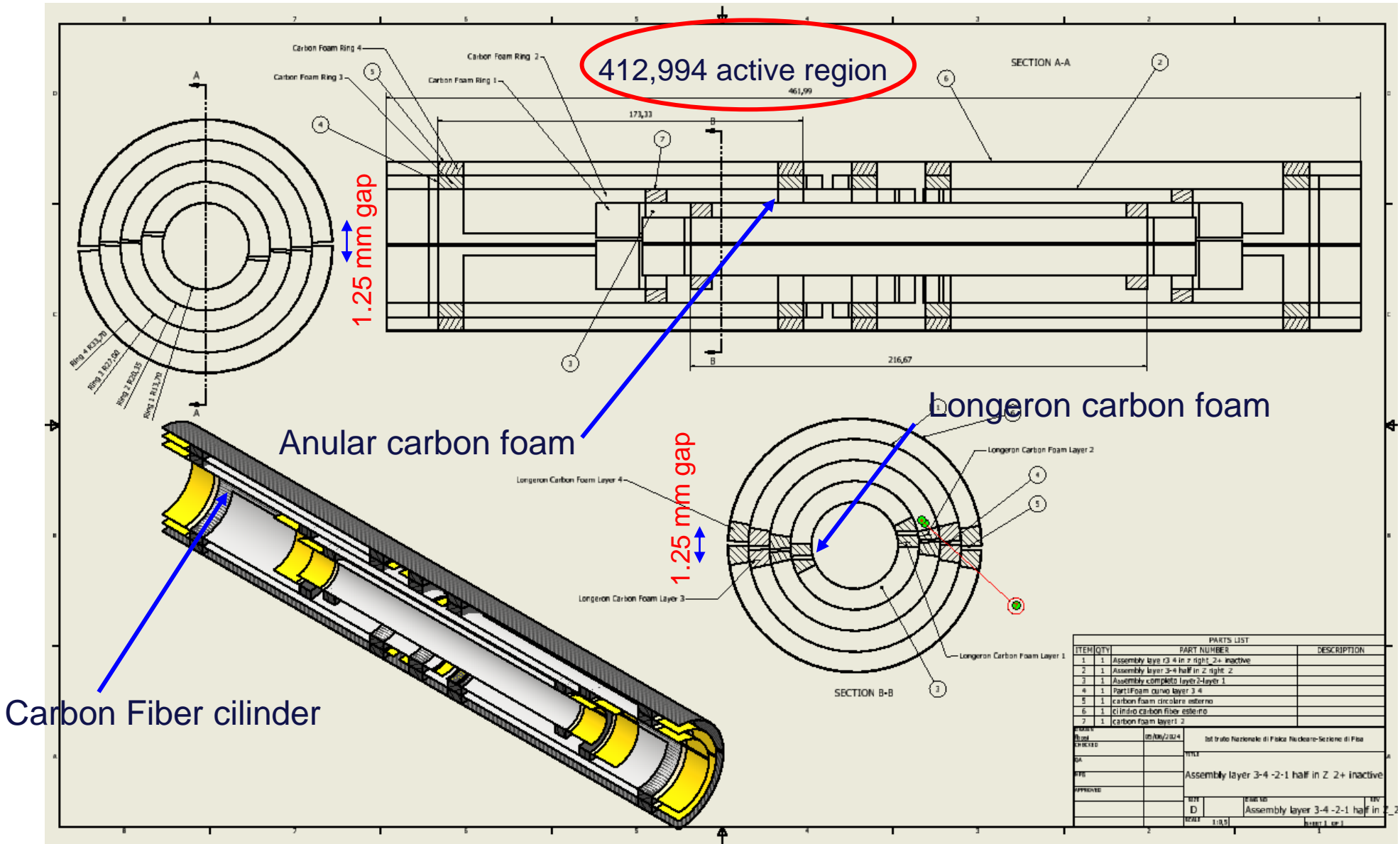
- Four “quarter” layers to allow ~same angular coverage for all layers and use 12” wafers
- **Layer 4 has the same length of Layer 3 but higher radius**
- Quarter readout only on one side, the other only for power (wire)
 - Gap of ~ 2xO(10 mm) at $|z| \sim 2.2$ cm: **quarters with non-symmetric layout** (left quarter with 10 RSU and right one with 8 RSU, and swapped for L4)



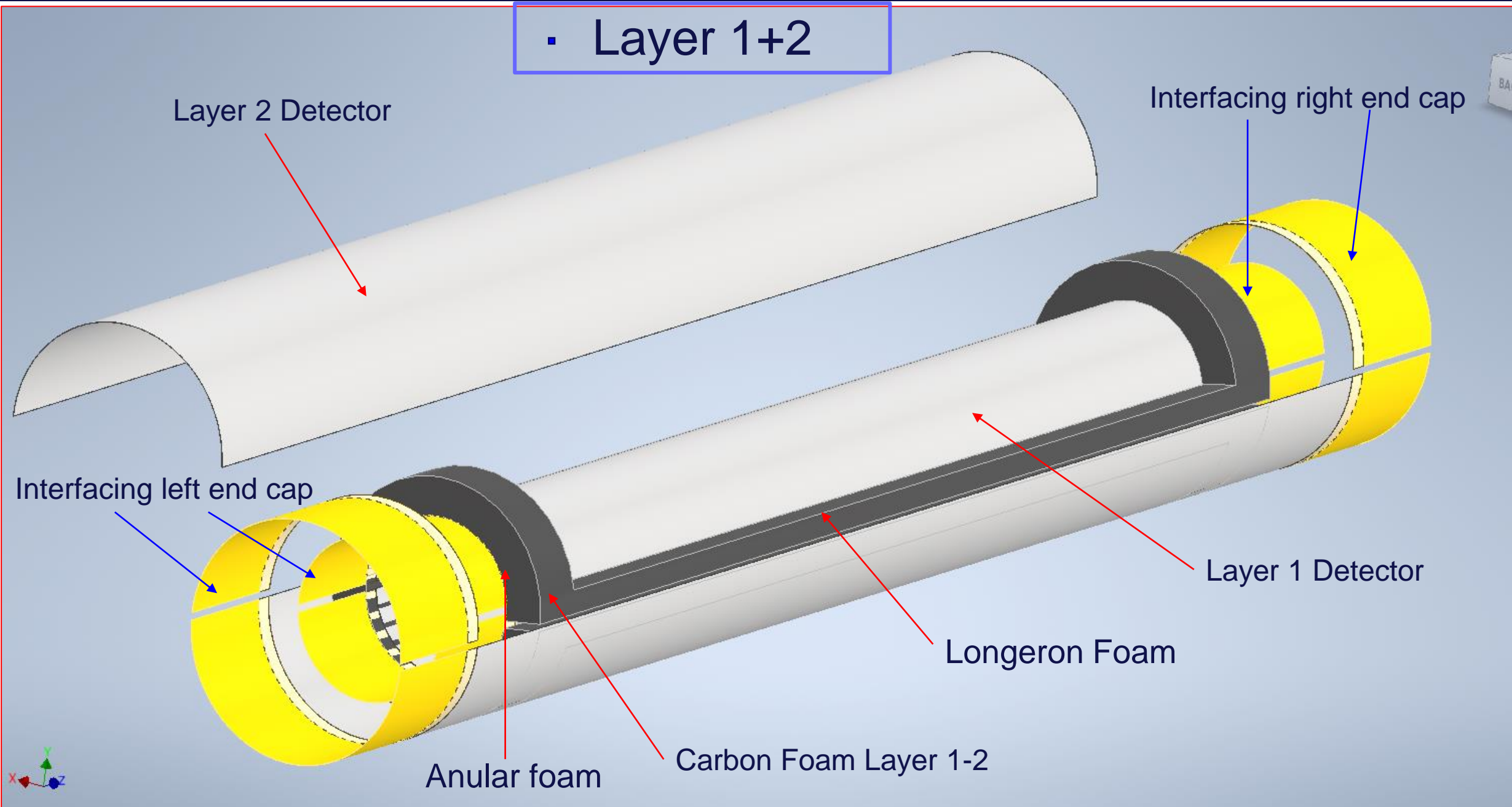
Material budget inner vertex



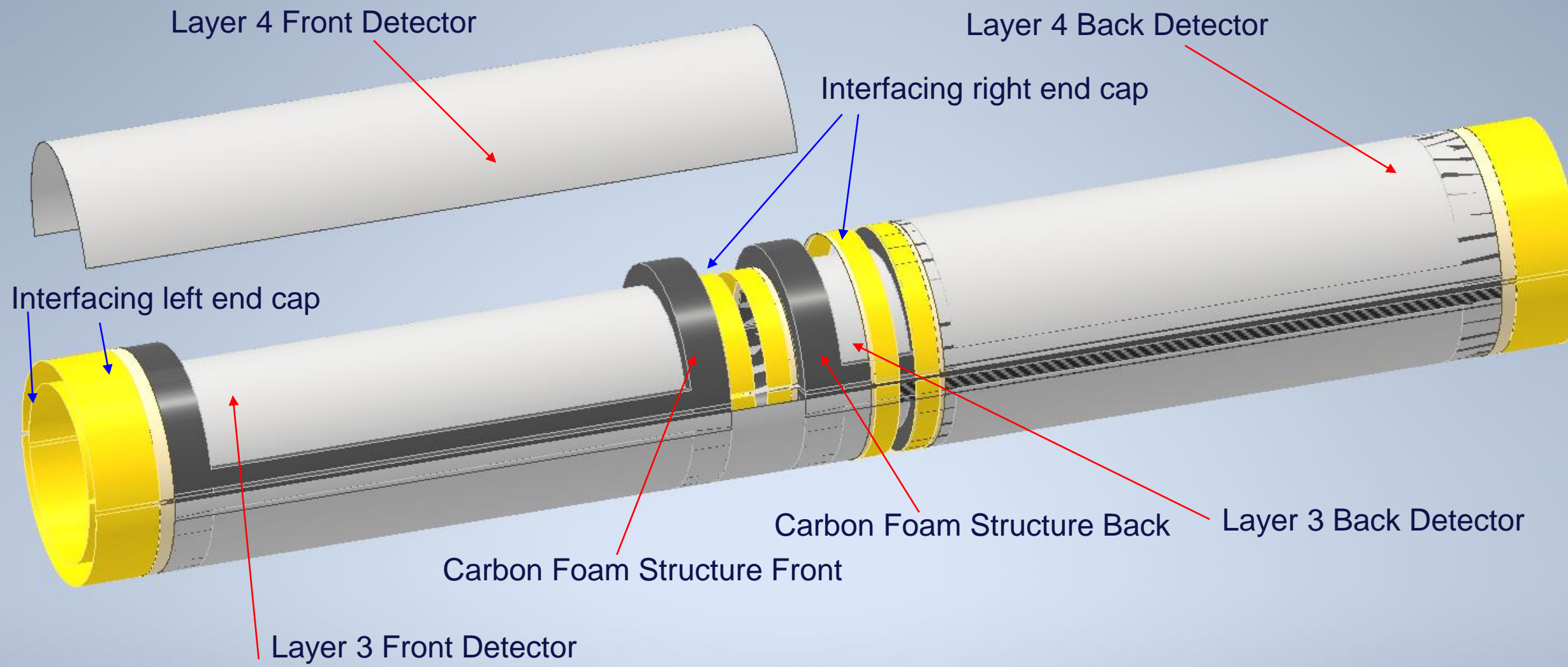
Starting engineering layout



▪ Layer 1+2



Layer 3+4



Fanout Layer 1

N.4 electronic board/side for Data&control

N.4 electronic board for Power

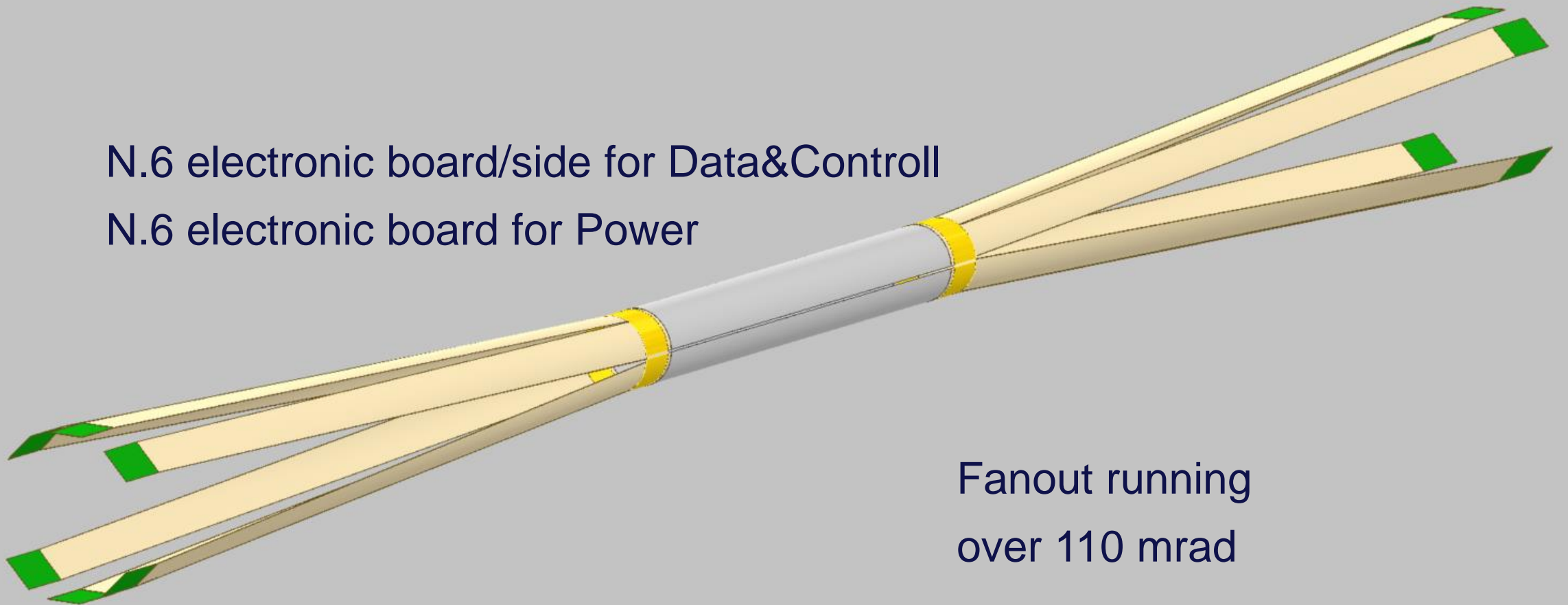
Fanout running
over 110 mrad



Fanout Layer 2

N.6 electronic board/side for Data&Control

N.6 electronic board for Power

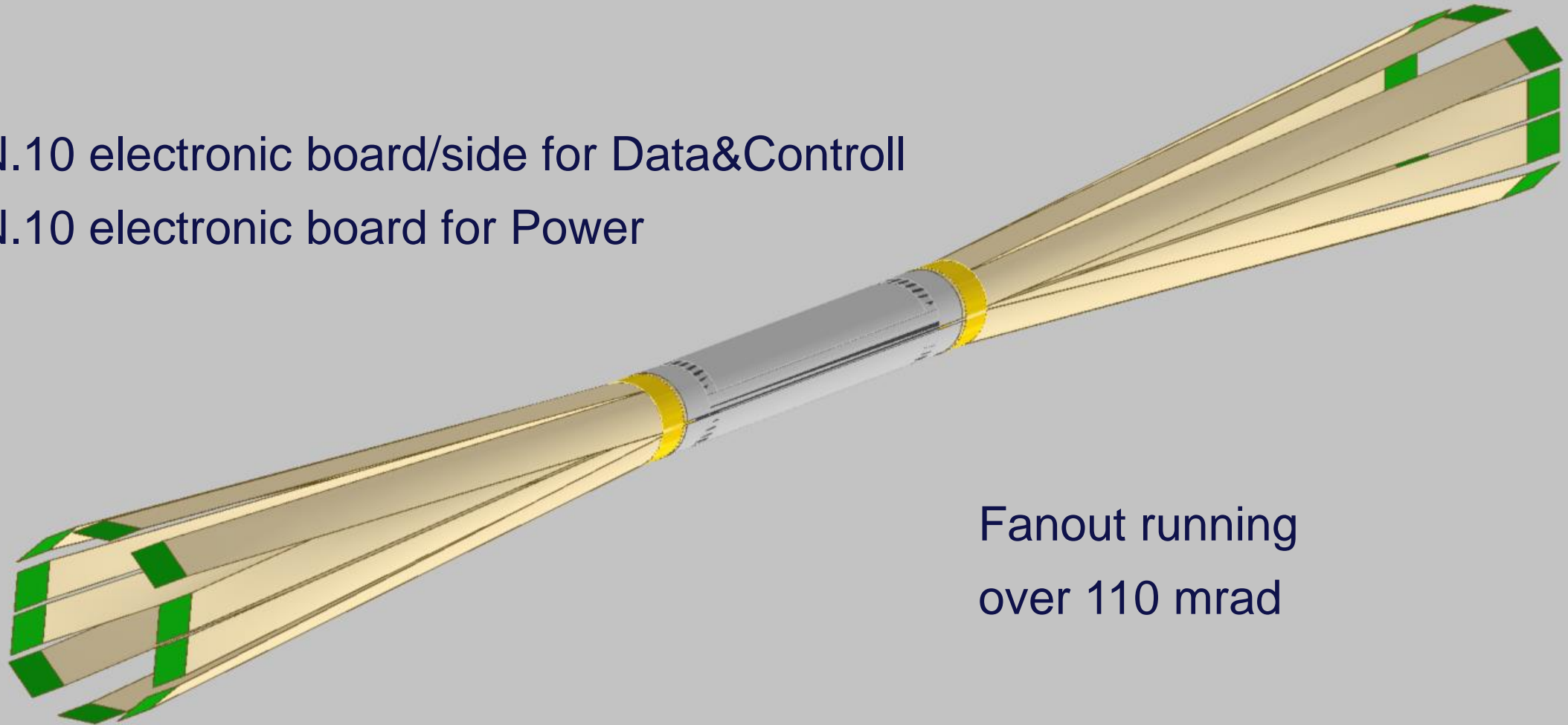


Fanout running
over 110 mrad

Fanout Layers 1+2

N.10 electronic board/side for Data&Controll

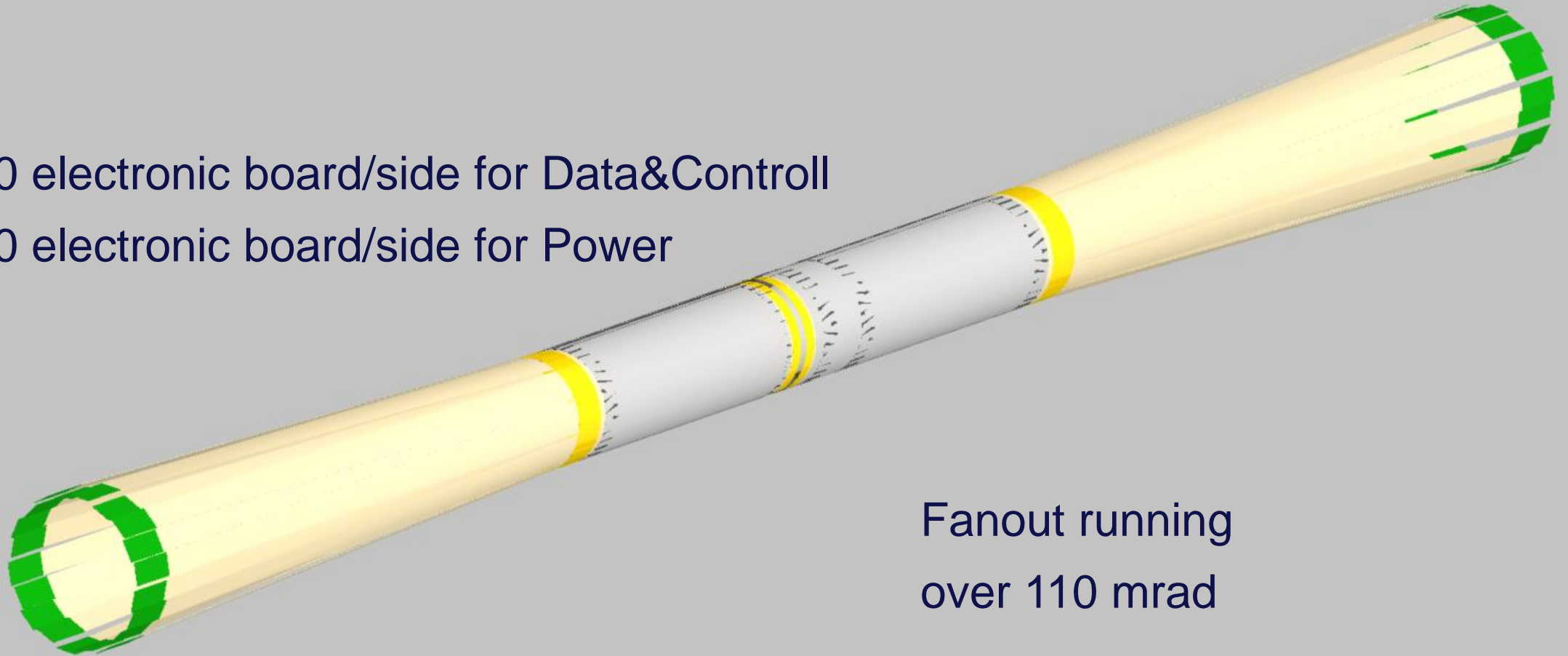
N.10 electronic board for Power



Fanout running
over 110 mrad

Fanout Layer 3+4

N.20 electronic board/side for Data&Control
N.20 electronic board/side for Power



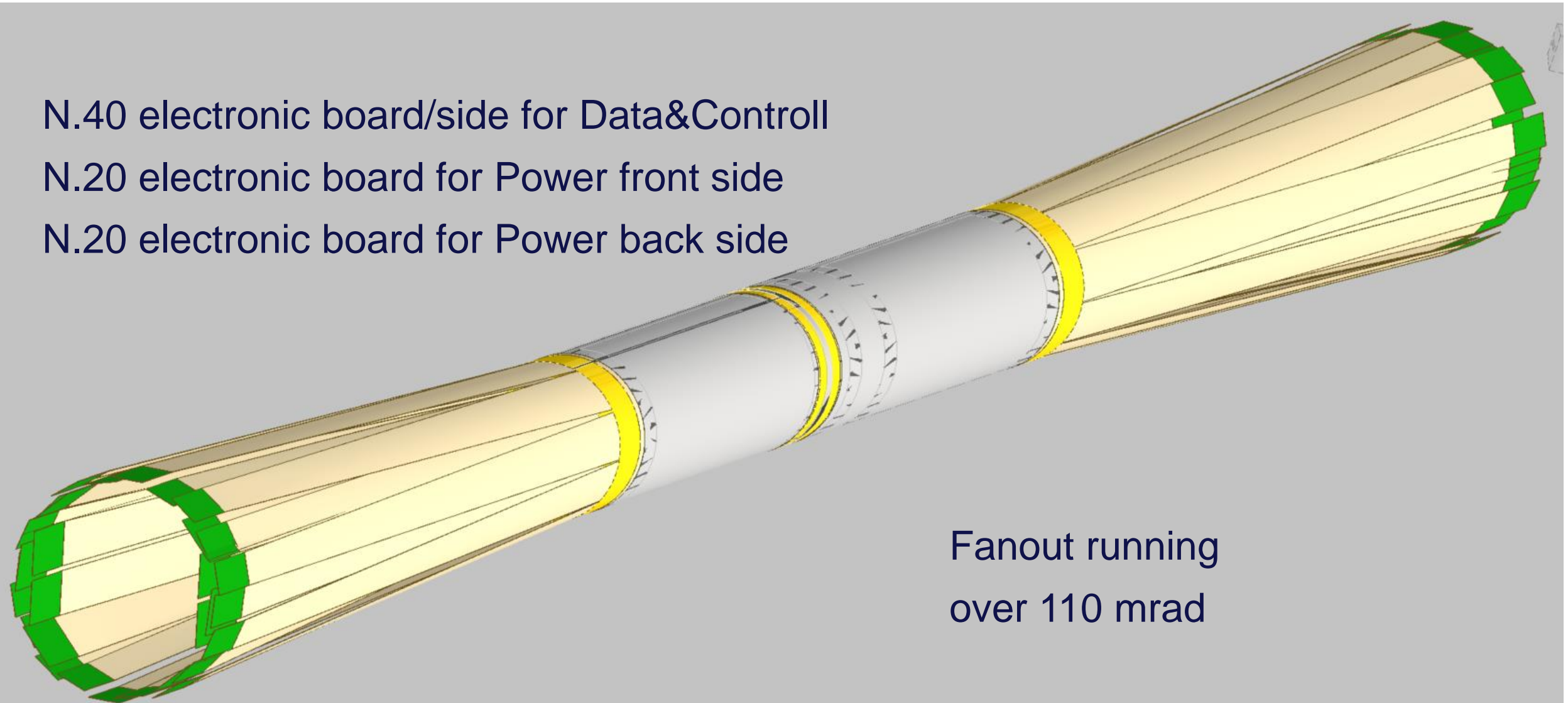
Fanout running
over 110 mrad

Fanout Layer 1+2+3+4

N.40 electronic board/side for Data&Control

N.20 electronic board for Power front side

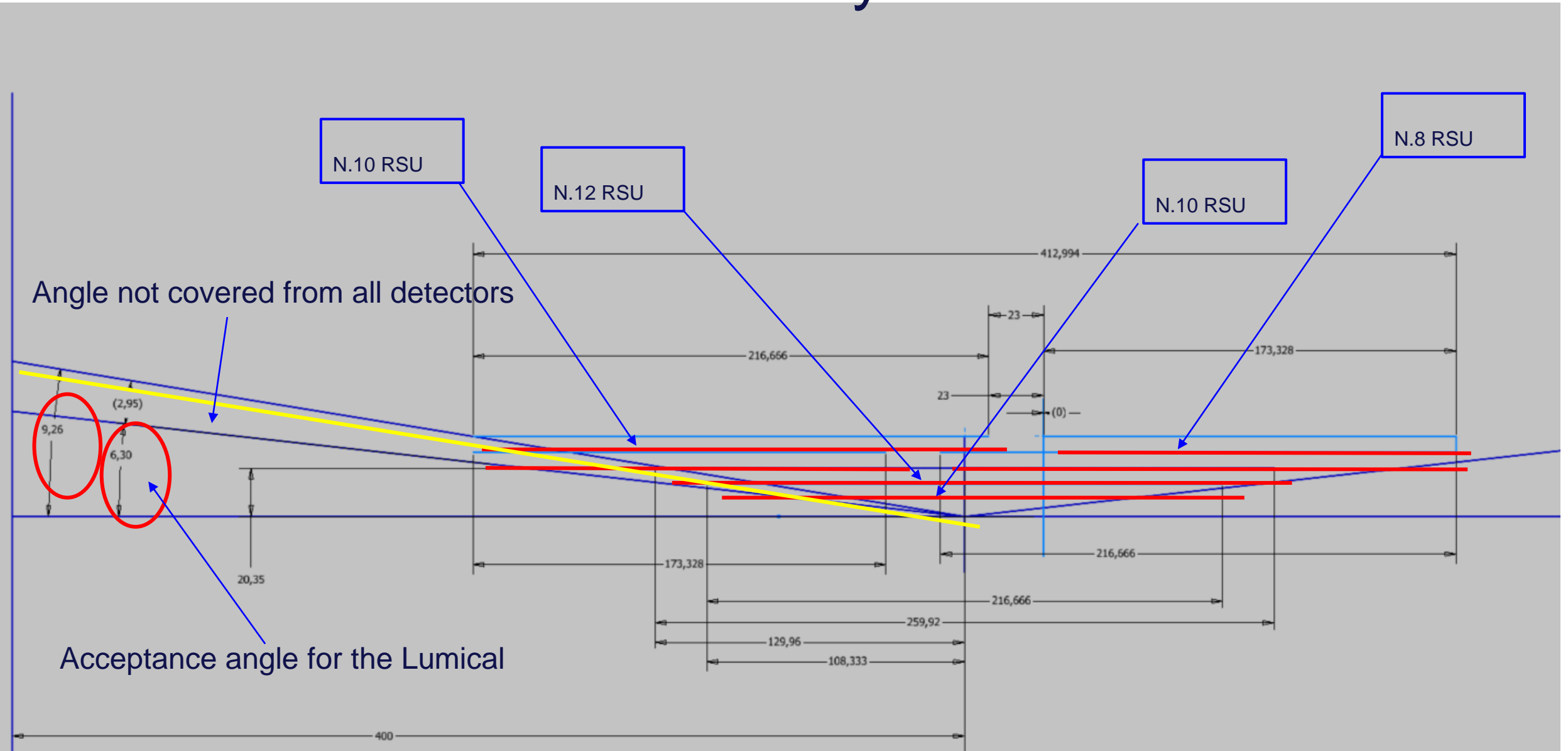
N.20 electronic board for Power back side



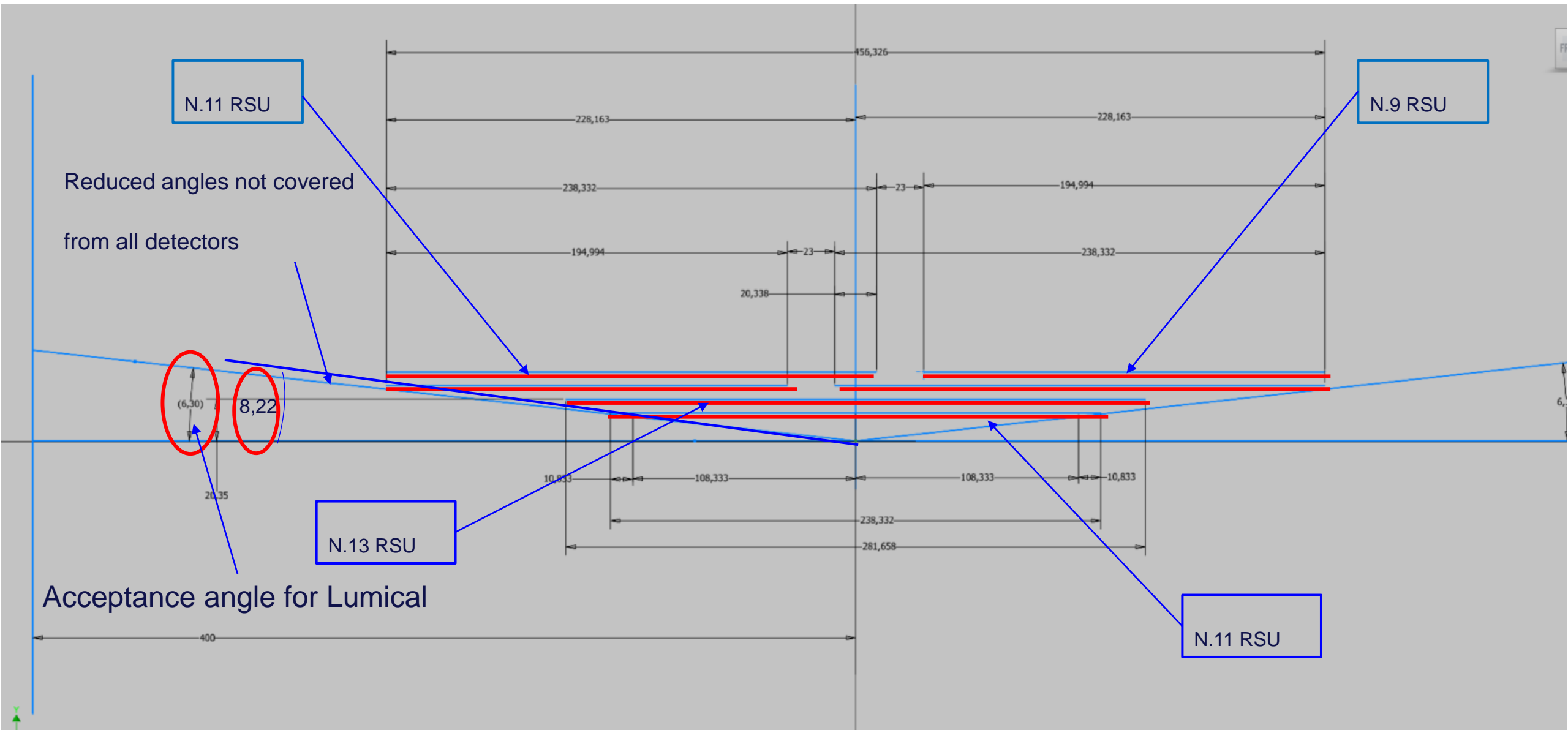
Fanout running
over 110 mrad



Problems with actual layout Curved Vertex



New Layout Curved Vertex



Conclusions and next steps

- **A Vertex Detector layout has been engineered**
 - Integration with the machine elements being developed
 - Services integration and cooling being finalised
 - Thermal and structural simulations look promising
 - A test setup is being constructed to validate simulations
 - Useful iterations between designers and simulations to keep material budget under control
- **A lighter concept with curved and stitched MAPS is being engineered**
 - First layout done
 - New Layout in progress
 - Engineering drawings started, having in mind construction sequence
 - Cooling (air) and flex circuits routing will be addressed shortly

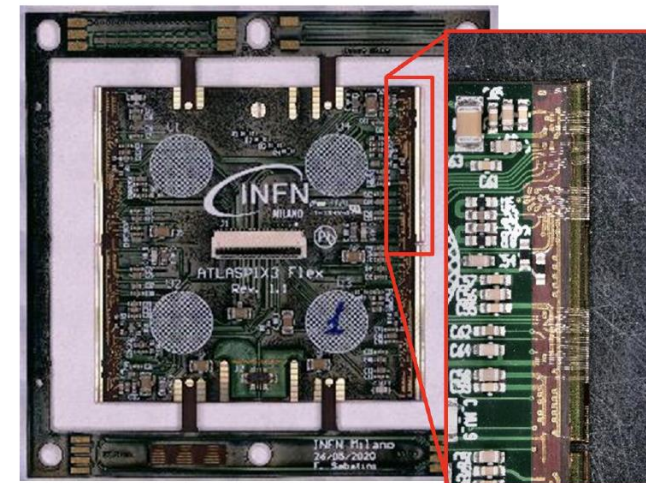
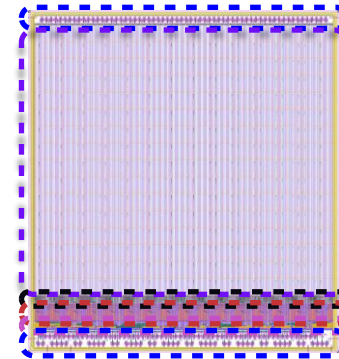


Thank you
for your attention.

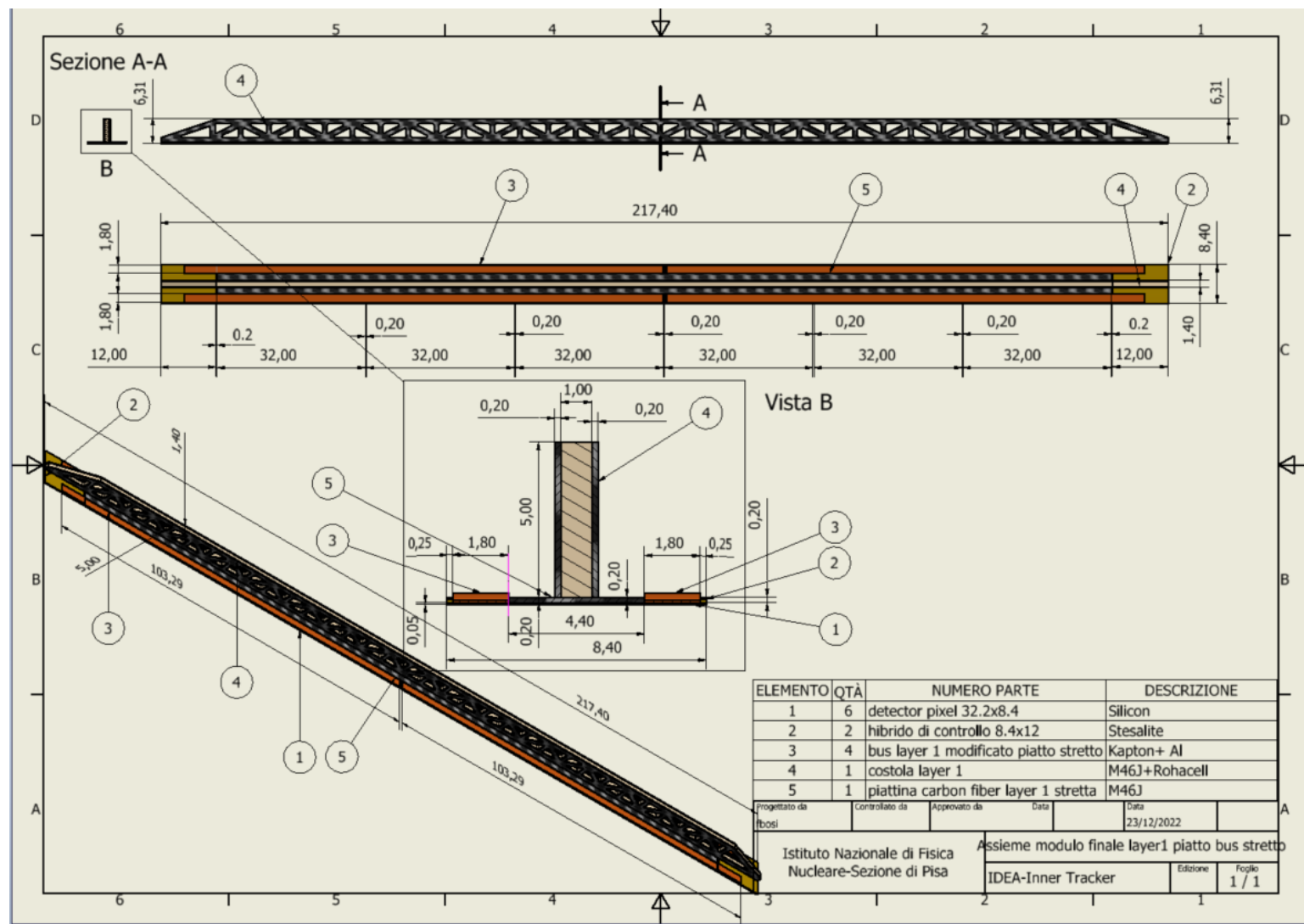
Sensors technology and dimensions

Depleted Monolithic Active Pixel Detectors

- **Inner Vertex (inspired to ARCADIA):**
 - Lfoundry 110 nm process
 - *50 μm thick, 25 μm x 25 μm*
 - Module dimensions: $8.4 \times 32 \text{ mm}^2$
 - **Power density 50 mW/cm^2** (core 30 mW/cm^2)
 - **Current at 100 MHz/cm²**
- **Outer Vertex and disks (inspired to ATLASPIX3)**
 - TSI 180 nm process
 - *50 μm thick (50 μm x 150 μm)*
 - Module dimensions: $42.2 \times 40.6 \text{ mm}^2$
 - **Power density: assume 100 mW/cm^2**
 - **Up to 1.28 Gb/s downlink**



Layer 1 stave detail



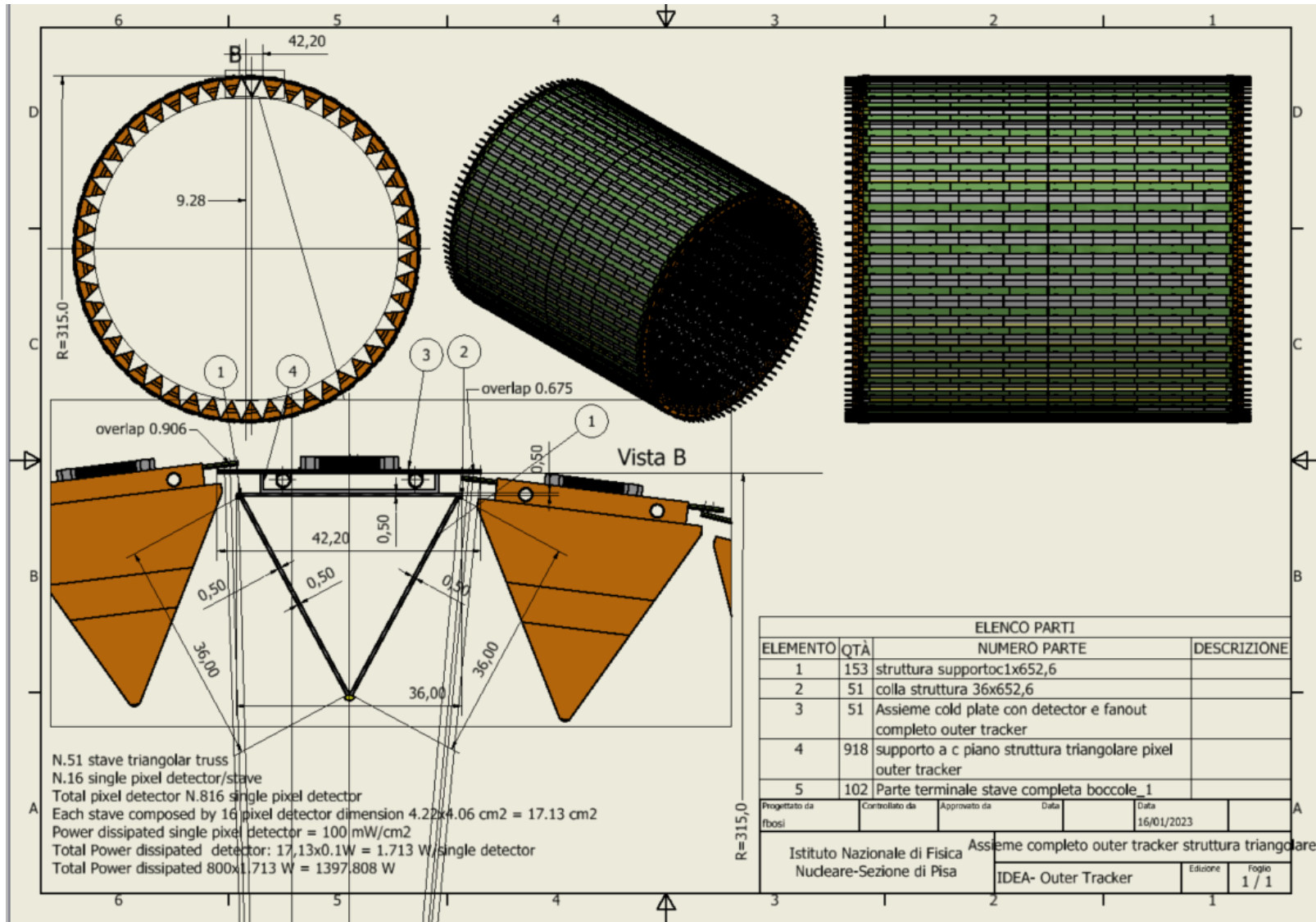
Reticular lightweight support to provide stiffness

- Thin carbon fiber walls interleaved with Rohacell
- 2 buses (data and power) 1.8 mm wide and 250 μm thick (50 μm Al, 200 μm kapton) per side
 - Inspired to low mass hybrid R&D

Sensors facing interaction point w/o any other material in front

Readout chips either sides

Air cooled



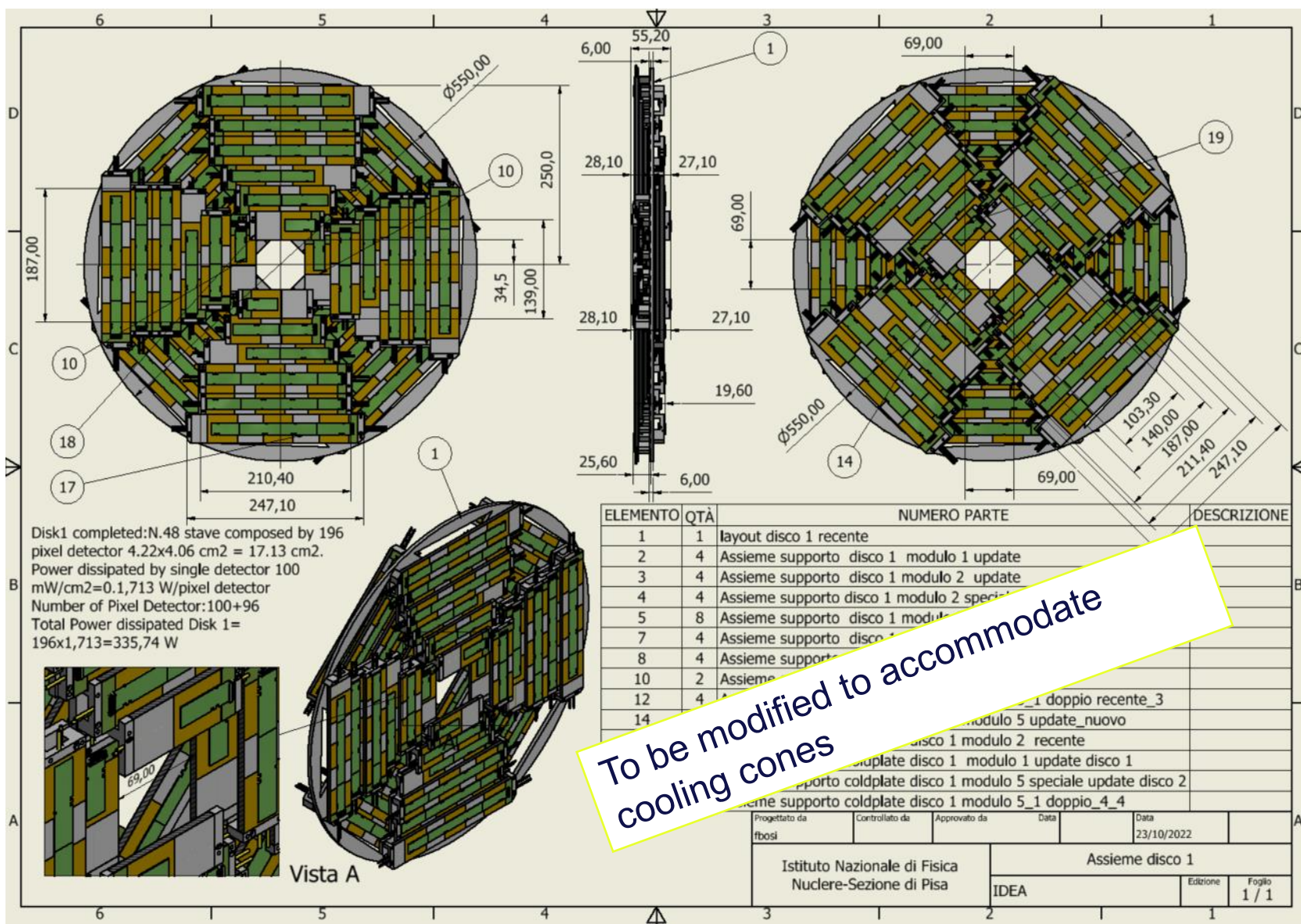
Outer Vertex Tracker Barrel
 At 31.5 cm radius

51 staves of 16 modules each

Lightweight reticular support structure (ALICE/Belle-II like)

Total weight ~3.7 kg
 Readout chips either side
Power budget ~1400 W

Water cooled (2 pipes of 2 mm diameter)



To be modified to accommodate cooling cones

Outer Vertex Tracker Disk 1
 2 sides (front and back) each with 4 petals.

One petal is made of different staves of overlapping modules

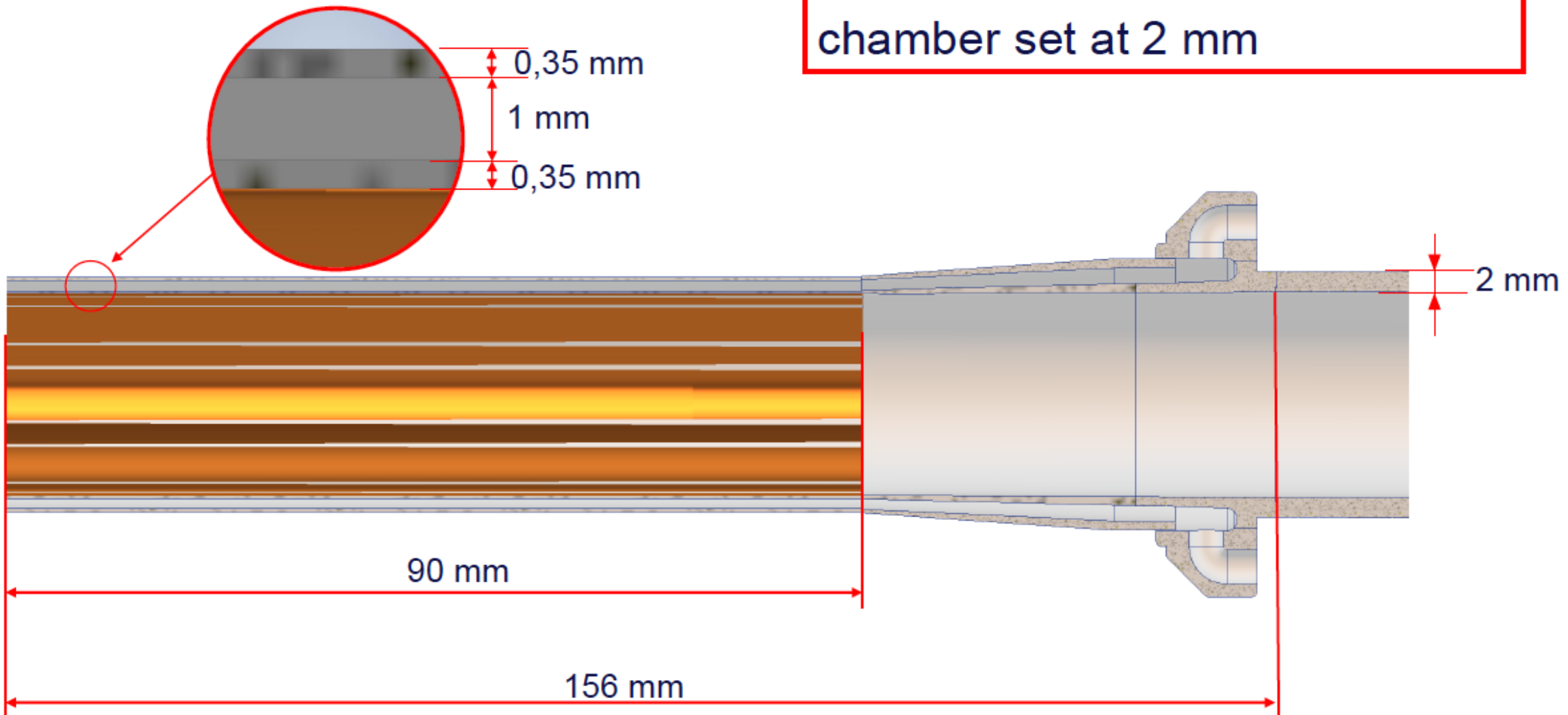
Total modules per disk: 196
 Total weight ~850 grams
 Power budget ~ 336 W

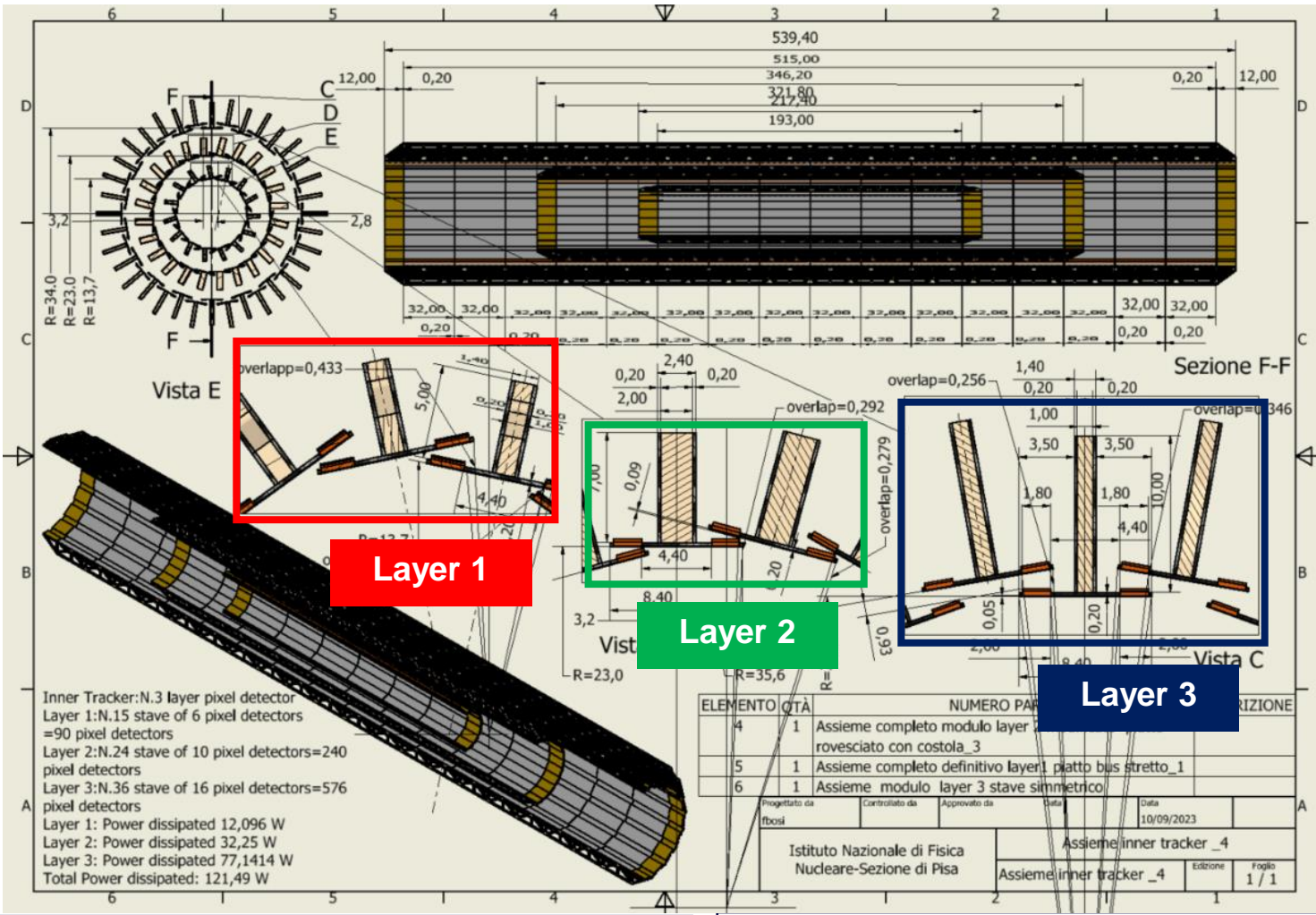
Cooling using 1 water pipe (2 mm diameter)

Similar geometry for the other two disks

Thickness of the chamber

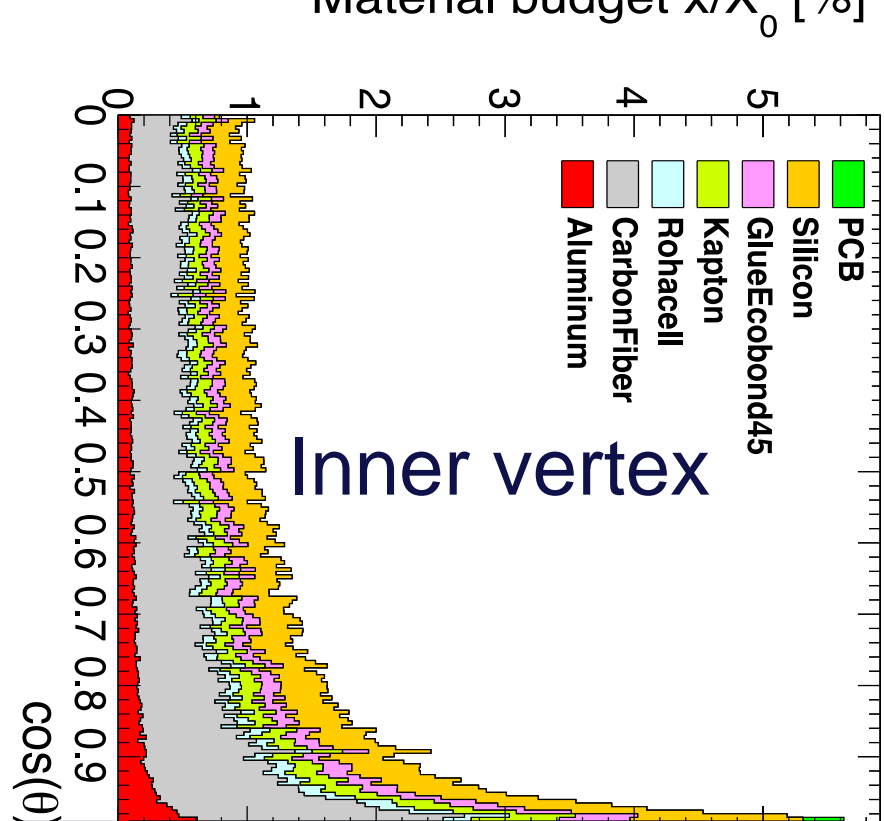
Uniform thickness of the conical chamber set at 2 mm





Total thickness 0.25% X_0 per layer

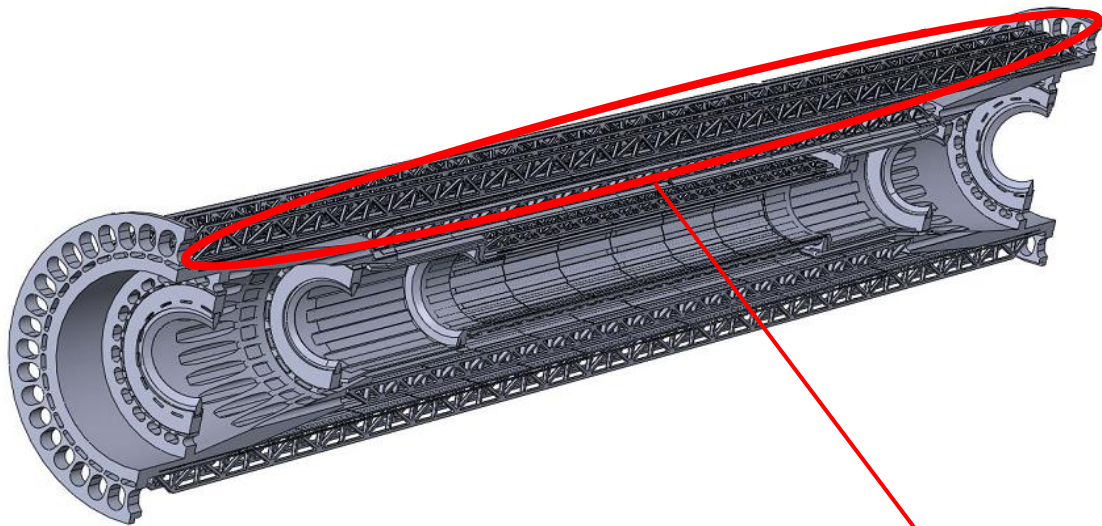
- Silicon: 0.053% X_0
- Power and readout bus: 0.056% X_0



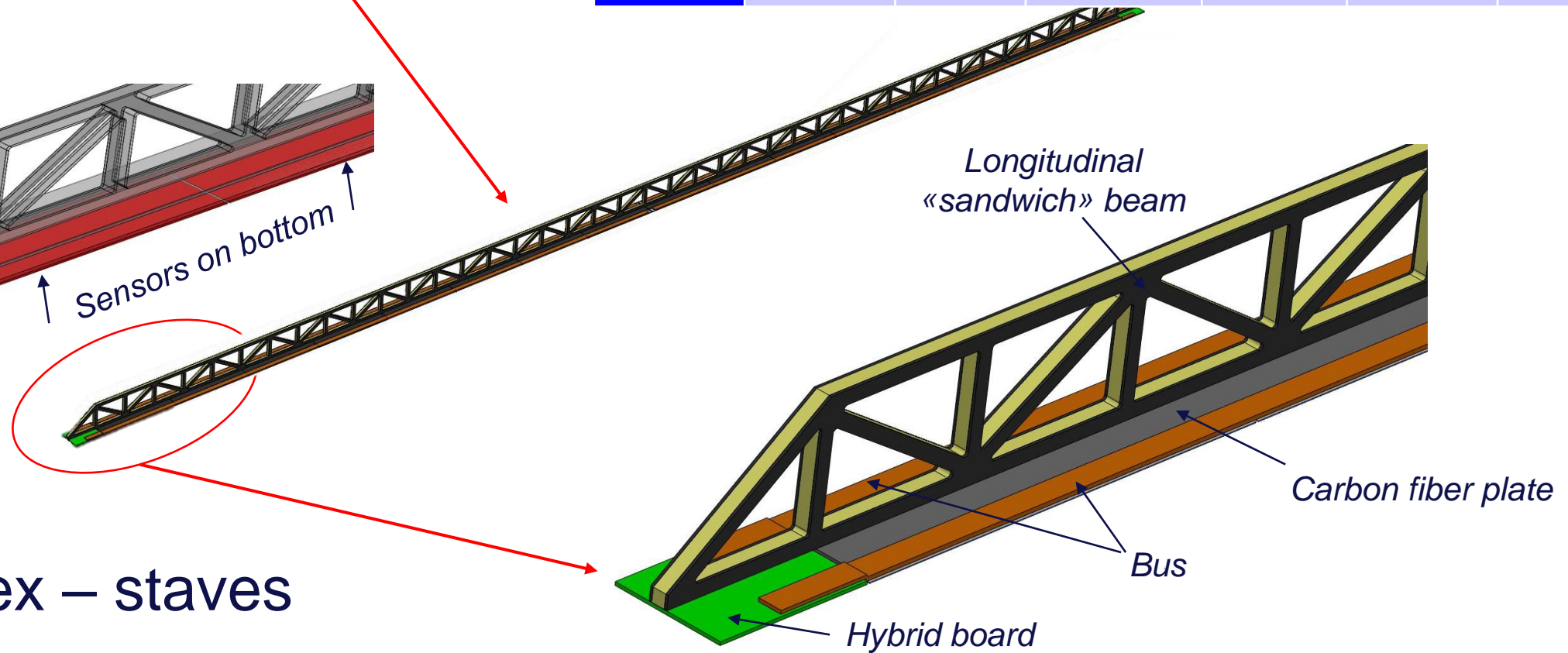
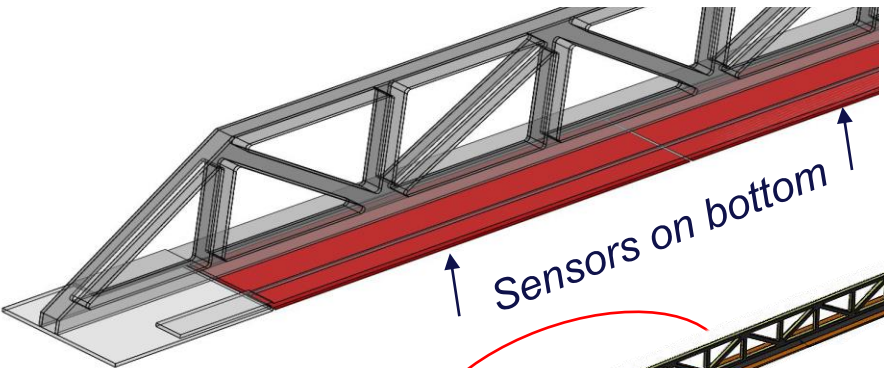
- Layer 1**
- Overlap to allow alignment ~500 μm
 - Pinwheel geometry
 - Total weight ~22 grams
 - Power 12 Watt

- Layer 2**
- Pinwheel geometry
 - Counter-rotated wrt layer 1
 - Total weight ~63 grams
 - Power 32 Watt

- Layer 3**
- Lampshade geometry.
 - Total weight ~150 grams
 - Power 77 Watt



Layer #	Radius [mm]	No staves	No modules /stave	Total Length [mm]	Active Area [cm ²]	Power [W]
1	13.7	15	6	217.40	241.92	12
2	23.7	24	10	346.20	645.12	32
3	34 & 35.60	36	16	539.40	1548.29	77



Inner vertex – staves

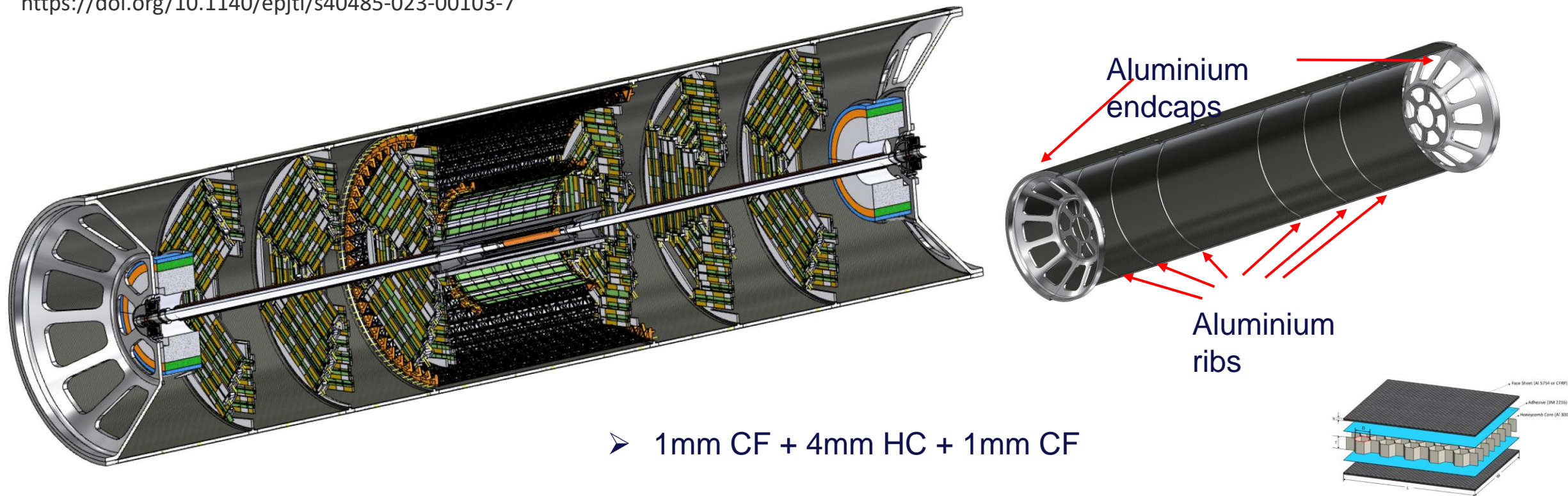
Support cylinder

All elements in the interaction region (Vertex and LumiCal) are mounted rigidly on a support cylinder that guarantees mechanical stability and alignment

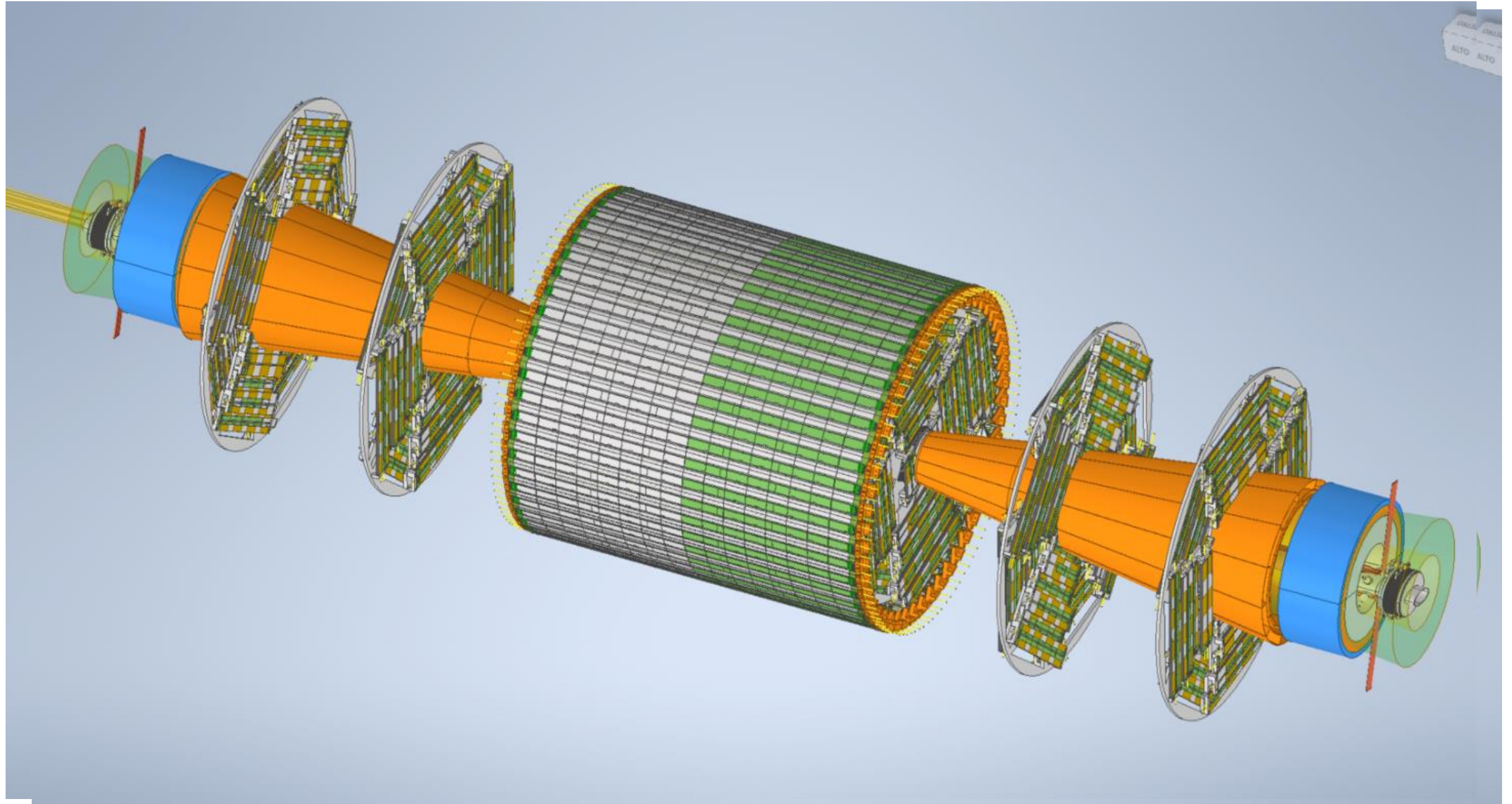
- Once the structure is assembled it is slid inside the rest of the detector

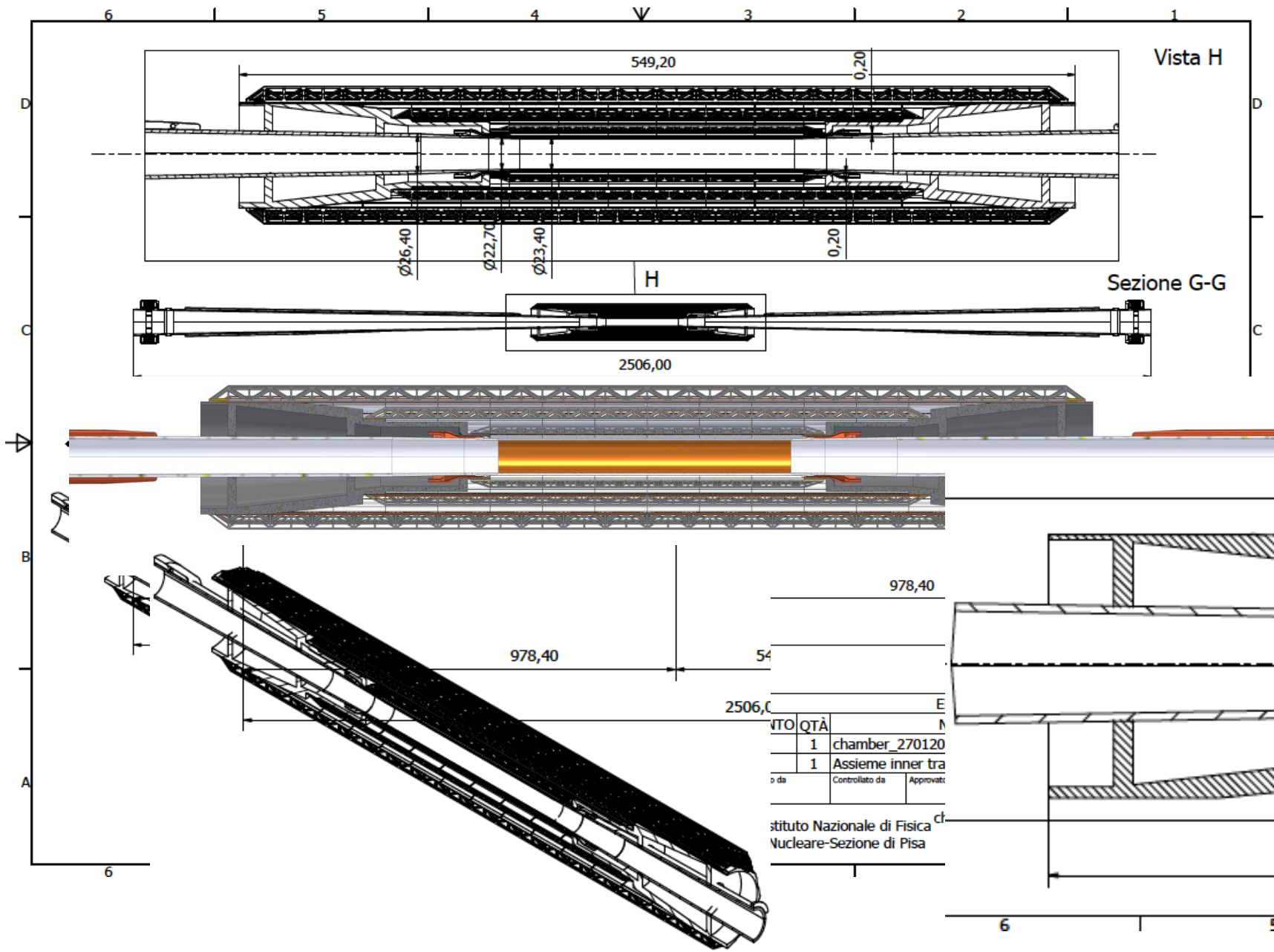
M. Boscolo, F. Palla, F. Franesini, F. Bosi and S. Lauciani, Mechanical model for the FCC-ee MDI, EPJ Techn Instrum 10, 16 (2023).

<https://doi.org/10.1140/epjti/s40485-023-00103-7>



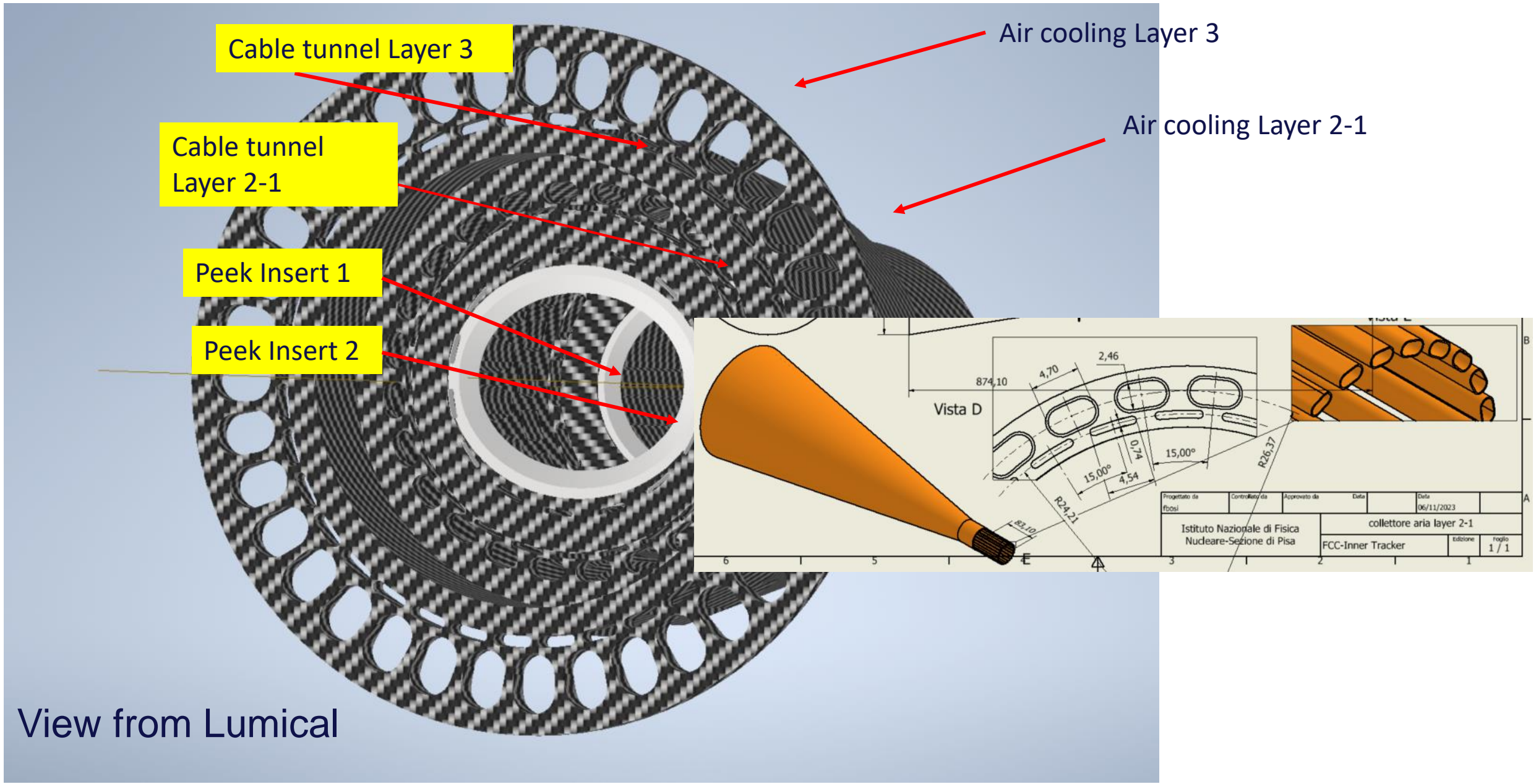
➤ 1mm CF + 4mm HC + 1mm CF





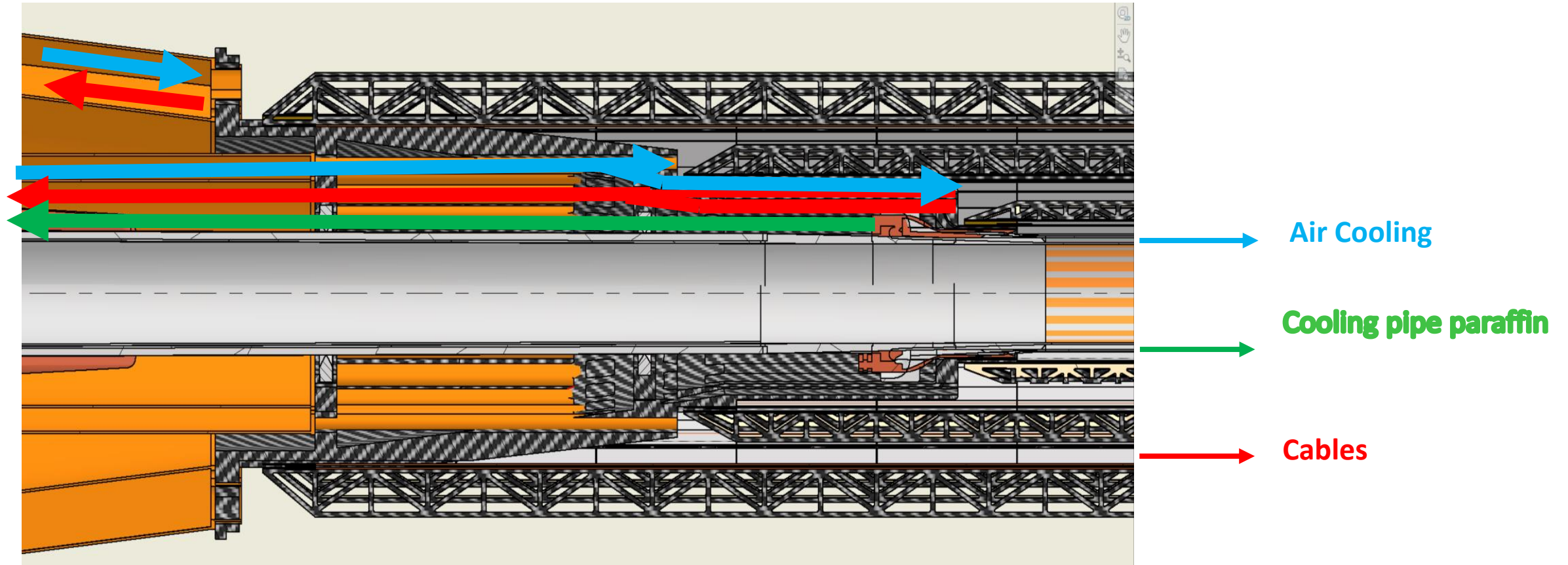
Inner vertex detector supporting conical structures on elliptical chamber
~450 grams

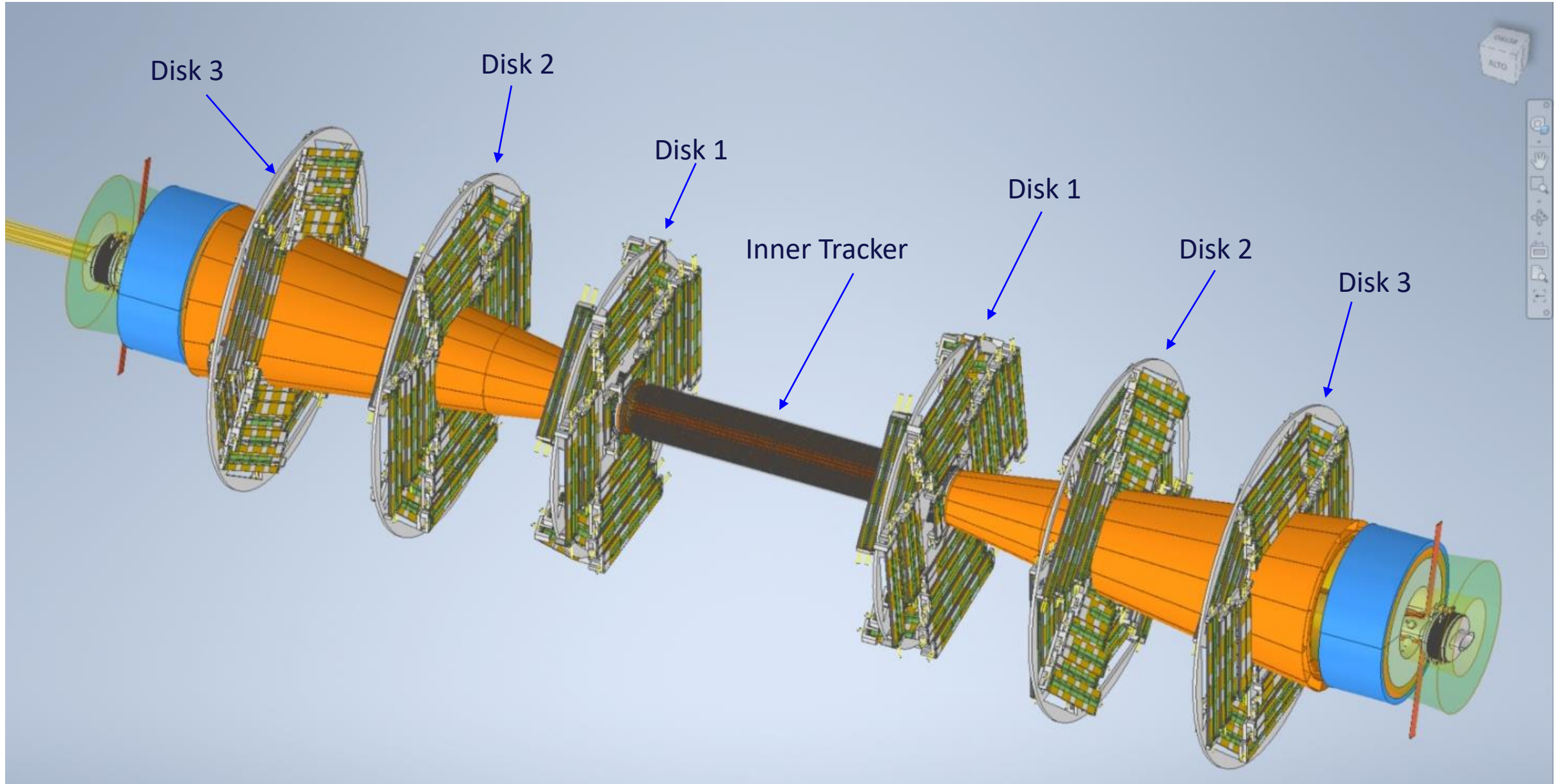
Engineered for air ducts and thermal isolation from the beam pipe during bakeout



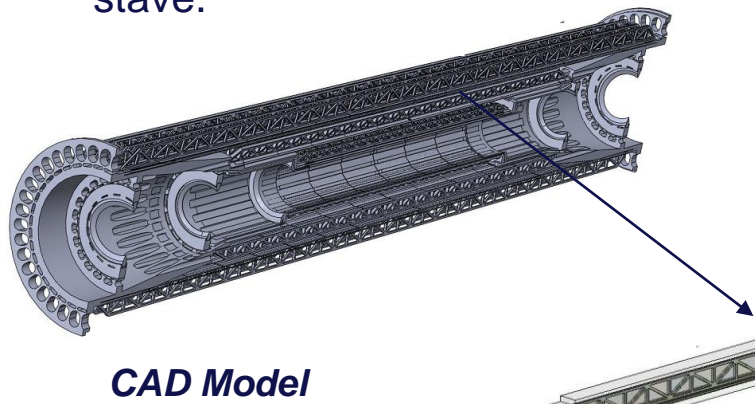
View from Lumical

Integration with beam pipe cooling manifold



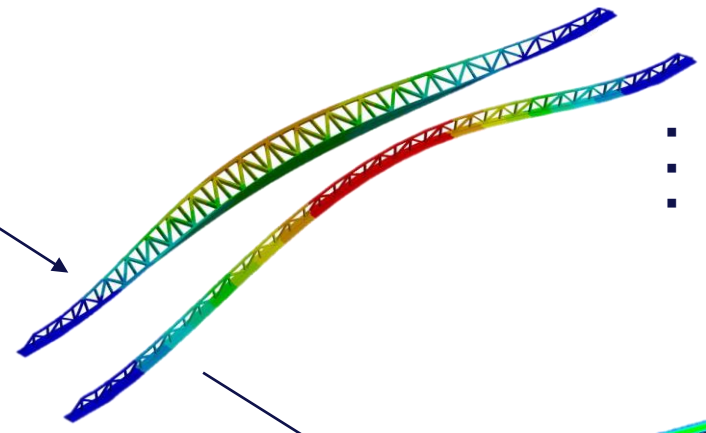
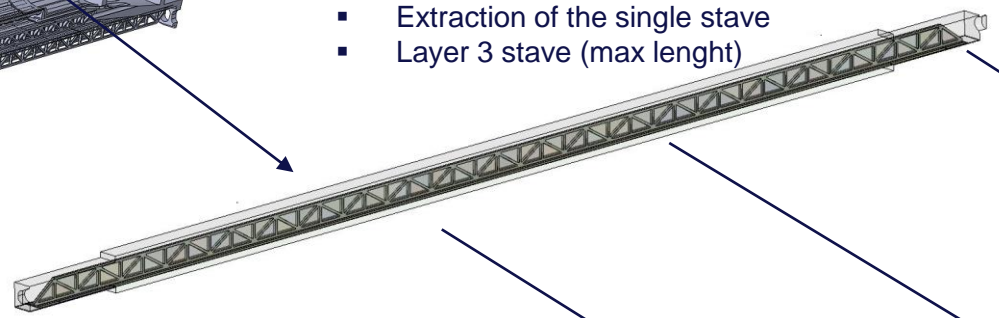


- Define a tool to evaluate whether the air flow necessary to remove the heat generates excessive vibrations on the stave.



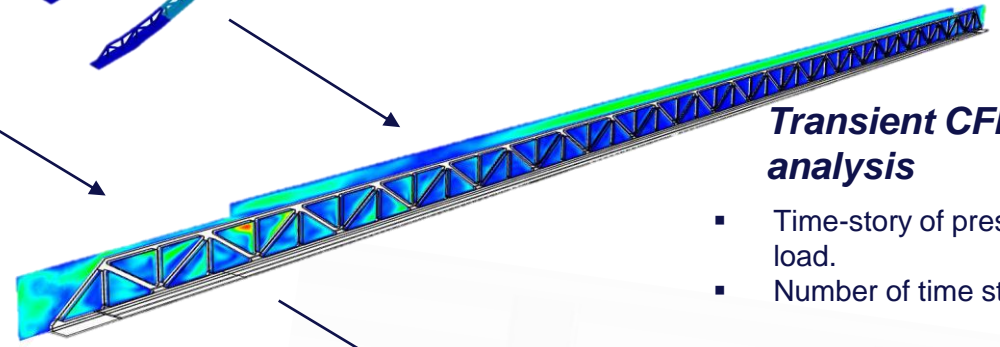
Geometry simplification

- Extraction of the single stave
- Layer 3 stave (max length)



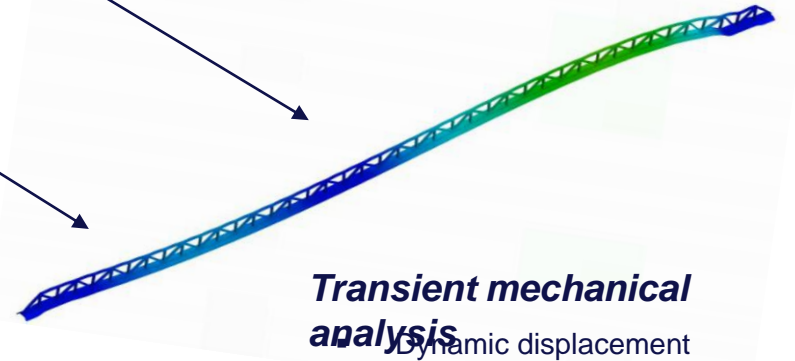
Modal analysis

- Participation factors.
- Natural frequencies.
- Duration of time step.



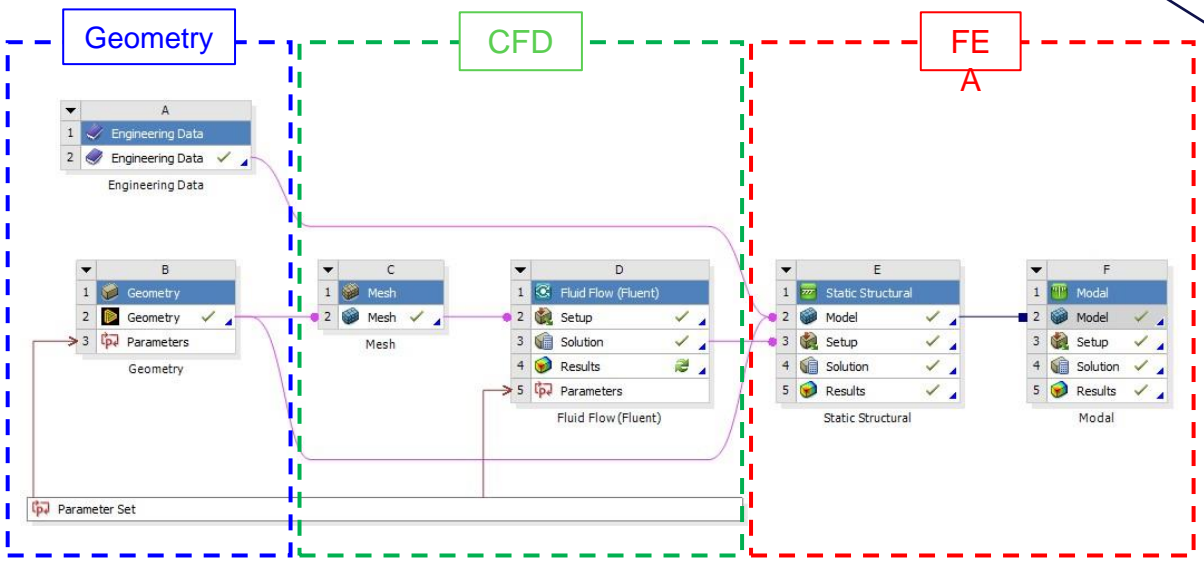
Transient CFD analysis

- Time-story of pressure load.
- Number of time steps.

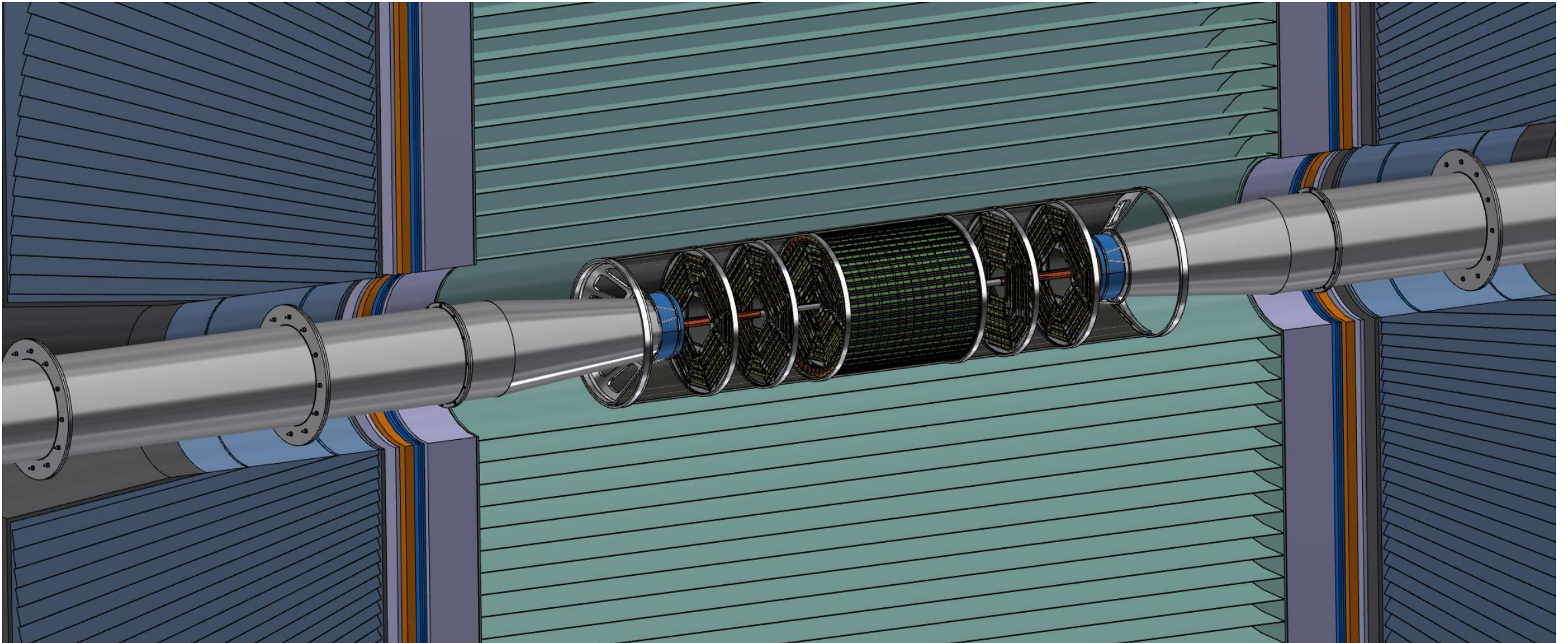


Transient mechanical analysis

- Flow of data managed by Ansys Workbench



General integration



ELECTRICAL UNITS

MOSAIX - Top Integration Diagram

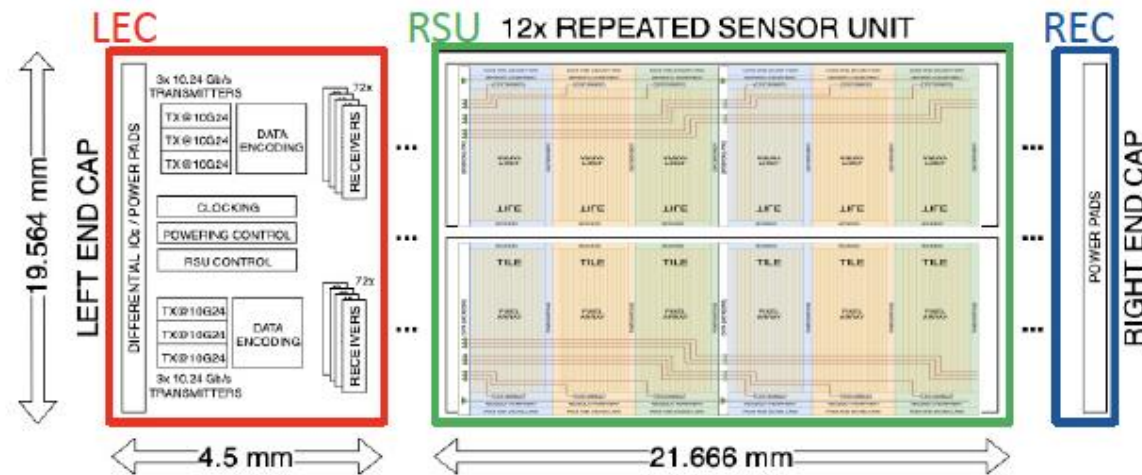
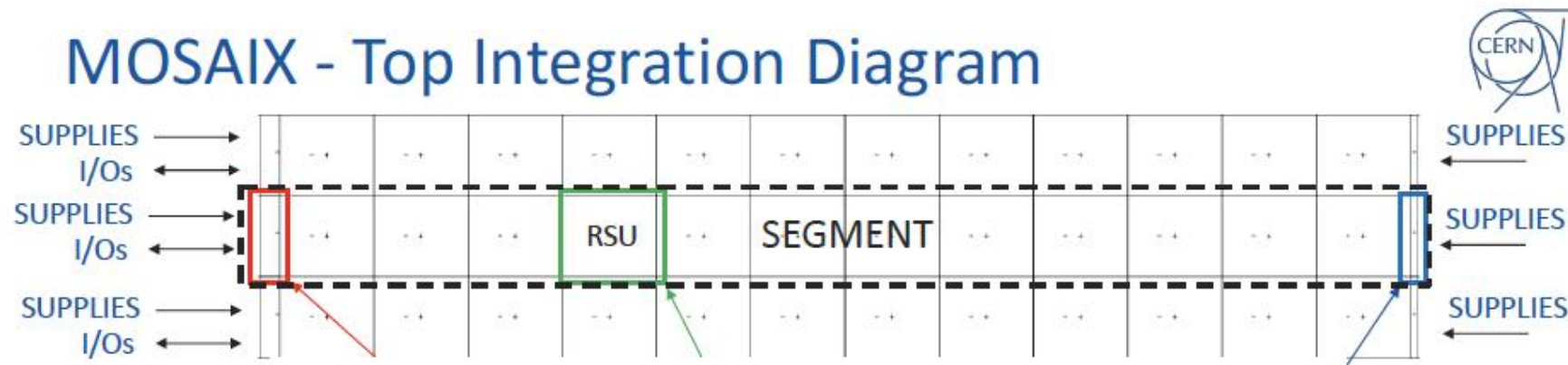


Figure 3.34: Block diagram of the sensor segment.

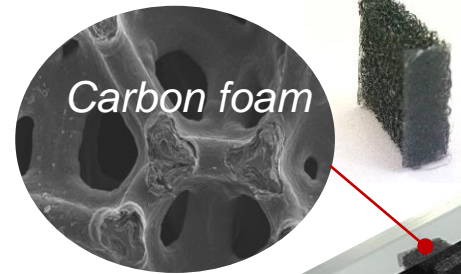
2023/11/01 WP1 / Primary / FR7 Stacked Sensor Design

7

A column driven approach reaches higher bandwidth, but needs low power consumption

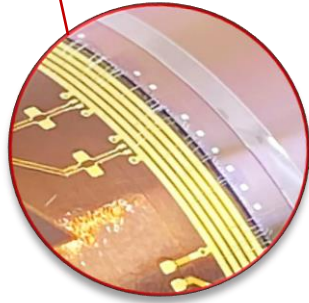
R&D Based on present effort in the design of the ITS3 (RUN4 -LS3)

→ minimum material support and gas cooling

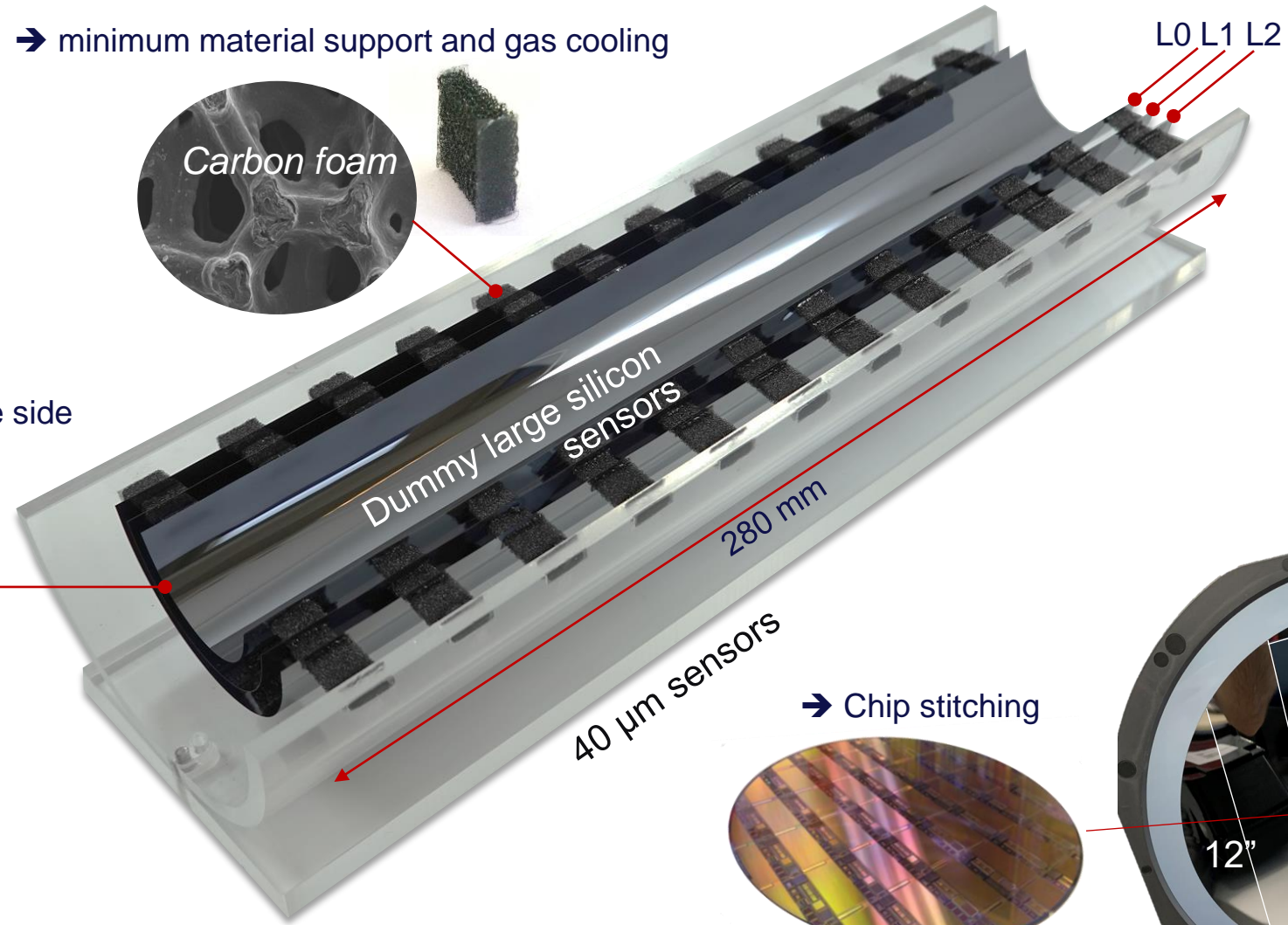
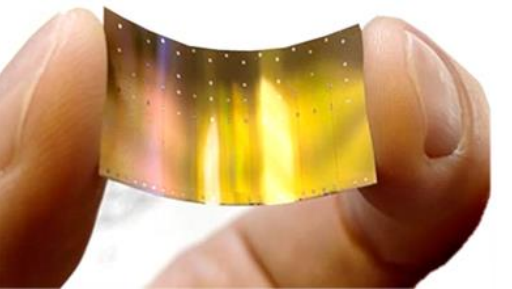


Carbon foam

→ Wire bonding at the edge side



→ Curved Silicon sensors



→ Chip stitching

