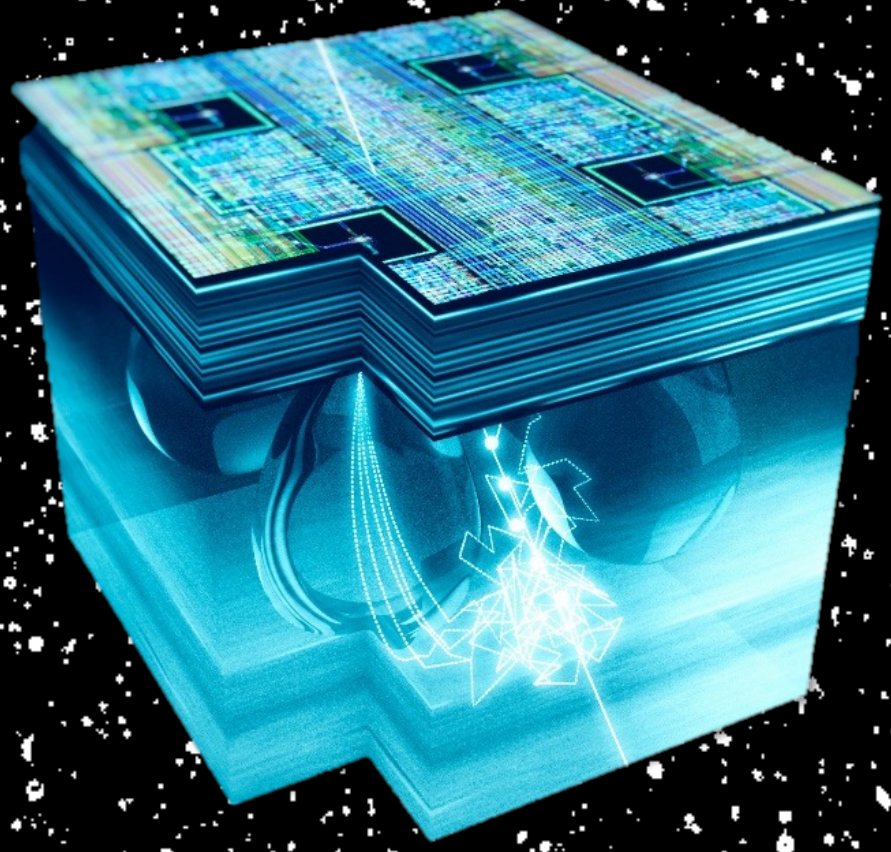
Electronics challenges and considerations including triggered vs data push architectures



ALPIDE prototype: 200 MeV protons at PSI

Walter Snoeys

Many thanks to colleagues from CERN, the ALICE ITS2 and ITS3 upgrade, ATLAS Itk, WP1.2, …

FCC-EE, CERN, July 1st 2024

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Challenges

- Technical
  - Position resolution
  - Hit rate
  - Power consumption
  - Yield and stitching
  - Technology qualification and support
  - Volume production: foundry can deliver (1M 300 mm wafers/year/fab), our community needs to improve on volume test and assembly.

- Non-technical
  - Relation with the foundry: need production volume
  - Concentration of resources, maintaining expertise in the community

ALICE 3 sensor specification estimates https://arxiv.org/pdf/2211.02491.pdf very similar to vertex FCC-EE

LOI estimates, 24 MHz pp collision rate, $1/r^2$ – scaling					Hit Rate		Bandwidth					
	Layer	Radius (cm)	Surface (m2)	Pixels (1e6)	Hit Rate (1e6/cm^2/s)	Hit Rate (1e9/layer/s)	Hits (Gbit/s)	Noise (Gbit/s)	Total (Gbit/s)	Power (W)	NIEL (1 MeV n_eq/cm^2)	TID (Mrad)
Vertex Detector	0	0.5	0.016	160	94	17	274	1	275	13	9,00E+15	288
	1	1.2	0.038	380	16	7.3	117	2.4	119	32	1,60E+15	50
	2	2.5	0.079	790	3.8	3.6	57	5	62	66	3,60E+14	12
Middle Layers	3	3.8	0.29	120	1.7	1.8	28	0.7	79	175	1,60E+14	5
	4	7	0.55	220	0.48	1.2	18	1.4	43	131	4,60E+13	1.5
	5	12	0.94	370	0.16	0.8	13	2.4	27	224	1,60E+13	0.5
	6	20	1.6	620	0.058	0.6	9.9	4	19	374	5,60E+12	0.2
Outer Tracker	7	30	2.3	930	0.026	0.5	7.9	6	16	561	2,50E+12	0.08
	8	45	7.5	3000	0.012	0.6	9.6	19.1	33	1792	1,10E+12	0.04
	9	60	10	4.00E+03	6.50E-03	0.5	8.2	25.5	36	2389	6,30E+11	0.02
	10	80	13.3	5.30E+03	3.70E-03	0.4	6.8	34	42	3185	3,50E+11	0.01

	Vertex Detector	Middle Layers	Outer Tracker	ITS3	ITS2
Pixel size (µm^2)	*O(10 x 10)*	*O(50 x 50)*	*O(50 x 50)*	*O(20 x 20)*	*O(30 x 30)*
Position resolution (µm)	2.5	10	10	5	5
Time resolution (ns RMS)	100	100	100	100* / O(1000)	O(1000)
in-pixel rate (/ pixel / s)	100	100	100		
Fake-hit rate (/ pixel / event)	<1e-7	<1e-7	<1e-7	<1e-7	<< 1e-6
Power consumption (mW / cm^2)	70	20	20	20**	47 / 35***

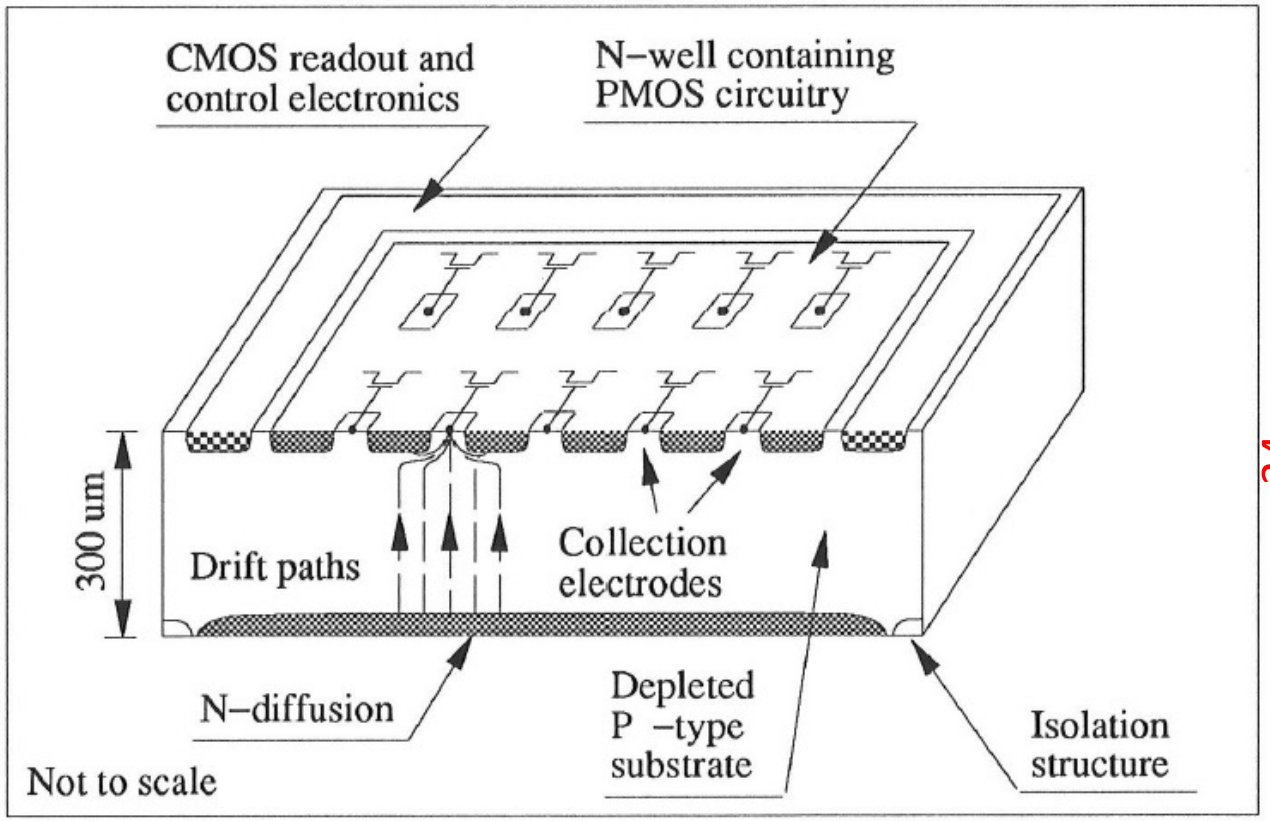
F. Reidt et al.

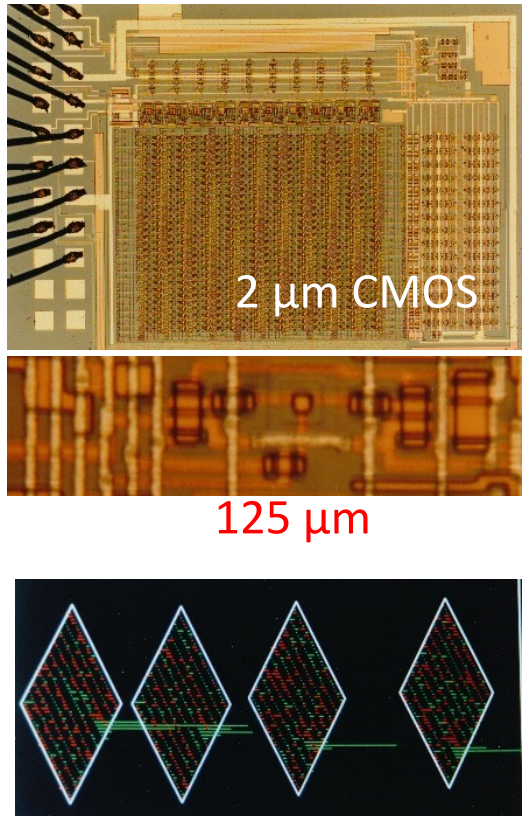
Need significant improvement in:

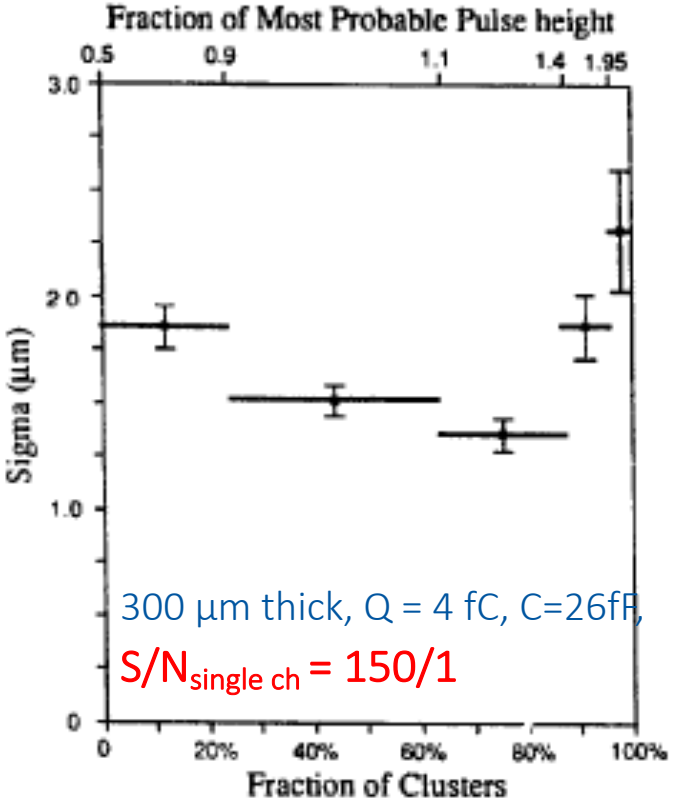
- Power-performance ratio, not only in front end, but also on and off chip data transmission, and architecture
- Radiation tolerance for inner layers

=> Observing convergence in sensor development targets, mostly common in the short term for different HEP applications, with longer term incremental R&D (L. Musa https://indico.cern.ch/event/994685/contributions/4181740/attachments/2193327/3707745/MUSA_ECFA_IS_2021FEB.pdf) see also D. Contardo

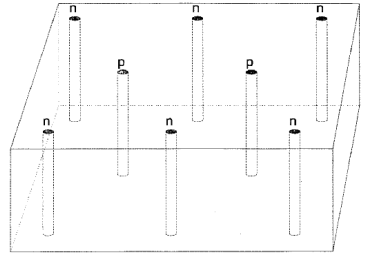
A monolithic detector for high energy physics (PhD thesis 1992), CMOS with double sided processing







- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side isolation with trenches lead to sensors with 3D electrodes (S.Parker) →

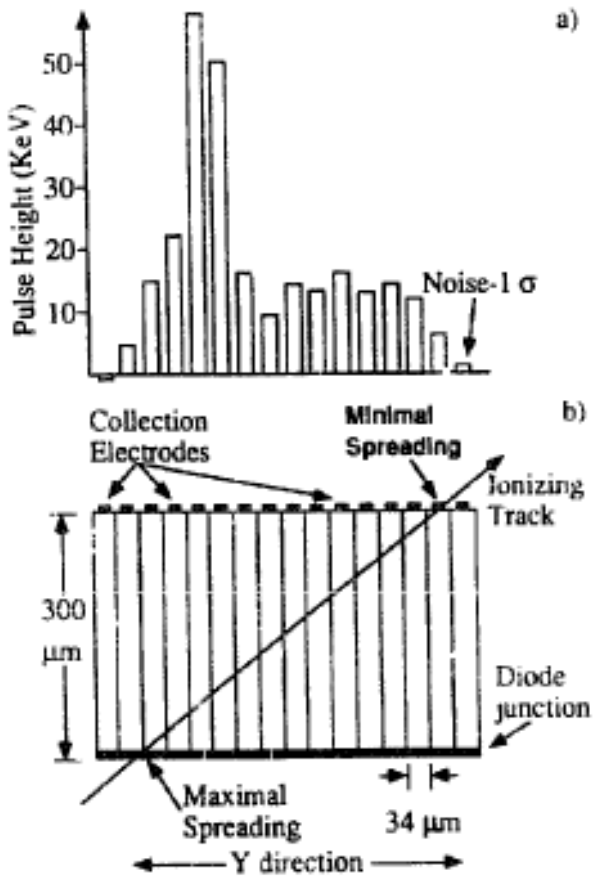


C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

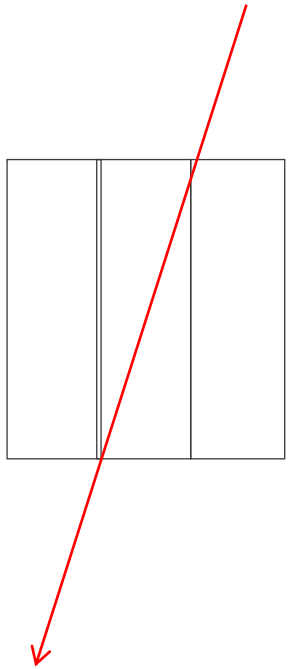
Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

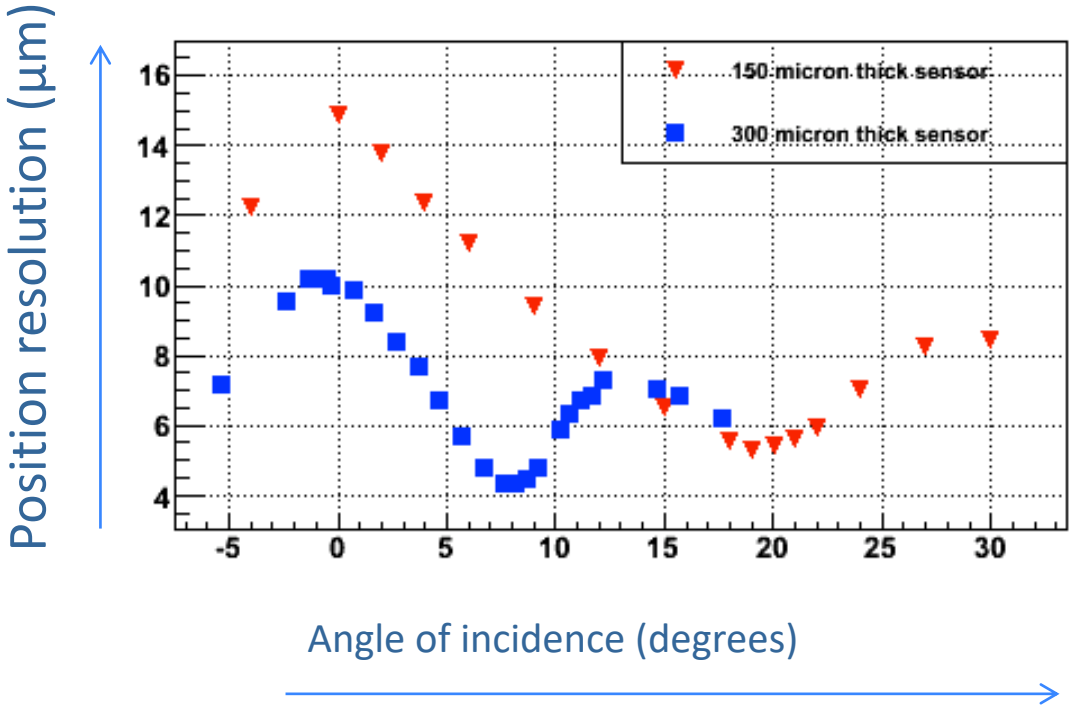
Position resolution: good S/N for interpolation Junction separation and back side processing: see below

Position resolution: inclined tracks



C. Kenney et al. NIM A 654 (2011) 258-265





Timepix3: X. Llopart, J. Buytaert, M. Campbell, P. Collins et al.

Average of extreme pixels in the cluster gives better results
In this case the signal (and the S/N) for a single channel reduces with track inclination

Can optimize resolution using track inclination to enhance charge sharing, can also be done using a magnetic field

Single point resolution

- Sensor can deliver ~ 1µm point resolution if granularity and S/N sufficient
- Examples used analog interpolation. With binary readout, single point resolution can be achieved as well. Need sufficient granularity, but also sufficient S/N.
- Unless S/N is very large, detector depth and pixel pitch should be comparable to avoid degradation in S/N and hence resolution for inclined tracks (for instance in the forward part of the barrel)
- With thinner sensitive layers, it becomes more difficult to exploit charge sharing with sufficient margin, pushes towards lower pitch. Without or with very limited charge sharing, a pitch of about 10-15 µm is needed to achieve 3 µm position resolution. Sensor radiation tolerance may also push towards lower pixel pitch.
- Smaller pixel pitch requires reduction of the power per pixel, but also clever ways to organize readout to reduce the amount of circuitry per pixel.

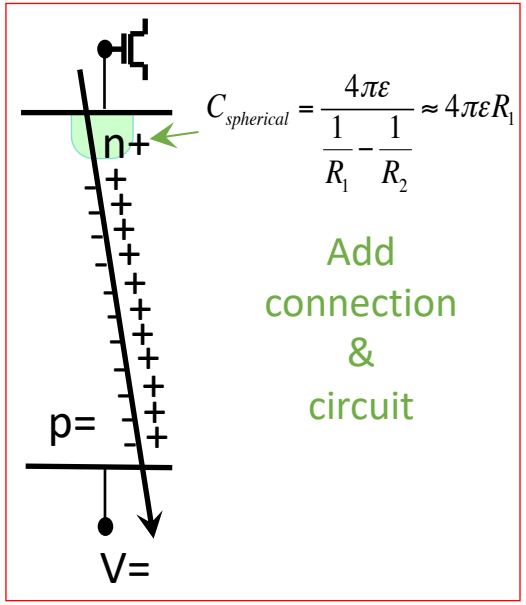
Power consumption

$1\ mW/cm^2 = 1\ nA/pixel$

for a 10 x 10 μm^2 pixel and 1 V power supply !

- Analog: need improvement on power/speed performance
- Digital: leakage (see Gianluca's presentation), local activity and long distance data transmission
- Off-chip data transmission: serializers

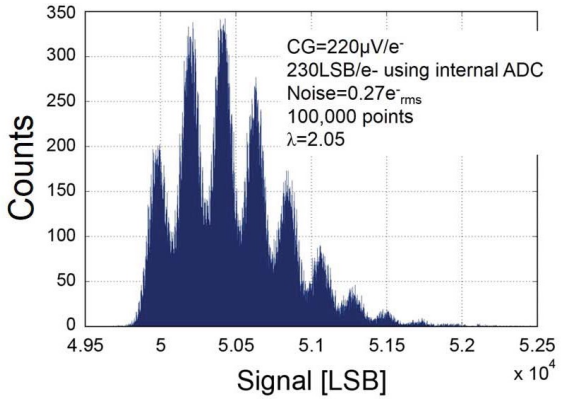
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

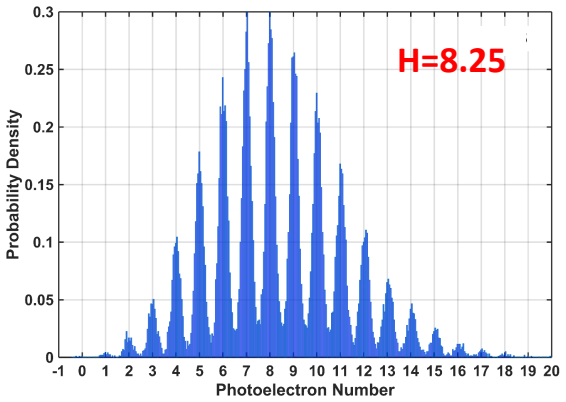
Add connection & circuit

M.W. Seo and S. Kawahito EDL 2015



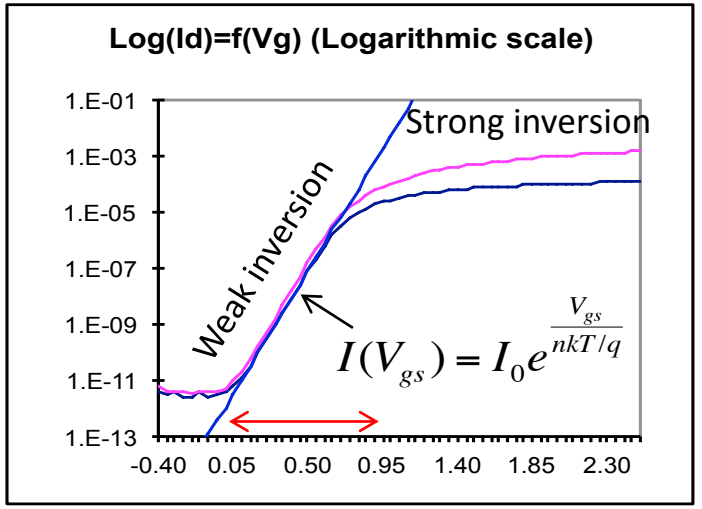
220 μV/e⁻ in 0.11 μm, C=0.73 fF

Ma, Masoodian, Wang, Fossum 2017



350 μV/e⁻ in 45 nm, C=0.46 fF

Non-linearity in weak inversion

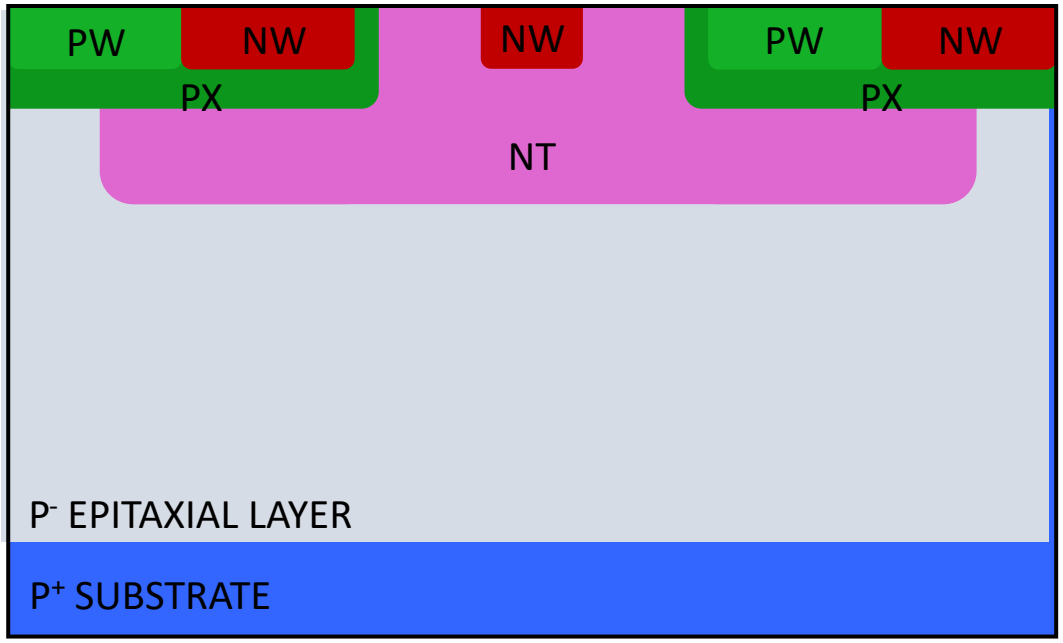


- Q/C several 10's of mV in 180 nm
- "Conventional" approach
  - Improve power performance ratio of the front end -> new topologies
  - Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored?
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar
- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero.

Process optimization for lower capacitance and higher radiation tolerance

Further process modification in TPSCo 65nm, adapting the sensor implants, to:

- reduce the sensor capacitance, this translates directly in more margin on efficiency vs fake hit rate.
- increase radiation tolerance, aimed more at even higher radiation levels (> 1E15 n_{eq}/cm^2).



C. Lemoine and G. Borghello

- See also TWEPP last year 2024 *JINST* **19** C02033)

Power consumption in full CMOS

Energy to transfer 1 bit to the periphery (assume line toggle, not step):

1 cm line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ**

Lower VDD in deep submicron = 2 pF x $(1\ V)^2$ = **2 pJ** (1.2V in MOSAIX, so 2.88 pJ…)

Caveat: 2pF/cm can increase depending on the line load…

- Digital power density proportional to activity level (hit densities…) and column height, but now leakage also important !!

- Advantage of full CMOS transmission is the simplicity of the repeaters. Power consumption can be reduced by low swing differential transmission but complexity increases significantly. The advantage of low swing differential transmission is less interference with analog: 1 V x 1 fF = 1 fC already way over threshold !!! With full CMOS over the matrix, one needs virtually perfect shielding.

Power consumption: example CMOS

For a hit rate of 400 Mhits/cm^2/s and a 20 cm long barrel with readout on both sides of the barrel, transmitting 1 bit per hit over 5 cm on average in CMOS corresponds to a power density of:

Pdensity/line toggle per hit (CMOS) = 400 Mhits/cm^2/s x 5 cm x 2pJ/cm = 4 mW/cm^2 (at 1 V)

or 4 nA/pixel for a 10x10 sq. micron pixel (this is per line toggle per hit)

Note:

- This is per line toggle per hit (if normal serial transmission to be divided by 2 per bit).
- Will have to be very careful in encoding of the data !! Precision timing probably not in the first layer !
- 1-2 Gbit/s is about the maximum for on-chip data transmission: will need to reduce area feeding into one transmitter well below the cm^2

- Can opt for low swing data transmission but development for higher bandwidth is necessary.

  Example low swing differential transmission work by BNL as well (chiplet on the next run)

Power consumption results in voltage drops !!

- Voltage drops proportional to the square of the column height and power density

Estimate for 65 nm with more conductive metal stack, and a 20 cm long barrel powered from both sides:

2 mV voltage drop per mW/cm^2 (for both VDD and GND !)

See also G. Aglieri Rinella's presentation

- Shorter barrel gives significant reduction in voltage drop and therefore 400 Mhits/cm^2/s for FCC-EE is equivalent to 100 Mhits/cm^2/s for ALICE3 if the barrel of FCC-EE is two times shorter.

- However, power for local data handling needs to be reduced (in MOSAIX power is no longer dominated by front end!) and this for much higher hit rates than in ITS3.

- Significant challenge for stitched devices, in addition to yield.

Triggered vs non-triggered readout

Two conflicting requirements:

- Push towards lower pixel pitch for position resolution and other arguments
- To reduce power consumption and supply drops in the matrix, data should be stored locally in the matrix, otherwise there is much less benefit, but this costs space and power, and it is not clear that this realistic in the end.
- Probably better to push data out without triggering

Off-detector transmission:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

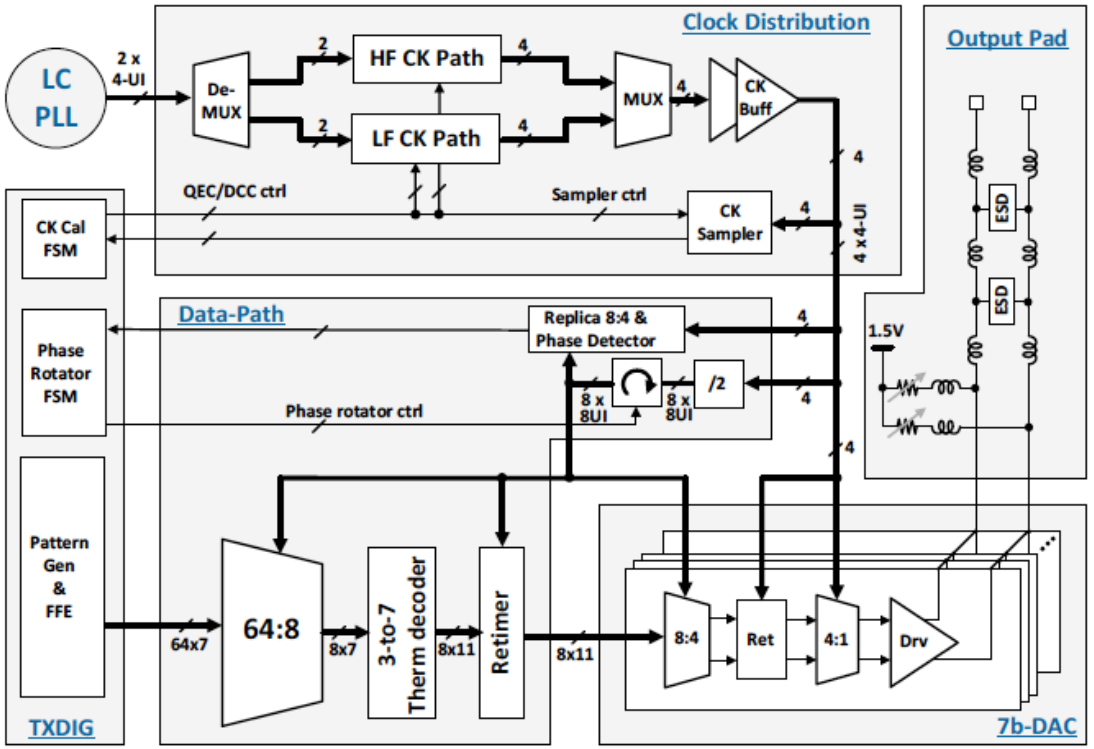
2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths in advanced technologies (chiplets ?)

Significant circuit complexity

For HEP important penalty for SEU robustness due to triplication/larger devices…

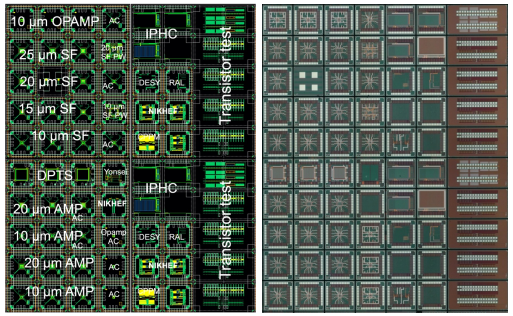
Important: data concentration, physical volume for material budget, and technology

TPSCo 65 nm (MLR1, ER1 and ER2): ***POWERING***

Last EP R&D report: https://cds.cern.ch/record/2891650
ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

MLR1: Dec 2020: 1.5 x 1.5 mm^2 test chips

qualification of TPSCo 65 nm for HEP

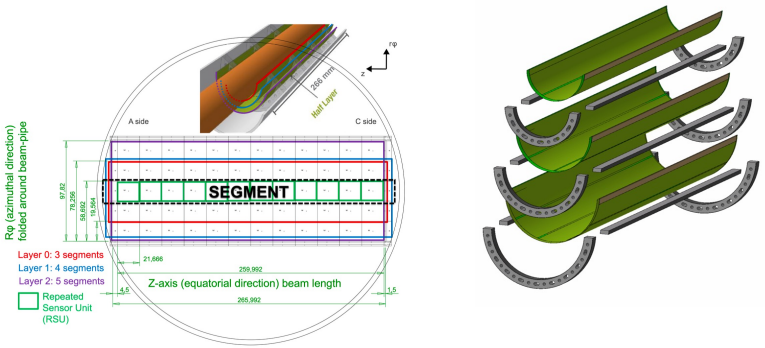


- Fully efficient at RT before and after 10^{15} n_{eq}/cm^2
- Sensor time resolution ~ 70 ps (10 µm pitch)
- Investigating path to tolerance to higher irradiation levels and lower input capacitance

(C. Lemoine *et al* 2024 *JINST* **19** C02033)

ER2: MOSAIX: Fall 2024:

First full prototype for ALICE ITS3



See presentations G. Aglieri Rinella, F. Reidt

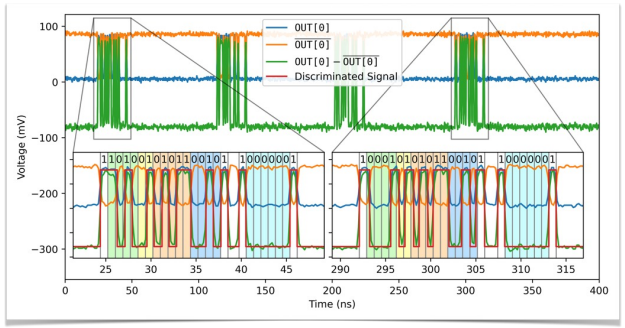
ER1: Dec 2022:

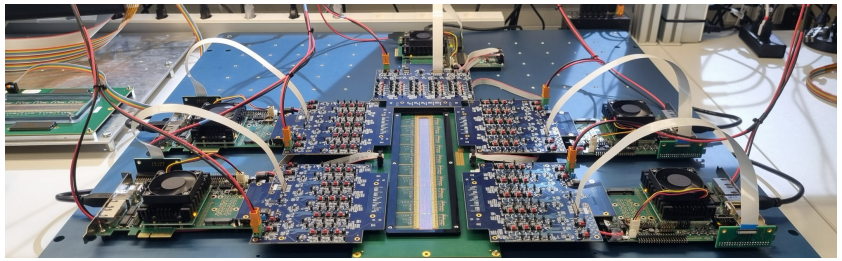
Learning about stitching

Two stitched sensors with 10 repeated units:
Both functional, learnings to be included in ER2

MOST (25.9 cm x 0.25 cm):

- 18 µm pitch, very densely designed pixel matrix
- **Global power distribution + conservatively designed highly granular power switches to switch off faulty parts**
- Asynchronous, hit-driven readout, low power consumption + timing information
- Pulsing signal and output signals at the end of the chip, round trip more than 50 cm, ~ 300 ns, with ~800 repeaters, all 256 signal lines functional

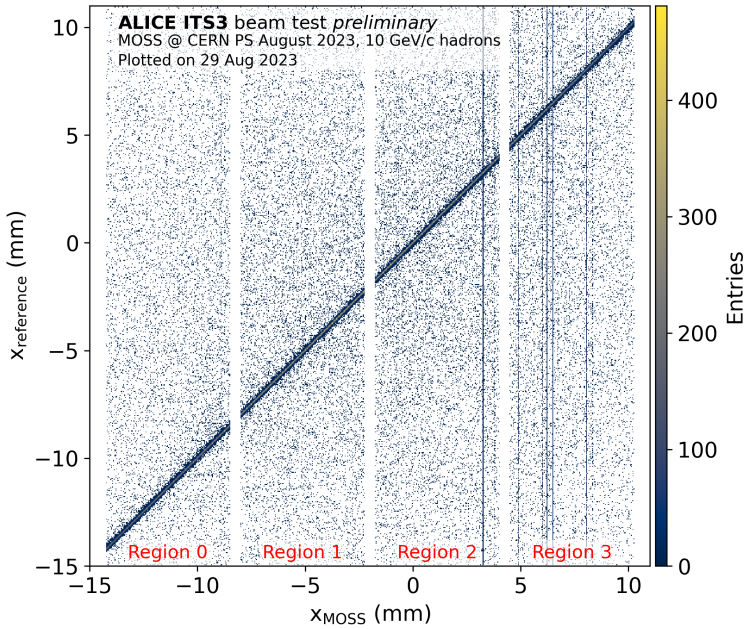




MOSS (25.9 cm x 1.4 cm):

- Top half 22.5 µm pitch, bottom half 18 µm pitch
- **Each half powered completely independently with 4 conservatively designed submatrices -> many power domains**
- Synchronous readout

Hit x-coordinate correlation between MOSS and reference ALPIDE telescope



CONCLUSIONS and OUTLOOK

- Several technologies qualified for HEP, including radiation tolerance requirements for FCC-EE. Select technologies supported through DRD7.

- Significant technical challenges pushing towards smaller pixel pitch for position resolution, radiation tolerance, and hit rate requirements. Power density and long distance on-chip data transmission major challenges. 3D stacking may help to reduce the pixel pitch.

- The increasing complexity of Monolithic Active Pixel Sensors requires digital-on-top design techniques and verification by a team of expert chip designers, and sensor optimization and simulation by device/TCAD/Monte Carlo experts.

- Non-technical challenges are related to maintaining expertise within the community, concentration of resources, good relation with the foundry etc.

- Specifications for vertex detector for FCC-EE more or less equivalent to those for ALICE3. Development towards ALICE3 will be very beneficial as an R&D towards a vertex detector for FCC-EE. In general also LHCb upgrade relevant for R&D for later detectors. Experience in existing systems like ITS2 very relevant as learning experience for the future.

- Triggered vs non-triggered: really taking advantage of the triggered readout within the pixel matrix far from trivial, non-triggered readout may be preferable.

- Significant learning 3D wafer stacking now allows the connection of a readout wafer to a detector wafer, and deliver the fully finished diced assemblies to the customer. This reduces the distinction with hybrid sensors, but provides opportunities well beyond with multiple connections within each pixel and stacking of even more than two wafers.

- Unprecedented integration in electronics systems continues to be driven by the computation needs of AI. Stitching and wafer stacking brings pixel pitches around 10 um within reach. The circuitry on a monolithic sensor allows the mitigation of local, otherwise fatal defects for large, even wafer-scale sensors. Efficient volume test, assembly, and mounting, together with significant progress towards lower power densities and on-chip resistive drops, will be enablers for large area detectors, and this for practically all applications in HEP.

- CMOS monolithic sensors will become widely applied in HEP, in tracking, calorimetry and timing detectors. Non-negligible MAPS production volumes within HEP should allow our community to impact not only the quality of its own measurements, but also society in general, with access to the most advanced technologies.

THANK YOU !

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