Stave electrical bus

Distribution of power and data signals along the stave

- reducing power dissipation on the distribution lines
- minimize the number of connections

Read-out units are:

- **multi-chip modules** (example 2x2 quad modules)
- large stitched detectors
- bias is in parallel within the components of a module

Minimal I/O connection on chip requires:

- Serial powering chain: all biases generated internally by shunt-LDO regulators
- chip-to-chip data transmissions: local data aggregation on module
- clock data recovery

Reduce material by developing PCB with Al as conductor

Relevant IPs should be better developed in parallel to the matrix developments: reduce risk in larger chip submission