High Speed Links

EP R&D

WP6 High Speed Links

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Introduction

- High data-rates coming out of particle physics experiments in the LHC era ➜ optical data transmission has become ubiquitous
  - Each large experiment has tens of thousands of optical links
  - Need to optimise fibre bandwidth utilisation led to need for development of aggregation/ serialisation solutions
- Environmental conditions inside the detectors (radiation, (low) temperature, magnetic field) require:
  - some level of customisation of COTS parts (the optoelectronic components)
  - full customisation of the electronics, necessitating the design of custom ASICs for all link functions (de/serialiser, laser driver, receiving amplifier)
- Over-arching development strategy has been to follow telecom/datacom industry developments and minimally customise only as needed by the requirements
  - Projects matched to LHC experiments' upgrade schedules
    - LHC installation 2006-8 ➜ LS1 (2010) ➜ LS2 (2018) ➜ LS3 (2027) ➜ LS4 (2032)

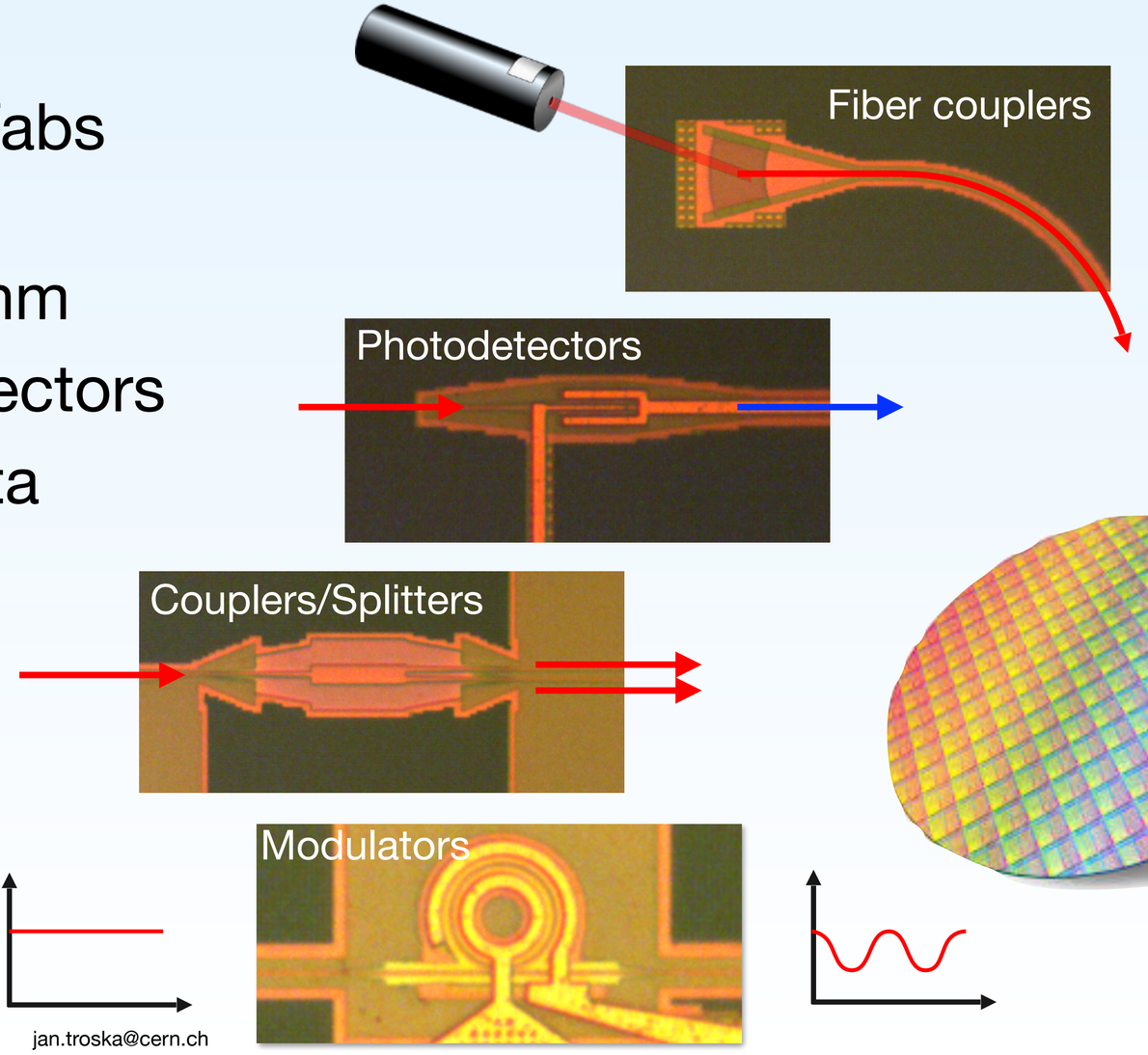
Telecom/Datacom Industry BW drivers

- Increase in end-user and device (IOT) traffic
  - This was the traditional driver for the internet and by extension what happens inside data-centres
- Increase in AI/ML applications
  - Now the major driver for increases in interconnect bandwidth within data-centres, which are growing in size

- During the initial LHC experiment installations, each experiment deployed as large or larger optical data transmission systems than commercial data-centres
  - This is nowadays very far from true, both in terms of the individual link bandwidths and in terms of the number of link components installed
    - Will have an impact on our ambitions in terms of having special requirements
    - Interoperability of existing standards important if we want to avoid developing both ends of the link (currently we only develop the custom front-end components and use “standard” back-end components)

Silicon Photonics

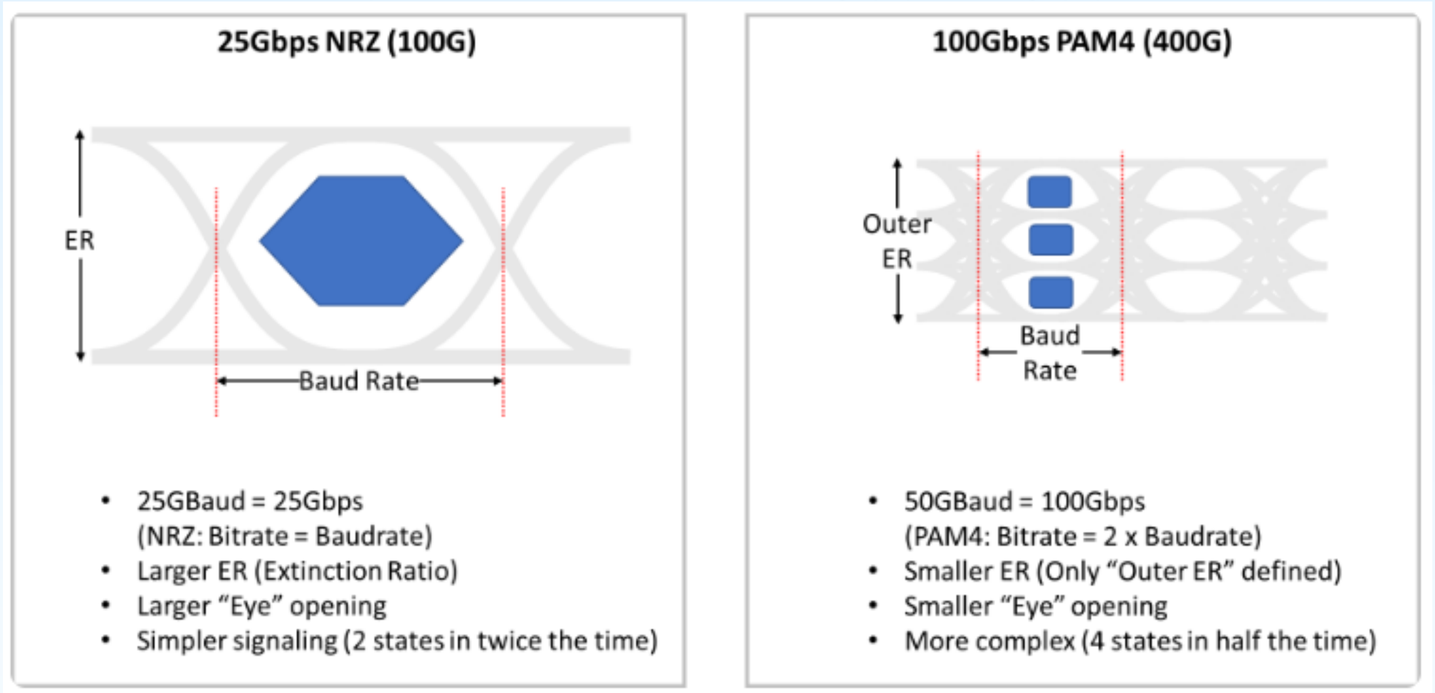
- Silicon is patterned (deep UV lithography) with sub-micron precision
- Fabricated in “standard” CMOS fabs using Silicon SOI wafers
- Wavelength: 1310 nm and 1550 nm
- Germanium epitaxy for photodetectors
- Complete platform for optical data links

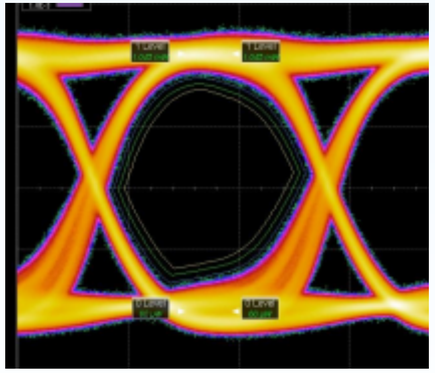


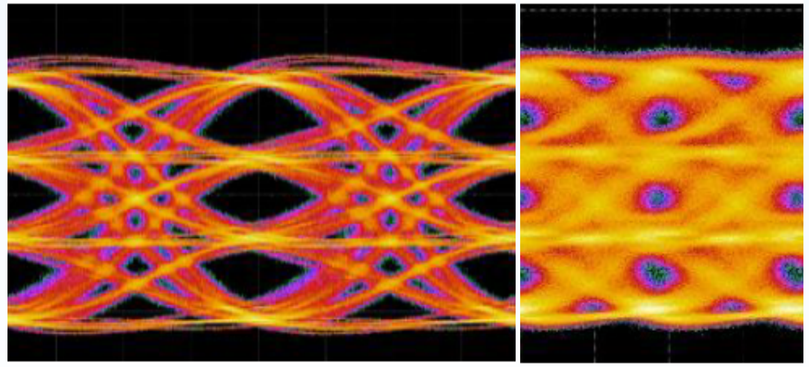
Modulation formats

- Non-Return to Zero (NRZ) vs 4-level Pulse Amplitude Modulation (PAM4)
  - Optical physical layer is Signal-to-Noise Ratio (SNR)-limited at both 28 Gb/s NRZ and 56 Gb/s PAM4
  - Strong FEC schemes are needed to reach errors rates of below 10^{-12}
    - This is particularly important for PAM4, which comes with an 11-13 dB SNR penalty.

https://www.linkedin.com/pulse/100g-qsfp28-400g-qsfp56-dd-sean-davies/







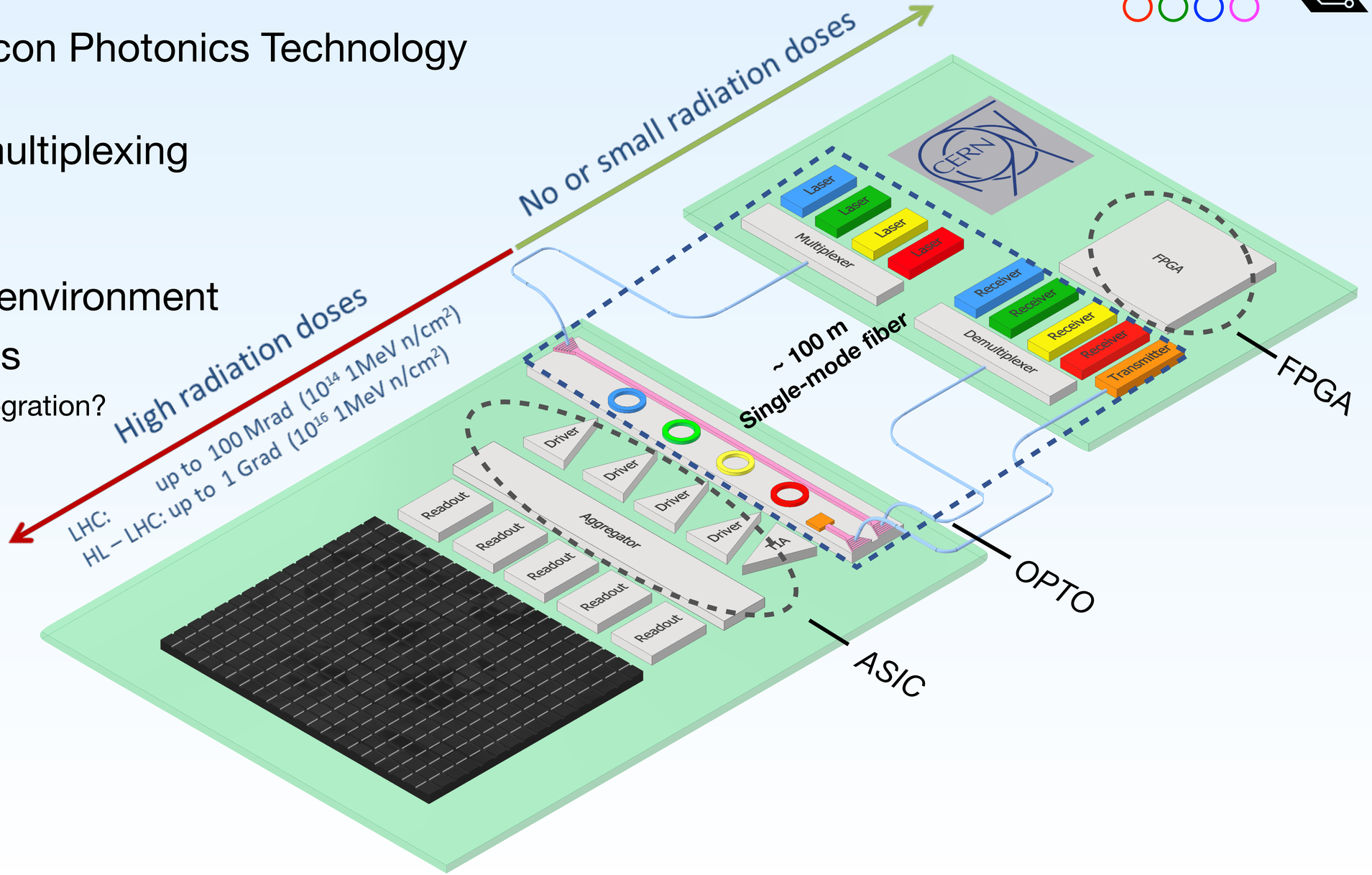
Electrical *Optical*

CERN EP R&D WP6 - High Speed Links

- Provide the future HEP systems with:
  - High bandwidth – reaching 100 Gb/s / fibre
  - High radiation tolerance – exceeding 1 MGy & 10^{16} particles/cm^2
  - Low power, low mass
- Evaluate new technologies to achieve those goals
  - More advanced CMOS ASIC processes
    - Aligned with WP 5 – move to 28 nm CMOS
  - Evolution of supported line rates in latest and future Optical Networking protocols, as supported by FPGAs
    - Two-level On-Off keying (NRZ) data rates up to 56 Gb/s vs higher-order modulation (PAM4) for 112+ Gb/s
    - Settled on 25 Gb/s NRZ due to design complexities of higher rates & modulation formats
  - Wavelength-Division Multiplexing (WDM)
    - using several (e.g. 4) wavelengths to send “parallel” data-streams down the same physical optical fibre
  - Silicon Photonics
    - Using standard CMOS manufacturing processes to build structures that manipulate light in optical waveguides on a silicon substrate

WP6 Project Overview

- 28 nm CMOS and Silicon Photonics Technology
  - RadHard “promise”
- Wavelength division multiplexing
  - Lane: 25 Gb/s NRZ
  - Fibre: 100 Gb/s
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



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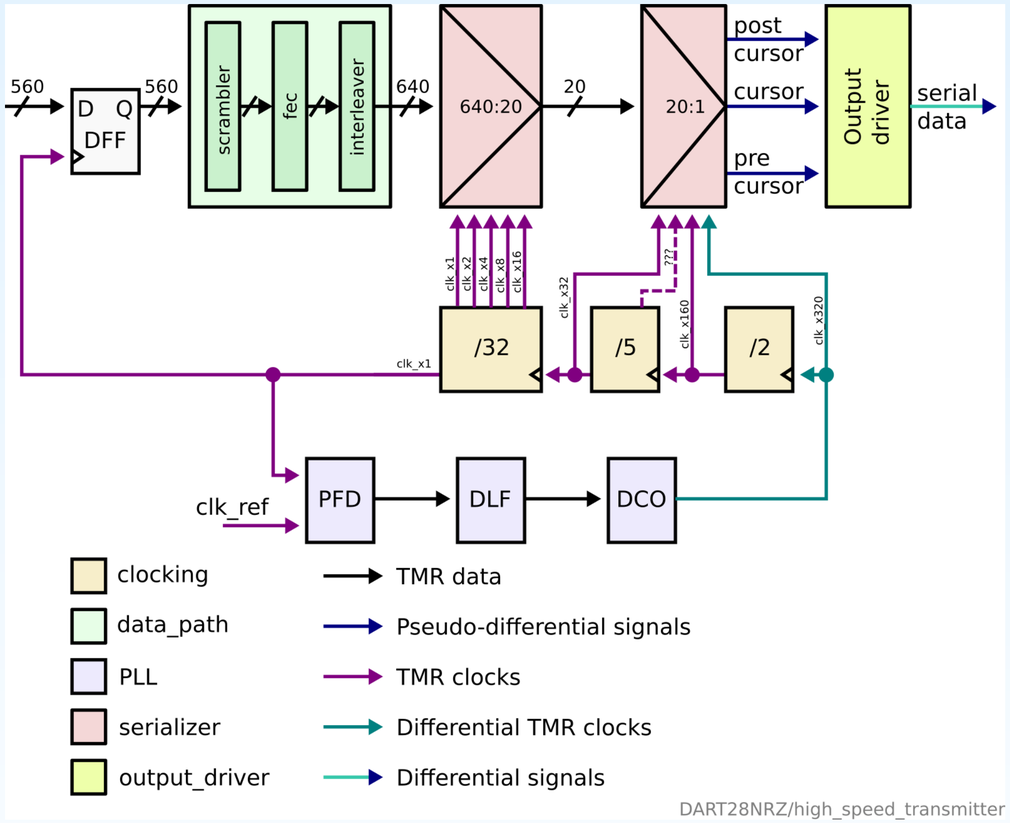
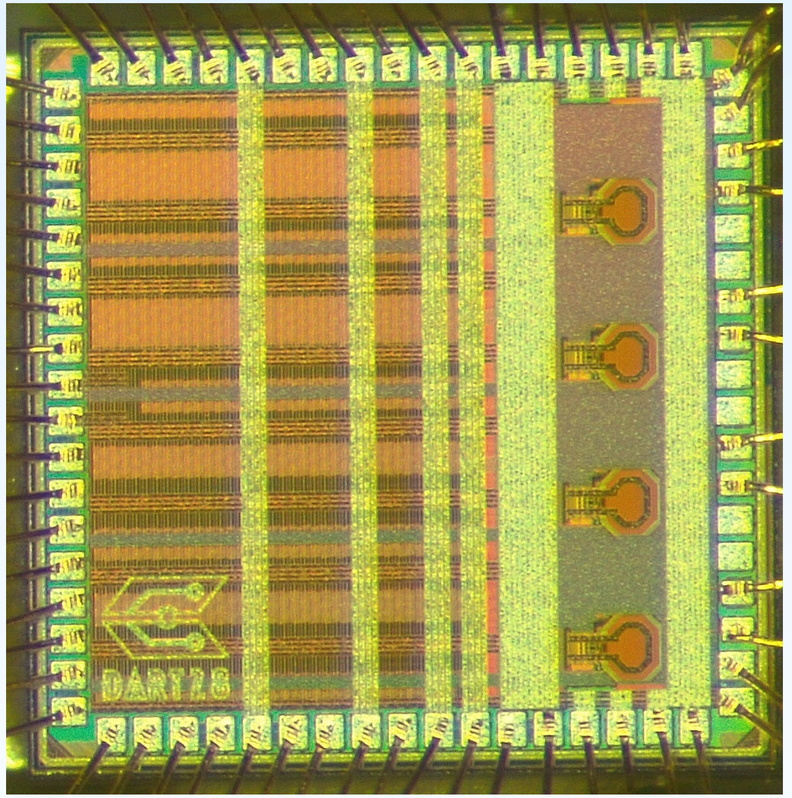
Activity area 1: ASIC

- Aim to demonstrate ASIC design feasibility in 28nm CMOS for
  - High-speed serialiser with 25 Gb/s output
  - High-performance PLL-based clocking circuitry needed for serialiser
  - High-speed line driver with 25 Gb/s output
  - High-speed Silicon Photonics ring modulator driver with 25 Gb/s output
  - High level of radiation tolerance at the 10 MGy level

- Single ASIC demonstrator: DART28

DART28

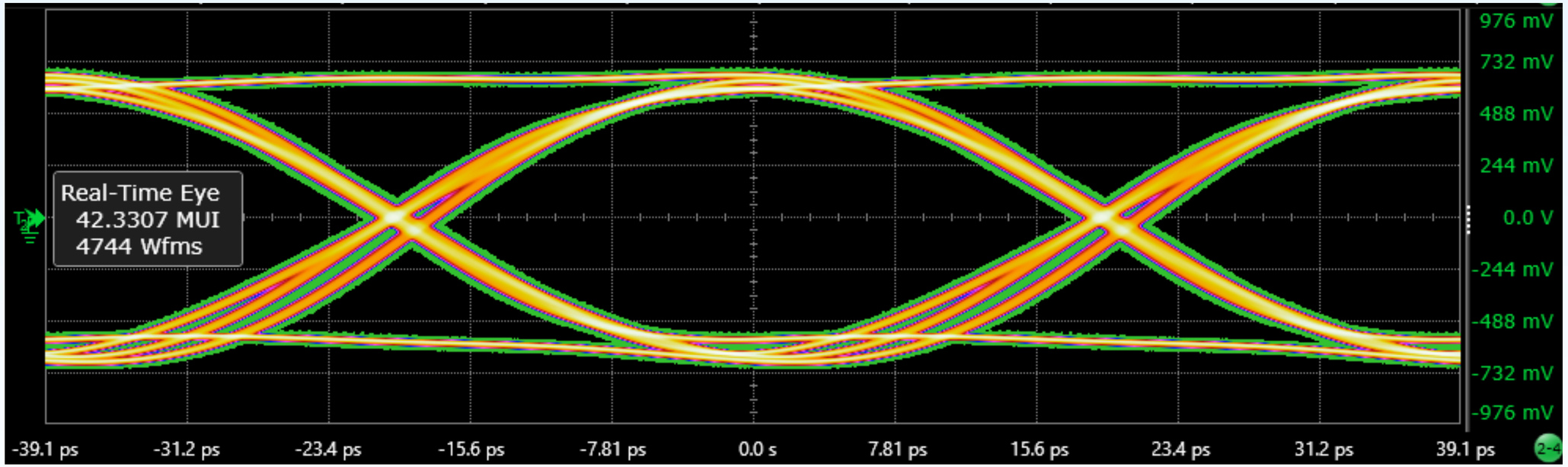




- Design successfully completed and submitted
  - Samples received in late summer 2023

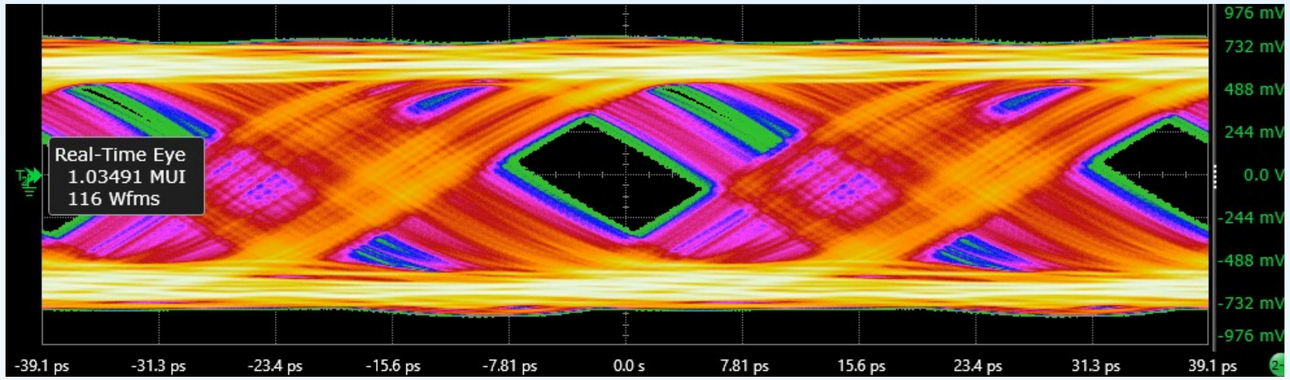
DART28 Performance

- Measured excellent high-speed performance of the electrical output
  - Transition times clearly sufficient for 25 Gb/s data-rates



DART28 power decoupling

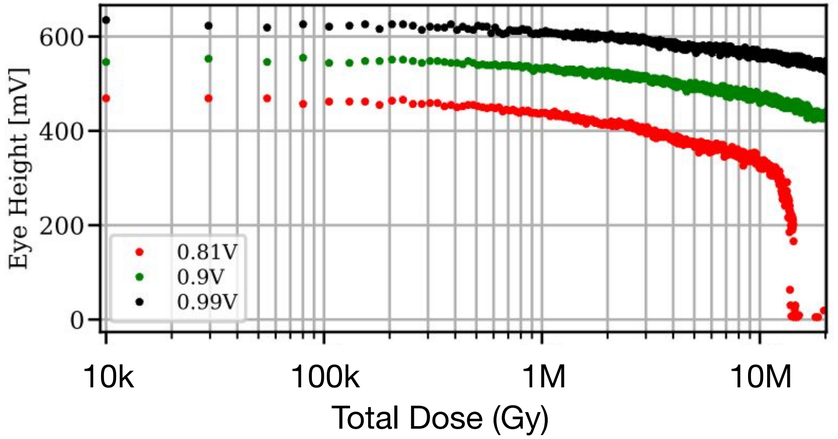
- A limitation was found when running arbitrary data

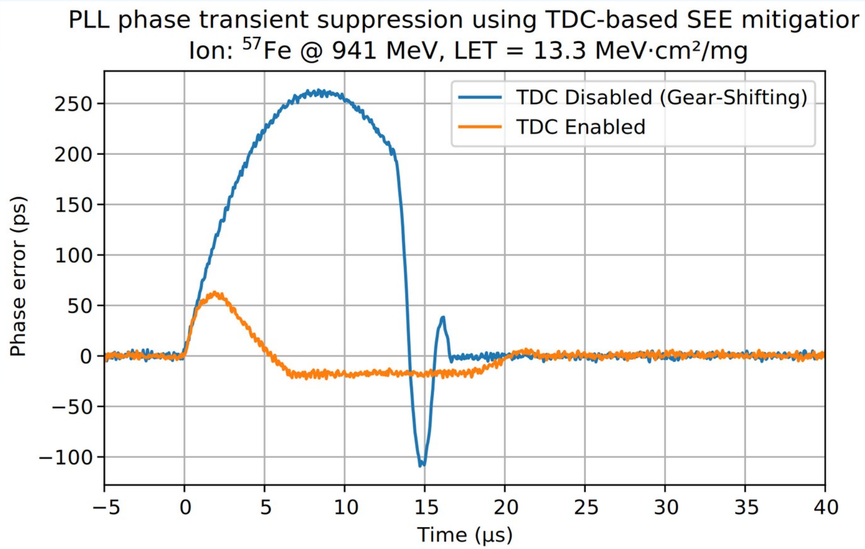


- Was shown in simulation and lab-testing to be due to limitations in the power delivery network
  - Combination of on-chip decoupling, interconnect & PCB inductance
  - Currently working on methodology for host-board and chip simulation to ensure that it can be mitigated in future prototypes/implementations

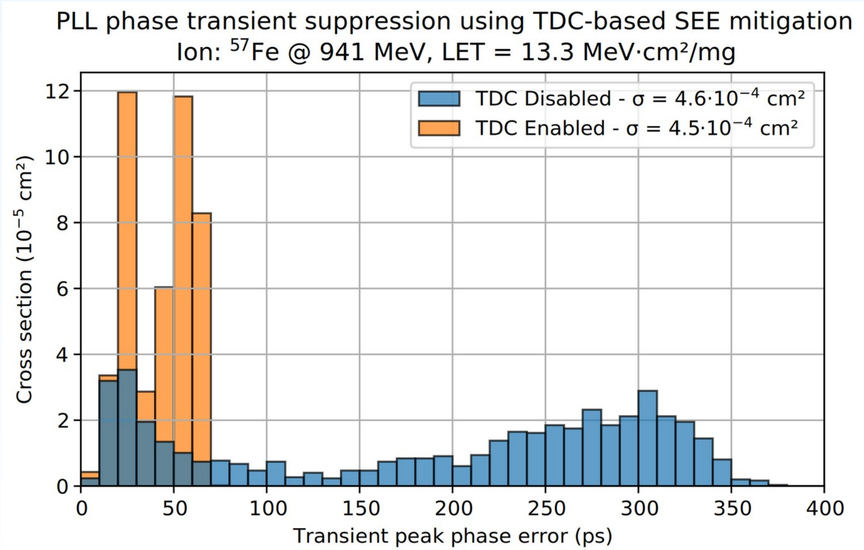
DART28 Irradiation testing

- Total Dose testing with CERN X-ray machine
  - No significant changes in performance observed up to 14 MGy
- Heavy-Ion testing
  - Concentrated on Single Event Effects in PLL
  - Novel ADPLL design to mitigate phase jumps that were observed in e.g. lpGBT shown to be effective in removing PLL-induced bit errors





Long-lived phase excursions mitigated by design



When enabled, phase deviation is suppressed eliminating Bit Errors

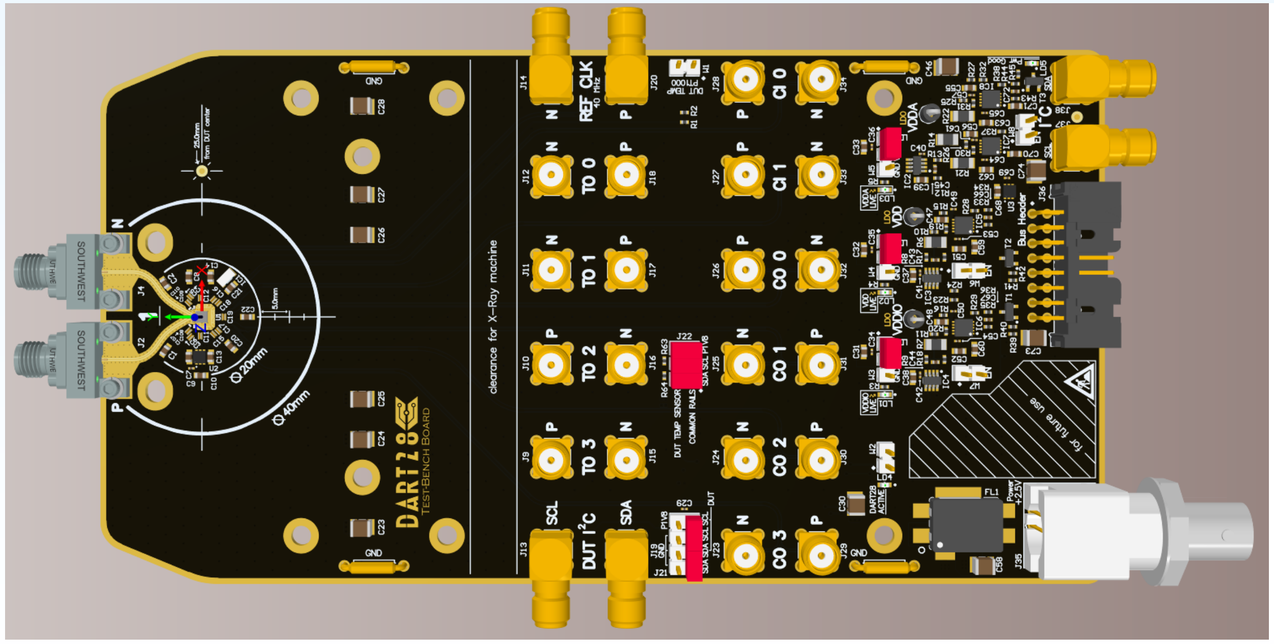
Activity area 2: FPGA

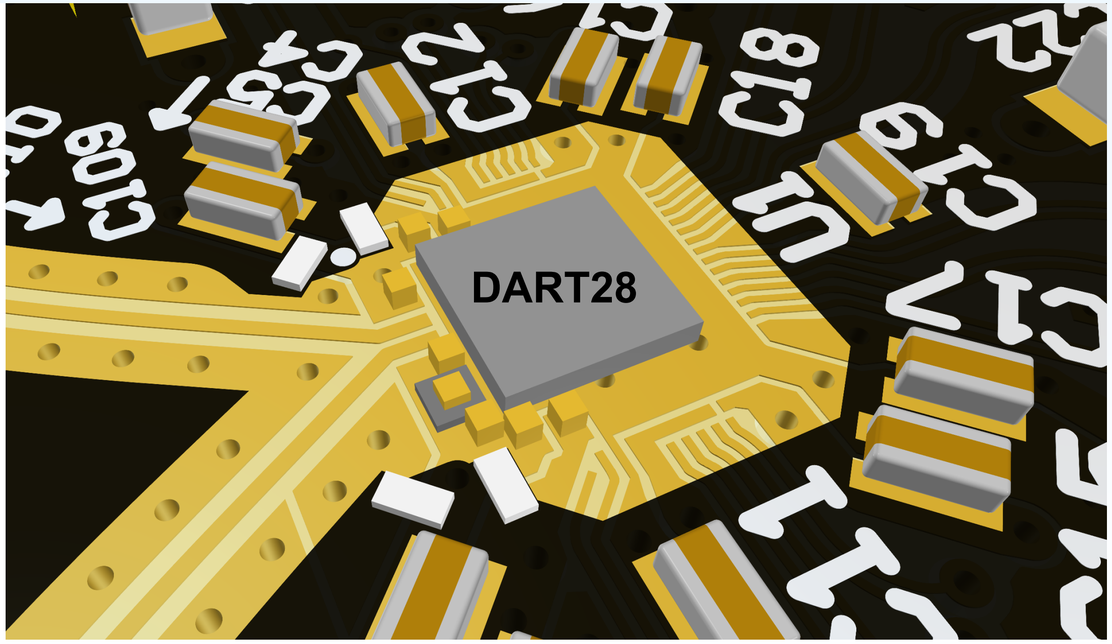
- Two main activities so far:
  - Emulation and testing of the DART28, evaluation of COTS and FPGAs for high-speed links
  - 100GbE2FE: a new addition started in mid-2023 to investigate the possibility of transmitting data directly from Detector Front-Ends into commercial 100 Gigabit Ethernet networks

- Added a third activity in Feb-2024:
  - High Precision Timing: investigate deterministic timing link solutions independent from FPGA family/manufacturer

Emulation and testing of DART28

- Logic Emulation & Testing:
  - Full DART28 chip logic translated into FGPA firmware to allow emulation and testing by being able to receive data transmitted by DART28 for lab- and irradiation testing
- Hardware Testing:
  - Design and fabrication of DART28 test board using high-speed design and layout techniques
  - Boards used for all DART28 characterisation





100GbE2FE

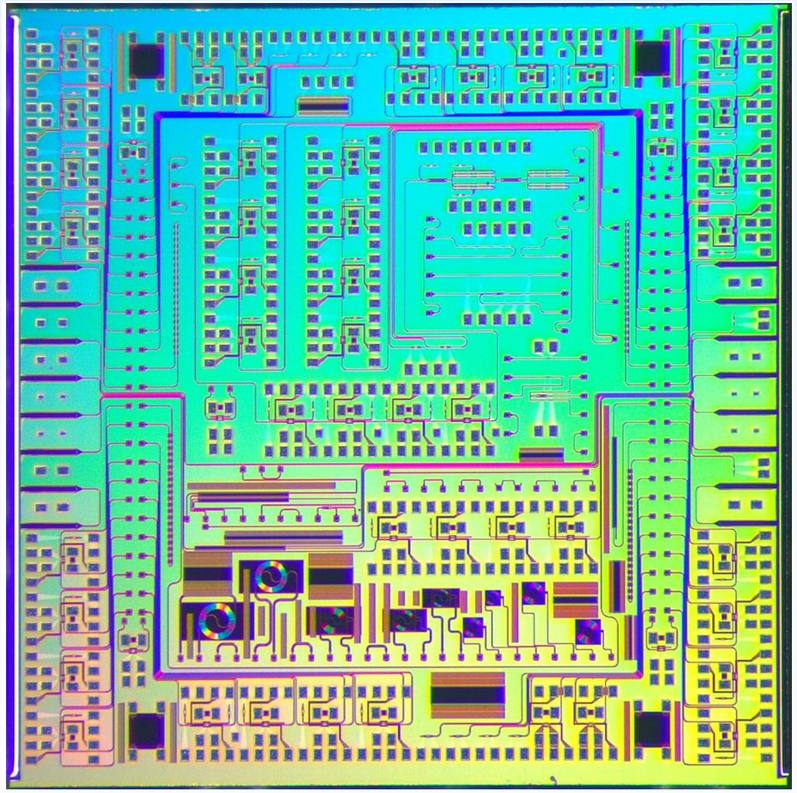
- Long-standing topic of sending data from detector front-ends directly into a commercial standards-based DAQ network
- Challenges
  - Asymmetry of data volume – detectors output far more readout data than they need control data
  - FEC – larger ethernet frames use different FEC than currently implemented in custom FE links
  - Fixed/low latency – depending of system-level choices, could be as important as it is in current FE links
  - LHC-clock synchronisation – Ethernet base clocks are not compatible with accelerator timing
  - Compatibility with existing links – can e.g. lpGBT links be aggregated into a commercial network
- First results
  - Unidirectional 100GbE link between a FE-emulator in FPGA and a commercial NIC
  - Compatibility of 100GbE standard FEC with irradiation-induced link errors in DART28 confirmed
  - Protocol translator implemented for lpGBT -> 10GbE in Artix and Polarfire as a first step towards 100GbE (in collaboration with WP9)
  - FPGA-based SFP+ pluggable module for lpGBT -> 10GbE with a commercial network switch identified

Activity area 3: Silicon Photonics

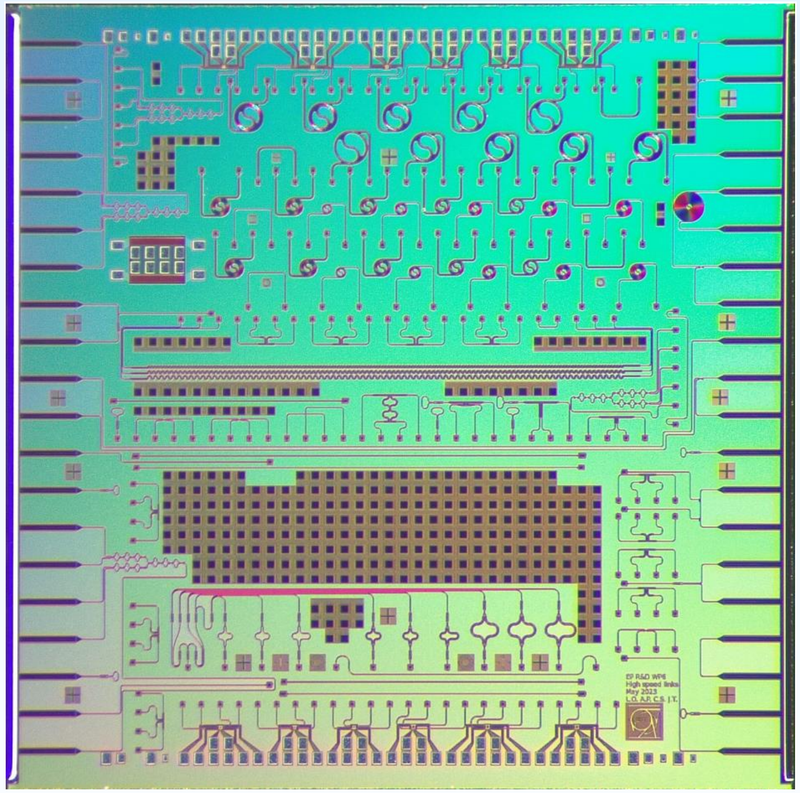
- The Silicon Photonics activity area is split into three sub-topics:
  - System and component design, simulation, and testing
  - Irradiation testing and simulation
  - Packaging/integration

Photonic Integrated Circuit design

- Have recently received two PIC designs



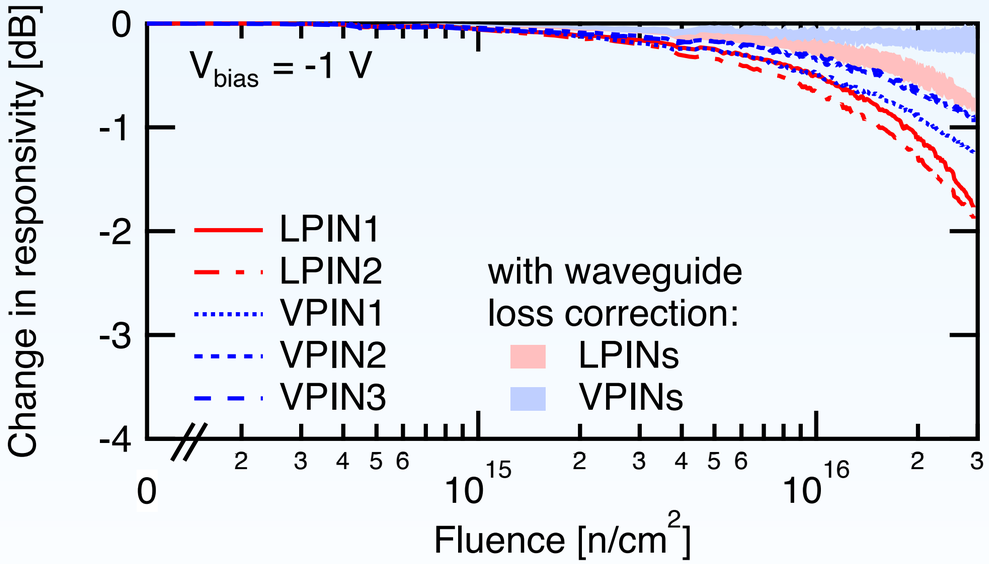
System PIC
Doped devices (modulators, photodiodes)
4-channel WDM demonstrators
Polarisation-diversity test structures

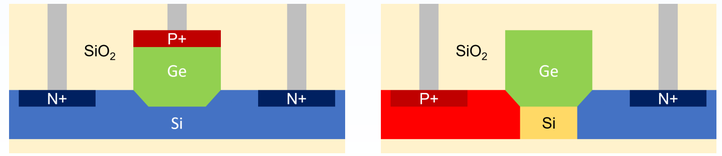


Packaging PIC
Edge-coupling test structures
WDM demux test structures
Waveguide performance test structures

PIC Irradiation

- Radiation tolerance studies have investigated the impact of Ring Modulator design parameters and impact of temperature on device degradation
  - High-levels of doping in the RM junctions make these devices radiation tolerant
  - Raising device temperature using built-in micro-heaters further improves radiation tolerance
  - Small amounts of forward current are also effective at annealing radiation damage
- Heterogenously integrated Germanium Photodiodes will be a key component in bi-directional links
- Extensive study of irradiation of Ge-PDs show impressive radiation tolerance
  - With small reverse bias, Vertical Junction PIN photodiodes are tolerant well beyond 10^{16} /cm^2

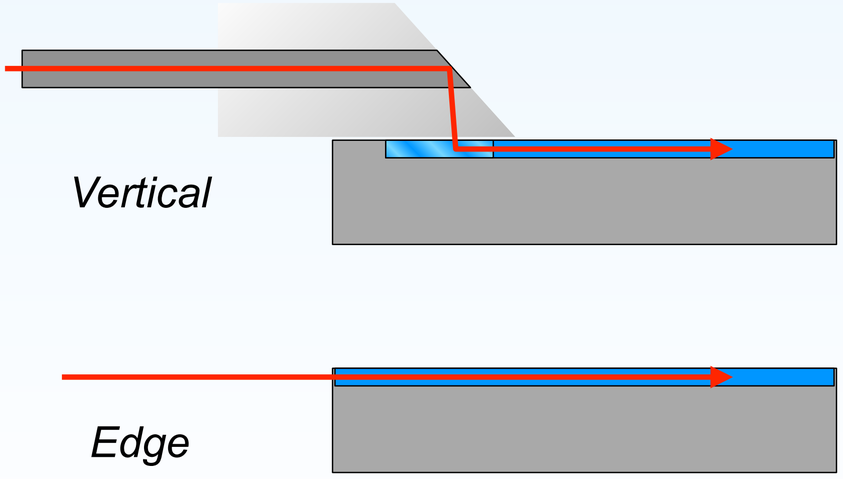


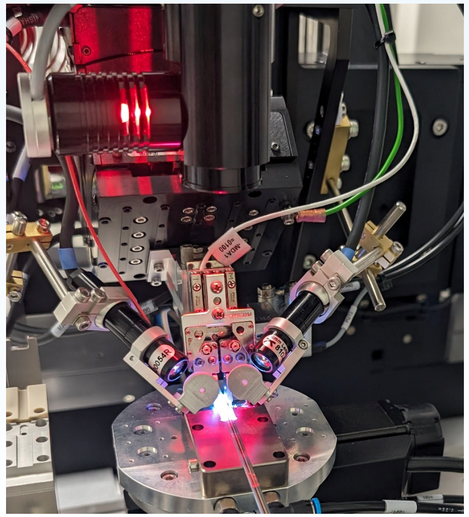


VPIN *LPIN*

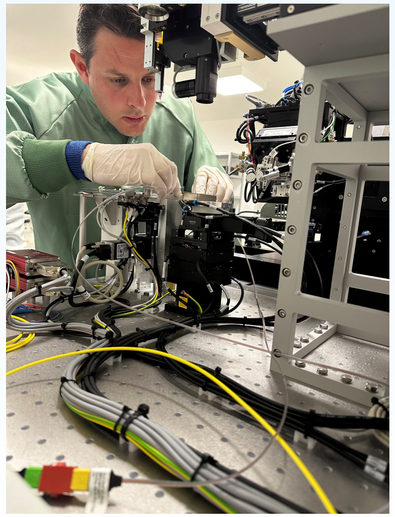
Packaging/Integration

- Reinstatement of activity in 2023, to investigate methods of fibre coupling to PIC as well a more generally how to integrate photonic with electronic circuits
- Major step has been the purchasing of an automated optical fibre alignment machine to enable the use of edge-coupling of optical fibres to PICs
  - Edge-coupling loss significantly lower than the vertical coupling used so far

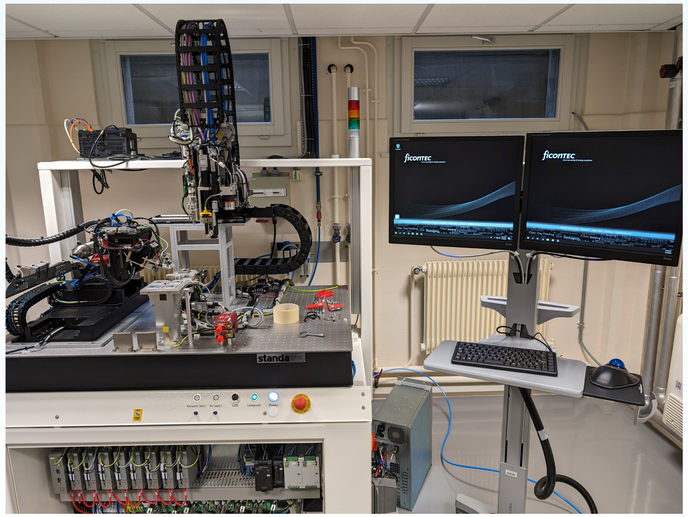




Alignment head



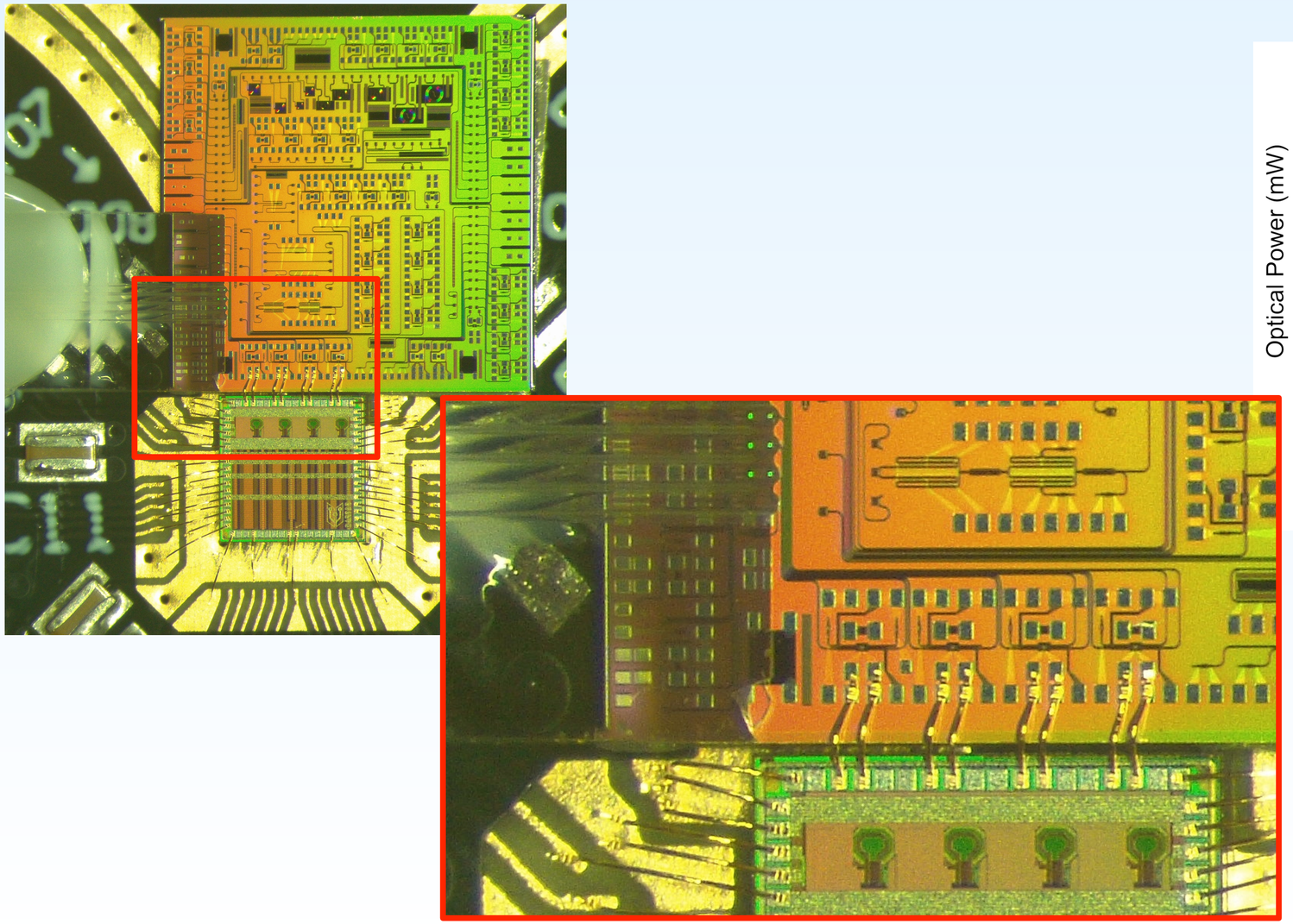
Device loading

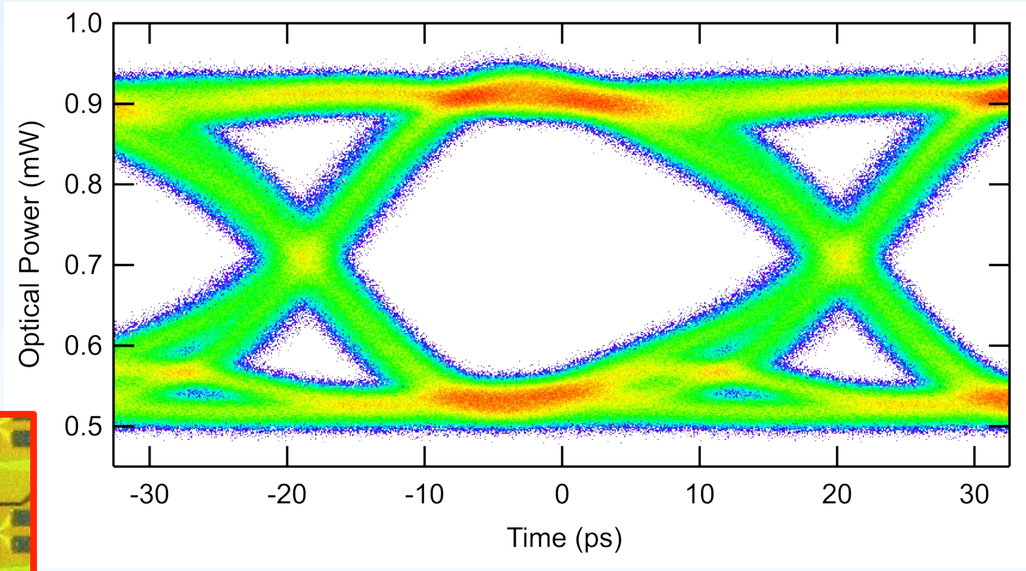


Machine installed in B13

DART28 Driving SiPh Ring Modulator

- Joint evaluation bringing together all WP6 areas





Transmitting 25.6 Gb/s PRBS7 data

Next Steps: ASIC

- Consolidation of understanding of high-speed output driver powering
  - Recommendations for implementation of host-board interface
- Packaging of the existing design blocks to allow their exploitation by other projects
- Investigation of new circuit architectures to increase the output drive amplitude for Ring Modulators
- Design and implementation of feedback and control loop for RM temperature control to allow wavelength-locking of WDM channels
  - Based on ADCs for monitor photodiodes and DACs for micro-heaters
- Full chip integration into a second demonstrator
- Implementation of a CDR circuit and TIA for control data, followed by a demonstrator chip
- Kick-off RadHard FPGA study

Next steps: FPGA

- Link Back-End and System
  - Contribution to host-board interface implementation
  - Preparation of firmware for PIC automatic configuration and startup
  - Preparation of next-gen DART emulation and testing
  - Continued evaluation of suitable back-end parts for interoperability with custom front-end
- Timing (new activity)
  - Preparation and implementation of test benches for timing-related ASIC testing/evaluation from WP6 and beyond
- 100GbE2FE
  - Asymmetric link demonstrators
  - Conversion module to link FE to commercial switch

Next steps: Silicon Photonics

- System
  - Evaluation of system-control devices/circuits (temperature, polarisation, wavelength)
  - Evaluation of RM design parameters
  - Submission of next-gen system testing PIC based on evaluation results
- Irradiation
  - Evaluation of radiation tolerance of waveguide structures
  - Evaluation and modelling of RM radiation effects
- Packaging/Integration
  - Exploitation of fibre-attachment machine to demonstrate and evaluate fibre edge-coupling
  - Evaluation of industry developments in PIC packaging

Collaboration

- The EP R&D WP6 team is tightly integrated into several projects within DRD7
  - Project 7.1a “Silicon Photonics Transceiver”
  - Project 7.3c “Timing Distribution Techniques”
  - Project 7.5b “From Front-End to Back-End with 100GbE”

- In addition, there are synergies with other groups investigating the adoption of this technology in future experiments, e.g. LHCb

- More broadly, integration techniques for use on future front-end hybrids might provide additional opportunities in future

Summary

- Future HEP detectors will deploy high-speed optical links for readout and control
  - Specific detectors may well have their own development sweet-spot due to their specific requirements
    - Data-rates, SWAP, radiation tolerance, magnetic field immunity, cost…
  - Some level of industry compatibility will be essential to contain the overall system cost
    - Customisation is always more expensive than expected!
- Generic technology building blocks are being investigated in multiple HEP labs -> DRD7 project on Silicon Photonics
- The earlier we hear about new system requirements, the sooner we can assess how far removed they are from the current investigation paths
  - Then DRD7 would be the right place to add R&D