BLM Thresholds WG

https://indico.cern.ch/event/1419391/

BLM ASIC: DEVELOPMENT SUMMARY & FUTURE PROSPECT

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OVERVIEW

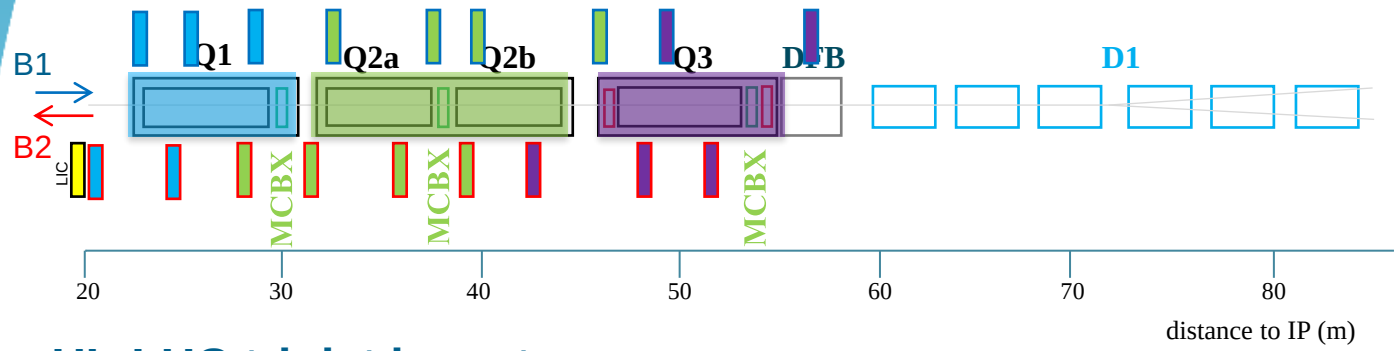
HL-LHC BLM Deployment Plan

- LS3
  - Extension of the current BLM system with additional detectors following HL changes
    - e.g. IP1 & IP5 Triplet, Collimation, BBLR, etc. areas
  - First deployment of the full new electronic stack at strategic locations in parallel to the current electronics
    - to complete and validate development
- LS4
  - Full deployment of new electronics
    - replacement of the complete tunnel electronics stack (mini-racks, crates, power supplies etc.).

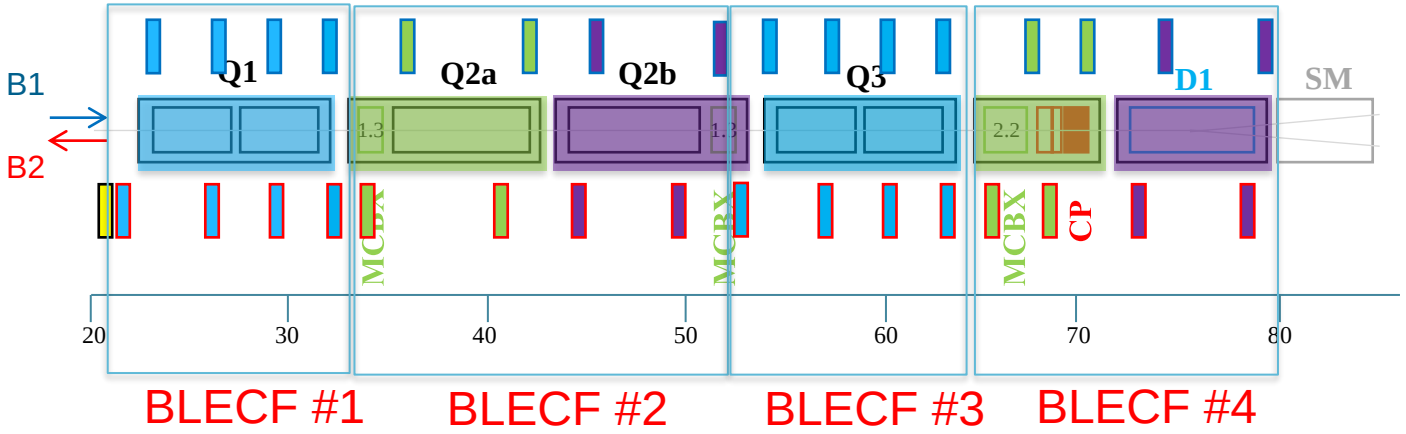
BLM detectors at LS3 Triplet Layout

Work in progress between SY-BL, SY-STI & WP15;
Final integration might change numbers

LHC triplet layout



HL-LHC triplet layout



Single multiwire cable per module
One BLECF or BLEIC module accepts 8 channels

During LS3 will extend the current system for the new topology and deploy the new system (BLEIC) in parallel in half of the locations.

Will allow validation for full deployment during LS4 and (some) redundancy in this critical area long-term.

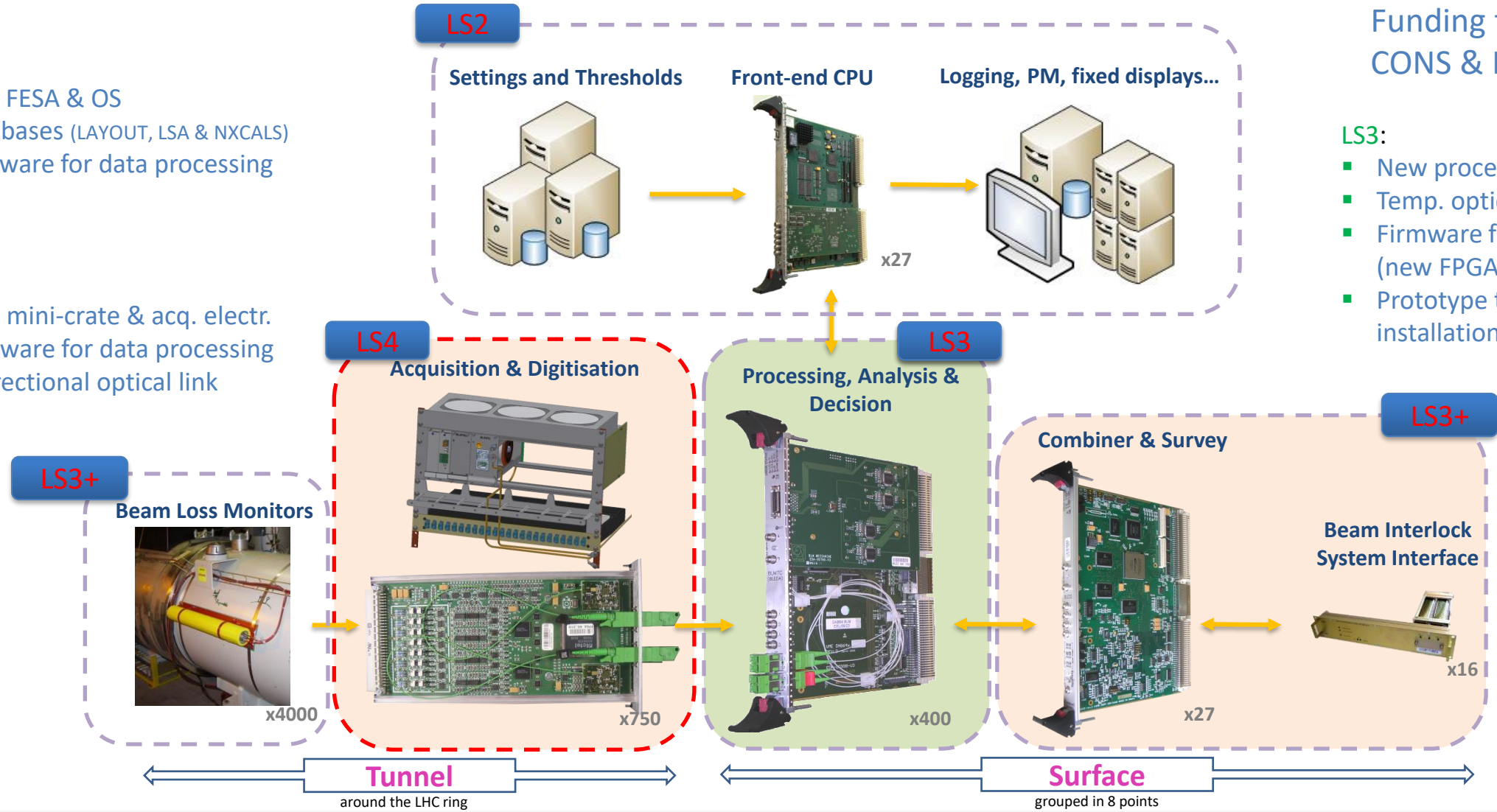
Current system w/ BLECF // BLEIC/2 (Half channel redundancy)

Number of detectors: Total for IP1 + IP5 (both sides)			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	72	128	56
BLEIC – new	0	**64**	64
Total IP1+IP5	**72**	**192**	**120**

LHC Beam Loss Monitoring System – Upgrades

LS2:
- New FESA & OS
- Databases (LAYOUT, LSA & NXCALS)
- Firmware for data processing

LS4:
- New mini-crate & acq. electr.
- Firmware for data processing
- Bidirectional optical link

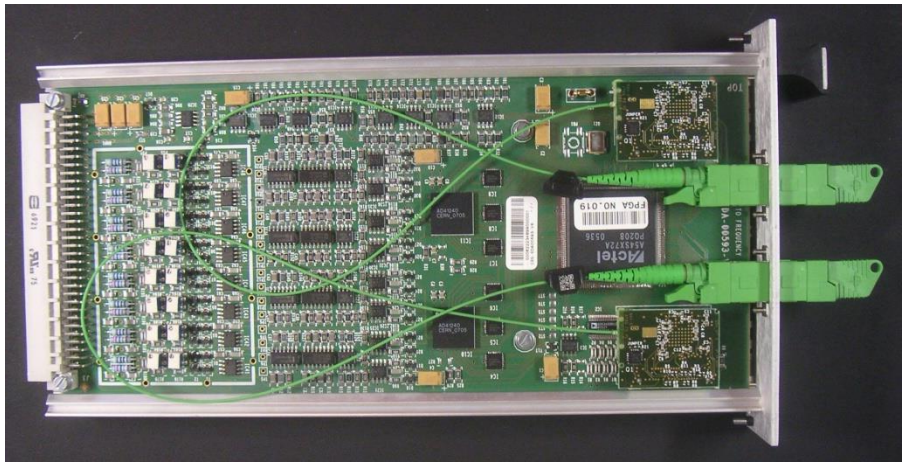


Funding through R2E, CONS & HL-LHC projects

LS3:
- New processing electronics
- Temp. optical receivers
- Firmware for data processing (new FPGA)
- Prototype tunnel electronics installations at LHC & SPS

LS3+:
- Add. Detectors
- New BIS Interlock concentrator (CIBFX)

BLM LHC Acquisition module



Components:

- 8 inputs Current-to-Frequency Converter (COTS)
- AD41240 ADC (EP-ESE)
- LM4140 voltage reference
- Antifuse FPGA for data collection
- Redundant GOH from CMS (GOL from EP-ESE)
- CRT910 Line driver (EP-ESE)
- AD5346 DAC

Specifications:

- Radiation tolerant up to 500 Gy
- Reliability level SIL3 (1E-7 to 1E-8 failure/h) to damage of equipment
- Current measurement range 2.5pA to 1mA
- Integration time of 40 us
- Input protection
  - Current ~ 10A @100us
  - Voltage ~ 1500V @100us
- Redundant optical data transfer to surface
- Test features for system check
  - Survey of the card voltage supplies
  - Survey of detector high voltage supply

Future Specifications Summary

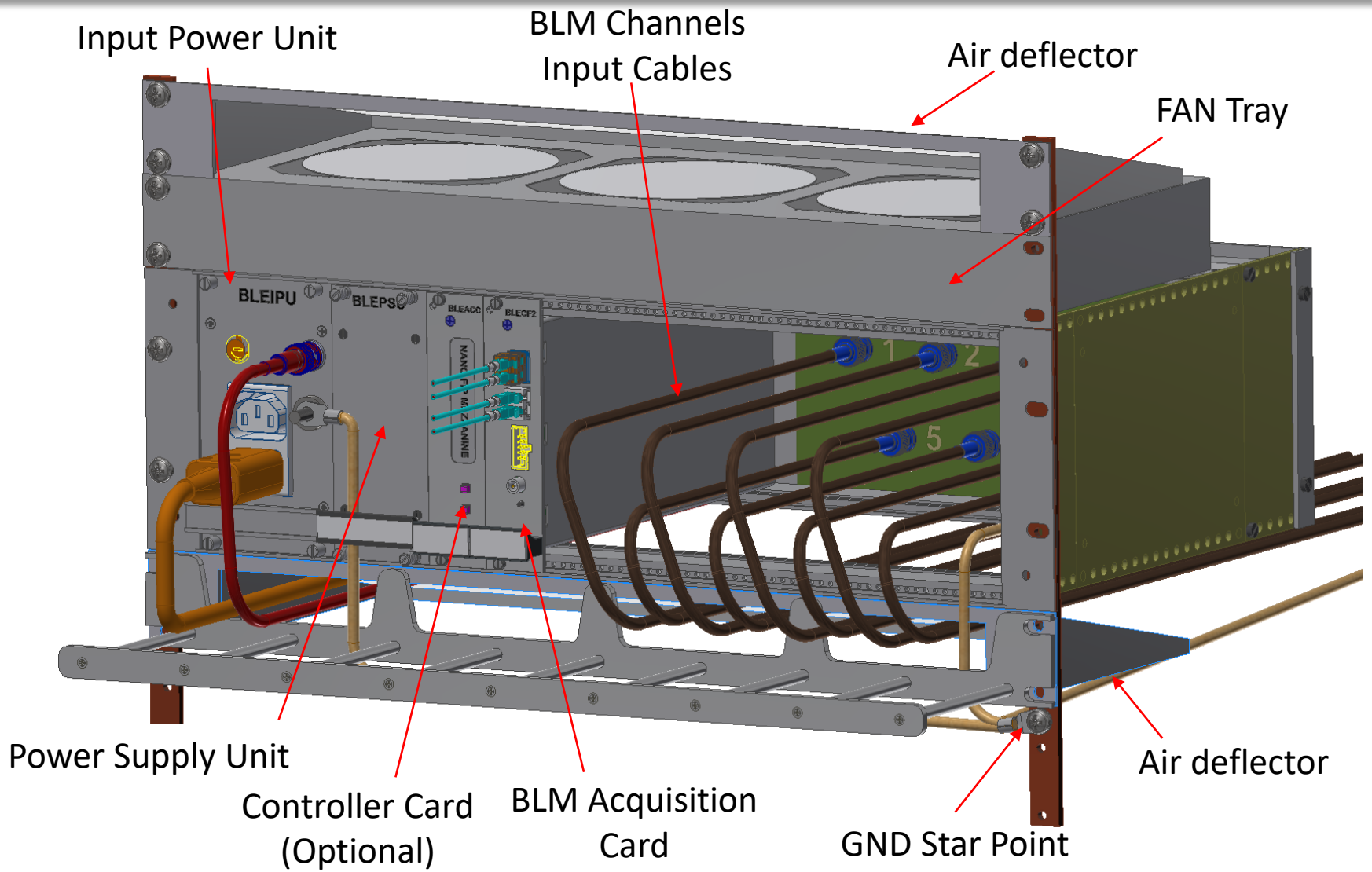
- Main functionalities
  - Radiation tolerant electronics up to 1 kGy
  - 10 µs acquisition period & real-time processing
  - 8 orders of dynamic range (from few pA to 1 mA)
  - On-board diagnostics and telemetry
  - Bidirectional communication with the acquisition electronics
- Equal/similar specifications needs for SPS and LHC
  - Deployment at LHC during LS4, i.e. after validation in SPS
  - Harmonisation across the Accelerator Complex with two systems to maintain (PS Complex and LHC/SPS systems)
    - Reduce effort in procurement, testing and spares management

Design Objectives

- Build a configuration able to host both the BPM & BLM upgrades:
  - those systems share location and resources (power, fibres etc.)
- Harmonise electronics across machines:
  - Common SPS & LHC BLM architecture (on-going global harmonization effort)
  - Share elements between LHC & INJ BPM systems
- Maintain backwards compatibility (on the LHC BLM side)
  - BLM Acquisition module & Power Supply Units
  - i.e. pin to pin compatible with the current chassis backplane
- Improve the acquisition system performance:
  - Radiation tolerant up to 1 kGy (currently at 500 Gy).
  - Integration period of 10 µs (currently at 40 µs).
- Improve safety:
  - Additions to maintain the SIL3 for safety critical systems.
  - Protection against direct contact to HV or 230 V_{AC}.
  - Grounding improvement
- Improve reliability:
  - All modules encapsulated in metal boxes (prevent transport damage)
  - Reduce number of interconnections
  - Simplify manufacturing
  - Simplify optical transceiver interconnection.
- Improve maintainability:
  - Reduce repair time
  - Declassify the repairing complexity
  - Additional diagnostics.

Requirement	Critical/ Wish	Target
Radiation tolerance	C	1kGy / 20 years
Chassis MTTF calculated with handbook 217plus at 40˚C	C	> 1 E+07 h
Power supply MTTF (using MIL217plus at 40˚C)	C	> 1 E+06 h
Component derating	C	< 50%
Global Power requirement	C	≥ 50 W
Mini-crate height	C	< 400 mm
Chassis height	C	3U
Chassis depth	C	220 mm
Connector Pins pitch	C	≥2.54 mm
Connector mating cycles	C	500
Backplane connector P.N.	W	09 03 264 2825
Backplane PCB thickness	C	2.2 mm
PCBAs quality	C	* See note below
Required voltage 1	C	+1.5 VDC (5 W)
Required voltage 2	C	+2.5 VDC (10 W)
Max ripple for digital voltages	C	50 mVpp
Required voltage 3 (with linear voltage regulator)	C	+5 VDC (5 W)
Required voltage 4 (with linear voltage regulator)	C	-5 VDC (5 W)
Max ripple for analog voltages	C	10 mVpp
Ventilation air flow	C	500m^3/h
FAN MTTF (using MIL217plus at 40˚C)	C	> 4 E+05 h
Component quality	W	Automotive

New BLM mini-crate

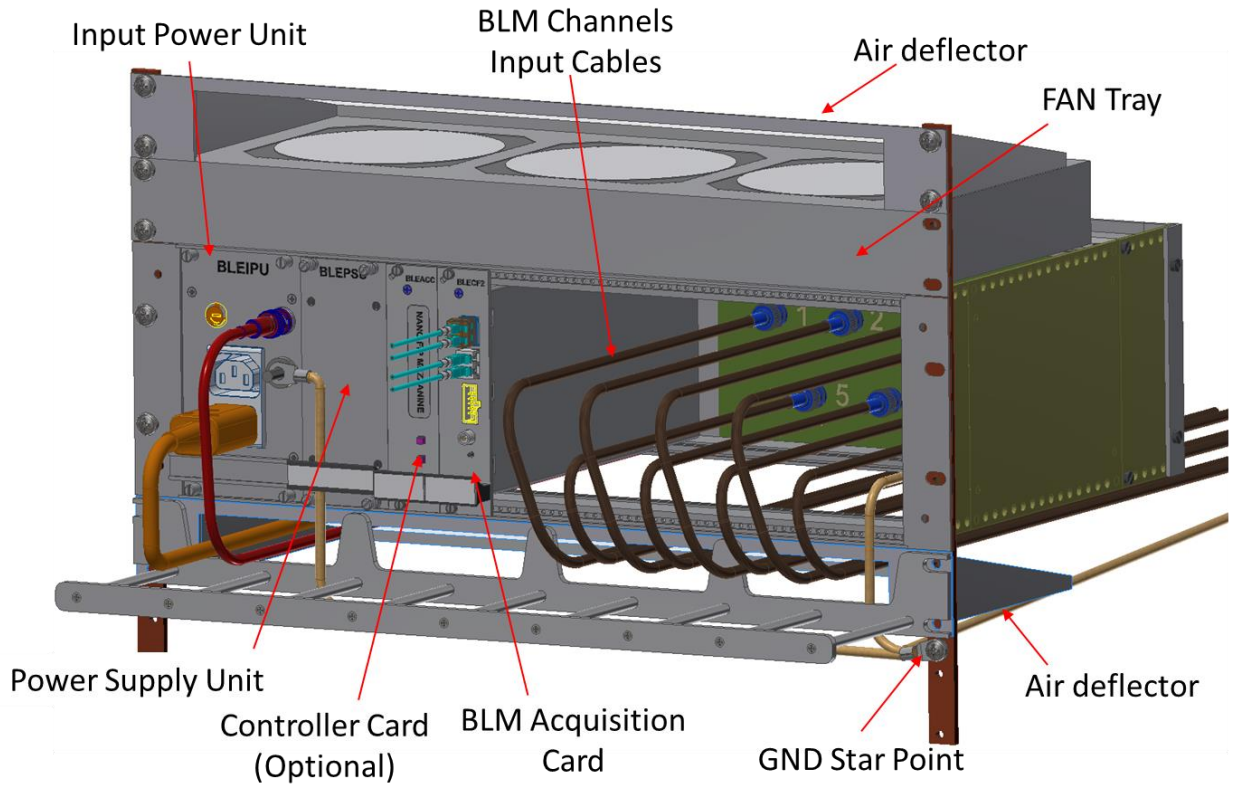


Characteristics:

- Front access
  - Applies to all connections and modules
  - Allows mini-crate to be installed at the wall side
  - Easier access during maintenance
- Controller card
  - Redundant functionality
  - nFIP connection
- Custom backplane
  - Targeted design
  - Completely passive
  - Better cable management, i.e. 8x CB50 (coaxial) with BNC connectors

New BLM mini-crate

- New crate design completed
  - Optimised or reliability, low current measurements and quick interventions
  - Prototype version available
  - All critical components in-stock or ordered
- Rad-Tol Power Supply prototype
  - Using several EP-ESE ASICs
  - Tested at CHARM (two runs, ~ 2.5 kGy accumulated)
  - Tested in climatic chamber
- Rad-Tol Front-end prototype
  - Using custom BLM ASIC & several EP-ESE ASICs
  - Tested at PSI (seven runs, ~ 3.5 kGy)
- Currently working on system integration
  - Development of back-end firmware for communication and control
  - First version of the real-time data processing & decision making under test

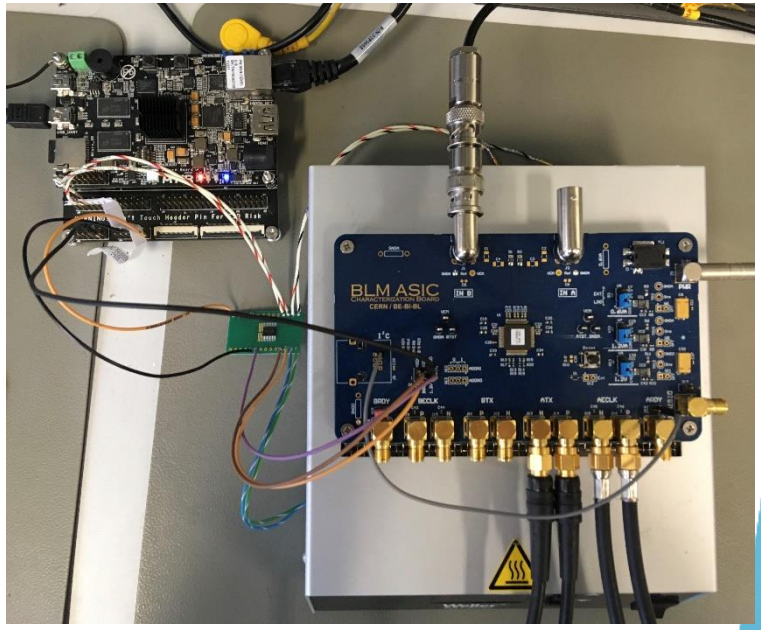


BLM ASIC & BLEIC MODULE

BLM ASIC R&D Timeline

Prototype development timeline:

- 2018 Q1: project start; technology selection and feasibility
  - Parallel design of two methods:
    - CFC asynchronous better suited to handle large currents and quickly varying signals
    - Delta-Sigma ideal for high accuracy due to oversampling and filtering
- 2019 Q4: V1 delivery
  - Issue with internal power distribution and ESD protection
  - Could not test full range
- 2020 Q4: V2 delivery (some delays due to COVID)
  - Mostly functional;
  - Metastability issues with the sync between the analogue and digital domains
  - High current leakage of the input stage FETs; poor low current meas.
  - Decision to continue with the CFC asynchronous method only
- 2022 Q1: V3 delivery
  - Analogue & digital circuits fulfil needs; all currently known issues resolved
  - New minor issue w/ sync between CFC & ADC data; mitigation possible at the backend



Development of custom ASIC verification testbench

BLEIC: BLM Rad-Tol Front-end

New prototype PCB design complete

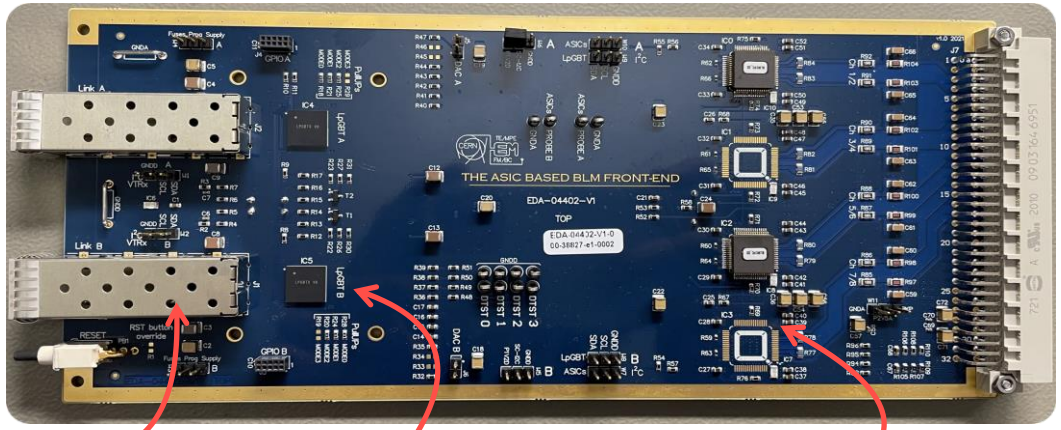
- Based on rad-hard components only
- Includes all functionalities expected from the final system
- Common digital parts, control and form with standard BLM acquisition board.

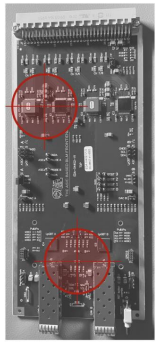
Prototype production completed and tested to be functional

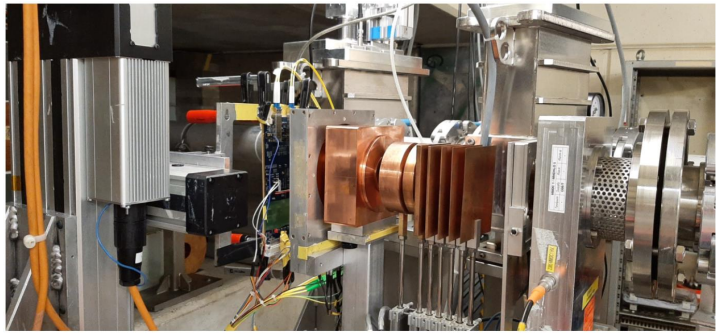
- This board variant is able to accommodate both BLMASIC v2 & v3

Currently working on system integration

- Development of back-end firmware for communication and control
- Next step, integration in the real-time data processing and decision making







Radiation testing at PSI:

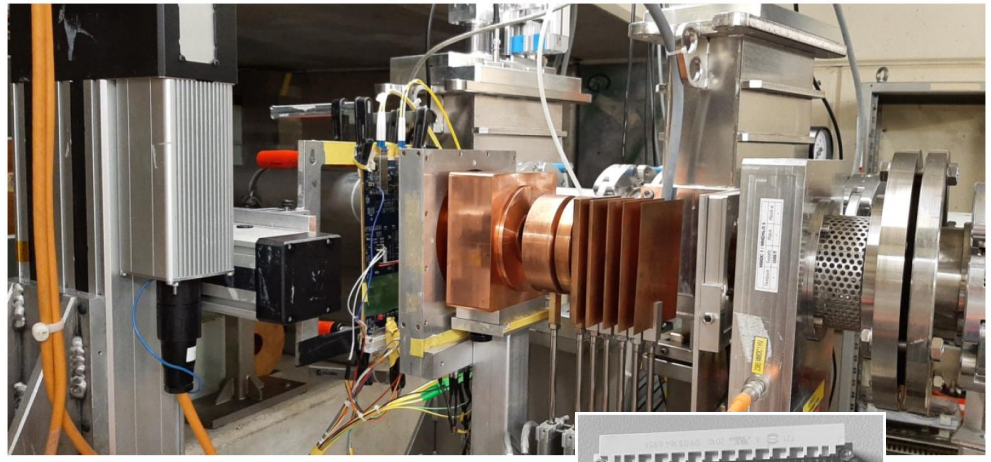
- Beam energy of 200 MeV and
- Flux, at maximum current of 10 nA, was 3.7 × 108 p*cm−2*s−1
- Run 1-6 targeted two ASICs and linPOL12V reaching ~3.3 kGy
- Run 7 (short) targeted the transceivers with 200 kGy

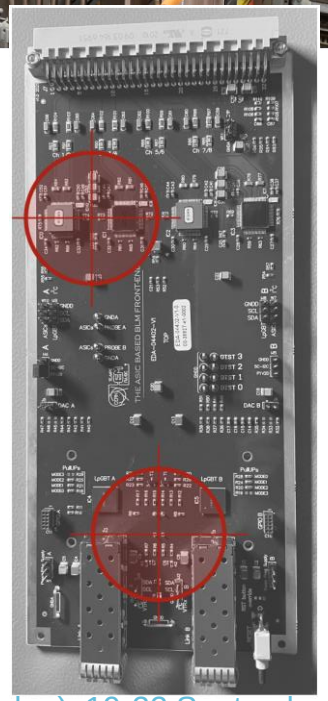
Comparison of old and new technology of radiation tolerant front-ends

	BLECF COTS & ASIC hybrid version	**BLEIC** ASIC version
Components	> 2000 parts	< 400 parts
Cost	> 3 kCHF/unit	~ 1 kCHF/unit

Irradiation – Protons (PSI)

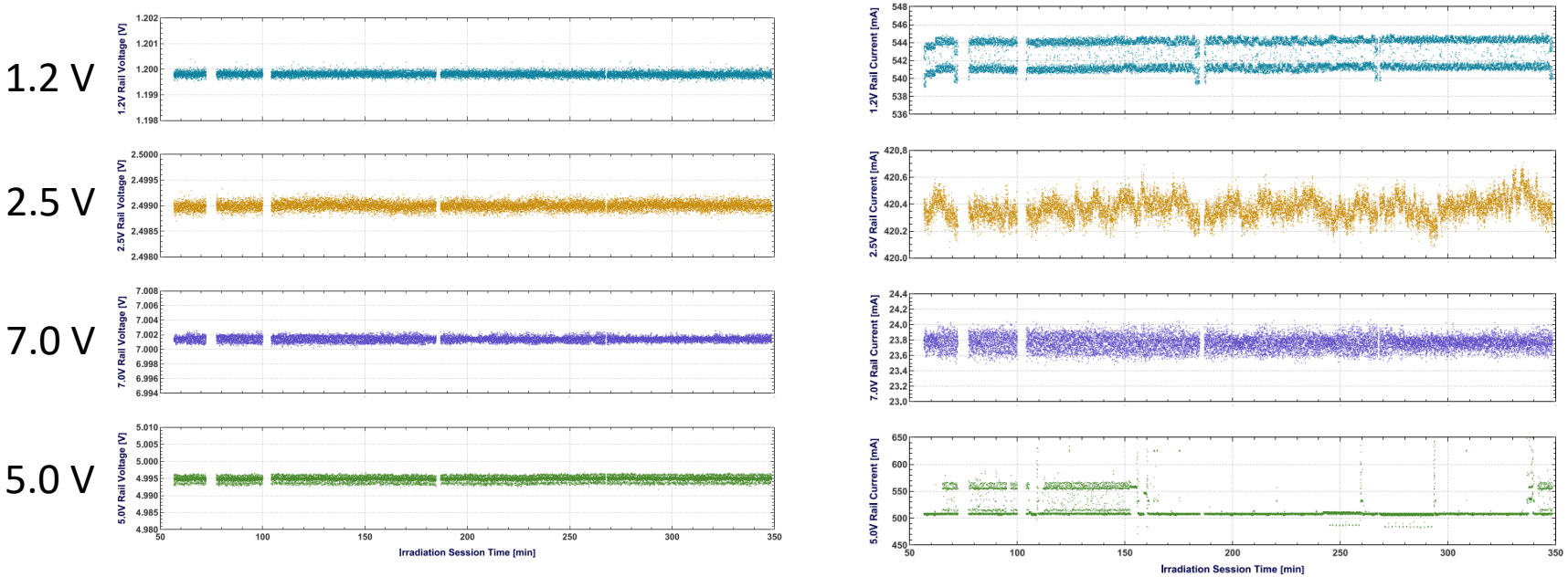
Run	Start Time	Stop Time	Beam Current [nA]	TID [Gy]	Target Area
1	*23:34*	*00:25*	1	50	IC0 / IC1
2	*00:30*	*00:46*	3	50	””
3	*00:51*	*01:14*	7	200	””
4	*01:17*	*02:39*	10	1k	””
5	*02:41*	*04:00*	10	1k	””
6	*04:02*	*05:22*	10	1k	””
7	*05:31*	*05:52*	10	200	Transceivers





- Beam energy of 200 MeV and
- Flux, at maximum current of 10 nA, was 3.7×10^8 p*cm^{-2}*s^{-1}
- Run 1-6 targeted two ASICs and linPOL12V reaching ~3.3 kGy
- Run 7 (short) targeted the transceivers with 200 kGy

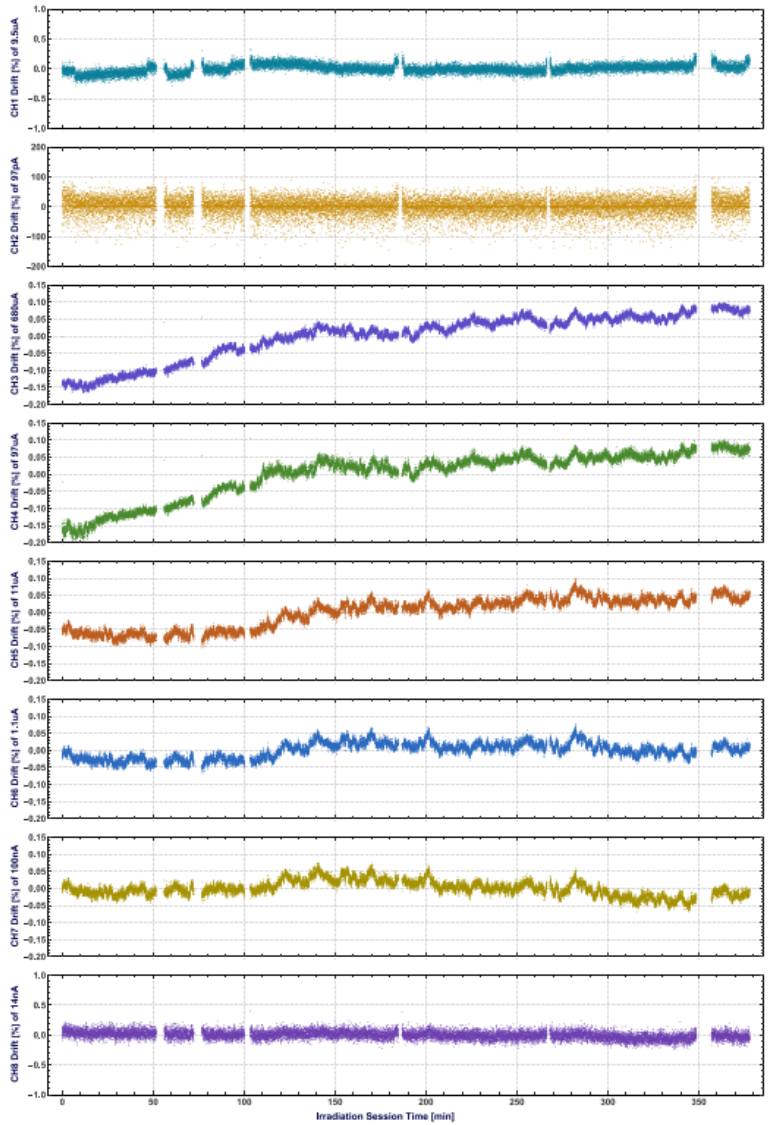
Irradiation – Protons (PSI)



Voltage (left) and Current (right) measurements of the supply rails

- The 1.2 V rail fluctuates into an interval of ≈ 3 mA. This is an intrinsic behaviour of the board that does not relate to radiation exposure nor to an abnormal condition
- No significant change observed. We conclude the onboard regulation is functional and has maintained stable supply throughout the session

Irradiation – Protons (PSI)



Percentage drifts of the current measurements during the irradiation session for each channel

- Channels 1-4 irradiated only
- Max. measurement deviations never exceed 0.5%

Digital domain check

- no errors detected in the 8b/10b coding and the frame parity check between the BLMASICs and the LpGBTs.
- continuity of samples was guaranteed
- no unexpected changes in the registers were observed in any BLMASICs.
- This means that even if SEUs might have occurred, the internal triple redundancy managed to mitigate it.

NEXT STEPS & CONCLUSIONS

Next steps

- Production of BLM ASICs underway
  - Submission to the July 2024 MPW for 2 wafers, i.e. 400 units
  - Dicing & Packaging in October 2024
  - All other ‘special’ components & ASICs bought or secured, e.g. VME, VFC, bPOL, LpGBT, nFIP, VTRx, transformer etc. all procured
- Tests to be performed
  - using a radiation source to induce a signal in the detector,
  - installation in the machine for beam measurements and
  - some destructive tests
- Finalise design of the BLEIC module
  - Series production expected Q3 2025 of 100 units
- Up to 12 extra crates will be available for LS3 installation in LHC
  - Cables have been requested in IP1 & 5 for 48 channels/IP; need to finalise positions
  - All material have been ordered
- Production of all other modules on-going
  - Design office (BE-CEM) has started RHA for BLEICU, BLEPSU, BLECCM modules

Conclusions

- On-going program to harmonise Beam Loss Monitoring across the Accelerator Complex with two systems
  - Common back-end electronics & detectors across the complex
  - Two acquisition systems (PS Complex/TLs and LHC/SPS)
- Development and procurement efforts on-going
  - BLM ASICs available before end of 2024
  - All other ‘special’ components & ASICs bought or secured for both SPS & LHC
- Prototype system in parallel to the LHC BLM
  - Together with the new processing electronics
  - Validation and development of future firmware & software stacks