Requirements for the signal readout electronics for LAr TPC are broadly discussed in the literature. We refer to the readout of the Near Detector proposed for the Deep Underground Neutrino Experiment (DUNE) [1] whose geometry and numbers of readout channels are comparable to the FLARE TPC.

The most probable energy loss for minimum-ionizing muons in liquid argon is 1.66 MeV/cm, which corresponds to ~70,000 electron-hole pairs (the W-value of 23.6 eV) [18, 19]. At a typical drift field of 500 V/cm, only ~70% of the electrons will escape the primary recombination. If we neglect the change losses due to electron trapping by impurities, we expect that ~5000 electrons per mm will arrive at the anode. The electron trapping becomes negligible when the electron lifetime is much longer than the drift time. The long electron lifetime of >3 ms, that was demonstrated in the past [8, 22], will satisfy this requirement.

Our simulations suggest that a 4-mm pixel size or pixel density of 25k/m2 will satisfy the requirements to track reconstruction accuracy. This number is also reasonable from the point of view of electron diffusion, which inevitably diminishes the advantages of using the finer spacing. Therefore, assuming 4x4 mm size we expect ~20,000 electrons per pixel from the minimum-ionizing muons at the 500 V/cm drift field. At the total electronic noise of 500 electron equivalent noise charge (ENC), this corresponds to a 30:1 signal-to-noise ratio (SNR) for minimum-ionizing muon signals.

The requirements for the power consumption per electronics channel can be estimated based on the heat flow through the detector cryostat walls, generally on the order of 10 W/m2. The ratio of the total area of the anodes to the total area of the inner walls is ***. Setting the power density of the readout under ** W/m2, which corresponds to *** µW per channel, we attain the total heat load from the readout electronics less than the heat flux through the cryostat walls.

The anode board with ASICs must be carefully designed to avoid the localized boiling of liquid argon that may cause electrical discharges and noise signals. Suppressing potential bubbling must be considered when designing the anode boards. An effective way to prevent the local bubbling is to ensure efficient heat transfer from the ASIC chips to the anode board, which could be enhanced by using diamond substrates as heat conductors???.

Further reductions in the heat generated by the readout can be achieved by designing electronics which remains inactive most of the time, taking little power and becoming active only when a signal occurs. This idea found its use in several recently proposed readout concepts (and corresponding ASIC architectures) which allow for substantial reductions of power and transfer data. For the FLARE TPC baseline design, we consider two approaches summarized below.

1.1. LArPix readout scheme

The approach is implemented in a cryogenic temperature operating LArPix ASIC developed for the DUNE Near Detector. Its operation principle is similar to a conventional charge-sensitive amplifier with an external reset. Each ASIC channel operates as an independent self-triggering charge integrator followed by a digitizer and multiplexed readout. The signal digitization and readout only occur when its amplitude exceeds a configurable threshold, resulting in a drastic reduction of the power consumed by the digitizer and data I/O system. A block diagram of the LArPix ASIC is shown in Fig 1. The main characteristics of the amplifier are a rise time of 45 ns, a gain of 25 mV/fC, and a dynamic range of 1.2 V (equivalent to 3×10^5 electrons).

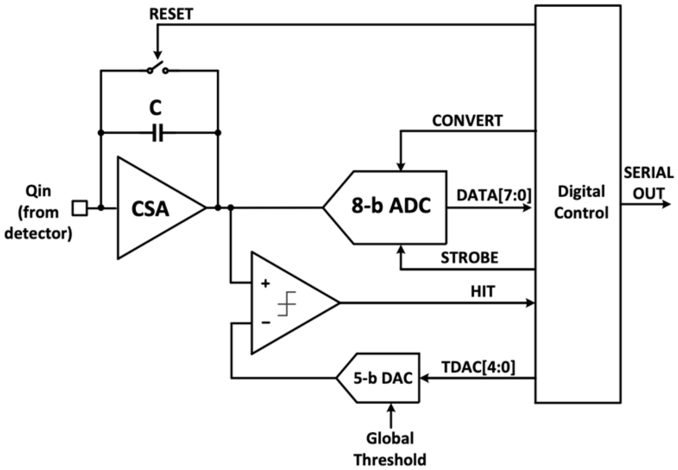


Figure 1. Block diagram of the LArPix ASIC [1].

When the rising front of the input signal crosses a threshold a trigger from the discriminator initiates digitization after the controllable delay to capture the amplitude of the fully collected signal. After conversion, the digital control resets the CSA and after a short delay, the channel is ready for the next signal [1]. The FIFO buffer on each ASIC holds up to 2048 digital records awaiting transmission out on a single data wire using a serial UART-like protocol at a rate of one bit per system clock cycle (e.g. 5 Mb/s with a 5 MHz system clock). The data I/O configured into a daisy-chain, enables communication and controls up to 256 ASICs (8192 channels) via a single pair of wires. This allows for the extremely large number of readout channels while relying on small number of data I/O cryostat penetrations and simplify the cryostat design. The LArPix ASIC electronic noise is 500 e ENC at ~5 pF pixel capacitance, the is 2048 event memory depth (~5 ms) and the power consumption is <100 µW per channel. The full ASIC specifications can be found in Ref. [1].

1.2. Q-Pix readout scheme

This readout approach is currently under development by the Q-Pix consortium for large-scale detectors [8-10]. Like in a previous approach, a charge-sensitive amplifier integrates charge on the feedback capacitor until it reaches the preset threshold. The Schmitt trigger turns on the MOSFET switch that quickly discharges the capacitor and resets the Q-Pix readout to its initial state while the times at which the resets occur are recorded using a local clock (Fig.2(a)). Q-Pix captures signal waveforms by measuring time per unit charge rather than using the classic waveform amplitudes sampling method. Mathematically it means that Q-Pix captures an inverse dependence of the continuously rising change vs. time. If such, it cannot follow the signal when it changes a sign of its first derivative, i.e., a direction of the current.

However, this scheme results in the charge loss accumulating during the reset times. This problem can be solved by the charge replenishment scheme illustrated in Fig. 2 (b). When the feedback capacitor reaches the threshold voltage, the MOSFET replenishes a charge of ΔQ=I·Δt, where Δt is the pulse width using a current that flows opposite to the input current. Thus the ΔQ becomes a charge quantum of each measurement at the time when the replenishment is recorded using a local clock.

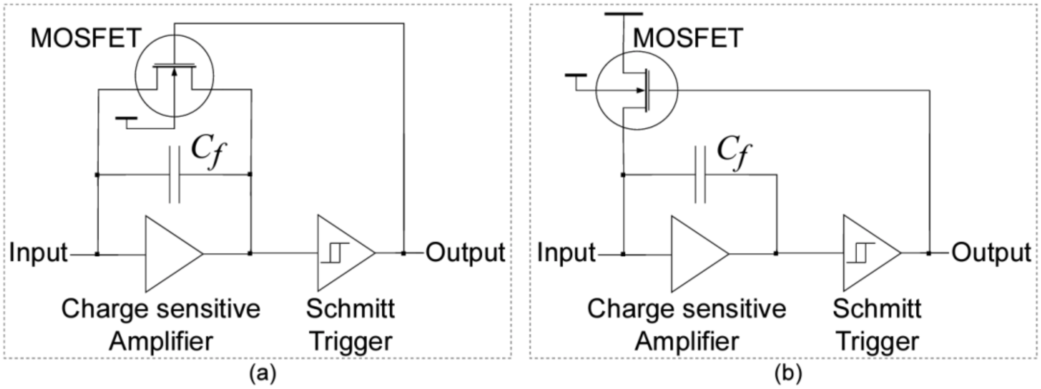


Fig. 2. Q-Pix reset (a) and replenishment (b) schemes [10].

The clear advantages of the replenishment scheme are eliminating charge loss, allowing for tunable reset pulse widths, and reducing noise at lower frequencies similar to a first-order Sigma-Delta modulator. It is believed that Q-Pix can achieve better sampling resolution and waveform reconstruction.

We note that a similar readout approach was implemented in the Mixed-Mode Pixel Array Detector (MMPAD) readout ASIC for high-speed, high-dynamic range imaging [11,12]. The difference is that at the end of the integration period, MMPAD ASIC also reads the residual analog voltage as shown in Fig. 3. This feature allows for higher sensitivity to small input signals.

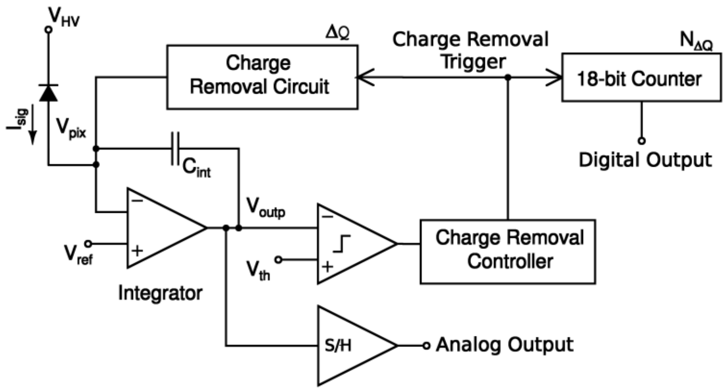
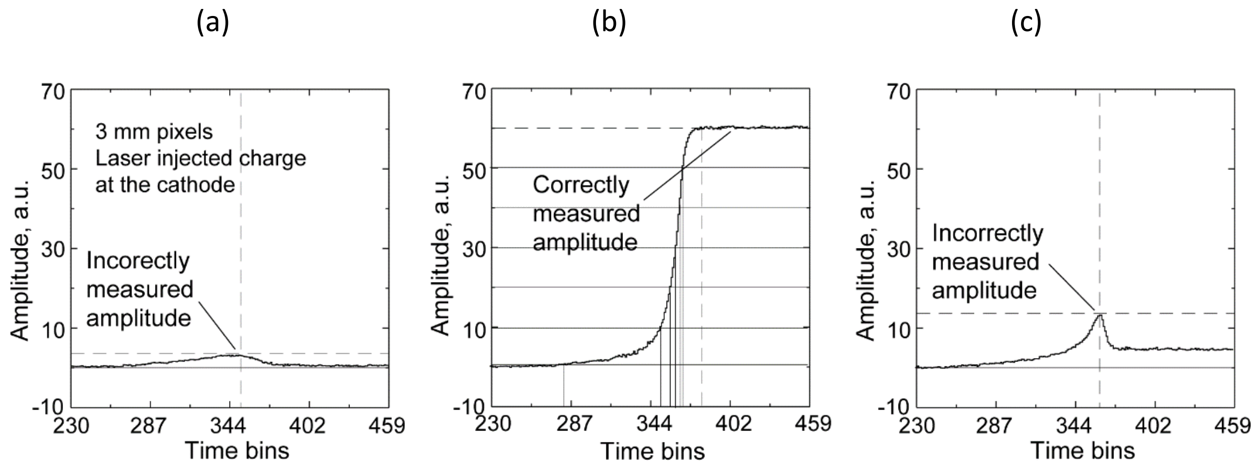


Figure 3. Schematic of MMPAD ASIC. The remaining amplitudes of the output signals are read out at the frame end [12].

Fig. 4 illustrates a basic idea of the Q-Pix approach using examples of the charge signals generated in a 20-mm drift distance CdZnTe detector on three adjacent 3-mm pixels. Fig. 4(b) shows a collected charge signal with vertical lines representing measured clocks corresponding to the incremental changes of the signal. The signal amplitude corresponding to the last clock represents the total collected charge.



Figs (a) and (c) show the signals captured from the adjacent pixels, which have strong induced charge components. In both signals, the maxima of the signals will be incorrectly recorded by Q-Pix as total collected charges. In reality, no charge is collected at the left pixel, and a small charge is collected at the right pixel. Such incorrectly measured charge amplitudes can be identified using timing information. The induced signals reach their maxima well before the true collected charge signals. The peaking times and measured amplitudes are marked with dashed vertical and horizontal lines.

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