PDSU-CLIQ/DQHDS interlocking via BIS concentrator

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On behalf of the TE-MPE and WP7

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Inner Triplet circuit protection

- Magnet Protection
  - Heater Discharge Power Supply (HDS) units – in total 48
  - Coupled Losses Induced Quench (CLIQ) units – in total 6
- Quench Detection Systems (QDS)
  - Individual QDS systems for Q1, Q2 and Q3 – in total 3+3
  - QDS system for superconducting link (SC link) – in total 1+1
  - QDS system for bus-bar protection – in total 1+1
- Protection Devices Supervision Unit (PDSU)
  - HDS and CLIQ supervision and trigger distribution
  - Ensure the machine protection
  - PDSU systems for Q1, Q2 and Q3 – in total 3+3
- Powering Interlock Controller (PIC)

The new protection device

The UQDS development framework and EDAQ supervision

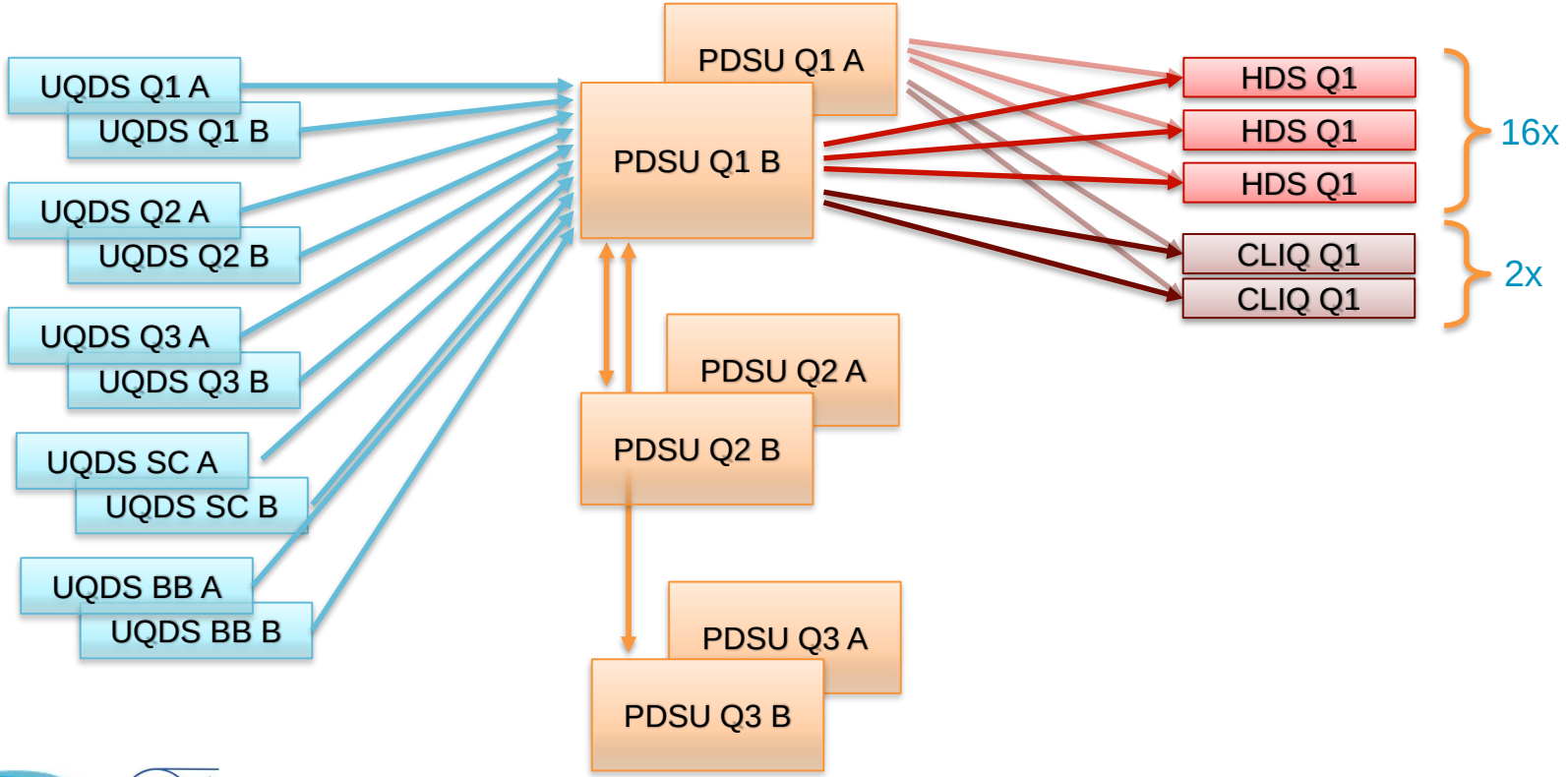
Key objectives for PDSU

- Activate DQHDS and CLIQ devices
  - Coupling between detection (UQDS) and protection (DQHDS and CLIQ) devices
- Interlock spurious triggers of protection devices
  - Triggers the remaining protection of the circuit
  - Triggers power abort
  - Triggers beam abort via dedicated connection to Beam Interlock System (BIS)
- Complement UQDS data for the detailed analysis of the events
  - Voltage and current monitoring of DQHDS and CLIQ
  - Complementary monitoring of triggering signals and statuses
- Provide powering interlocks and health monitoring
  - Provides QPS OK signal for the protection equipment
  - Slow power aborts in case of unavailability of the protection equipment
  - Monitoring of trigger, status and health signals

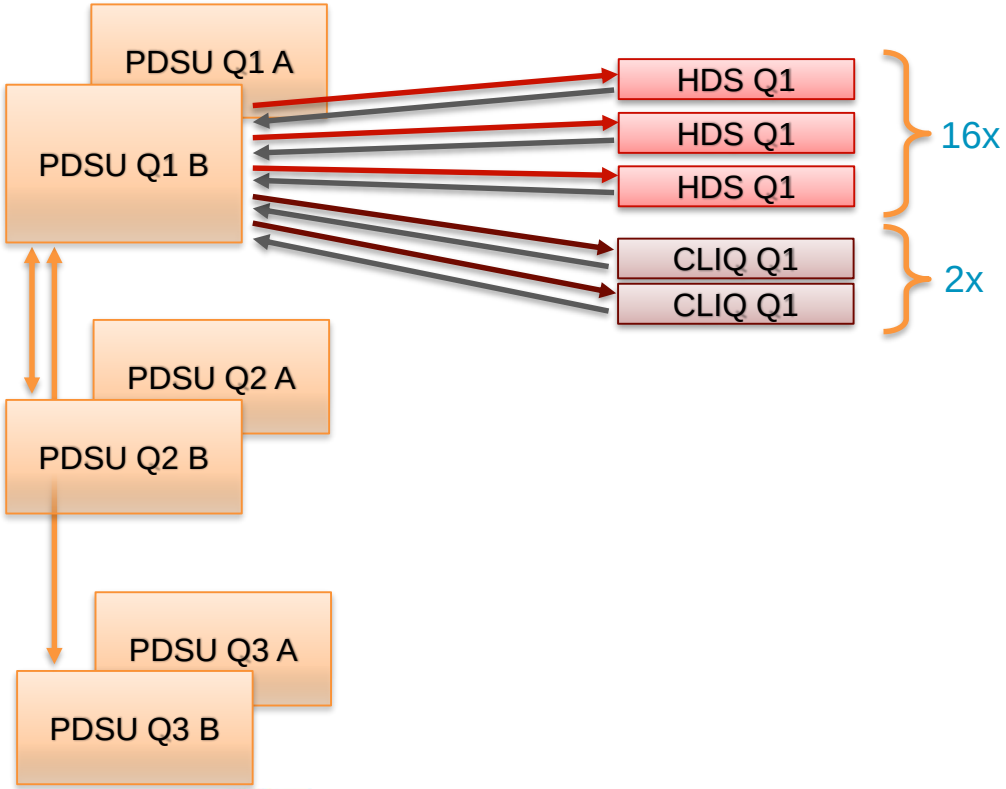
Interlocks and triggers of PDSU

- Two categories of trigger sources
  - External sources
    - UQDS
    - PDSU
  - Internal sources
    - Evaluation of current signals of HDS units
    - Evaluation of current signals of CLIQ units
- Powering and beam interlocking
  - Interface to PIC
  - Interface to BIS
  - Interface to LHC supervision for Software Interlocks

External trigger sources

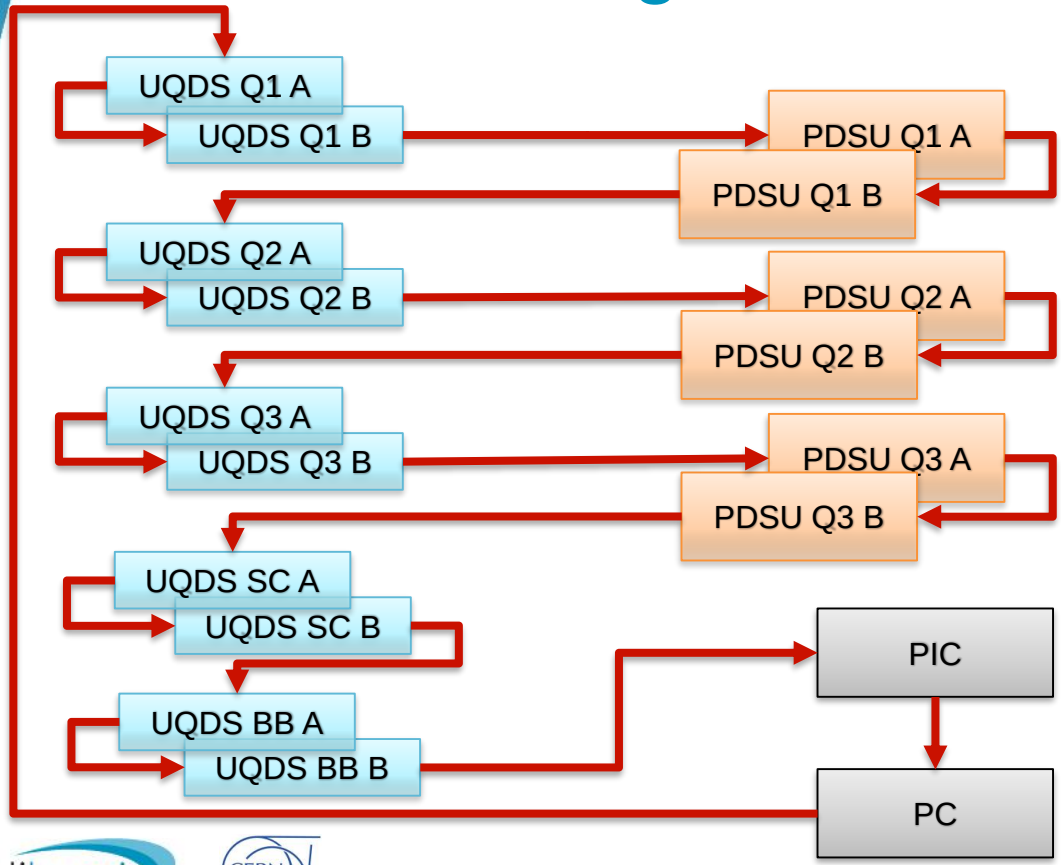


Internal trigger sources



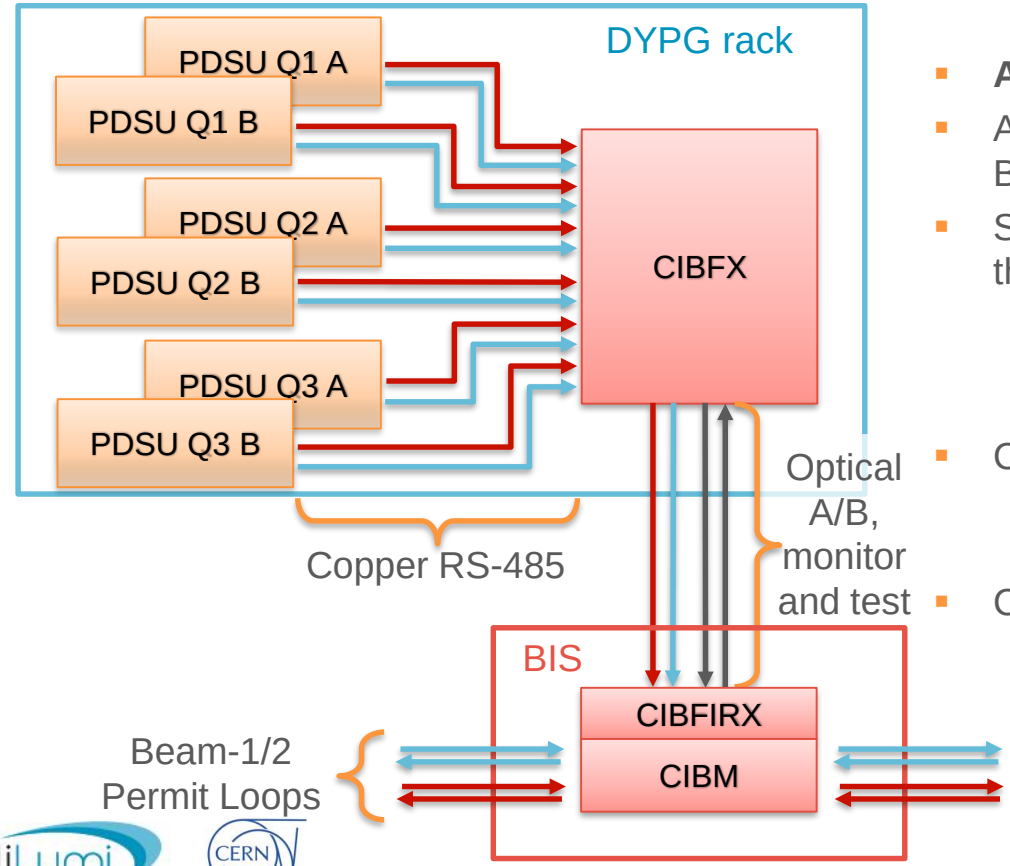
- HDS current and voltage
  - Monitored with 16 bit at 192 kHz
  - Current readout from the HDS current transformer
- CLIQ current and voltage
  - Monitored with 20 bit at 400 kHz
  - Current readout from the current transformer and dI/dt sensor
- Active triggering on the current
  - Variable threshold
  - Digital filtering
- Voltage signals used for QPS OK
- **PDSU re-triggers all protection units if a spurious trigger of HDS or CLIQ is detected**

Interlocking of the circuit powering



- Current loop interlock
  - Source is the Power Converter (PC)
- Powering Interlock Controller (PIC)
  - Interlocks powering process
  - Interfaces to the Beam Interlock System (BIS)
- **PDSU is an active device**
  - Requests Fast Power Aborts (FPA)
  - Interfaces via a PhotoMOS

Interlocking of the beam



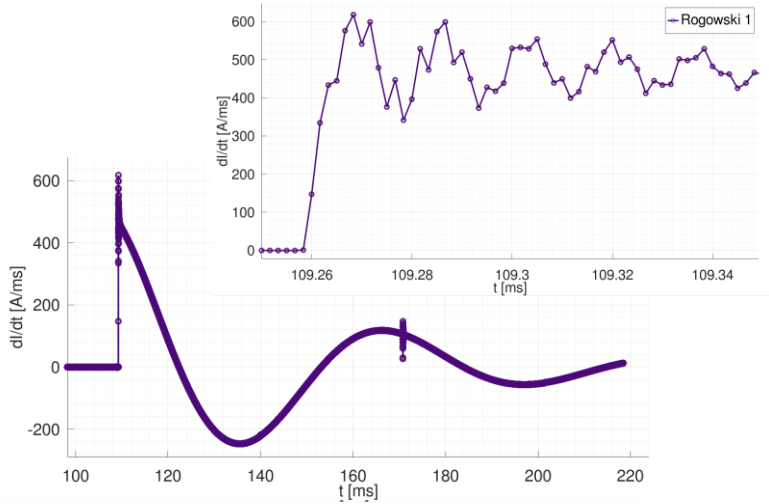
- **A new machine protection requirement**
- A direct path to the BIS CIBM via the new BIS concentrator
- Standard BIS signaling between PDSU and the BIS concentrator (CIBFX)
  - Fail-safe RS-485 receivers with the fault detection
  - Fail-safe beam permit encoding
- CIBFX/CIBFIRX provide direct path to CIBM
  - Redundant channels for A/B inputs
  - Embedded monitoring and test modes
- CIBFIRX installed in the BIS crate
  - Connects to CIBM via RS-485 interface
  - Removes beam permit if the respective optical user permit link is not available

The new machine protection requirement

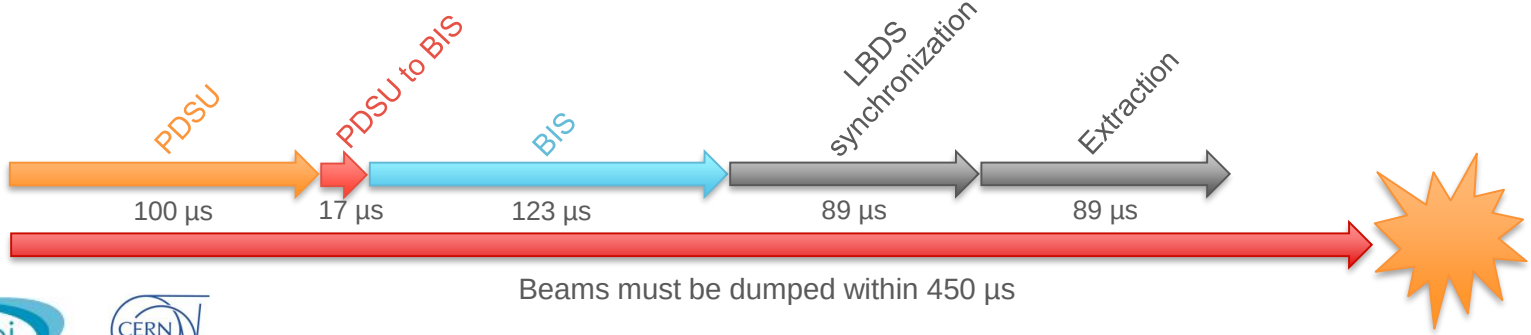
- A spurious triggering of either an HDS or a CLIQ device can lead to fast critical beam losses (> 1MJ) in the HL-LHC collimation system
  - Spurious CLIQ trigger in worst scenarios requires only 5 turns (450 µs)
  - Spurious HDS trigger, in the most critical case of D1, requires 40 turns (3,6 ms)
    - BLM reaction time has a solid margin (3-4 times earlier)
  - **Spurious CLIQ trigger is the most critical fast failure case identified for HL-LHC**
- **Timely requested beam abort is crucial**
  - Not possible through the standard connection (QPS-PIC-BIS)
  - All protection devices require supervision
- Cedric Hernalsteens has more on this topic:
  - “Update on failure case studies”, 10th of October at 11:35
  - “Recap. Of failure cases for round and flat optics”, 8th of October at 17:20

Latency budget for interlocks

- Detection of spurious CLIQ trigger = **100 µs**
  - Detection of spurious HDS trigger < 100 µs
- CIBFX to the BIS beam permit = **17 µs**
  - Max latency under normal conditions = 12 µs
- BIS latency between P1 and P6 = **123 µs**
  - The longest path from R1 to R6
- Beam abort sequence = **178 µs**
- Total time = **418 µs** < 450 µs
  - The target time to dump for round optics



Current transformer signals during the CLIQ discharge



System design

- **PDSU**
  - Based on the proven UQDS ecosystem to develop machine protection systems
  - Hardware to monitor HDS and CLIQ devices
  - Hardware interfacing to PIC and BIS
  - Ethernet-enabled data acquisition (EDAQ) enables high-definition data for event analysis and configuration management
- **BIS Concentrator (CIBFX/CIBFIRX)**
  - Standard BIS components for the beam interlock concentration for the accelerator complex
  - The well-establish BIS technology to transmit beam permit with safe encoding
  - Embedded supervision and isolated testing of the BIS concentrator
- Lukas Felsberger has details on the reliability
  - “Reliability studies on UQDS, PDSU and PDSU-BIS concentrator interface”, 10th of October at 9:50

CIBFX rear (top) / front (bottom)

CIBFIRX

Summary

- PDSU systems are crucial to address all protection schemes associated with the Inner Triplet circuit
  - Aggregation and distribution of triggers
  - Powering interlocking
  - Beam interlocking
- Beam interlocking is the new machine protection requirement within QPS
  - Close integration within QPS and BIS systems is necessary
  - Tight latency budget for the entire connection
- PDSU to BIS via CIBFX/CIBIFRX connection allows to fulfill requirements
  - Straightforward integration within BIS system
  - Maintained isolation between the systems
  - Complete supervision and full test coverage

Thank you!

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