HL-LHC BLM system development status update

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14th HL-LHC Collaboration Meeting, Genoa, Italy, 7-10 Oct. 2024

Outline

- Integration Study & Deployment Plan
- Status update on progress
  - Electronics Development
  - Component Procurement
  - Controls Integration
- Conclusions

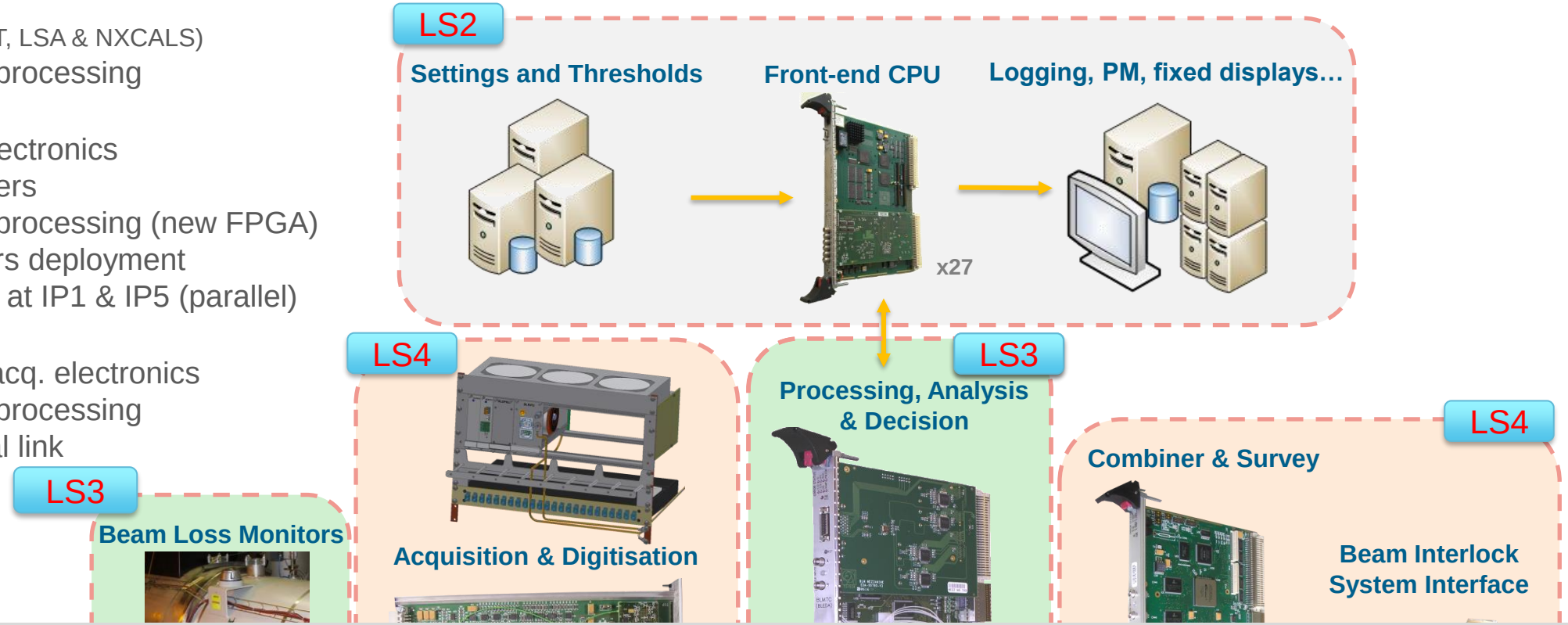
LHC Beam Loss Monitoring System – Upgrades

Funding through R2E, CONS & HL-LHC projects

LS2:
- New FESA & OS
- Databases (LAYOUT, LSA & NXCALS)
- Firmware for data processing

LS3:
- New processing electronics
- New optical receivers
- Firmware for data processing (new FPGA)
- Additional Detectors deployment
- Prototype systems at IP1 & IP5 (parallel)

LS4:
- New mini-crate & acq. electronics
- Firmware for data processing
- Bidirectional optical link



- Progressive Upgrade Plan
  - Additional complexity to ensure backwards compatibility of any change
  - Necessary to avoid degradation of functionality & blind faults

around the LHC ring

grouped in 8 points

Integration study & Deployment plan

HL-LHC BLM Deployment Plan

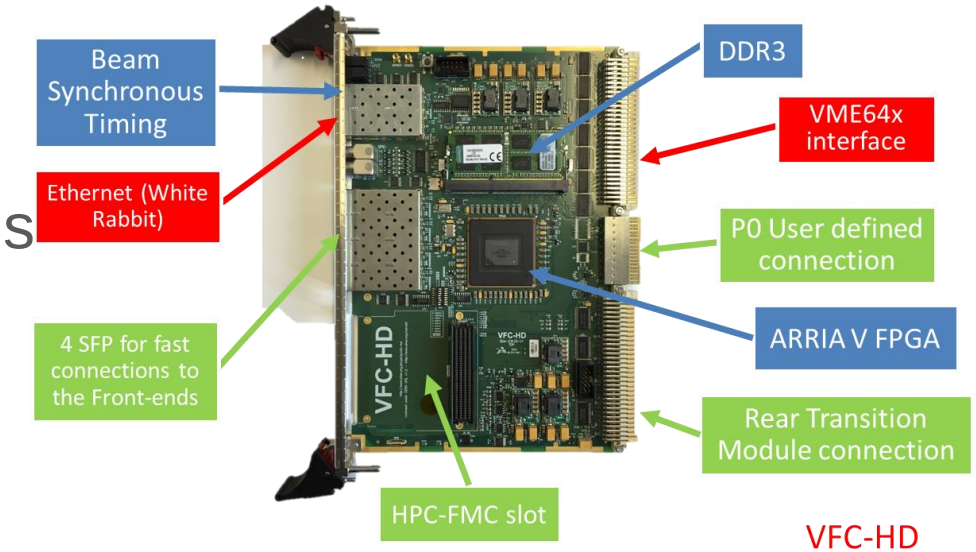
- LS3
  - Extension of the current BLM system with additional detectors following HL changes
    - e.g. IP1 & IP5 Triplet, Collimation, BBLR, etc. areas
  - First deployment of the full new electronic stack at strategic locations in parallel to the current electronics
    - to complete and validate development
- LS4
  - Full deployment of new electronics
    - replacement of the complete tunnel electronics stack (mini-racks, crates, power supplies etc.).

HL-LHC BLM changes during LS3 – Tunnel Installation

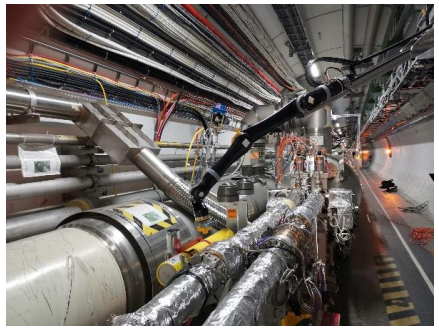
- New HL Triplet Layout at LSS1 & LSS5 (up to cell 6)
  - Complete removal of current installation
  - New 354 detectors with supports and cabling
  - 80 distribution boxes (signal & power)
  - 4 additional crates to host the electronics for the additional channels
  - 12 miniracks hosting the prototype HL BLM acq. System
- Progress
  - Integration (almost) completed for the majority
  - Cable lists completed (todo one more iteration for optimisation)
  - All material available or in production
  - Additional personnel requested through the BLM LHC-CONS EDMS#2782477
  - Planning needs update

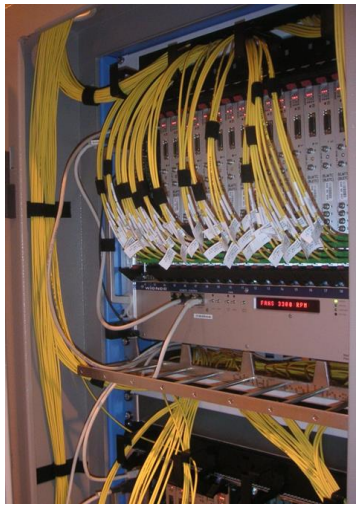
HL-LHC BLM changes during LS3 – Surface Installation

- Processing system upgrade
  - 400 new electronics boards (VFC-HD),
  - 2000 new optical fibre transceivers & patchcords
  - 16 Thermalised racks upgrade & maintenance
- New HL triplet layout (up to cell 6)
  - 2 new processing crates for the prototype
- System Verification
  - Re-validation of the complete BLM system in collaboration with the TIM robot (BE-CEM-MRO)



VFC-HD

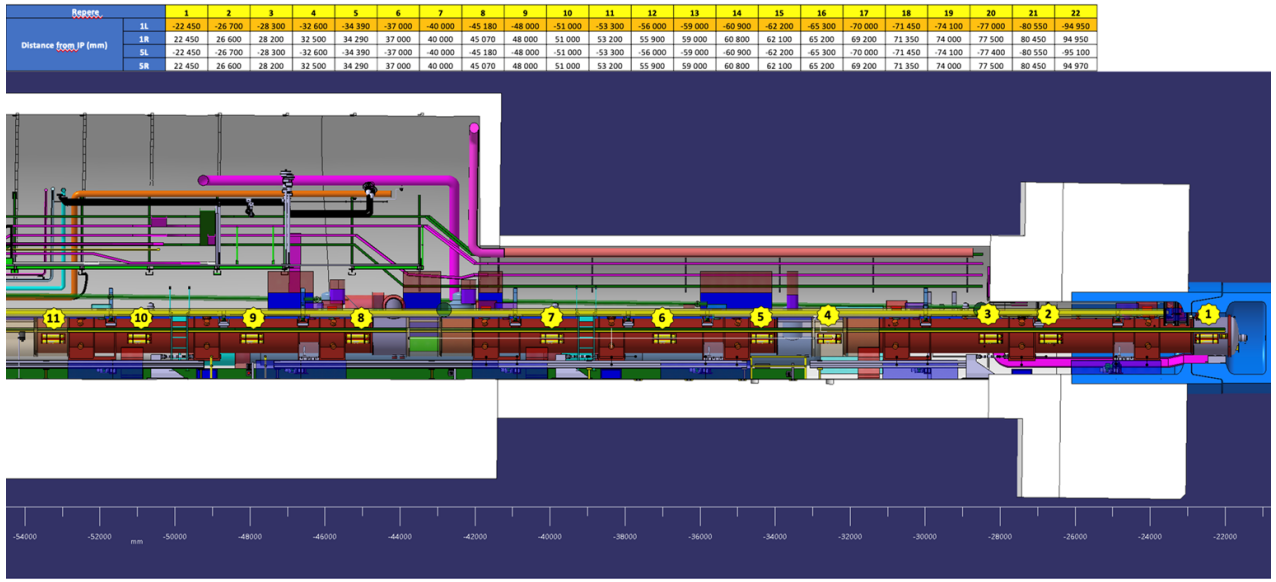



Processing Electronics

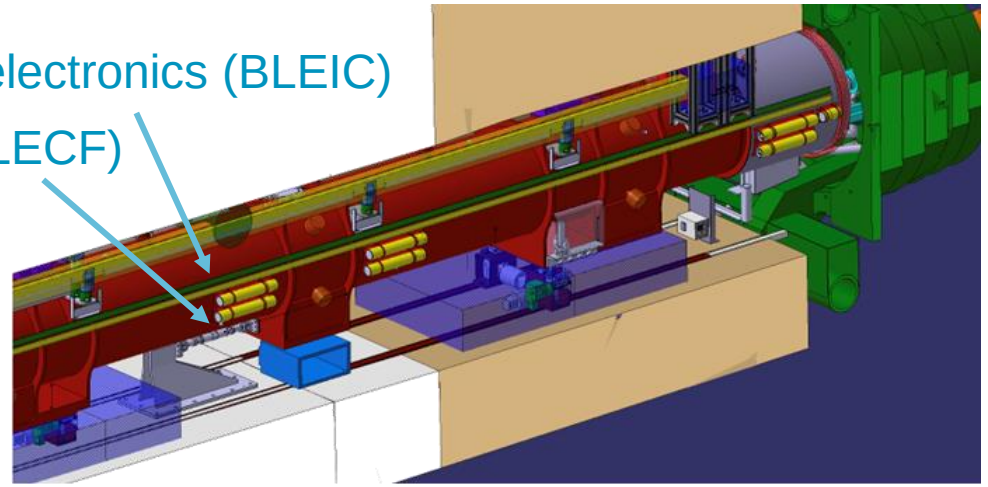
BLM Detectors at HL Triplet Layout

During LS3 will **extend the current system** for the new topology and deploy the **new system (BLEIC) in parallel**
Will allow validation for full deployment during LS4 and (some) redundancy in this critical area long-term.

Future access & maintenance tasks were taken into account
-> All detectors are placed at internal/passage side



See also presentation at 200th HL-LHC TCC by Sara & Belen
https://indico.cern.ch/event/1449142/

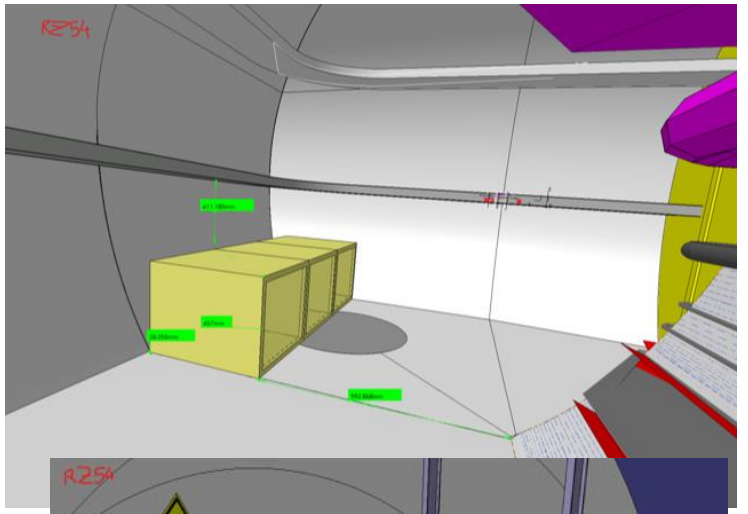


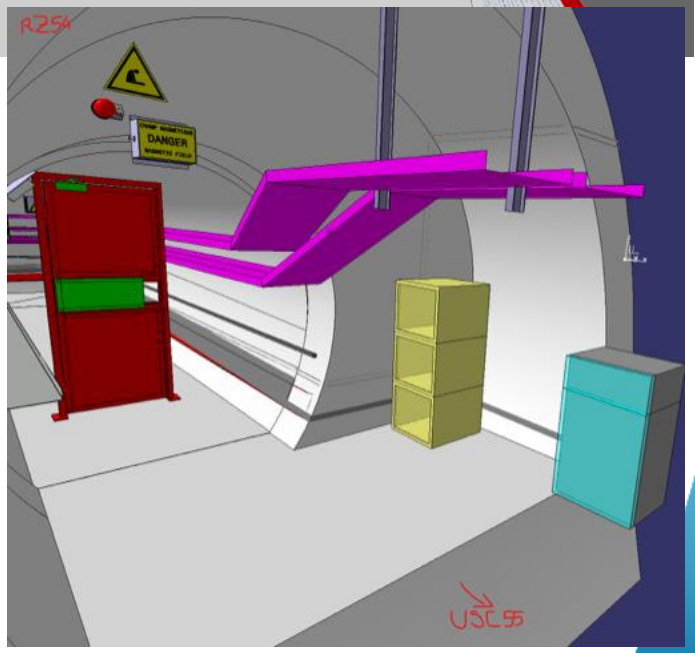
Configuration at HL-LHC triplet area

Number of detectors: Total for LSS1 & LSS5 (up to Q6)			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF (standard)	224	**270**	56
BLEIC (new)	0	**84**	84
Total IP1+IP5	**224**	**354**	**130**

New BLM Electronics at LSS1 & LSS5

- LSS1: 6x crates
  - Proposed locations in UJ14 and UJ16 but from the service side, i.e. on the UL14 and UL16 side
- LSS5: 6x crates
  - IP5R: Proposed location UJ56
  - IP5L: Proposed location in the ‘chicane’ at RZ54
- These should be accessible when the tunnel is closed
- Signal & HV distribution boxes also proposed in accessible locations, attached on the overhead cabletrays
- Cable lists have been updated with new schemas
  - Rad-hard cables requested for the tunnel side
  - Solution agreed with EN-EL (G. Girardot) to avoid cabletrays for the patchcords along the magnets.





Constrains: Resources Sharing

- BLM Intervention team(s) for all activities is shared across machines:
  - New system in SPS ring & transfer lines
  - New installation of NA-CONS/ECN3 BLM equipment
  - HL-LHC activities in the new triplet areas
  - LHC: removal and re-installation of BLMs for BST, Vacuum, Diodes, MKI, etc
  - PS and PSB: some removals for Vacuum and Magnets consolidation
- Schedule definition is still in progress
  - Interdependencies with other machine schedules
- Ex: LHC tasks involving many more group dependencies (TE/MSC, TE/VSC, TE/CRG, TE/MPE, etc) and being part of critical schedule paths will have bigger priority.
  - SPS BLM renovation tasks will need to be scheduled on available slots between LHC interventions and access restrictions

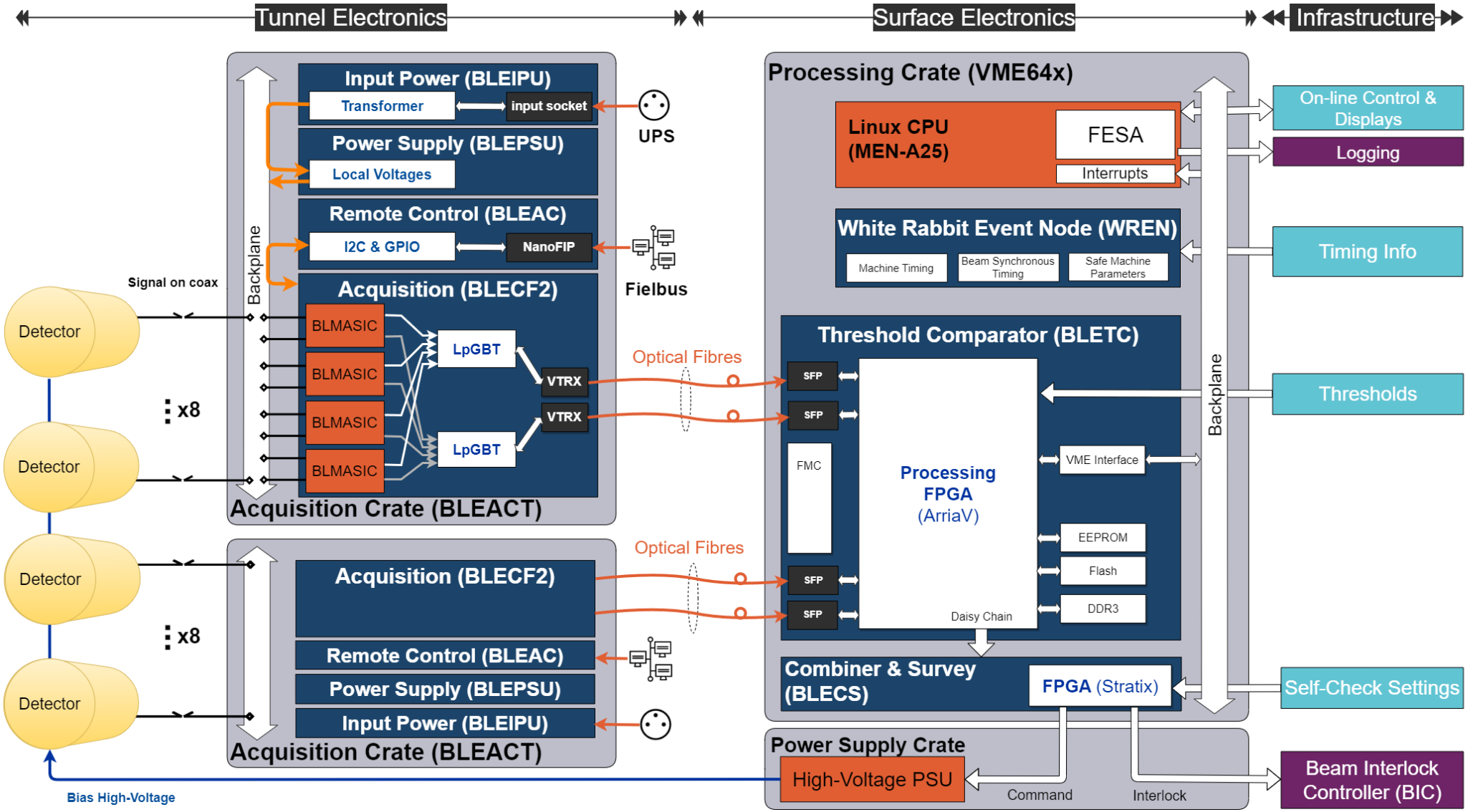
Development progress

HL-LHC BLM Development Plan

Development required for new:

- Rad-Tol card (BLEIC) to allow reduced cable lengths and improve S/N ratio
  - Hybrid COTS & ASIC version would be challenging and limited to < 1 kGy (study made; will keep as backup plan)
  - Rad-hard Application Specific Integrated Circuit (ASIC) under development to encapsulate all the analog-to-digital conversion.
- Crate and power supplies to host acquisition electronics
  - 3 variants required
  - ARC installations shared w/ BPM; LSS separate BPM & BLM installations
- Communication layer between tunnel and surface electronics
  - Multi-gigabit rad-tol bidirectional link
- Integration to the surface electronics
  - Processing and decision firmware
  - Control and supervision firmware

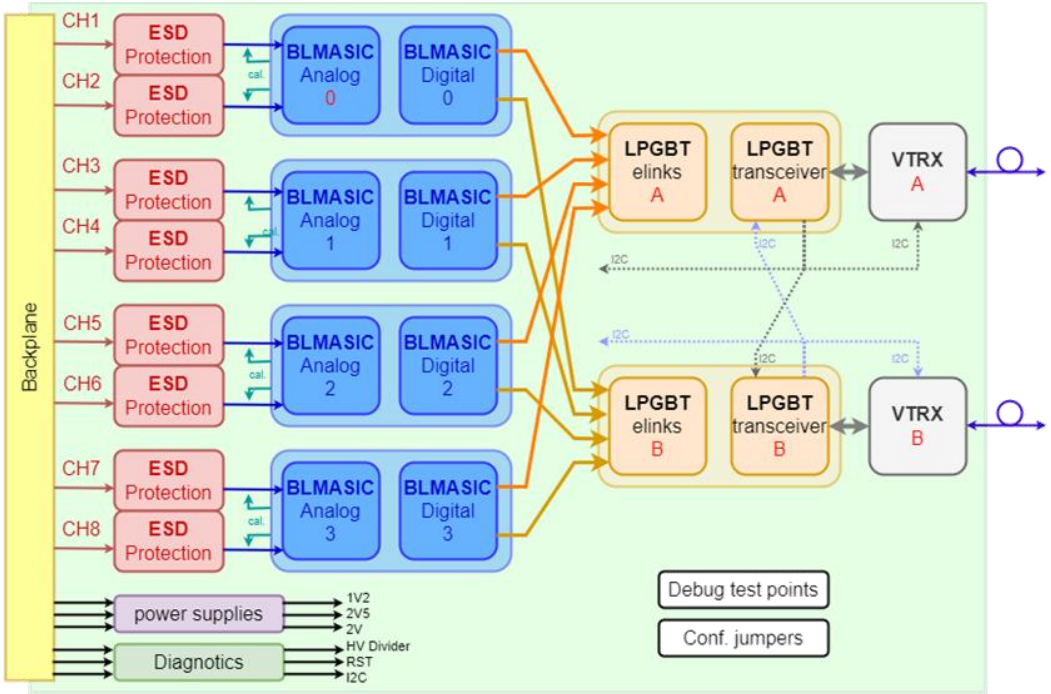
BLM System Architecture using the BLMASIC



BLEIC Data Acquisition Board

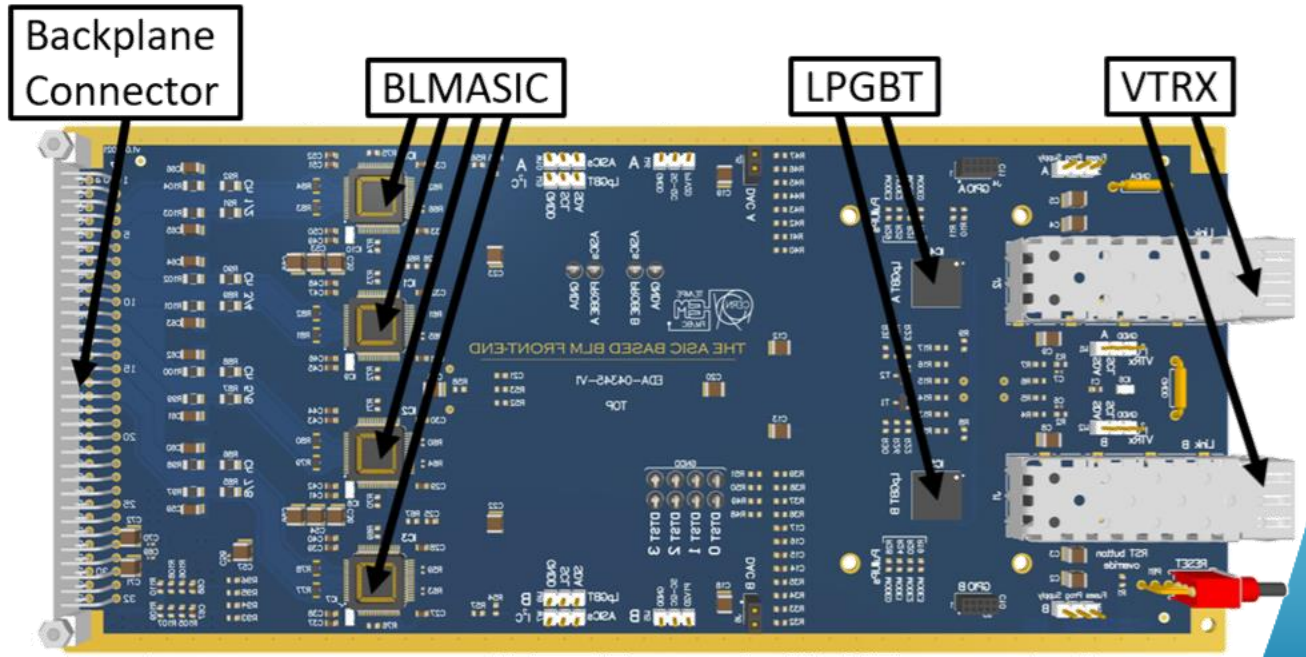
BLEIC v1 (EDA-04345-V1-0):

- 6 pieces produced
- Used in laboratory and for radiation testing
- Two installed in SPS in BA2 and BA5 for validation under beam conditions



BLEIC v2 design on-going:

- Add 2x GBT-SCA for better diagnostics
- Remove the debug jumpers and test points,
- Correct the auto-reset circuit
- I2C buses: merge, move to backplane, add a level translator to 1V2
- Add front panel features



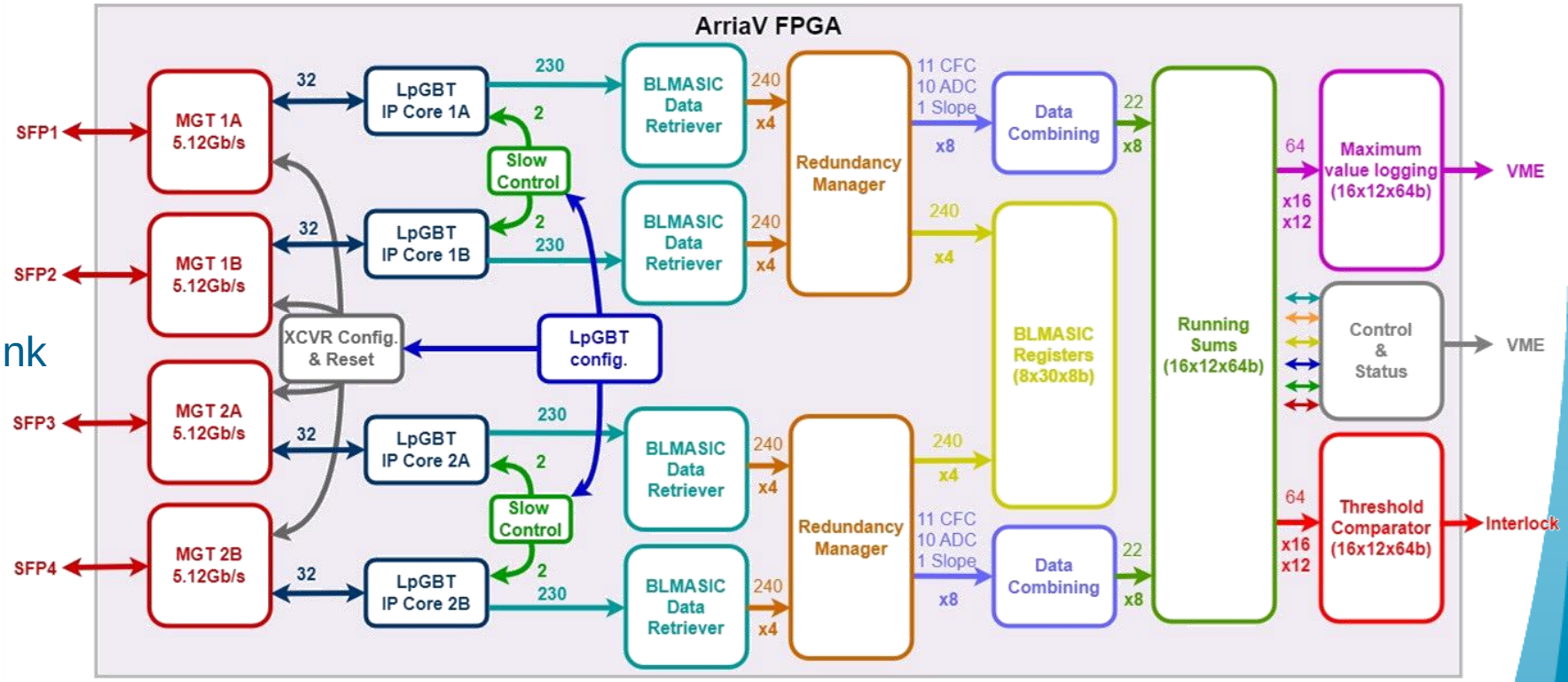
VFC-HD Data Processing

Implemented Features:

- BLEIC configure through fibre
- 12 running sums
- Max value logging
- Processing 16 channels
- 4 Rx/Tx Transceivers
- Full HW configuration - No software needed
- >100 diagnostic registers per link
- EDGE 3.1 driver
- Raw data over UDP

Remaining tasks:

- Threshold/settings in memory
- Threshold comparator
- Interlock interface
- Post-Mortem and Capture buffers (DDR3)

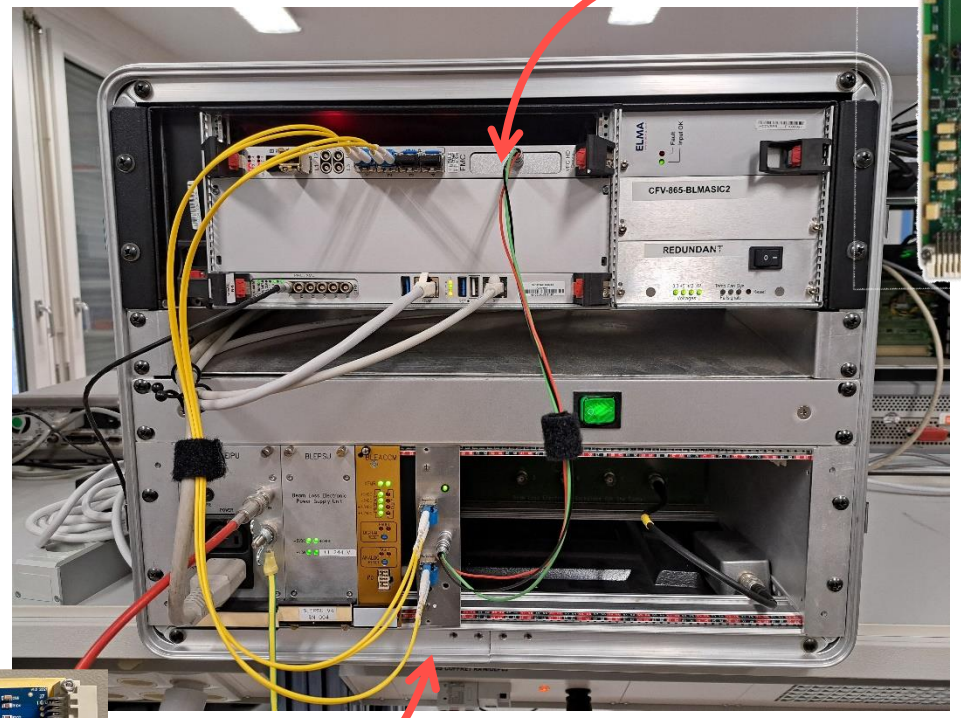


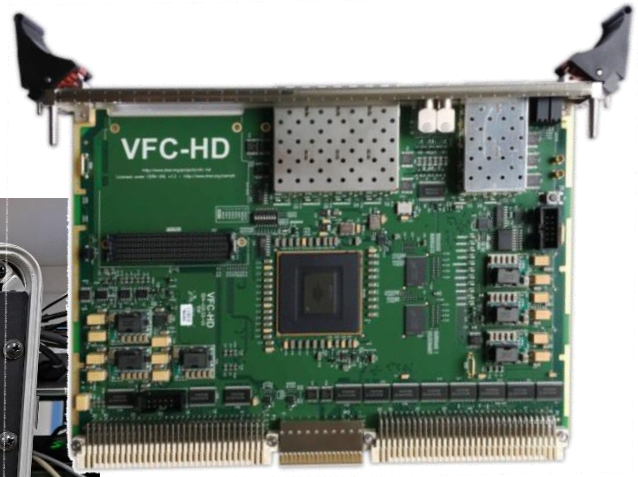
Controls Development

Verification of Functionalities in the TestBench

Back-end Firmware for

- Boot, setup and control over fibre link of the BLEIC
- Reception & decoding of the measurement packets
- On-demand self-diagnostic data
- Real-time processing & onboard high frequency data recording



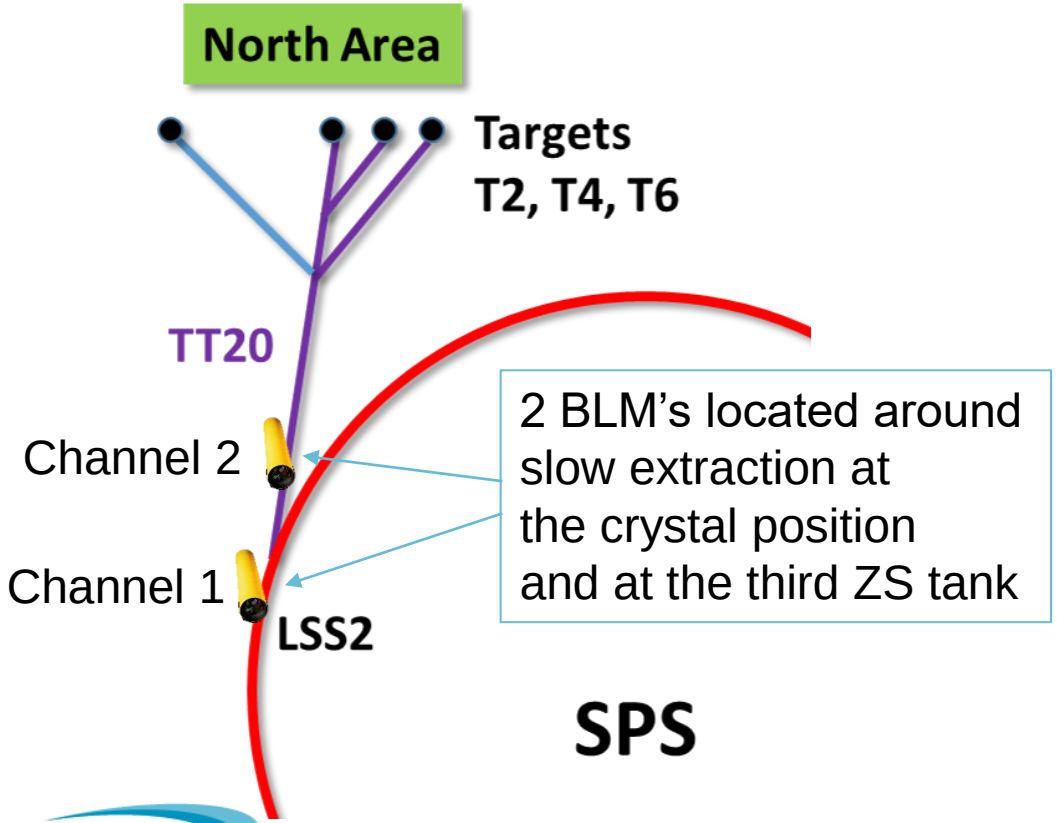


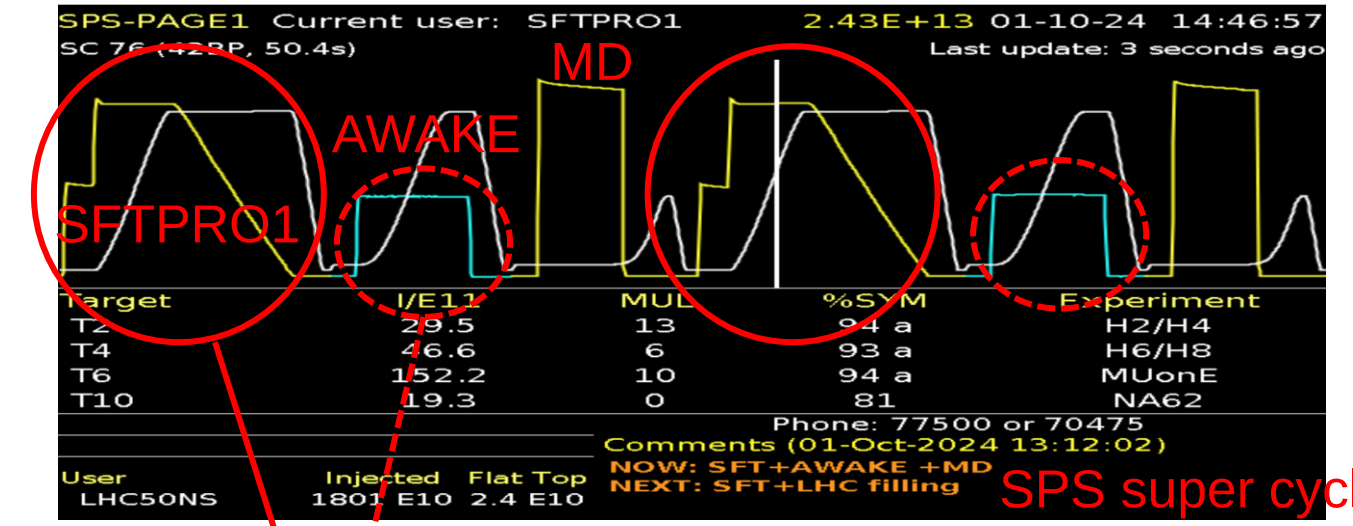
Front-end electronics for

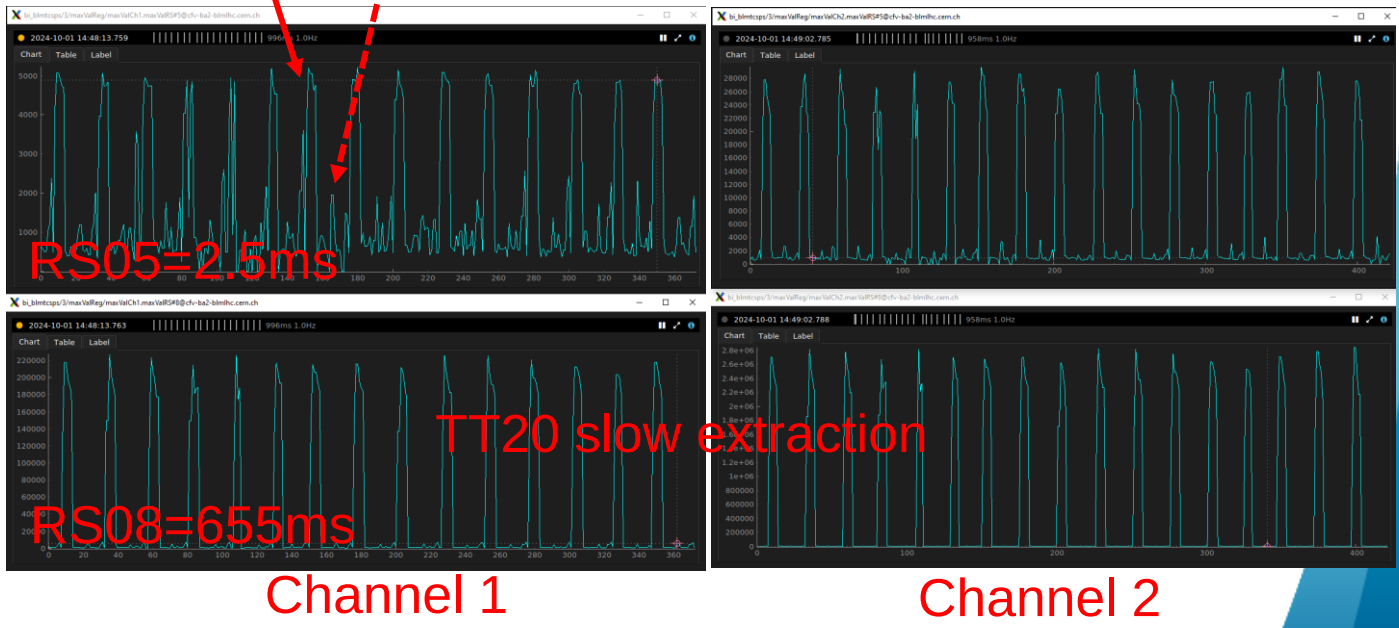
- Integration of all modules
- Validate power distribution, ramp and power cycle
- Collection of diagnostic data
- Programming & Control of all devices

Verification of Functionalities under Beam Conditions

- Validation of functionalities with beam is on-going

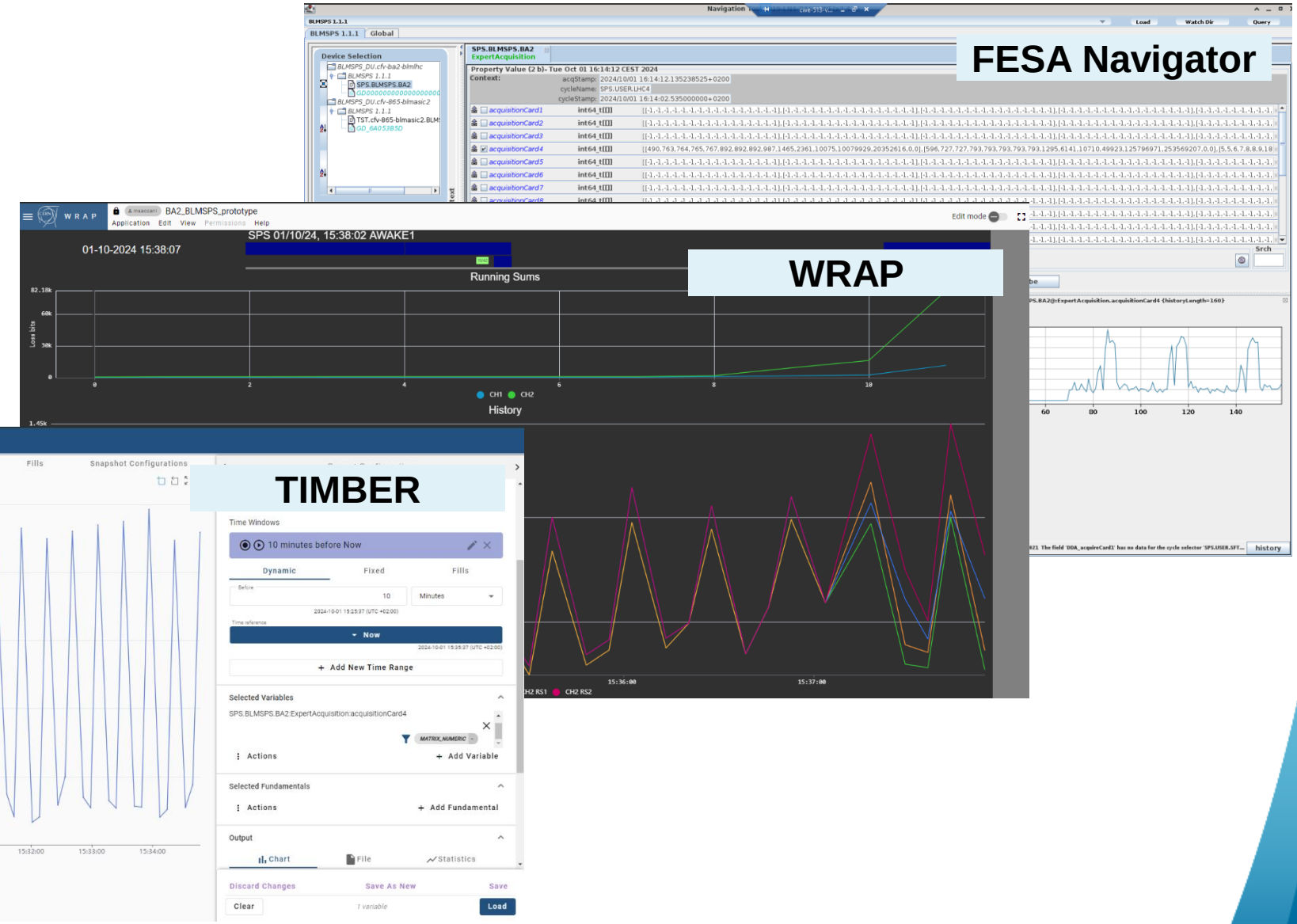






Software Development Tools

- FESA
  - Navigator & NavPy
- Expert diagnostic tools
  - pyQt & WRAP
- Data storage in NXCALS
  - TIMBER & Scripts

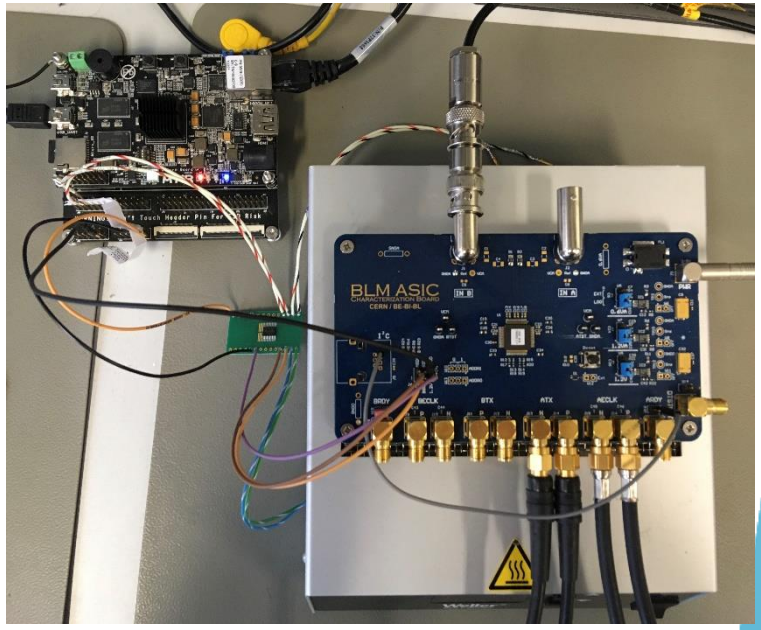


Procurement Progress

BLM ASIC R&D Timeline

Prototype development timeline:

- 2018 Q1: project start; technology selection and feasibility
  - Parallel design of two methods:
    - CFC asynchronous better suited to handle large currents and quickly varying signals
    - Delta-Sigma ideal for high accuracy due to oversampling and filtering
- 2019 Q4: V1 delivery
  - Issue with internal power distribution and ESD protection
  - Could not test full range
- 2020 Q4: V2 delivery (some delays due to COVID)
  - Mostly functional;
  - Metastability issues with the sync between the analogue and digital domains
  - High current leakage of the input stage FETs; poor low current meas.
  - Decision to continue with the CFC asynchronous method only
- 2022 Q1: V3 delivery
  - Analogue & digital circuits fulfil needs; all currently known issues resolved
  - New minor issue w/ sync between CFC & ADC data; mitigation possible at the backend
- **2024 Q1: Internal Review of achievement (EP-ESE & SY-BI)**
  - https://indico.cern.ch/event/1388673/
  - Further improvement with the current technology (130 nm) not possible
  - Few additional checks requested to complete validation
  - Proposal to go ahead with the production

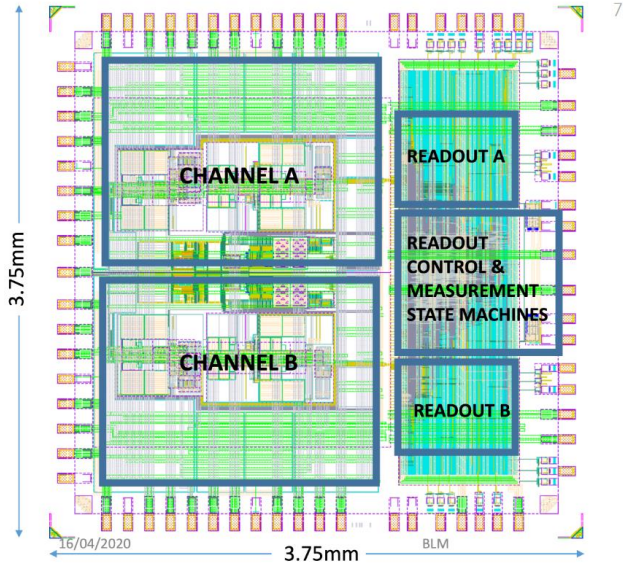


Development of custom ASIC verification testbench

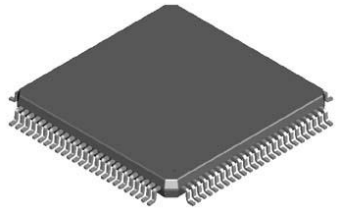
BLM ASIC Production Timeline

Production timeline:

- **2024 July: project submitted to the TSMC foundry**
  - After some negotiations, TSMC accepted to use the MPW process for the full production
  - 12 additional wafers requested, which should provide ~5200 chips
- **2024 Oct.: Dicing and packaging**
  - New contract with IMEC
  - Packaging to be done by their US subcontractor
  - Will package 500 chips, enough for all needs up to LS4
- **2024 Dec.: Expected delivery**



BLM ASIC block diagram



Standard 64-pin Quad Flat Package (10x10 mm)

Electronic Designs Progress Summary

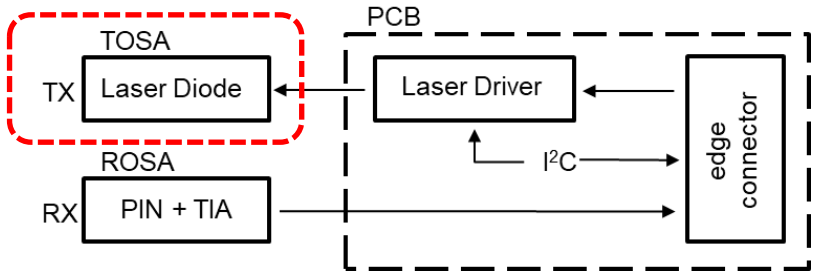
- All designs completed and tested electrically and under radiation
  - **Radiation Hardness Assurance** (RHA) and **component procurement** completed
  - **Production 2025#Q4** after BLEIC final design
- Diagnostic & Maintenance equipment in preparation
  - To be used also during the acceptance tests

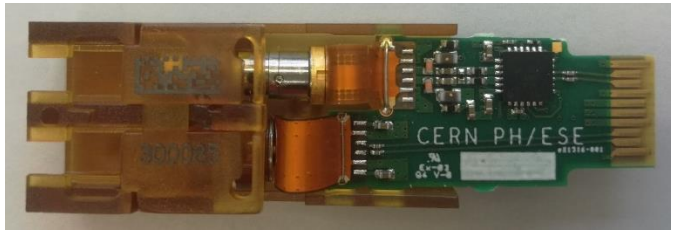
EDMS code	Acronym	Board function	Status
EDA-03916-V2-0	BLEACT	Beam Loss Electronic - **Acquisition Crate** for the Tunnel	Completed
EDA-03917-V4-0	BLEBPT	Beam Loss Electronic - **Backplane** for the Tunnel	Completed
EDA-03918-V3-0	BLEIPU	Beam Loss Electronic - Input **Power Unit**	Completed
EDA-03919-V5-0	BLEPSU	Beam Loss Electronic - Power **Supply Unit**	Completed
EDA-04846-V2-0	BLEACCM	Beam Loss Electronic - Acquisition Crate **Controller Card** – Manual	Completed
EDA-04932-V1-0	BLEBPTLS	Beam Loss Electronic - **Backplane** Tunnel for SPS Straight Section	Completed
EDA-04991-V1-0	BLEHVT	Beam Loss Electronic - **High Voltage distribution** for the Tunnel	Completed
SPBLEBS001 v.0	BLEBS	Beam Loss Electronic - Tunnel **Signal Patch Panel** Box	Completed
SPBLEBH001 v.0	BLEBH	Beam Loss Electronic - Tunnel **Power Patch Panel** Box	Completed
EDA-03704-V1-0	BLEIC	Beam Loss Electronic – **Acquisition module** (full ASIC version)	Under development

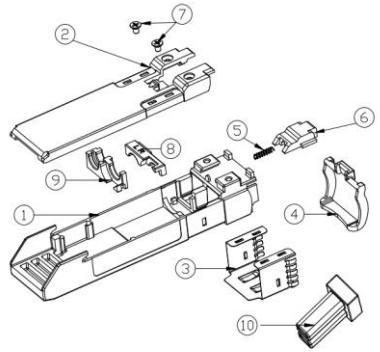
EDMS code	Acronym	Diagnosis and maintenance electronics	Status
	BLETE	Extender with **parameters monitoring**	Completed
EDA-0xxxx-V1-0	BLEACT	Handheld Maintenance **Tunnel Electronics Tester**	Under development

Rad-Tol Communication Layer

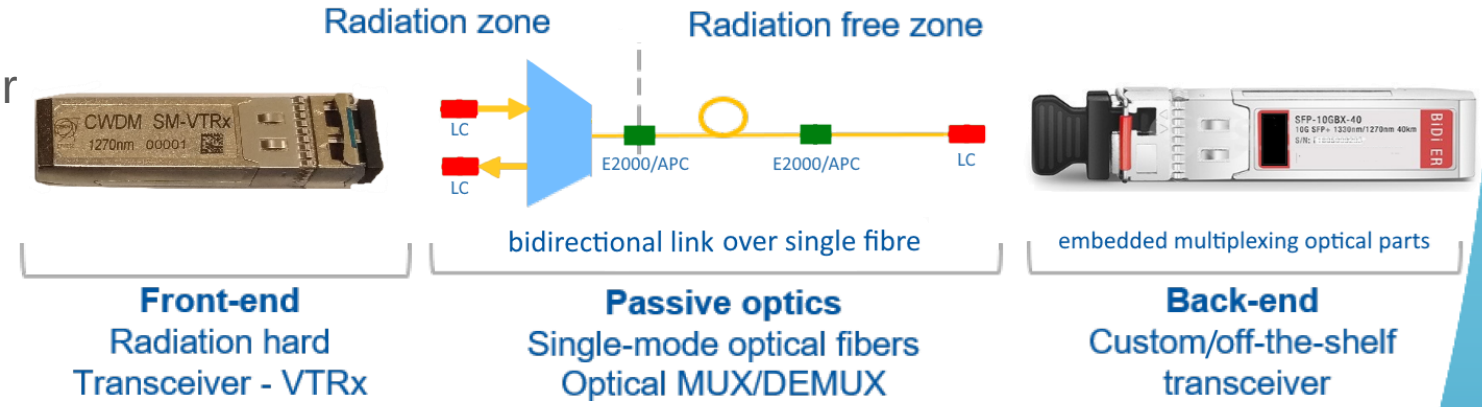
- Single-mode Versatile Link Transceiver - VTRx







- Custom design for SY-BI by EP-ESE
- Directly compatible with the LpGBT serialiser
- Bidirectional; operating from 4.8 to 10 Gbps
- Enclosed in SFP format
- Prototype qualified to 10 kGy



MS-4730/EP/ESE did not succeed / TOSA manufacturer retracted; new parts under qualification;
All other parts are being ordered and driver ASIC in manufacturing.

Conclusions & Acknowledgements

Summary I

- **Ambitious program on-going to harmonise Beam Loss Monitoring across the Accelerator Complex with two systems**
  - Two acquisition systems (PS Complex/TLs and LHC/SPS)
  - Common back-end electronics
- **BLM ‘Application-Specific IC’ (ASIC), currently in production**
  - Internal review after an extensive qualification for performance and radiation (X-Ray, protons and mixed-field) resistance completed
  - Significant cost optimisation with > 5x fewer components than previous COTS/Hybrid boards
  - Some savings due to MPW run for production, but extra costs in packaging balance the CtC
- **Critical component procurement completed**
  - Secured all other CERN ASICs (bPOL, LpGBT, CTRx, etc) as well as all custom parts (nFIP, transformers, etc.)
  - Radiation Hardness Assurance completed for all COTS parts to be used under radiation
- **New electronic & crate designs ready for production**
  - Prototype production & validation completed
  - Front-end module (BLEIC) to be finalised and
  - Production to start mid. 2025

Summary II

- **System integration in LHC Controls started**
  - Advanced version of the back-end firmware for communication and control available
  - Integration in the real-time data processing and decision making under validation
  - First version of FESA server and expert tools & GUIs available
- **Tunnel Integration (almost) complete**
  - 354 BLM detectors localised
  - Finalising now the positions for the distribution boxes and racks
- **Large number of LS3 installation & consolidation activities**
  - Cross-check of activities across machines needed
  - Additional personnel resources to be agreed in 2025

Acknowledgements

- BLMASIC
  - Kostas Kloukinas
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  - Leonardo Marcon
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  - Jeremy Blanc
- R2E
  - Giuseppe Lerner
  - Ruben Garcia Alia
- Integration
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  - Joao Oliveira
  - Paolo Fessia
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  - Raphael Berberat
  - Salvatore Danzeca
- IC Manufacturing
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  - Thibaut Coiffet
  - Alessandro Dallocchio

Thank you!!

Spare Slides

Design Objectives

- Build a configuration able to host both the BPM & BLM upgrades:
  - those systems share location and resources (power, fibres etc.)
- Harmonise electronics across machines:
  - Common SPS & LHC BLM architecture (on-going global harmonization effort)
  - Share elements between LHC & INJ BPM systems
- Maintain backwards compatibility (on the LHC BLM side)
  - BLM Acquisition module & Power Supply Units
  - i.e. pin to pin compatible with the current chassis backplane
- Improve the acquisition system performance:
  - Radiation tolerant up to 1 kGy (currently at 500 Gy).
  - Integration period of 10 µs (currently at 40 µs).
- Improve safety:
  - Additions to maintain the SIL3 for safety critical systems.
  - Protection against direct contact to HV or 230 V_{AC}.
  - Grounding improvement
- Improve reliability:
  - All modules encapsulated in metal boxes (prevent transport damage)
  - Reduce number of interconnections
  - Simplify manufacturing
  - Simplify optical transceiver interconnection.
- Improve maintainability:
  - Reduce repair time
  - Declassify the repairing complexity
  - Additional diagnostics.

Requirement	Critical/ Wish	Target
Radiation tolerance	C	1kGy / 20 years
Chassis MTTF calculated with handbook 217plus at 40˚C	C	> 1 E+07 h
Power supply MTTF (using MIL217plus at 40˚C)	C	> 1 E+06 h
Component derating	C	< 50%
Global Power requirement	C	≥ 50 W
Mini-crate height	C	< 400 mm
Chassis height	C	3U
Chassis depth	C	220 mm
Connector Pins pitch	C	≥2.54 mm
Connector mating cycles	C	500
Backplane connector P.N.	W	09 03 264 2825
Backplane PCB thickness	C	2.2 mm
PCBAs quality	C	* See note below
Required voltage 1	C	+1.5 VDC (5 W)
Required voltage 2	C	+2.5 VDC (10 W)
Max ripple for digital voltages	C	50 mVpp
Required voltage 3 (with linear voltage regulator)	C	+5 VDC (5 W)
Required voltage 4 (with linear voltage regulator)	C	-5 VDC (5 W)
Max ripple for analog voltages	C	10 mVpp
Ventilation air flow	C	500m^3/h
FAN MTTF (using MIL217plus at 40˚C)	C	> 4 E+05 h
Component quality	W	Automotive

Printed Circuit Board Prototype (BLEIC)

New prototype PCB design complete

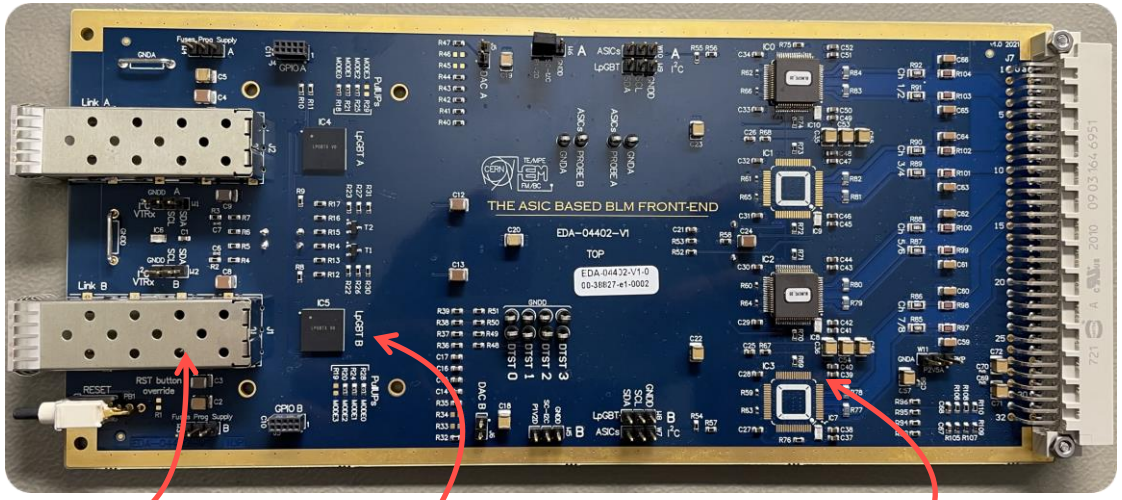
- Includes all functionalities expected from the final system
- Common digital parts, control and form with standard BLM acquisition board.
- Secured prototypes of the other custom parts, e.g. the SM-VTRx and LpGBT.

Prototype production completed and tested to be functional

- This board variant is able to accommodate both BLMASIC v2 & v3

Currently working on system integration (see also next slides)

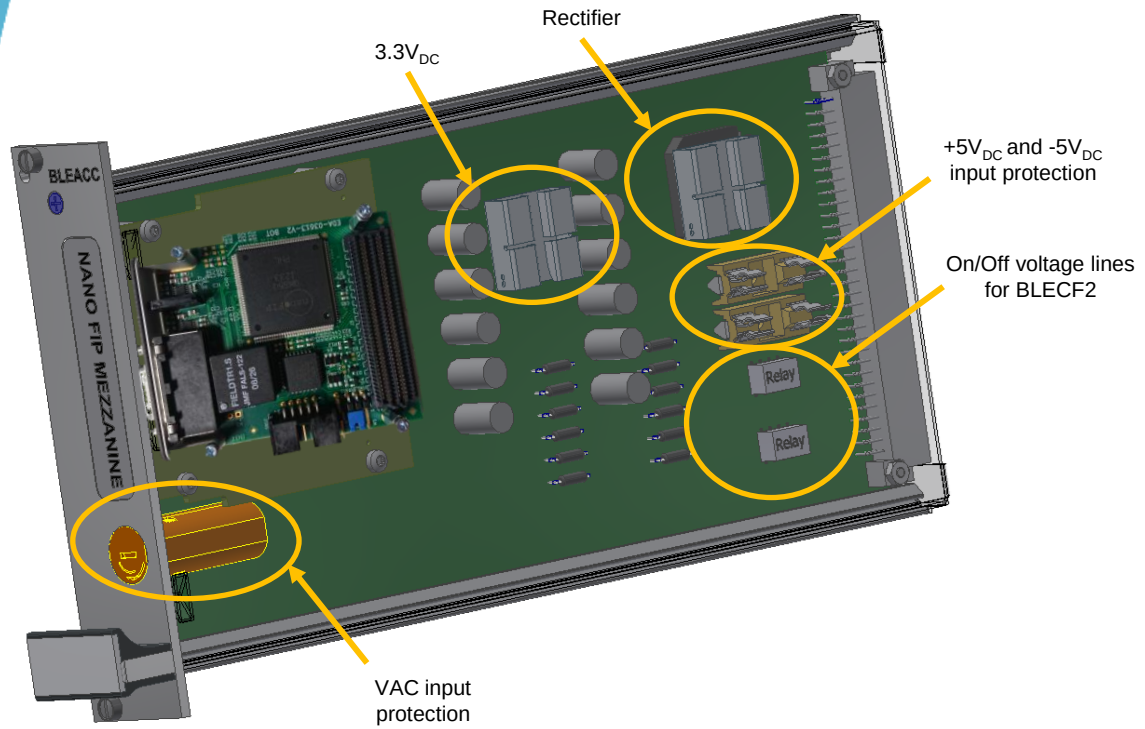
- Development of back-end firmware for communication and control
- Integration in the real-time data processing and decision making



Comparison of old and new technology of radiation tolerant front-ends

	BLECF COTS & ASIC hybrid version	BLEIC ASIC version
Components	> 2000 parts	< 400 parts
Cost	> 3 kCHF/unit	~ 1 kCHF/unit

Crate Control Module (BLEACC)



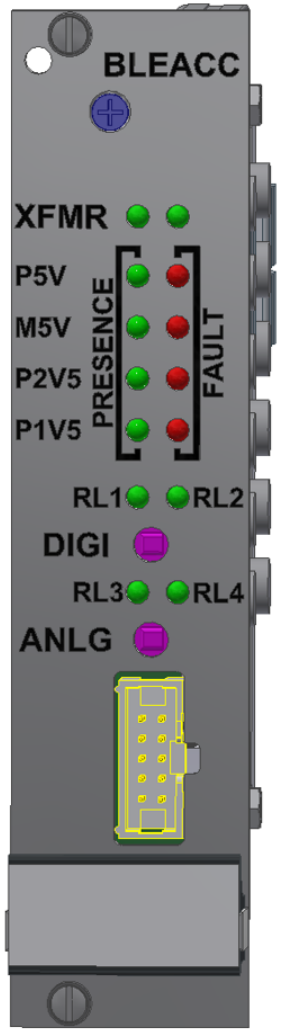
Design in collaboration with BE-CEM

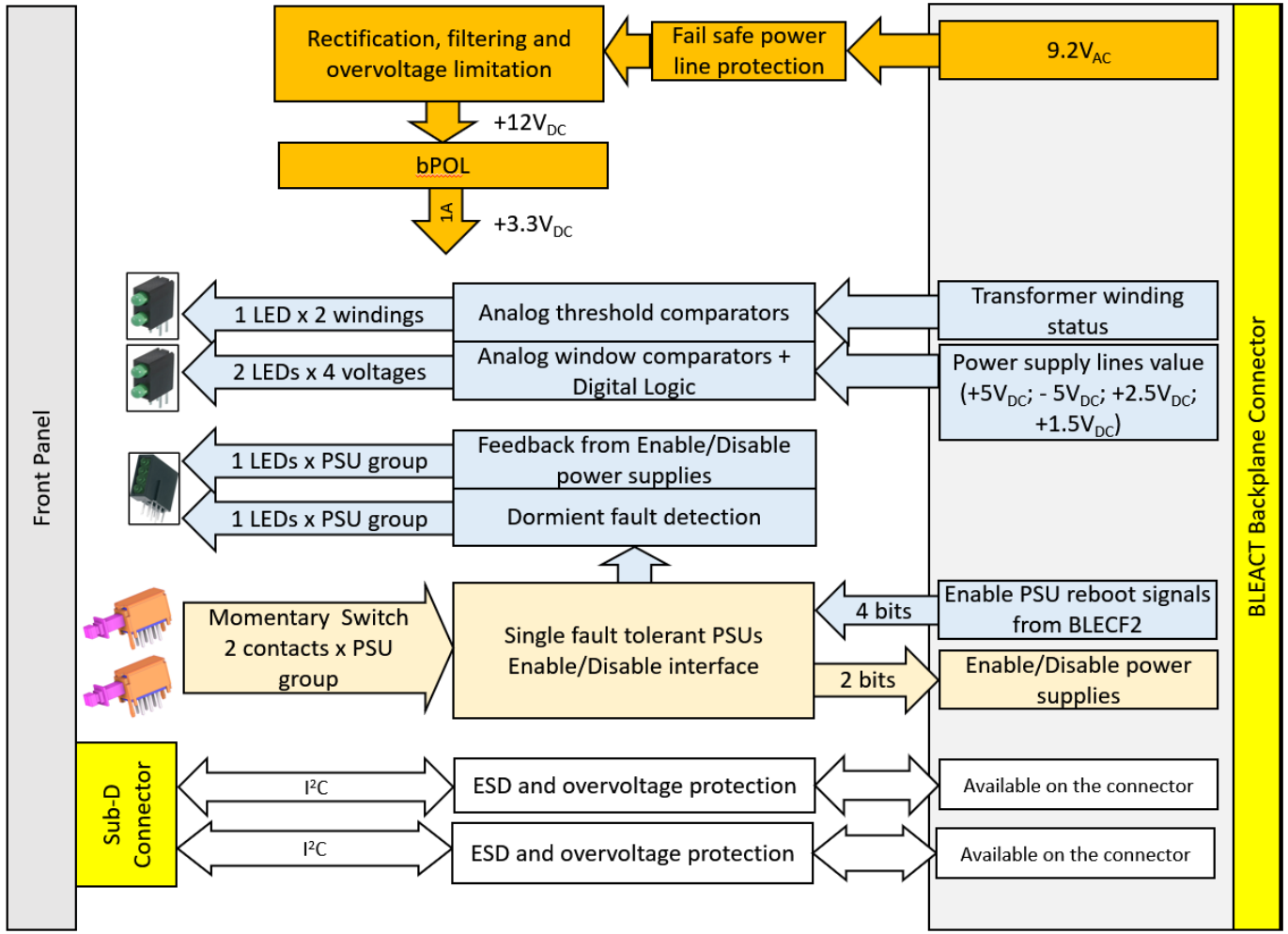
- Carrier to host the nanoFIP mezzanine
- Functionality:
  - Pass commands to acquisition module
  - Power cycle the acq. module through the PSU
  - Diagnostic collection for the PSU statuses
- New functionalities under design
  - Deliver bitstream & re-program FPGA

Crate Control Module (BLEACCM)

New module; Replaces the control module for locations without FIP

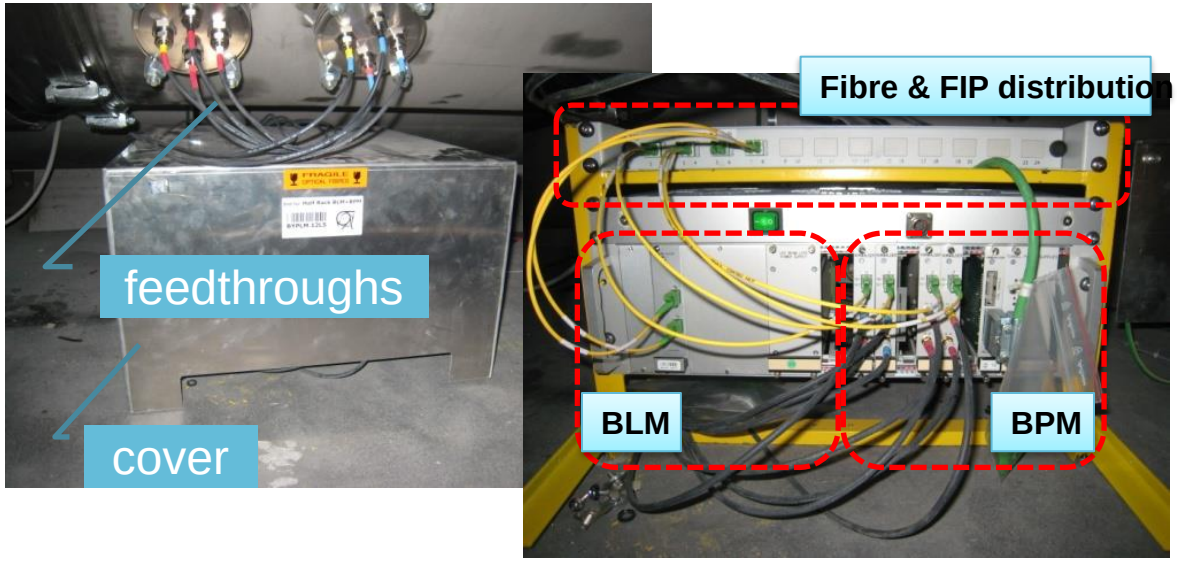
- Fail safe power input stage
- Double I²C bus communication with the Acquisition board
- BLEPSU On/Off function driven by front panel pushbuttons or BLEIC
- Diagnostic LEDs for
  - Transformer Output windings
  - Analog and Digital buses
  - Power cycling interface





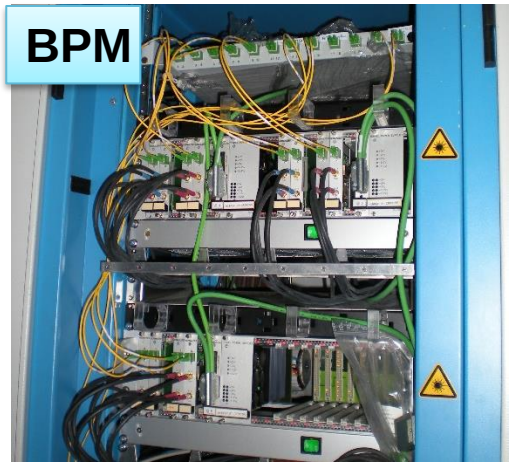
LHC Tunnel Installation

ARC electronics



- Installed under each Quadrupole
- Common mini-crate & fibre network
- Separate power supplies

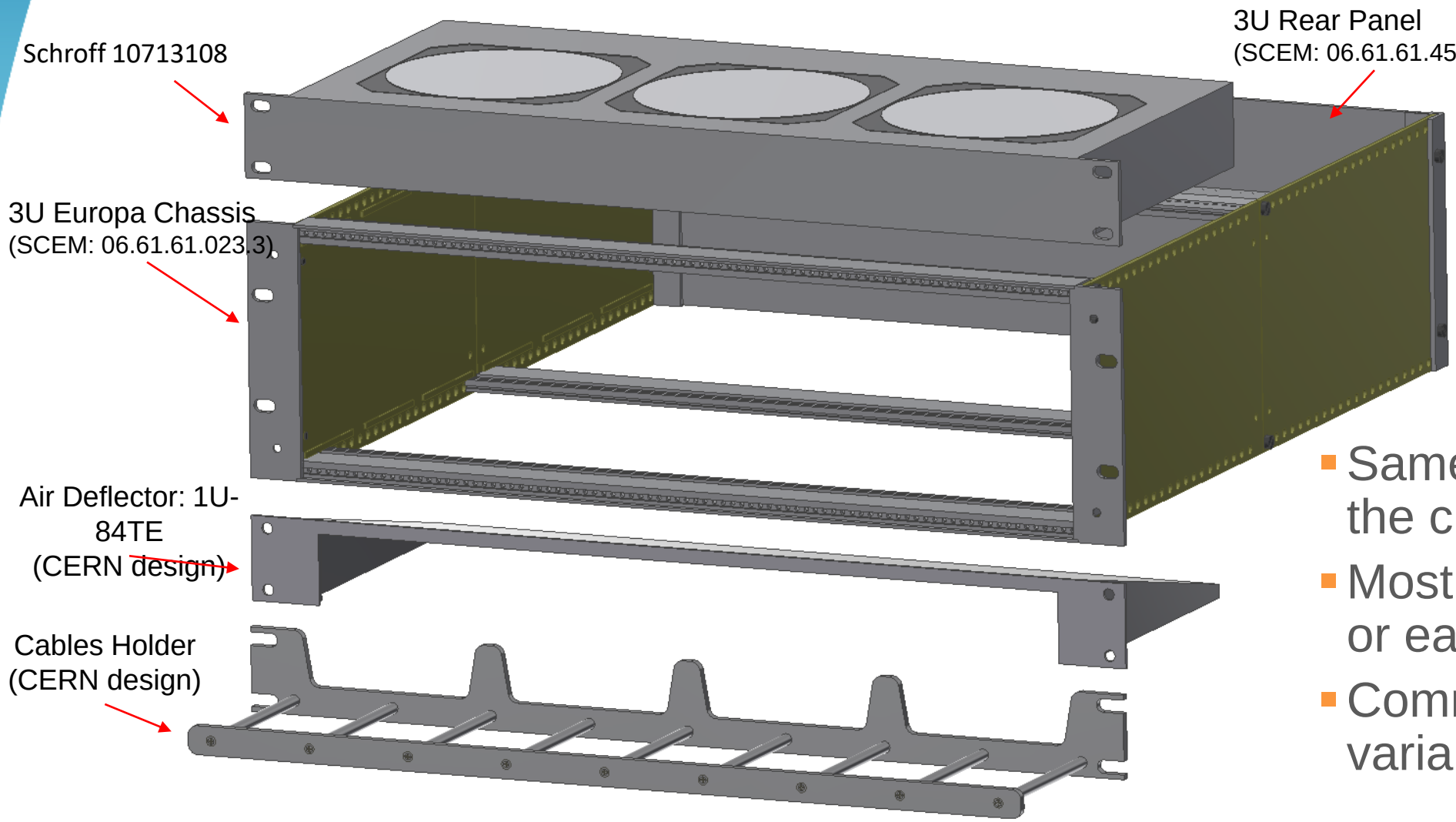
DS & LSS electronics



- Localised in alcoves like UA, UJ or RR
- Same electronics in a different configuration
  - Exception the BLM power supply

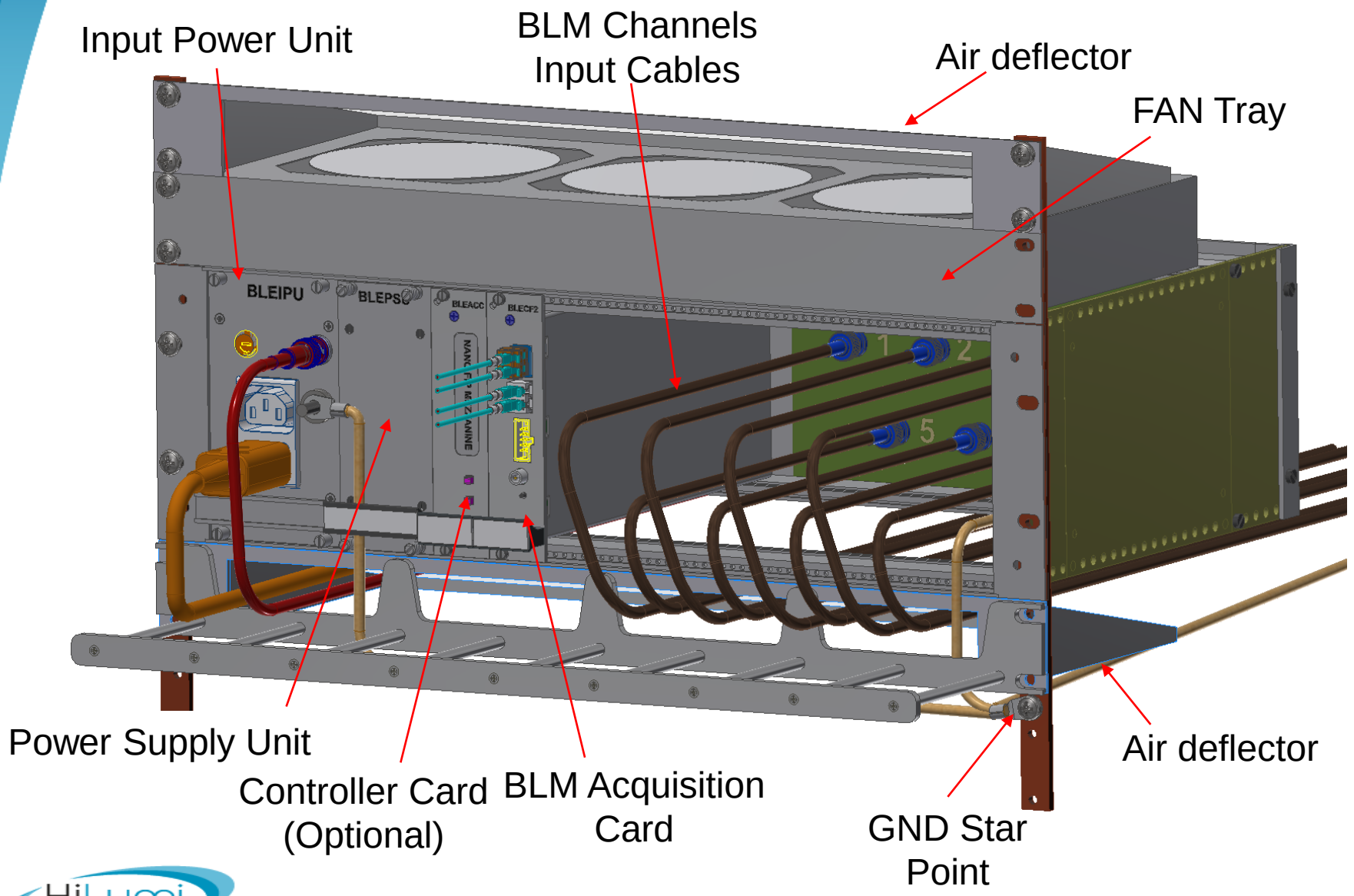
Three variants of the mini-crate needed for LHC BPM & BLM systems

Tunnel crate: Mechanical parts



- Same part numbers with the current installation
- Most in the CERN store or easily procured
- Common parts to all variant designs

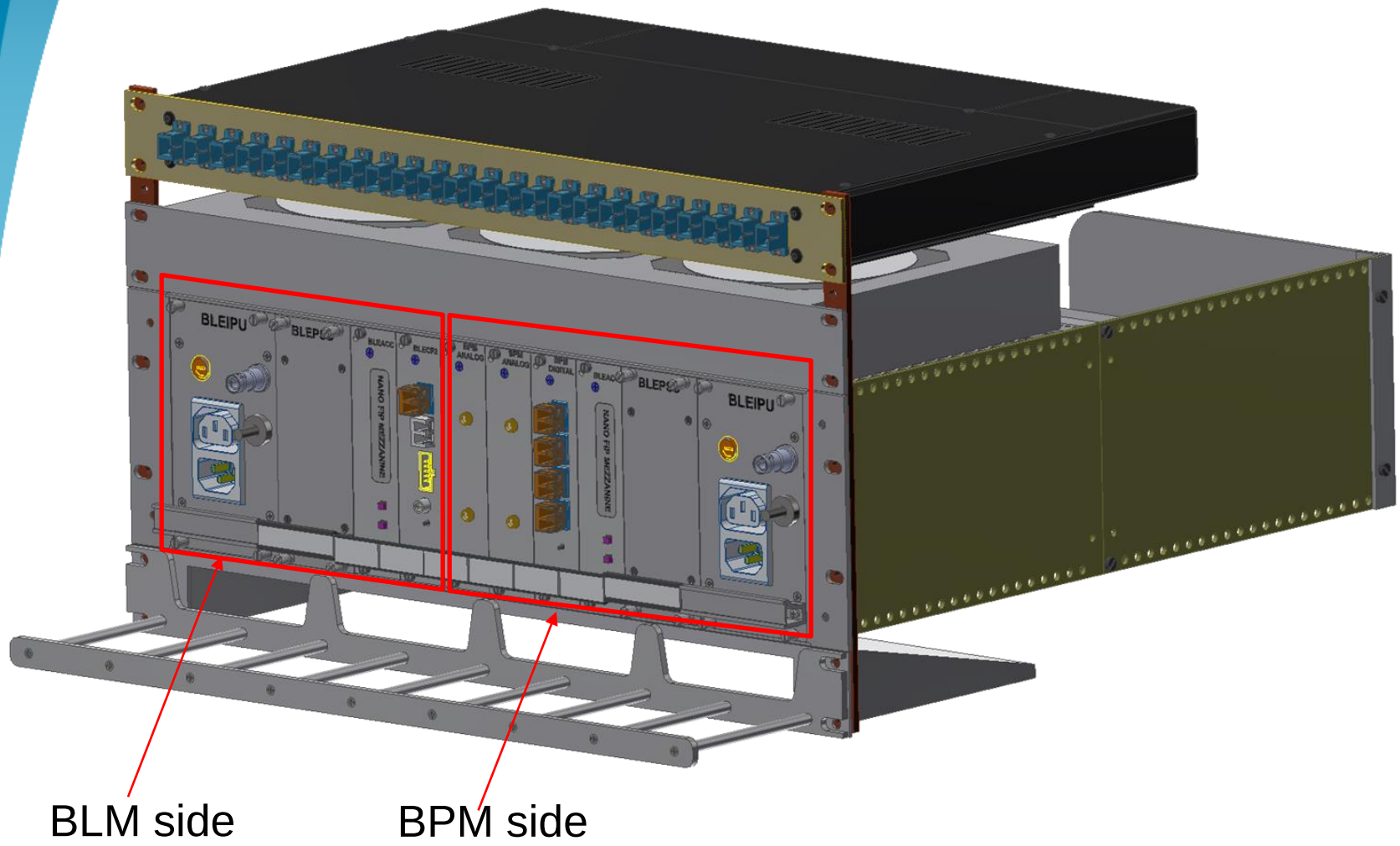
SPS BLM mini-crate



Characteristics:

- Front access
  - SPS specific requirement
  - Applies to all connections and modules
  - Allows mini-crate to be installed at the wall side
- Controller card
  - Redundant functionality
  - Missing infrastructure at SPS
- Custom backplane
  - Targeted design
  - Completely passive
  - Better cable management, i.e. 8x CB50 (coaxial) with BNC connectors

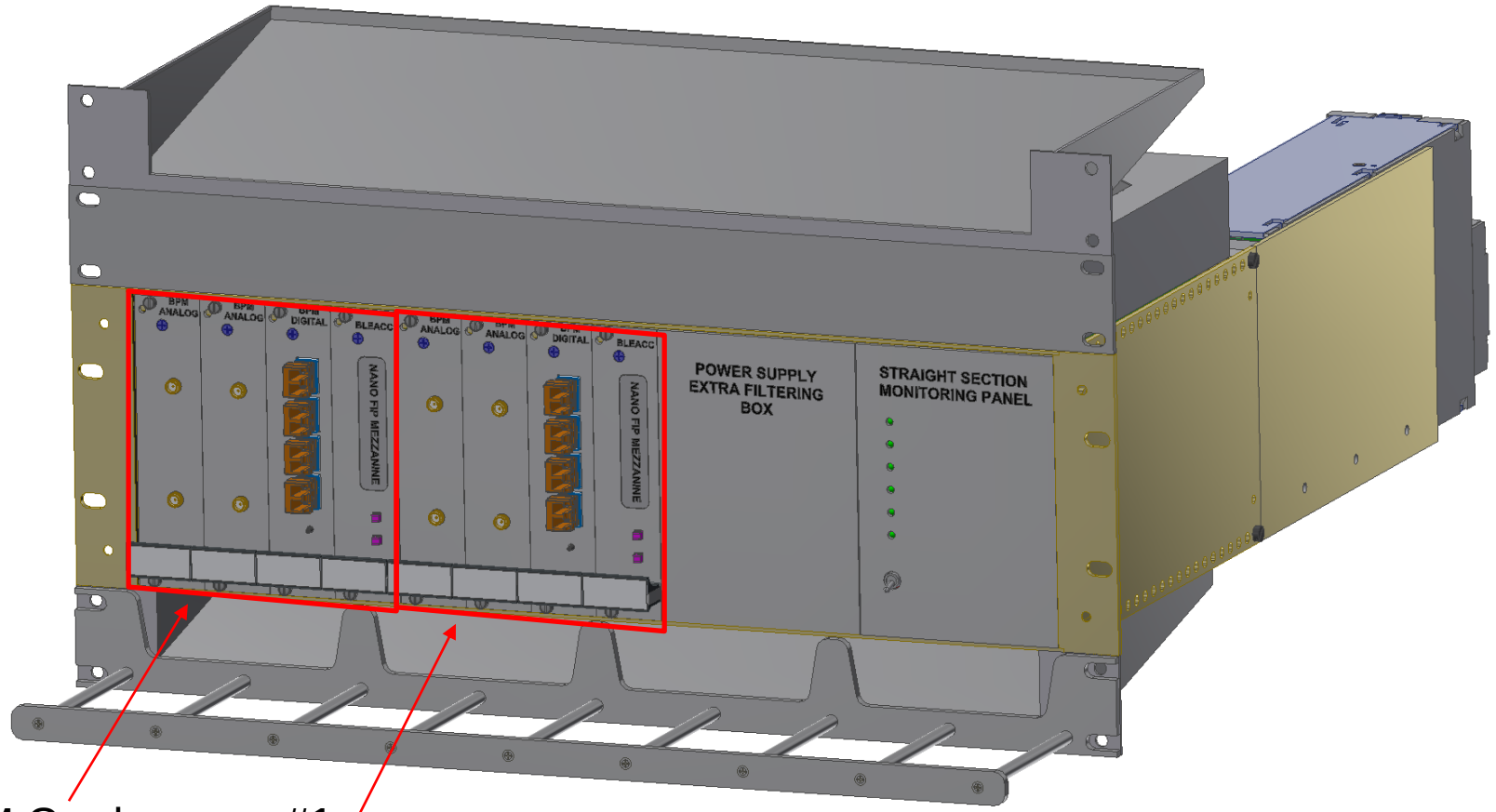
Common LHC (BPM & BLM) mini-crate



Characteristics:

- Common chassis
  - BPM & BLM shared
- Separate Power supply
  - Common part number
  - Isolate failures per system
- Separate backplane
  - Targeted design
  - Better cable management, i.e. for BLM 8x CB50 (coaxial) with BNC connectors & for BPM pass-through to digitiser

LHC BPM (LSS) mini-crate



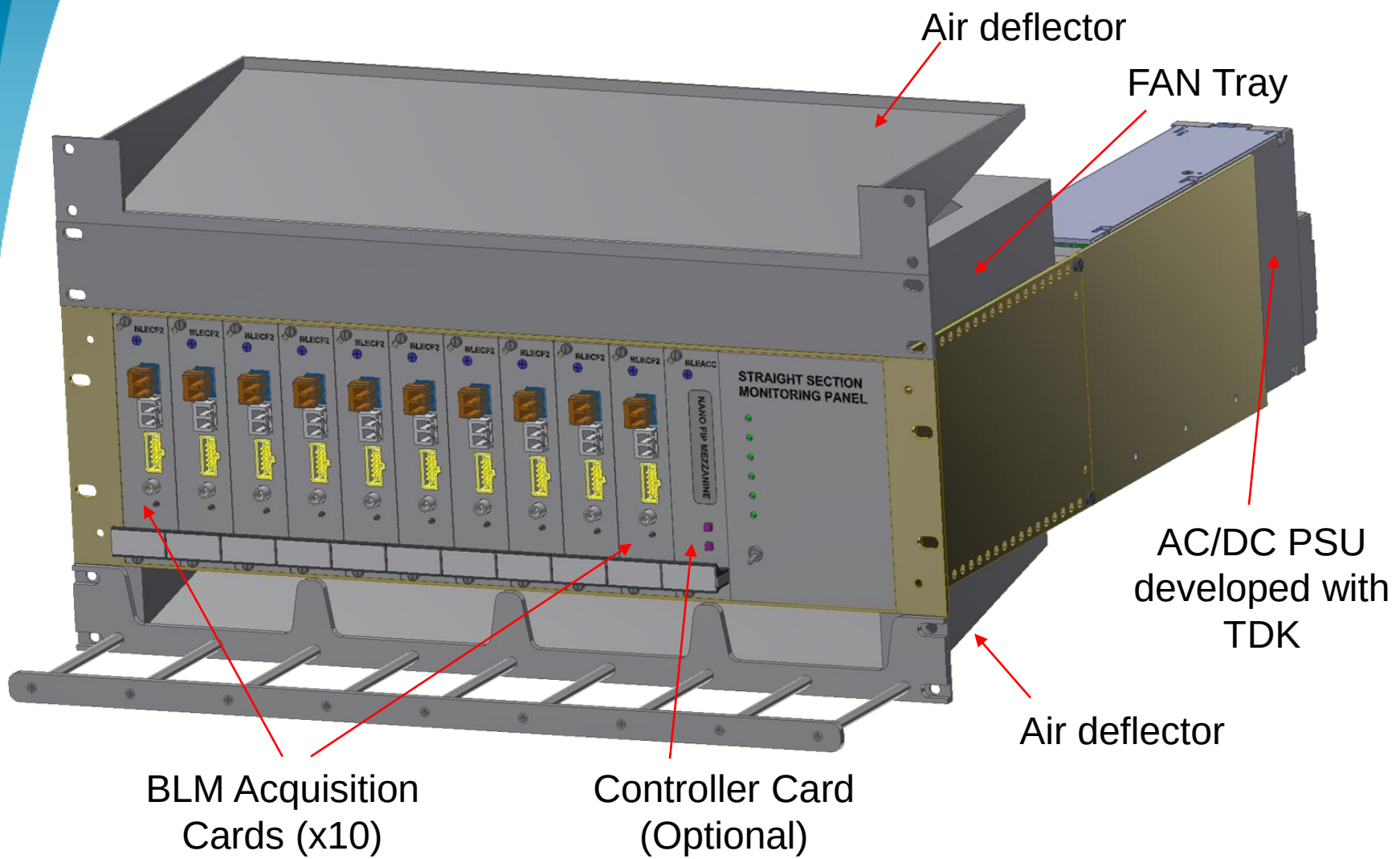
BPM Cards group #1

BPM Cards group #2

Characteristics:

- Front connections
  - all modules and
  - all fibre connections
  - WorldFip
- Rear connections
  - none
- Controller card
  - Unique functionality, i.e. control and re-programming
- Filtering module
  - Foreseen for the case COTS power supply too noisy.
- Custom backplane
  - Targeted design
  - Completely passive

LHC BLM (LSS) mini-crate

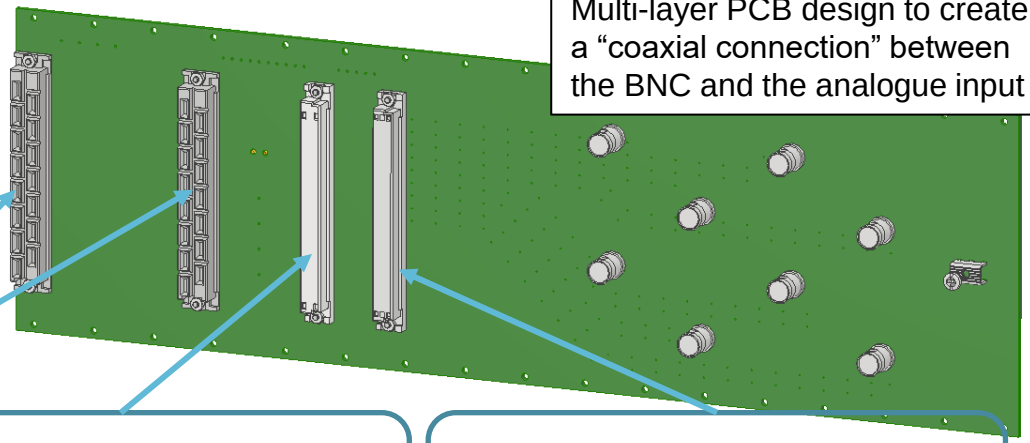


Characteristics:

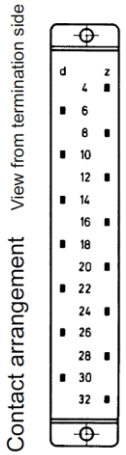
- Mini-crate inside a 45U rack
- Front connections
  - all modules and
  - all fibre connections
  - WorldFip
- Rear connections
  - All analogue signals
- Controller card
  - Redundant functionality
- Custom backplane
  - Targeted design
  - Completely passive
  - Better cable management, i.e. 10 x NES18 (multiwire) with Burndy connectors

Backplane template

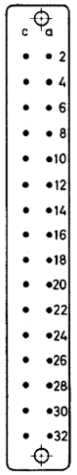
- PCB thickness = 2.2mm
- PCB materials = FR4
- Copper thickness = 35µm



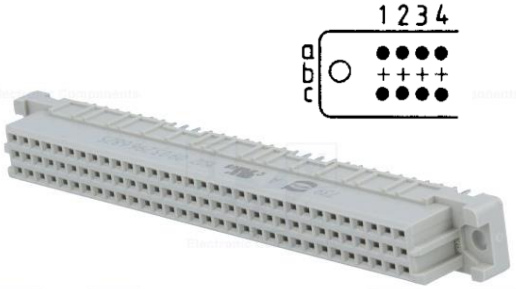
Multi-layer PCB design to create a “coaxial connection” between the BNC and the analogue input



BLEIPU and **BLEPSU** connectors
(SCEM: 09.61.41.565.4
Harting: 09 06 215 2821)



BLEACC connector
(Harting: 09 04 232 2831)



BLECF2 connector
(Harting: 09 03 264 2825)

Best connector IEC 60603 class 1 (mating times up to 500)

Module Connectors

Connector selection to prevent erroneous module swap

BLEPSU & **BLEIPU** connector
Harting: 09 06 115 2911

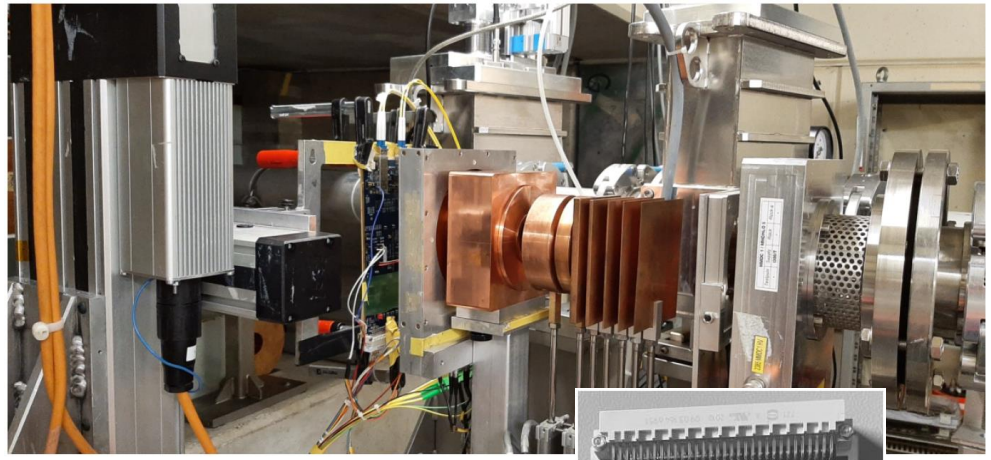
BLEACC connector
(SCEM: 09.61.36.015.4
Harting: 09 04 132 2921)

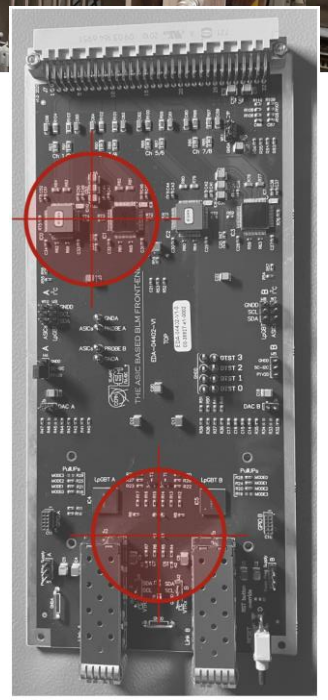
BLECF2 connector
(Harting: 09 03 164 2921)

Size difference prevents accidental swap between them.

Irradiation – Protons (PSI)

Run	Start Time	Stop Time	Beam Current [nA]	TID [Gy]	Target Area
1	*23:34*	*00:25*	1	50	IC0 / IC1
2	*00:30*	*00:46*	3	50	””
3	*00:51*	*01:14*	7	200	””
4	*01:17*	*02:39*	10	1k	””
5	*02:41*	*04:00*	10	1k	””
6	*04:02*	*05:22*	10	1k	””
7	*05:31*	*05:52*	10	200	Transceivers





- Beam energy of 200 MeV and
- Flux, at maximum current of 10 nA, was 3.7 × 10^{8} p*cm^{-2}*s^{-1}
- Run 1-6 targeted two ASICs and linPOL12V reaching ~3.3 kGy
- Run 7 (short) targeted the transceivers with 200 kGy