Minutes of meeting

Subject:	1) Software for new SPS BLM system 2) LHC sequencer tasks
Date:	06 June 2024
Speakers:	1) E. Poimenidou, SY-BI-SW 2) S. Jackson, SY-BI-SW
Chairs:	S. Jensen, B. M. Salvachua Ferrando, A. Boccardi
Indico:	https://indico.cern.ch/event/1422146/

1 Background and aim.

1) BLMSPS: To present the current implementation plans and timeline and receive feedback.
2) LHC sequencer: To give an overview of current situation and discuss plans/options for future work.

2 Action points.

Who	What	Ready by
S. Jackson	Compile and send to CSS/CEM a list of BI use cases for large/fast data storage, asking for a standardized solution.	Q3 2024
C. Zamantzas M. Saccani	Provide functional specification document for the hardware of the new SPS BLM system	Q1 2025
S. Jensen	Organize 2nd TB on LHC Sequencer	YETS 24-25
A. Topaloudis	Sequencer tasks: a) Identify owner of fBCT tasks b) See with Tom about needs for BST checks c) Specify how to do consistency- and reference checks for BI systems	Q3 2024
S. Jackson	Send Sequencer-task list to LHC OP, ask for comments: - New requirements (adding and/or removing tasks) - Which BI systems do they contact in their tasks	Q3 2024

3 Recommendations and agreements.

1) M. G. Berges: The Sequencer task code written by Magdalena must be carefully tested before it is deployed

4 Discussions and comments.

4.1 "BLM SPS software" by E. Poimenidou

4.1.1 Discussion

- Can we standardize on large/fast "high-frequency-data" storage?
    - Eva: BE-CEM-IN asked me to guarantee that the SSD solution used first for the dBLM system would not become part of a critical system. They consider SSDs in FECs a non-standard solution for which they will not provide operational support outside normal working hours.
    - Christos: We were the ones to request the SSD solution and it is not part of the critical operational system. It is a tool used for commissioning, fault finding and in rare cases or MDs.
    - Stephen: In general, we need localized solutions (such as an SSD) to be able to handle the high rates of data. In the BLMINJ we used desktop PCs but we should move to a standardized solution.
    - Belen: I see no reason why OP would be interested in such raw-data.
    - Thibaut: We have other systems requiring this as well, so there should be a standard solution => action point, Stephen.
    - Steen: We should compile a list of "raw-data" use cases and send it to CEM/CSS, asking for them to propose a standardized solution.
- Eva: Why will the conversion from ADC values to SI units be done in UCAP ?
    - Stephen: Because OP already does the explosion of channels to devices there and the HW experts prefer to look at the ADC values in the FESA device.
    - Belen: In LHC, the operators are not responsible for UCAP nodes.
    - Christos: In the past, FECs were too slow to do the conversion so we moved it away from the FECs, into the concentrator. Later, when developing the injector BLM's we moved it back to the FEC and published via separate FESA properties.
    - Ewald: I need to see the ADC values in the FESA class.
    - Eva: Should we now follow this approach everywhere?
    - Steen: Systems are too different to make it a general rule.
- Thibaut: Christos, do you have the requirement specifications for the new SPS BLM system as a written document ? In the past we have done the mistake of not having such a document.
    - Christos: We will provide the technical specification and BI-SW can drive discussions for the FESA specifications. Kevin is the contact person overall, for technical details we go to Fabio and Stephane. => Action point, Christos and Mathieu

4.2 "LHC Sequencer – past, present, future" by S. Jackson

4.2.1 Discussion

- Thibaut:
  - Who owns the fBCT Sequencer task?
    - Stephen: We do not know => Action point, Athanasios
  - Why was the BLM task change rolled out in April?
    - Stephen: To fix a bug introduced after the required EYETS 23/24 control changes, causing occasional, recurrent false errors due to a race-condition when accessing hardware. We had to make the change for the future system anyway.
  - It should be checked with Tom if we need a task for checking BST synchronization. => Action point, Athanasios
  - We should send our list of Sequencer tasks to OP and ask them for comments => Action point, Stephen
- Stephen: I think we should have another technical board on Sequencer tasks when we know more, i.e. during YETS 24-25. => Action point, Steen
- Athanasios: OP also do small checks on BI devices, so we do not always know how our FESA classes are used => Action point, Stephen
- Thibaut: We should investigate how to do complete consistency and reference checks => Action point, Athanasios
- Manuel: Magdalena wrote code for the Sequencer tasks, but not all was deployed. We must check the code very carefully before deploying the rest.
- Steen: Are other technologies than Java being considered for Sequencer tasks – a la Python, UCAP, …?
  - Stephen: No, Java will be available until the end of LHC
  - Thibaut: These are critical components – we should not change it if it works. But we must know well in advance if CSS will make changes.
  - Athanasios: It was mentioned at some point that the Sequencer core would be upgraded/improved.