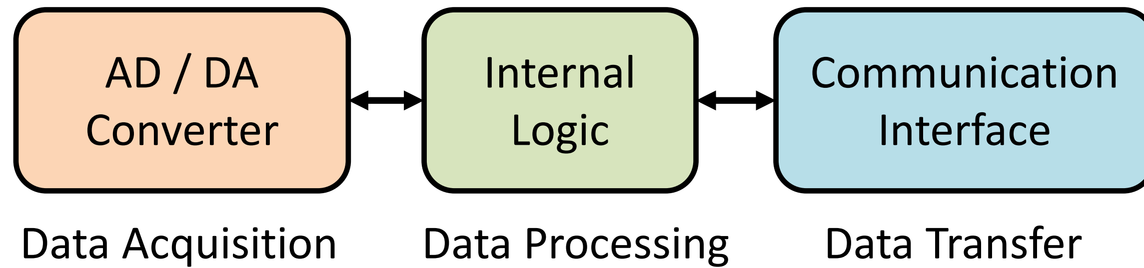
Fachhochschule Dortmund
University of Applied Sciences and Arts

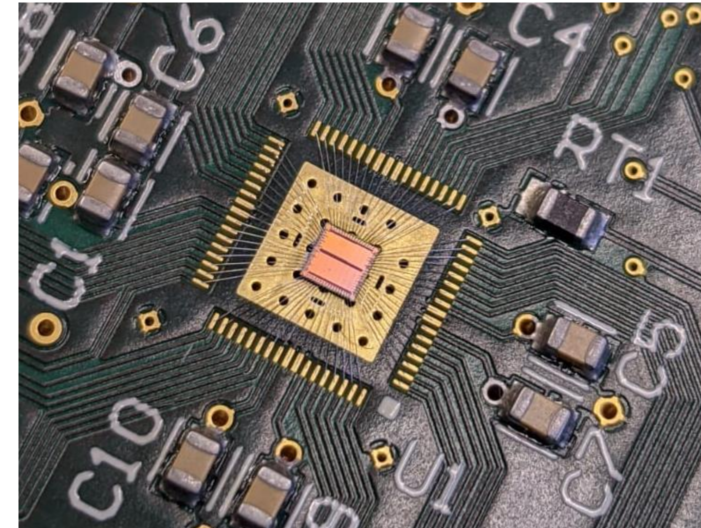
Characterization of an Radiation Hard RISC-V Microcontroller

CMOS Verbund Meeting – 19. Juni 2024

Introduction

- Many custom ASICs have a similar structure:





- Design and verification of a custom ASIC is complex and time consuming
- Reuse of generic blocks possible (ADC, voltage regulators, etc.)
- Adaptation of internal logic difficult, custom to original application

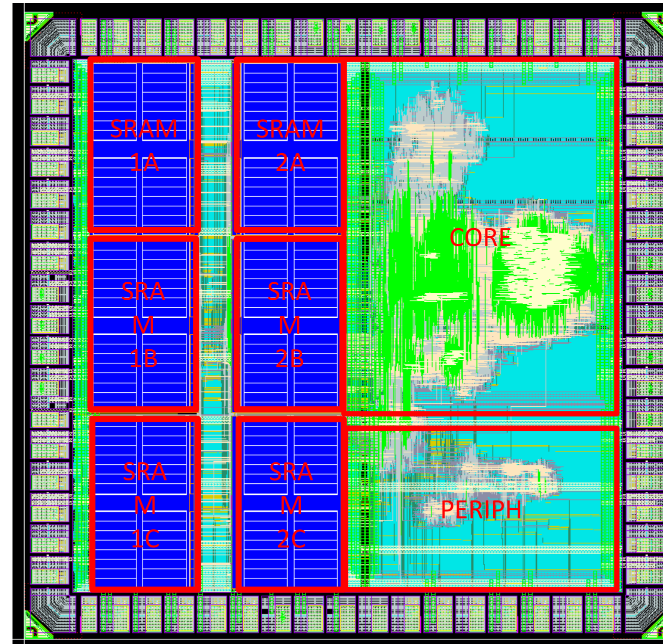
- Internal data processing logic replaced by with RISC-V processing system
  - Adaptation to new application / Bugfixes via firmware updates
- Hybrid detector with RISC-V-based microprocessor SoC

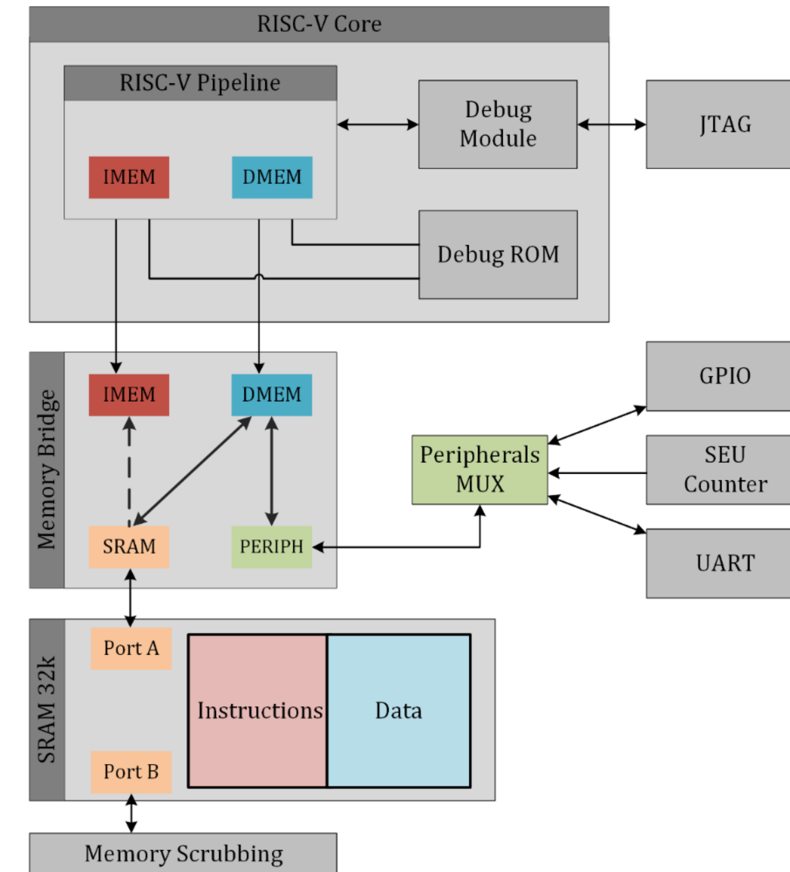
STRV-R1 – Architecture

- 2mm x 2mm in 65nm Technology
- RV32-IMC Core
  - 3 stage pipeline
  - Multiplication extensions
  - 50 MHz @ 1.2V
  - Fully triplicated Core

- TMR Strategy in RISC-V Core:
  - Triplication of
    - All sequential elements
    - All combinational logic
  - Majority voters after each sequential Element
  - Additional feedback path
  - Three separate clock-trees

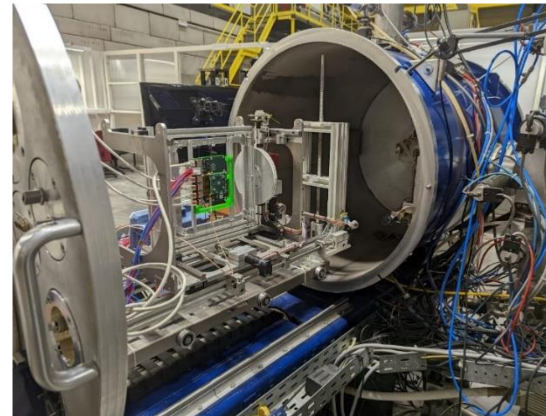
- TMR SRAM Strategy:
  - 3 Dual-Port SRAM Instances
  - Scrubbing on second SRAM port
  - 3x 32Kbyte

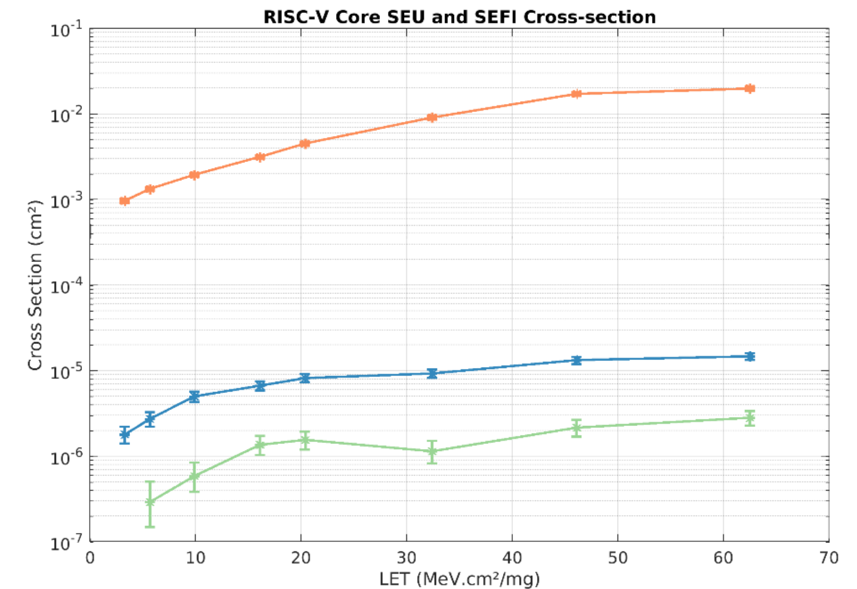




Heavy-Ion Irradiation

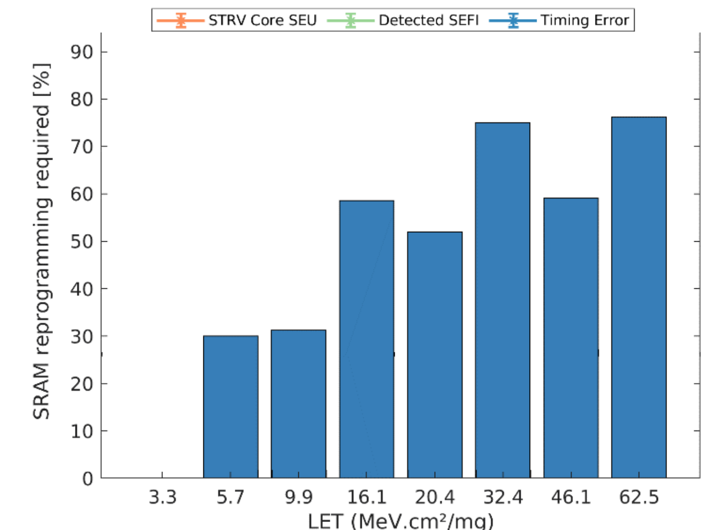
- Heavy-Ion irradiation results
  - Effective SEU cross-section is larger than in test-structures for sequential elements
  - TMR protection scheme in RISC-V core achieves up to 8000x improvement
    - SEFI cross-section directly compared to the SEU cross-section





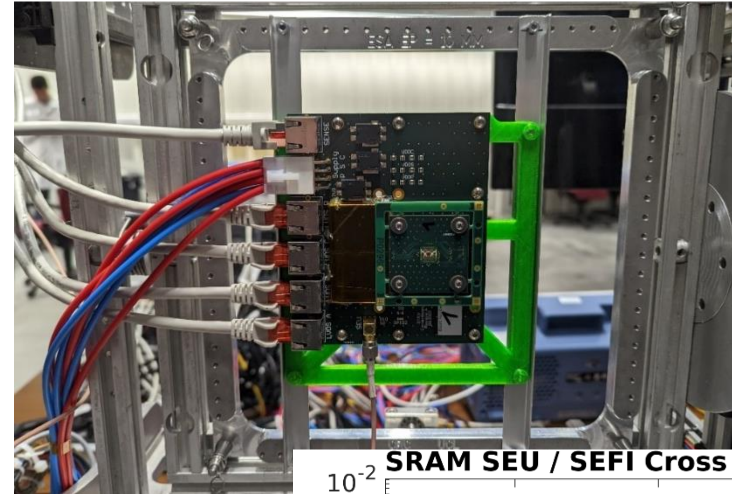
- Residual functional error rate remains
- Observed types of SEFIs during Irradiation:
  - **Silent Data Corruption (SDC)**
  - **Timing Deviation**
  - **Timeout** (Reset or reprogramming required)

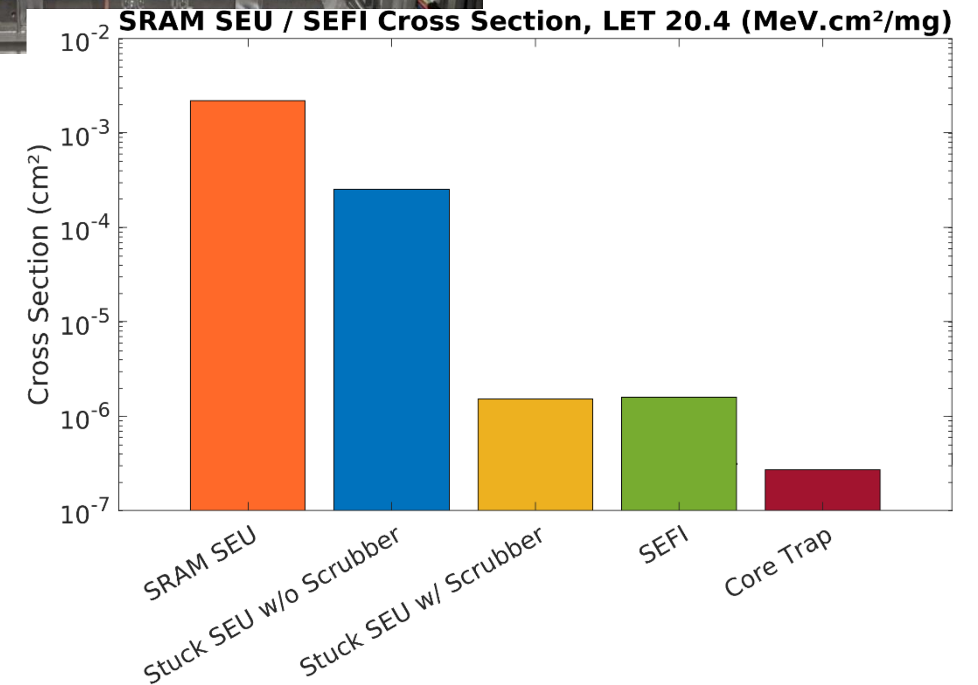
- SEFIs which can not be recovered by a reset of the RISC-V core:
  - Data or Instructions in the SRAM corrupted
  - Reprogramming of the SRAM required
- Reprogramming rate:
  - For low LET (<16 MeV.cm²/mg): Reprogramming required in 30% of SEFIs
  - For higher LET (>16 MeV.cm²/mg): Reprogramming required for >50% of SEFIs



SRAM Heavy-Ion Irradiation

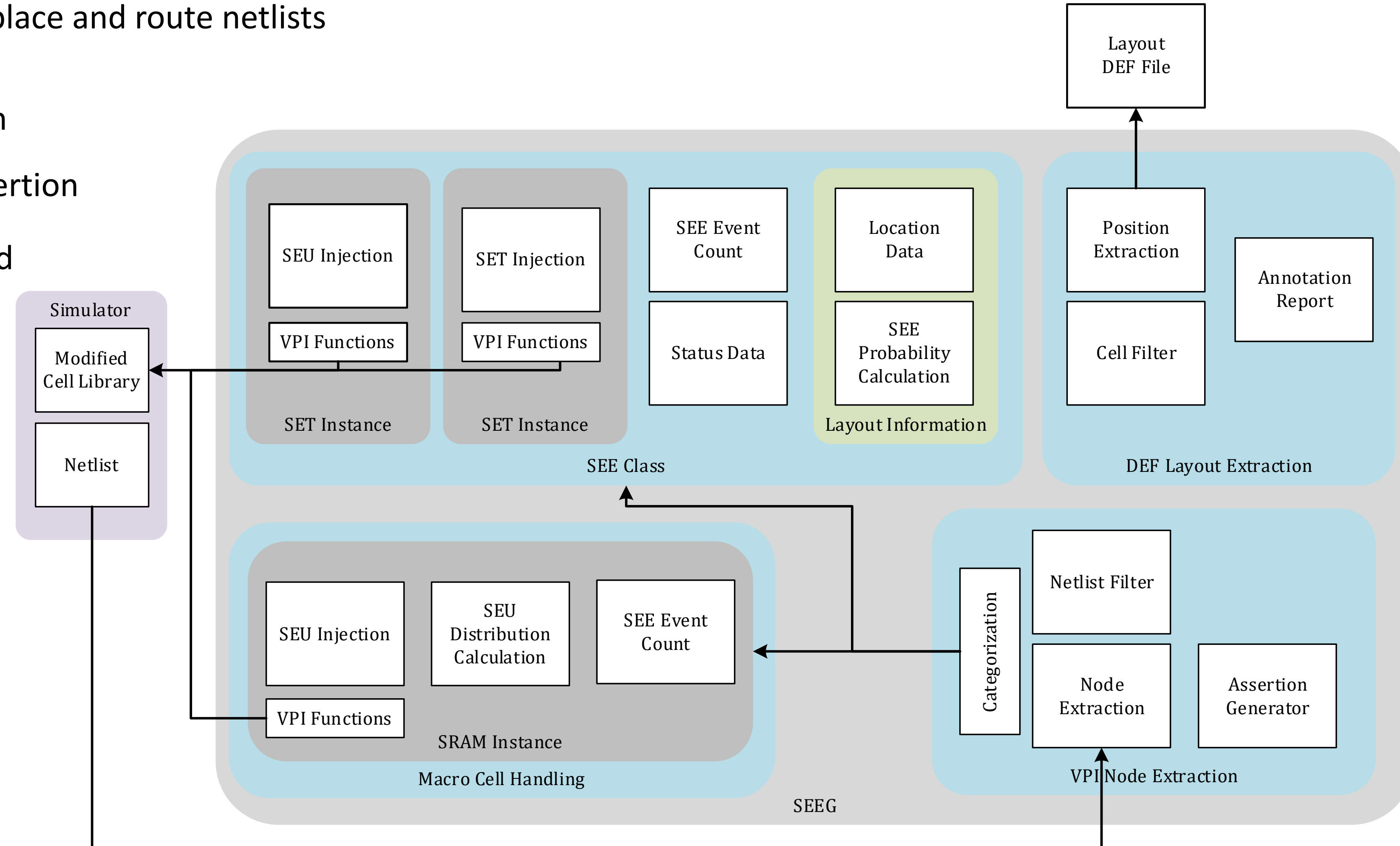
- Analysis of SRAM as SEFI error source
  - SRAM isolated analyzed under irradiation
  - RISC-V core deactivated
- Reduction of non-correctable SEUs in SRAM through:
  - Triplication of the SRAM
  - Scrubbing of the SRAM
- Residual error rate remains
  - Same order of magnitude as the system's SEFI rate
- Error pattern can be reproduced in SEE injection simulation
  - Occurrence of SEUs between two clock cycles
  - Incorrect scrubber correction can occur
- 17% of all permanent SEUs in SRAM lead to trap of the RISC-V core
  - E.g. invalid instructions or addresses
  - Dhrystone benchmark
  - Dependent on distribution of data / instructions
- Remaining permanent SEUs lead to SDCs or are masked by software





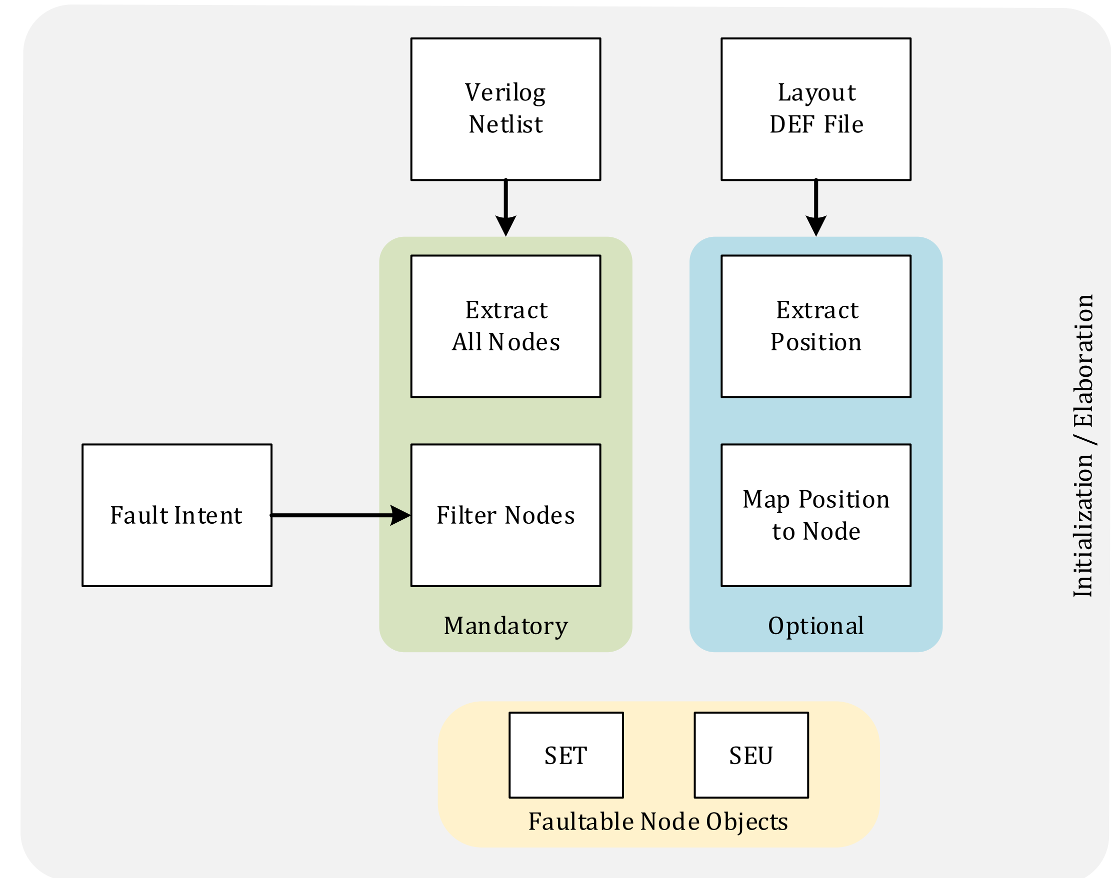
SEE-Injection Simulation Framework

- Designed to replicate real-world impact of SEE
- Intended for simulations with synthesis or place and route netlists
- Ability to include information about the physical placement of the cells in the design
- Automatic generation of SystemVerilog assertion
- No modification of design or netlist required
  - modification of cell library required
- VPI Functions used to communicate with simulator



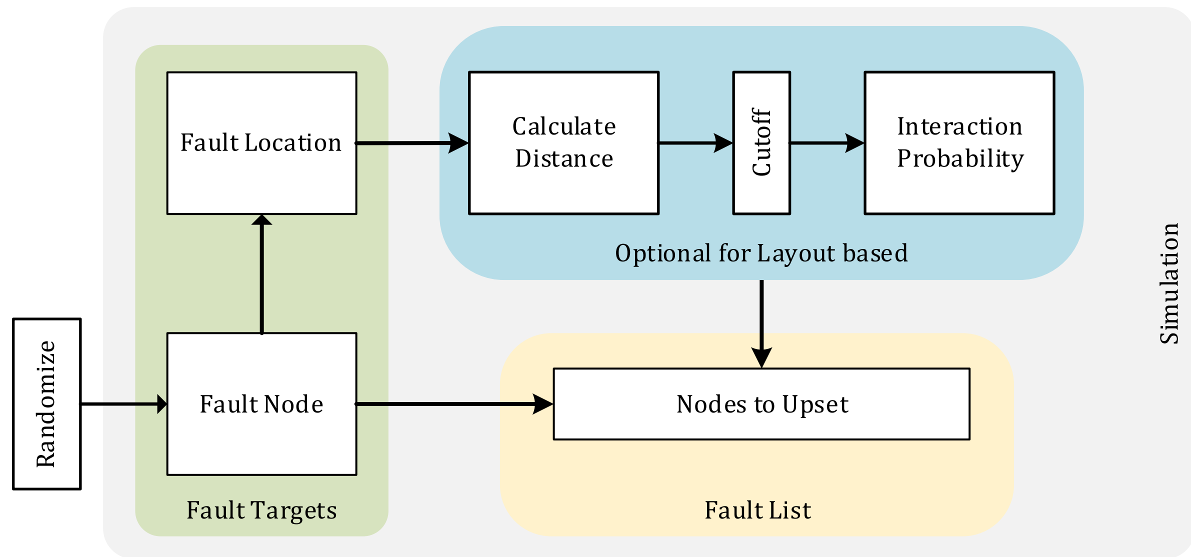
SEE-Injection Signal Selection

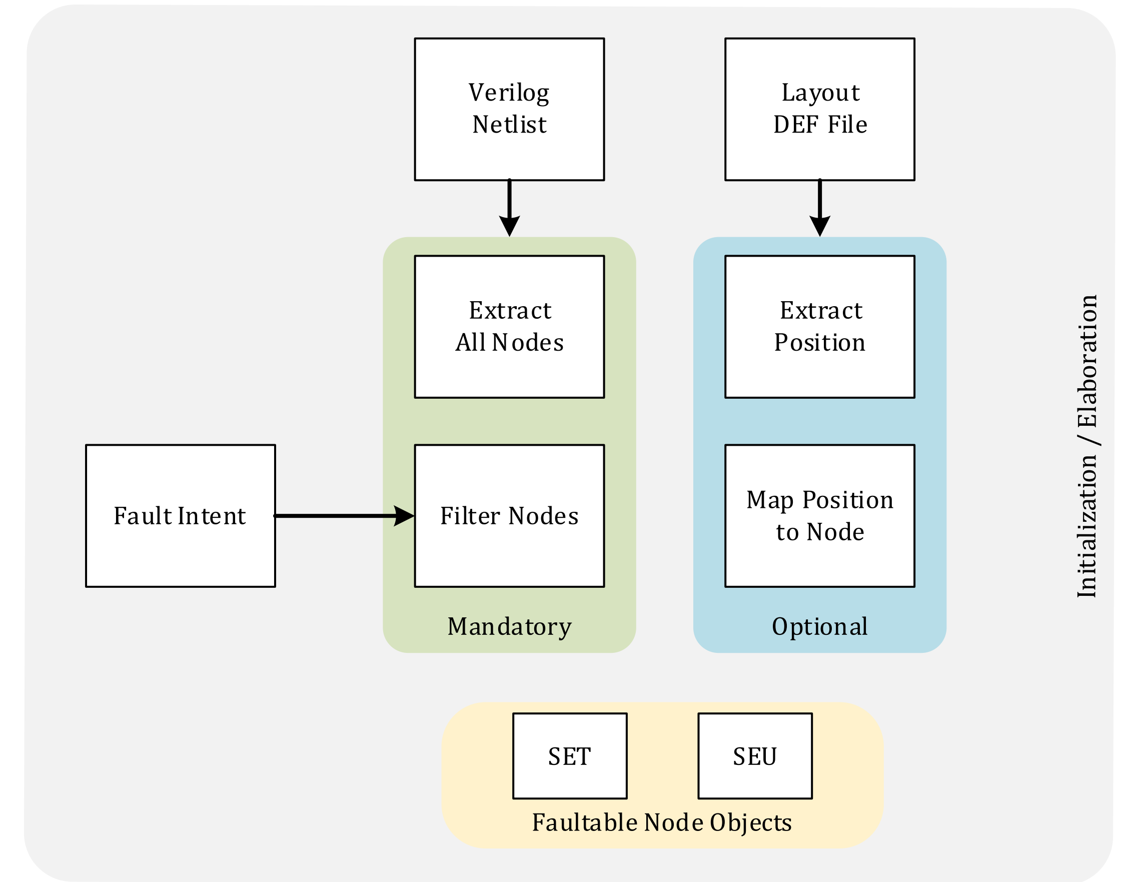
- Randomization
- Reproducibility and random stability
  - Framework uses PRNG with one-time seed provided by simulator
- Fault intent specification
  - Scope to be covered by injection (top level of injection)
  - Type of fault to inject (SET / SEU / Macro specific)
- Filtering options
  - Nodes to be injected on
  - Netlist exclusions (string manipulation)
  - Cell type selection (with DEF mapping)



SEE-Injection Layout Information

- Additional to randomized selection from netlist
- Layout Information from DEF
  - Positions mapped to faultable node objects
  - Distance from faulted node to other nodes calculated
  - Interaction probability determines secondary SEEs
  - Additional nodes upset



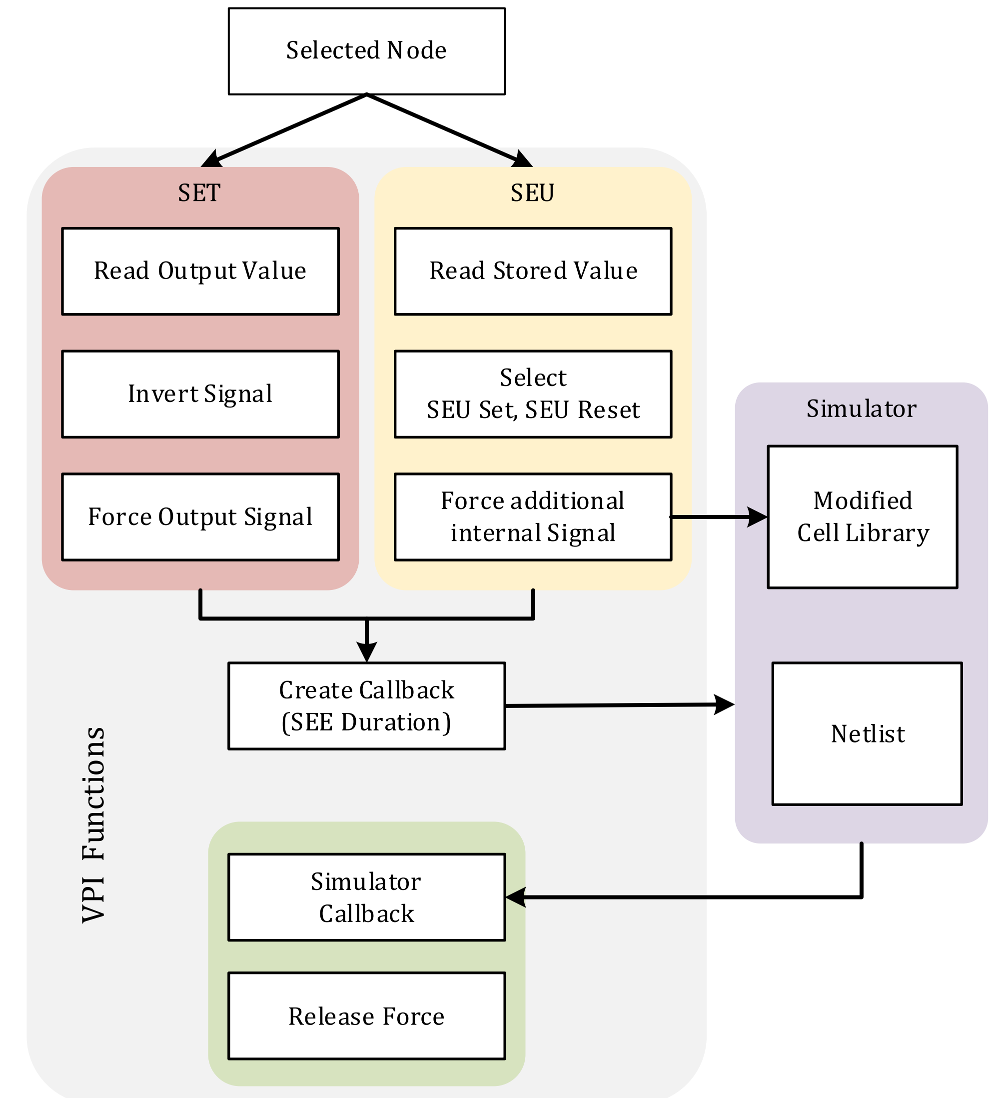


Runtime SEU | SET Modelling

- SET are less meaningful in RTL
  - Synthesis and place & route netlist used
- SEU Injection requires instrumentation of the STD cell library
  - Added internal signal for flipping the stored value

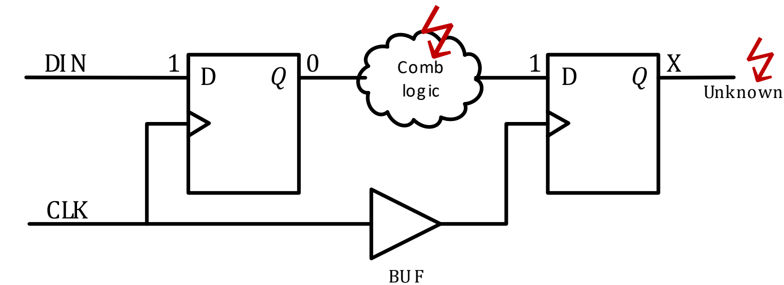
- Select (randomized) node and SEE duration
- Read state of selected node via VPI functions from simulator
- Invert state of the net using VPI put value function with force flag
- Create a callback for the SEE duration
- Simulator continues for the given amount of time
- Callback from Simulator when time elapsed
- Release the net using VPI function

- SEE duration in SEUs: Time the upset is actively forced
  - Upset is kept until next valid sequential activity



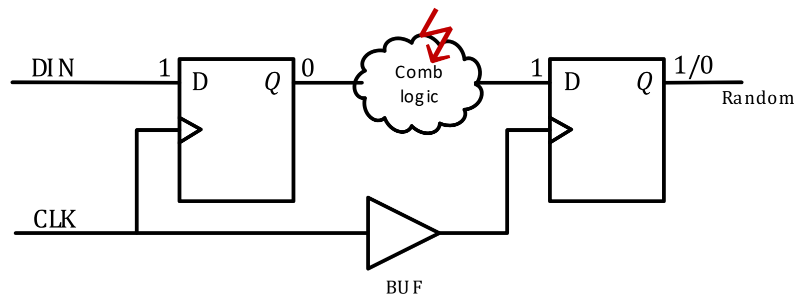
Standard Cell Library Instrumentation

- Timing of SEE independent of clock (randomized)
- SET in the combinational logic or clock-tree
  → Timing violations in sequential logic possible
  – Setup, Hold, Width violations
- Typical standard cell models set sequential output to X (unknown)
- Propagation through netlist according to simulator settings

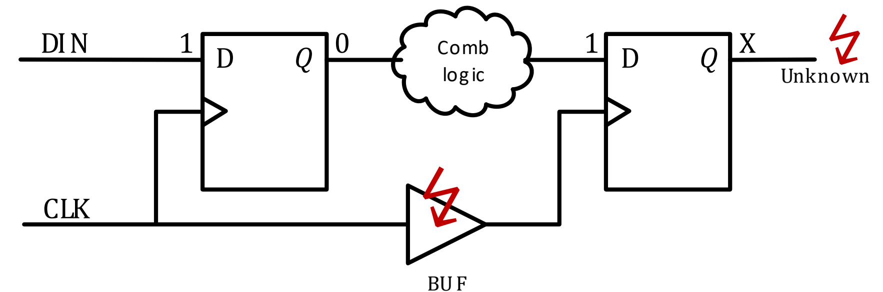


SET in comb. logic (setup / hold violation)

- Modified standard cell library to replicate real-world behavior
  – Randomized valid output propagated to next cells



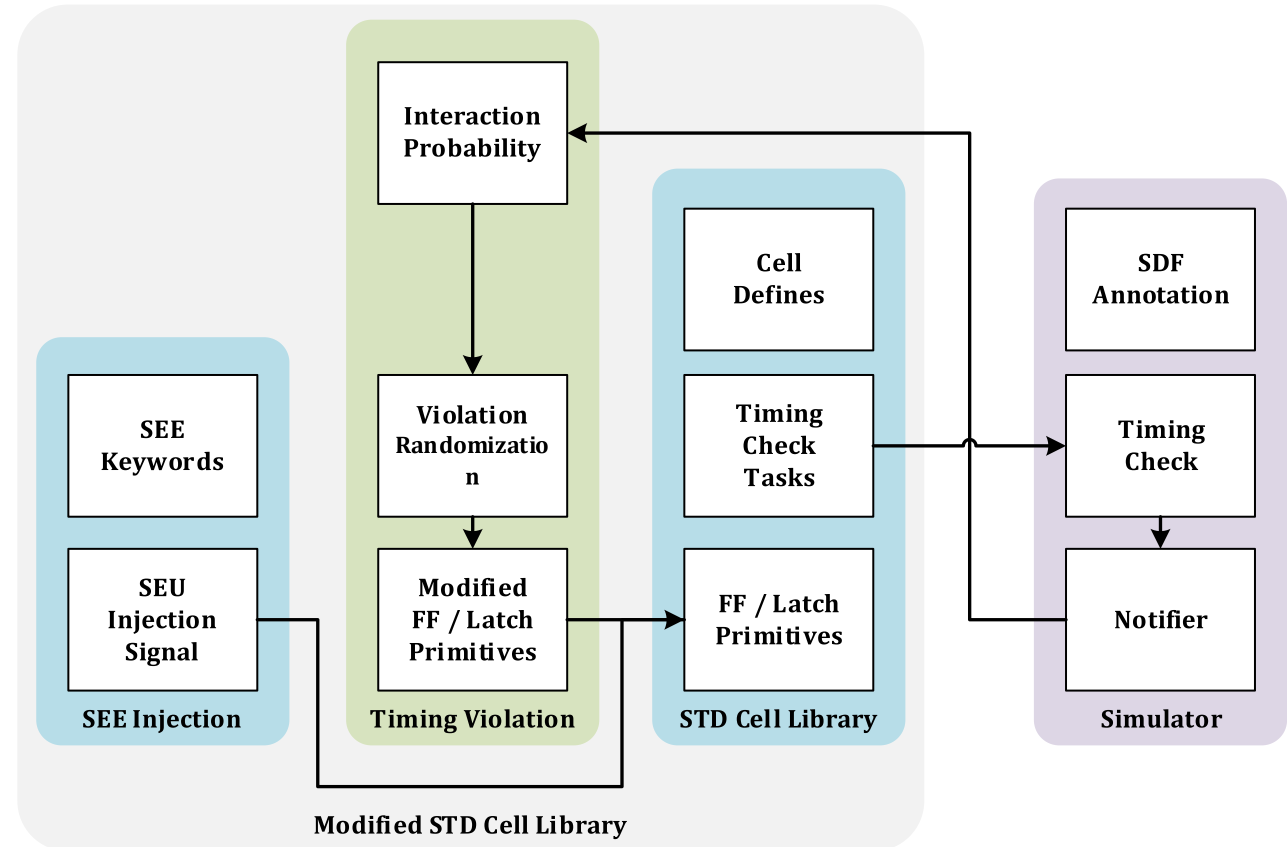
SET in comb. logic (setup / hold violation), output randomized



SET in clock-tree (setup / hold / width violation)

Standard Cell Library Instrumentation

- Timing violation propagation instrumentation:
  - Replicate real-world behavior of cell
  - Separate probability calculation for
    - Setup / Hold
    - Width (clock)
  - Randomized output
  - Modified primitives required



- SEE Injection instrumentation:
  - Introduction of Keyword
  - Detected by node extraction step of framework
  - SEU: Additional signal for inverting the stored value
  - Original STD cell primitives may be reused

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SRAM Macro Cell Instrumentation

- SRAM macros handled differently than standard cells
  - Depending on SRAM Cells used, location information not available
  - Interleaving architecture, the bits in a data word are not physically adjacent
  - Multiple-bit upset (MBU) distribution can be used
    - Randomized distribution across multiple bits & multiple words

- Typical foundry HDL SRAM models assume worst case
  - Read operations are generally not critical regarding internal state
  - Write operation to unknown address invalidates entire memory

- Foundry SRAM models modified to replicate real-world behavior
- Timing violation handling
  - Control Signals: Assume random operation
  - Address: Assume single randomized address
  - Data input: Store randomized word

Data (01011)
Address: x

x	x	x	x	x
x	x	x	x	x
x	x	x	x	x
x	x	x	x	x
x	x	x	x	x

Default foundry SRAM model

Data (01011)
Address: x

0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	0	1	1
0	0	0	0	0

Modified foundry SRAM model

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STRV-R1 SEU Contributing Sources

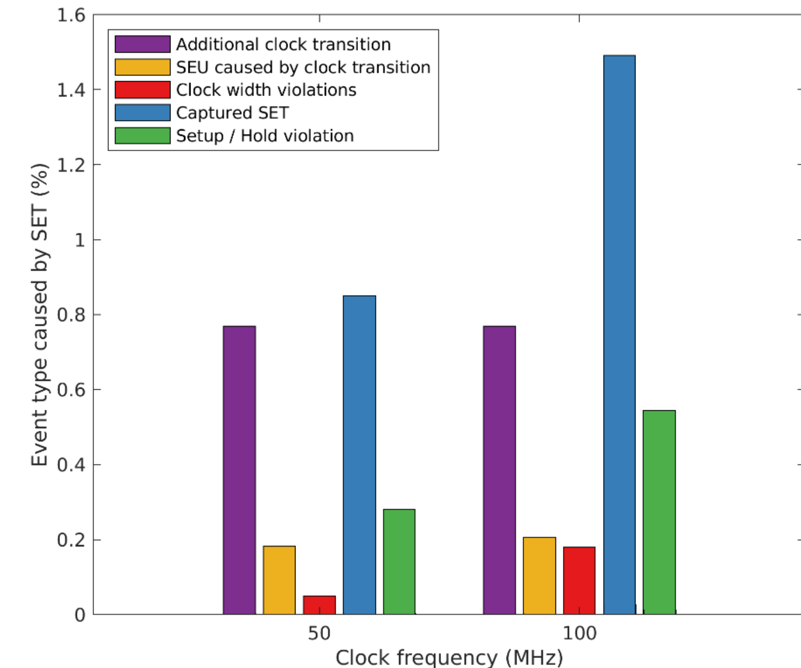
- **Apart from direct hits, data in sequential elements can be modified by:**

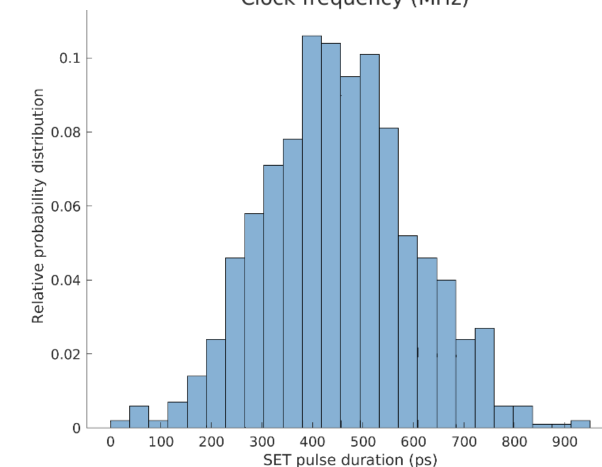
- SETs in clock buffers / inverter of the clock tree
  - Depending on the level in the clock tree large number of leafs affected
  - Additional clock pulses inserted
- Additional clock pulses can be masked by inactive / static data path
  - Static data paths common in general purpose circuits such as RISC-V core

- Clock pulse timing width violation in sequential logic
  - Sequential element may not store new state
  - Reduced impact compared to SET in clock signals

- Capture of SET in data path
  - Masked by combinational logic and application-specific state
  - Setup-Hold violations can mask impact of SET

- Simulation constraints for simulating additional contributing SEU sources:
  - Dhrystone Benchmark executed by RISC-V core
  - SETs equally distributed across clock cycle
  - Shown randomized distribution of SET pulse duration used

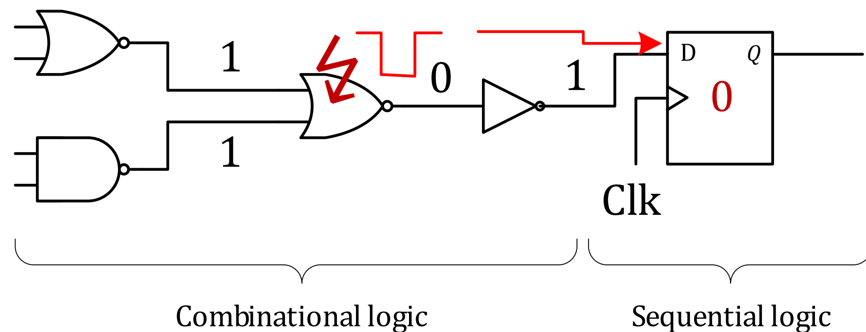


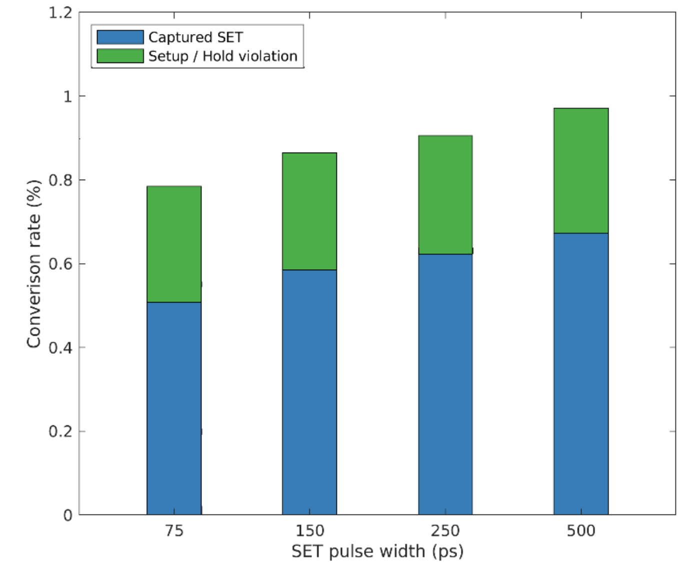


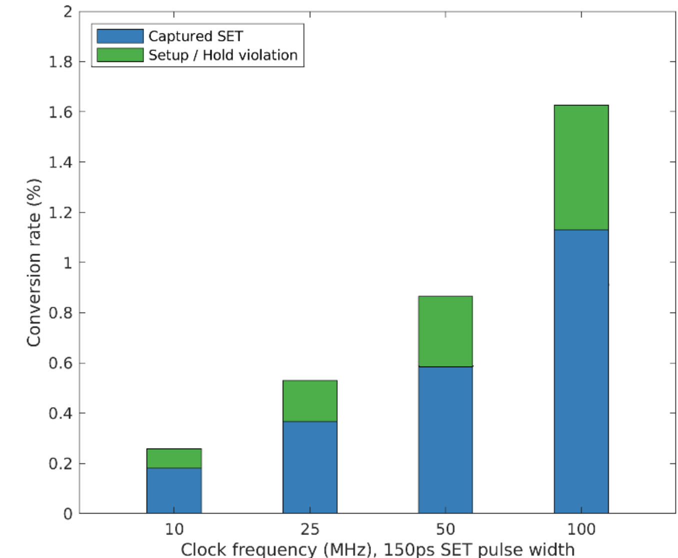
SET Capture in sequential logic

- Single Event Transients captured by endpoint sequential Logic
- Cone of logic as input to sequential Logic
  - Dissipation during propagation through design
  - Elongation during propagation through design
  - Masking via other combinational logic

- Application-specific designs contain a significantly number of masked data paths
  - SET capture rate in specific test structure is higher
- Simulation constraints for SETs in data paths:
  - Different application software executed
  - SETs equally distributed across clock cycle







Summary | Conclusion

- **Heavy-Ion irradiation results**
  - Effective SEU cross-section is larger than in test-structures for sequential elements
  - TMR protection scheme in RISC-V core achieves up to 8000x improvement
  - Residual error rate remains, SEFIs present
  - Second irradiation, SRAM individually analyzed
    - Despite SRAM triplication and SRAM, errors present in data stored in SRAM
    - Errors present without RISC-V core activity, cause in SRAM itself, not RISC-V core

- **SEE-Injection simulation framework has been developed**
  - Designed to replicate the real-world impact of SEE
  - Intended for simulations using synthesis or place and route netlists
  - Ability to incorporate physical placement information
    - Simulation of multiple concurrent SEEs