High frequency DC/DC converters for powering of future pixel detectors

Verbundmeeting

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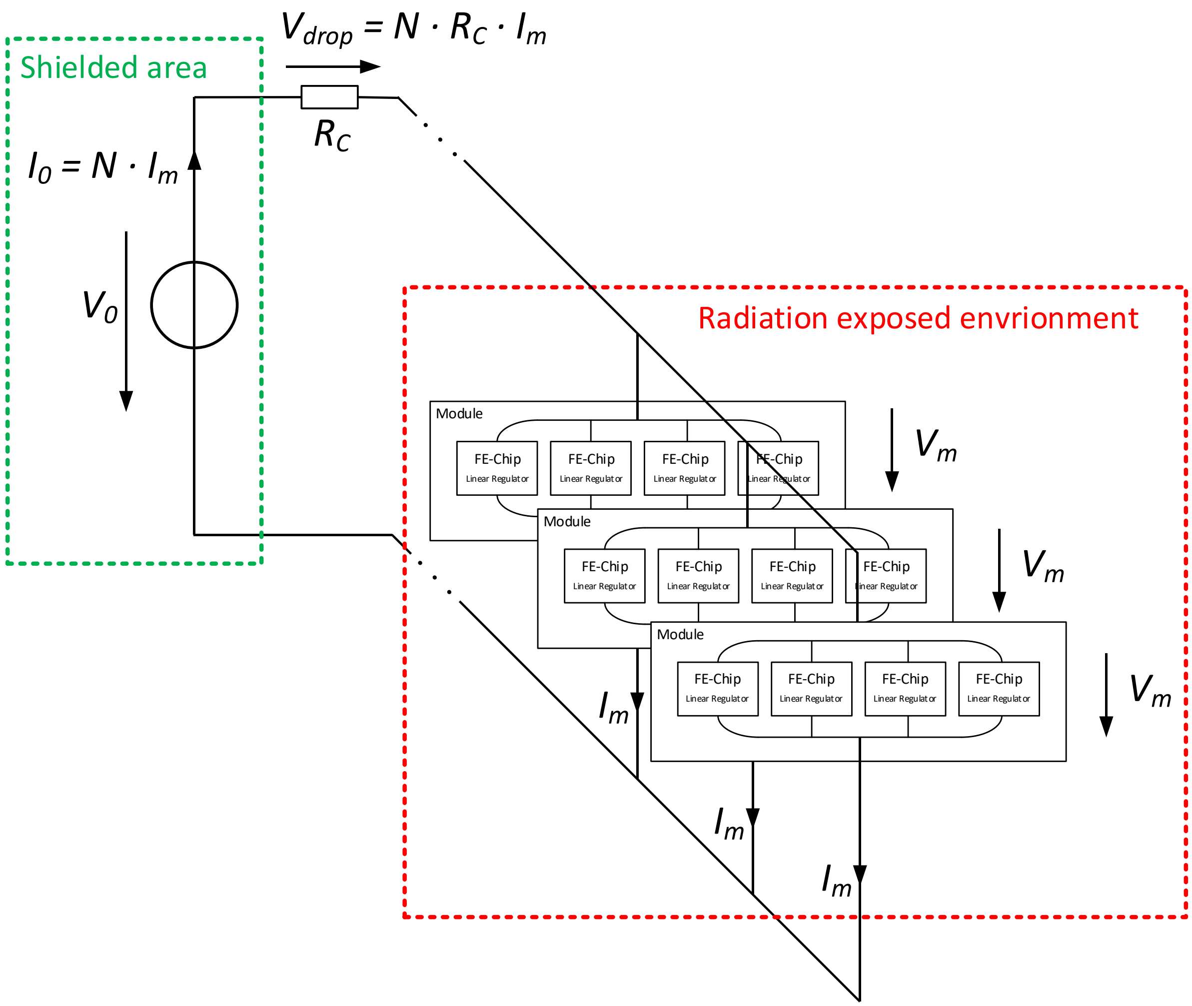
Introduction

- The pixel detector for the high luminosity upgrade is renewed
  - To keep the hit rate per pixel area constant, the area of the individual pixels is reduced and the **number of pixels within the detector is increased**
    - This requires more readout channels, resulting in higher power consumption
- Due to highly radiates environment, high magnetic fields and low temperatures, the DC **power supply is located in a shielded area**
  - The power is supplied to the modules via **long supply lines** (several 100 meters)
- In the actual power approach the **supply efficiency is only 20 %**
  - A higher power consumption in the upcoming upgrade would further decrease efficiency

→ New powering approaches are investigated to improve the overall efficiency while keeping the material budget low

Actual Powering Concepts



- N modules connected in parallel
- Modules are powered with a constant supply voltage V_0
- Supply current I_0 scales with number of modules N
- Efficiency:

$$\eta = \frac{1}{1 + N\frac{R_C \cdot I_m}{V_m}}$$

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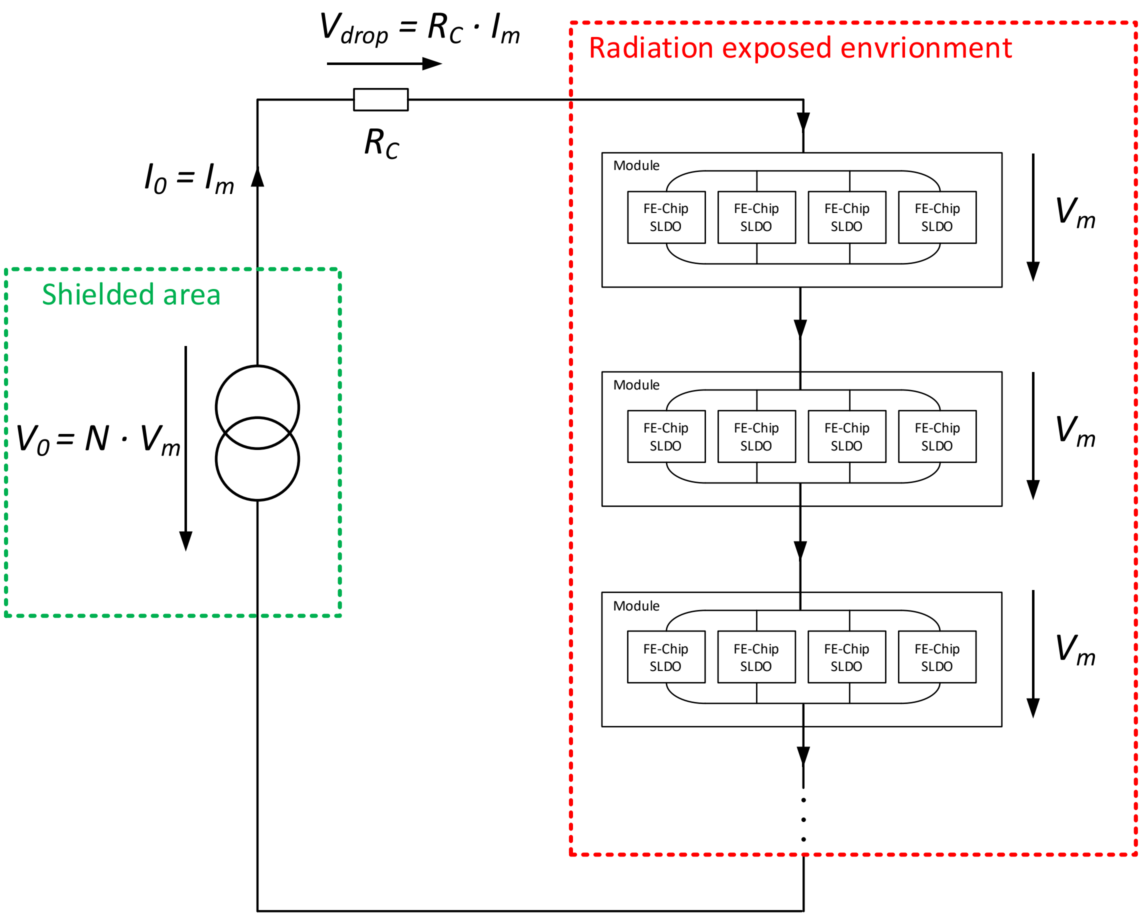
IMPROVED POWERING CONCEPTS

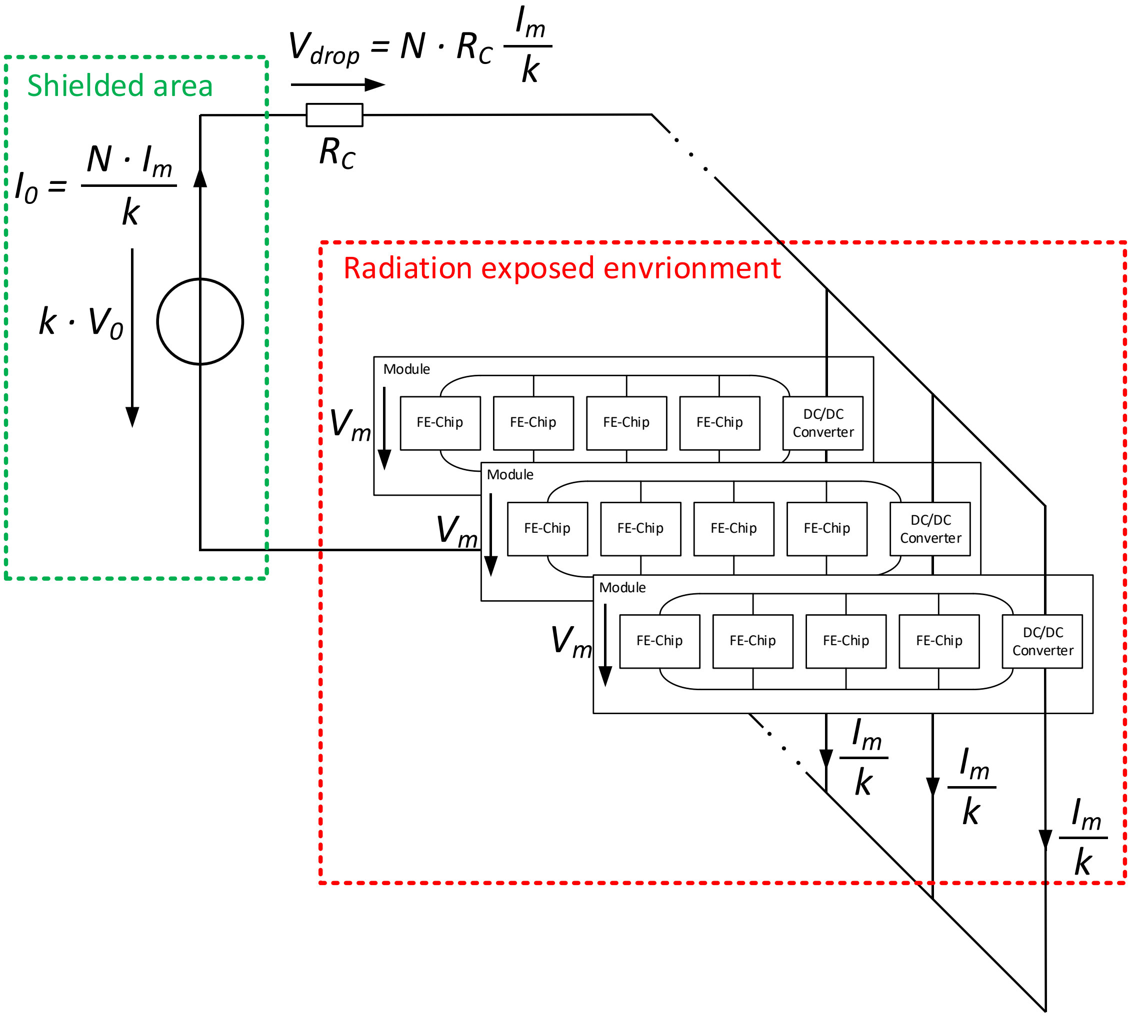
Serial Powering



- *N* modules connected in series
- Modules are powered by a constant current source
- **Supply current is determined by maximum load current of a module**
- Supply voltage scales with number of modules
- Special regulator (Shunt-LDO) required to convert the supply current into a voltage
  - Ensures redundant operation

$$\eta = \frac{1}{1 + \frac{R_C \cdot I_m}{\boldsymbol{N} \cdot V_m}}$$

Parallel Powering with DC/DC conversion



- N Modules connected in parallel
- **Power is distributed with a k times higher supply voltage**
- Supply voltage is stepped down by a factor of k in close proximity to the modules by DC/DC conversion
- Supply current scales with number of modules N and is reduced by a factor of k
- **Requires a radiation hard DC/DC converter with high power density**

$$\eta = \frac{1}{1 + \frac{N}{\boldsymbol{k^2}} \frac{R_C \cdot I_m}{V_m}}$$

Requirements for the voltage regulators in the innermost detector layers

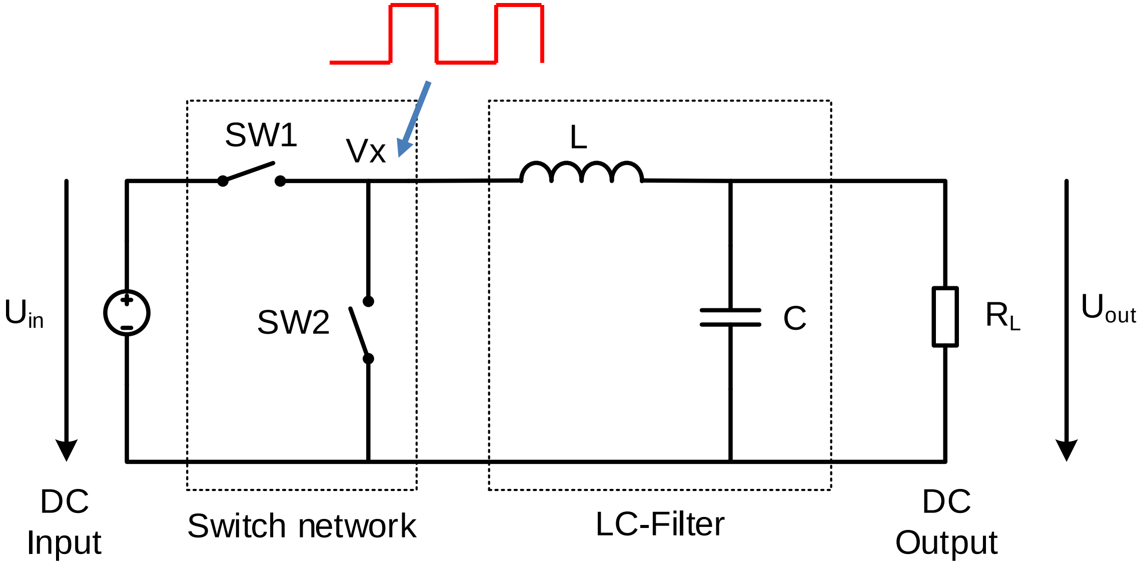
- **Challenges:**
  - The electronic in the innermost detector layer must withstand a radiation **dose of up to 1 Gigarad** over lifetime
  - **Limited space** within the detector
  - **Additional material inside the detectors must be avoided**, otherwise the quality of the measurement data will deteriorate
  - High magnetic fields of up to **2 Tesla**
- **Realization:**
  - Entire circuit is designed with **thin-gate oxide** core transistors (65 nm CMOS)
    - Transistors are **less affected by irradiation** due to the thin gate oxide
    - Nominal voltage rating is limited (1.2 V)
  - To improve the supply efficiency, a **high conversion factor of 4** is chosen for the DC/DC converter (Conversion factor: Vin/Vout)
    - Thick gate oxides Transistors are typically used to handle high voltages

    → Requires device stacking for the power stage
  - Ferromagnetic material for inductive components **saturate** due to the high magnetic field
    - Inductive elements are used as air coils (higher volume compared to coils with ferromagnetic cores)

    → High switching frequency of 100 MHz

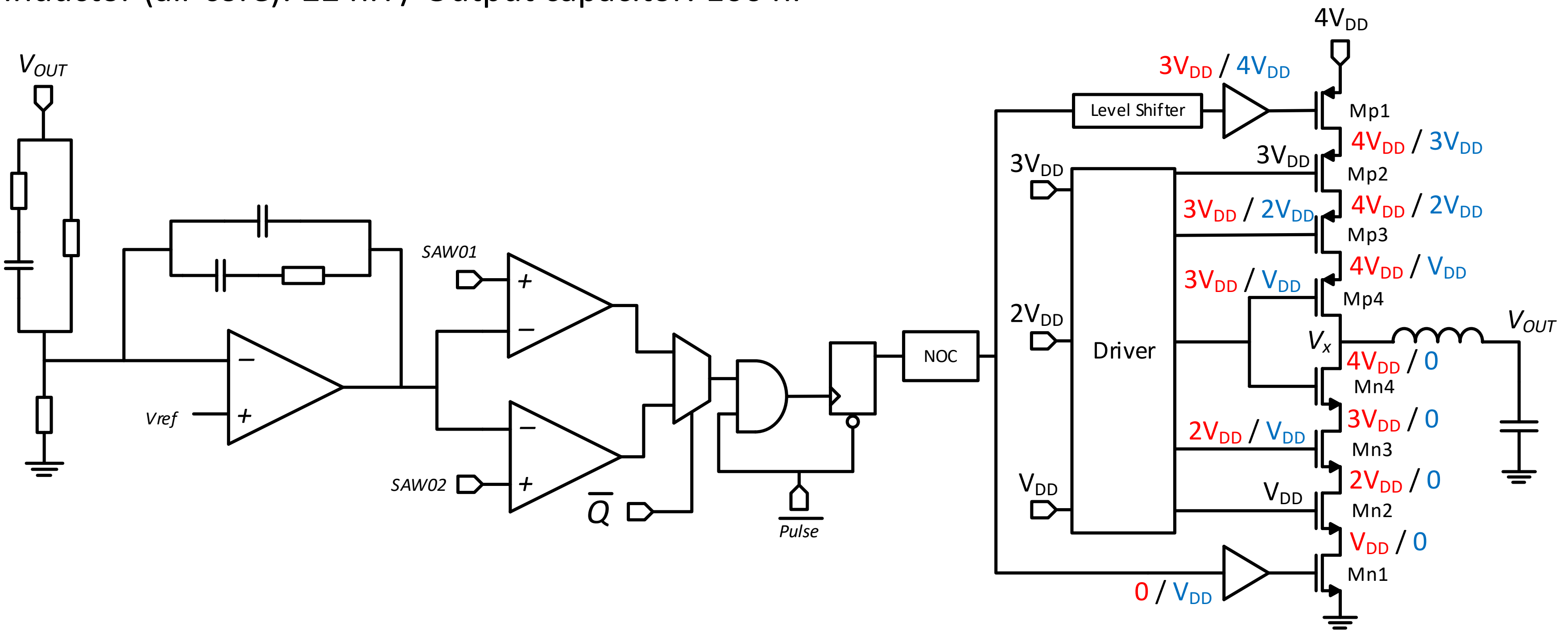
DC/DC converter basics

- The DC/DC converter is based on a classical step-down topology
- Switches are controlled by PWM voltage mode control
  - Control signal for switches SW1 and SW2 is adjusted to set the output voltage to the desired voltage level
  - Duty Cycle: $D = \frac{V_{out}}{V_{in}} = \frac{t_{on}}{T_{sw}}$
- Design of the passive components:
- $L = \frac{(V_{in} - V_{out})}{\Delta i_L \cdot f_{sw}} \cdot \frac{V_{out}}{V_{in}}$
- $C = \frac{\Delta i_L}{8 \cdot f_{sw} \cdot \Delta V_{out}}$



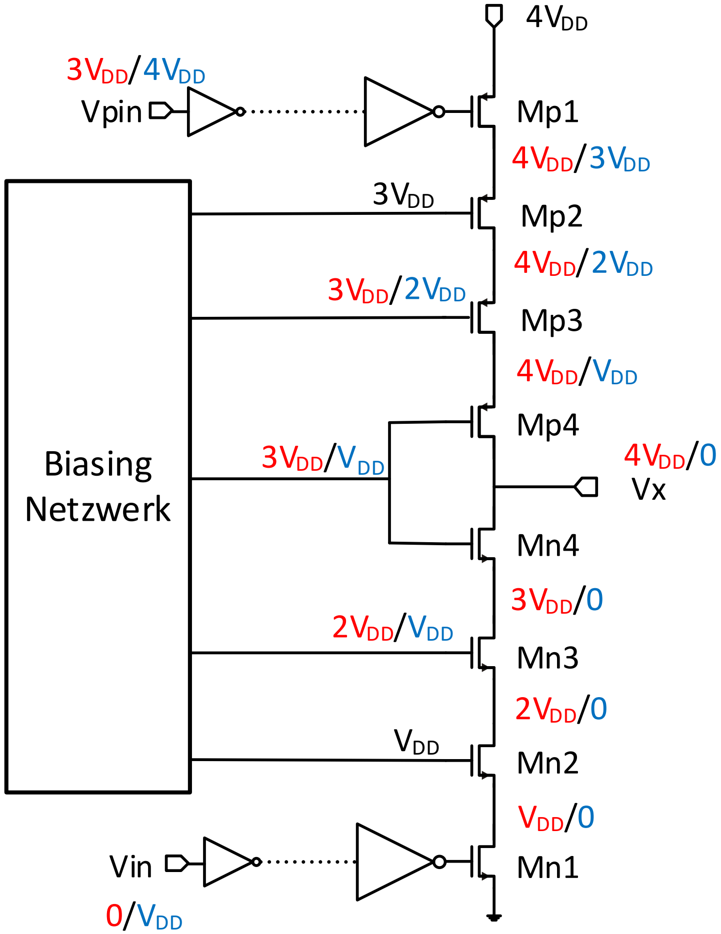
Circuit diagram of the DC/DC converter

- Entire circuit is designed with thin gate oxide transistors (65 nm CMOS)
  - Power stage is designed with 4 NMOS and 4 PMOS transistors in series
  - Enables the supply with an input voltage that is four times higher than the nominal voltage V_{DD} of the transistors (Vin = 4.8 V)
- Output voltage = 1.2 V (voltage conversion factor k = 4) / Max. load current: 1 A
- Switching frequency: 100 MHz
- Inductor (air core): 22 nH / Output capacitor: 100 nF



Device stacking for the power stage (switching network)

- Device stacking at the high-side and low-side domain enables the operation with a 4 times higher input voltage (4 VDD)
  - The input voltage is distributed evenly across the stacked transistors
- During normal operation there a 2 switching phases (**HIGH** and **LOW)**
  - High-state: PMOS transistors are conductive
  - Low-state: NMOS transistors are conductive
  - It has to be ensured, that the transistors operate within their voltage limits!
  - Driver network guarantees that the required gate voltage is applied to the transistor gates
    - Depending on the switching state
    - The additional network monitors the drain voltages of the stacked transistors and provides the required gate voltage based on the drain voltage sensed

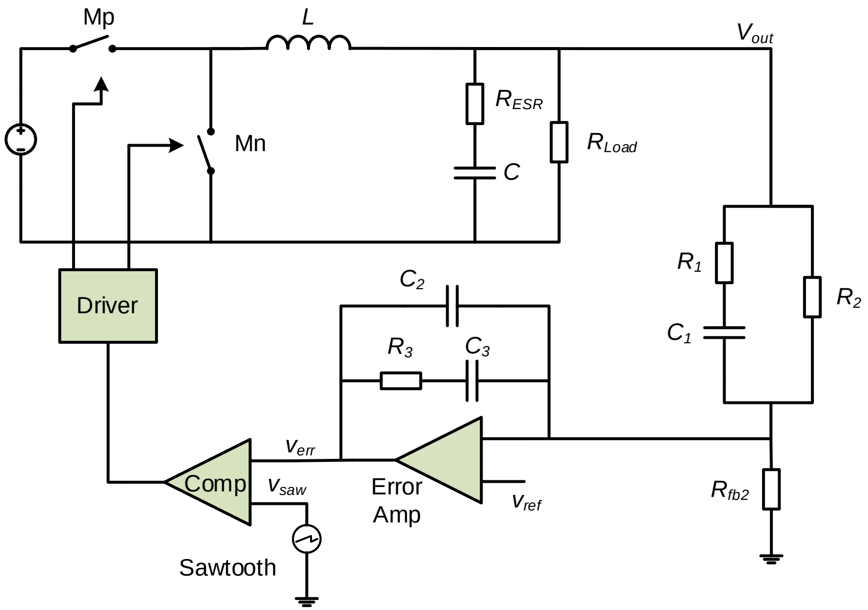


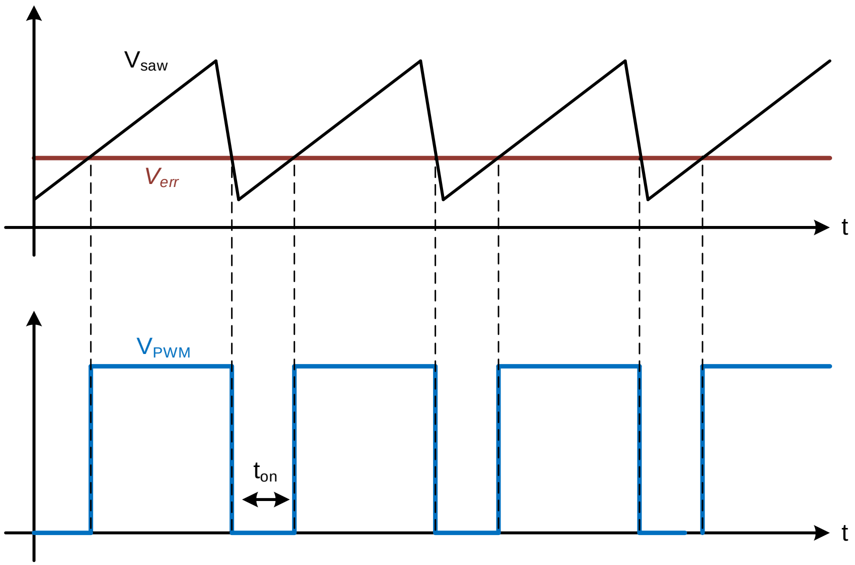
Control System

- The control system provides the signal to control the switching time of the power stage transistors
  - To keep the output voltage to the desired level
  - Guarantees a high immunity against load and input disturbances
- Regulation is based on a voltage mode Pulse Width Modulation (PWM) control
  - The duty cycle (on-time of the high side switch) is regulated while the pulse duration (switching frequency) remains constant
  - A high duty cycle enables a higher power flow to the load and therefore a higher output voltage
- Several measures have been implemented to guarantee a stable operation at high switching frequencies
  - To prevent faulty switching and system failures

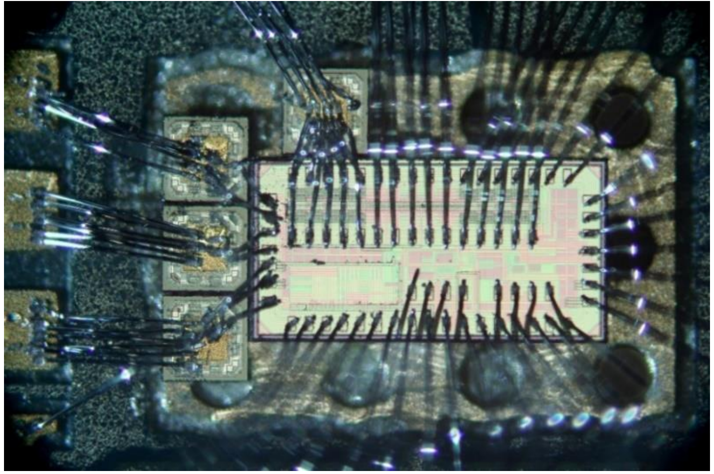
Control System

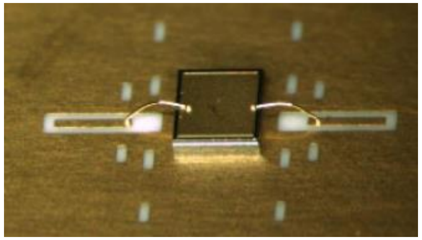
- Simplified schematic for the voltage mode PWM control
  - Output voltage is sensed by feedback mechanism
  - Error amplifier output V_{err} is compared to a sawtooth (ramp) V_{saw} signal
  - Comparators output the control signal for the power stage transistors
  - Switching frequency is defined by means of the sawtooth generator
- $V_{out} = 2\ V_{ref}$

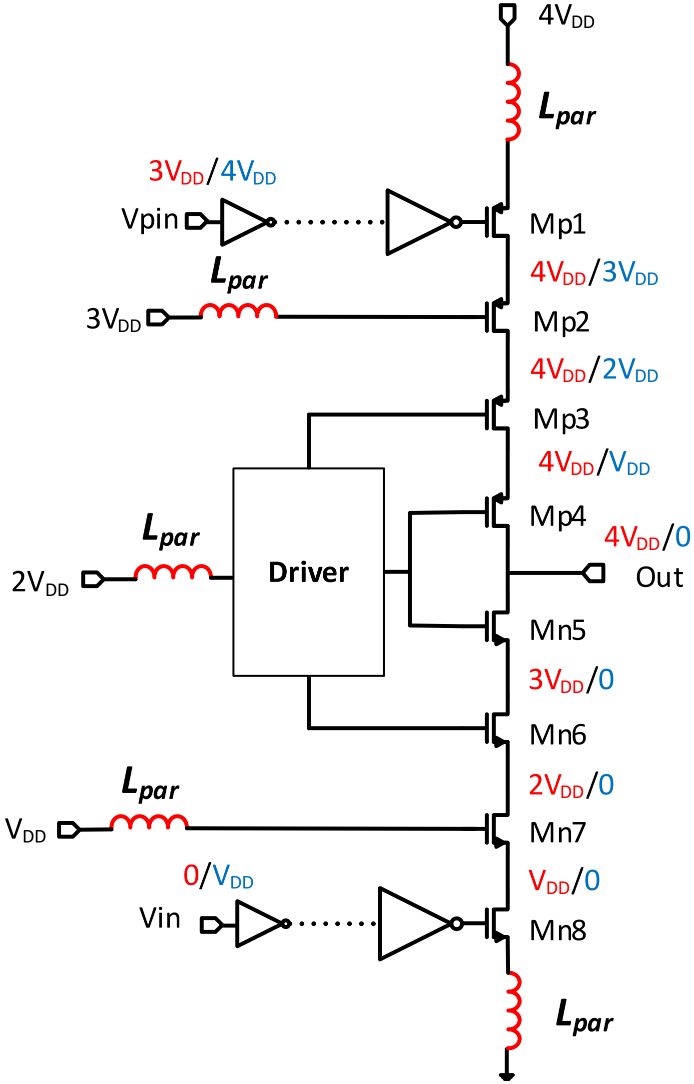




Overview Testchips



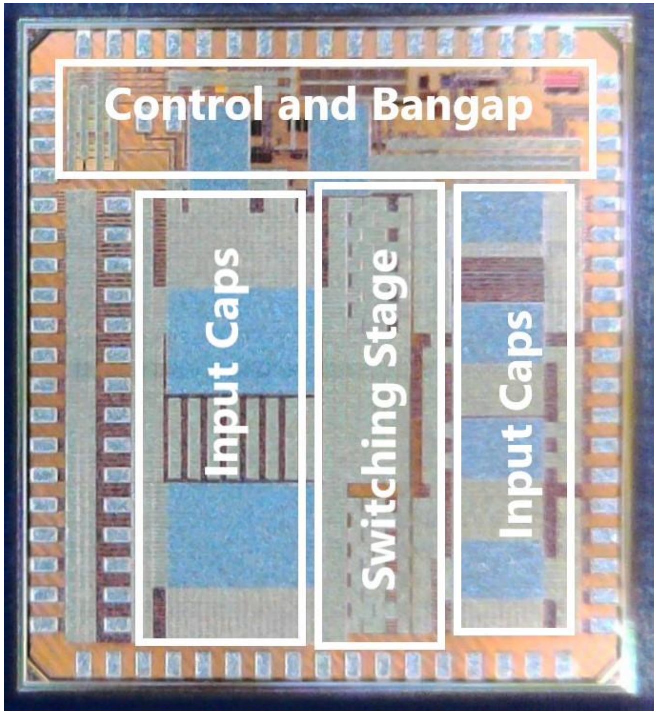




- Submitted July 2022
- Chip area: 1 mm x 2 mm
- 65 nm Technology (core transistors)
- A high di/dt leads to voltage overshoots at the input terminal due to the parasitic inductances (bond wire and PCB)
  - Faulty switching were observed
- Bondable silicon capacitors (Murata) were implemented
  - Decoupling Capacitor close to the Chip
  - Bondwire length is reduced

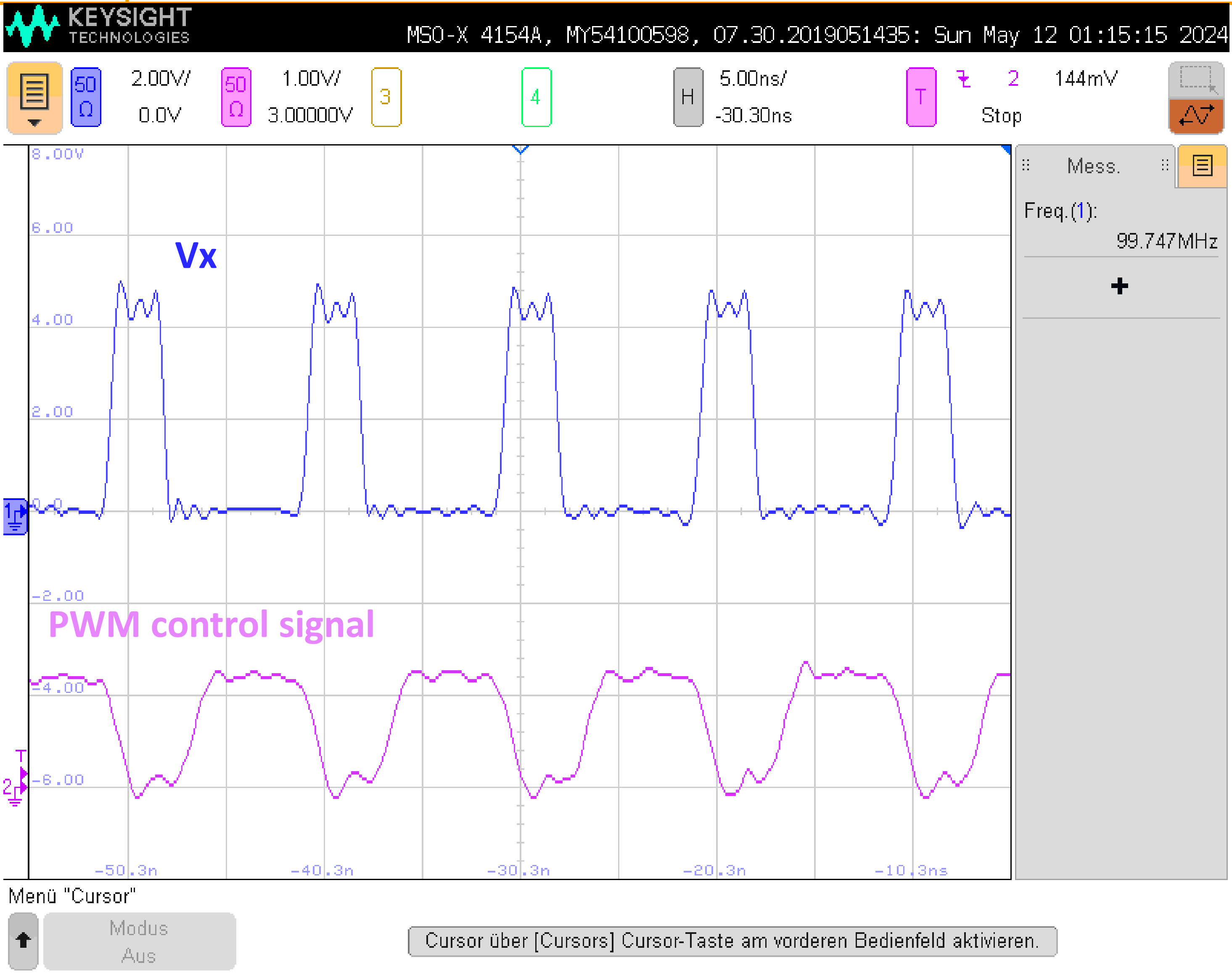
Overview Testchips

- Submitted May 2023
- Chip area: 2 mm x 2.2 mm
- Large on-chip decoupling capacitors are integrated
  - Necessary to reduce ΔV_{in}
- Several tests were performed which have confirmed the functionality and reliability:
  - Line and Load Regulation (< 1%)
  - Transient Response (< 2µs)
  - Efficiency (70%)
  - Temperature Sweep between -60 to +60°C



MEASUREMENTS

Transient Measurements

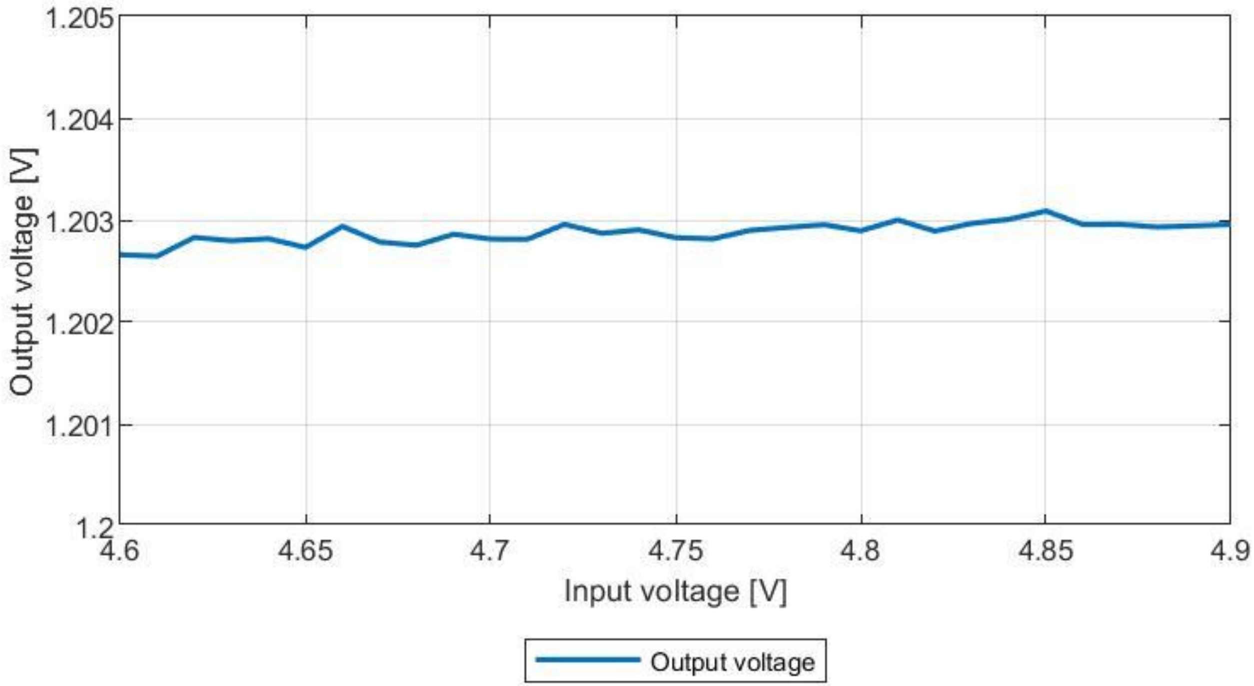


MSO-X 4154A, MY54100598, 07.30.2019051435: Sun May 12 01:15:15 2024

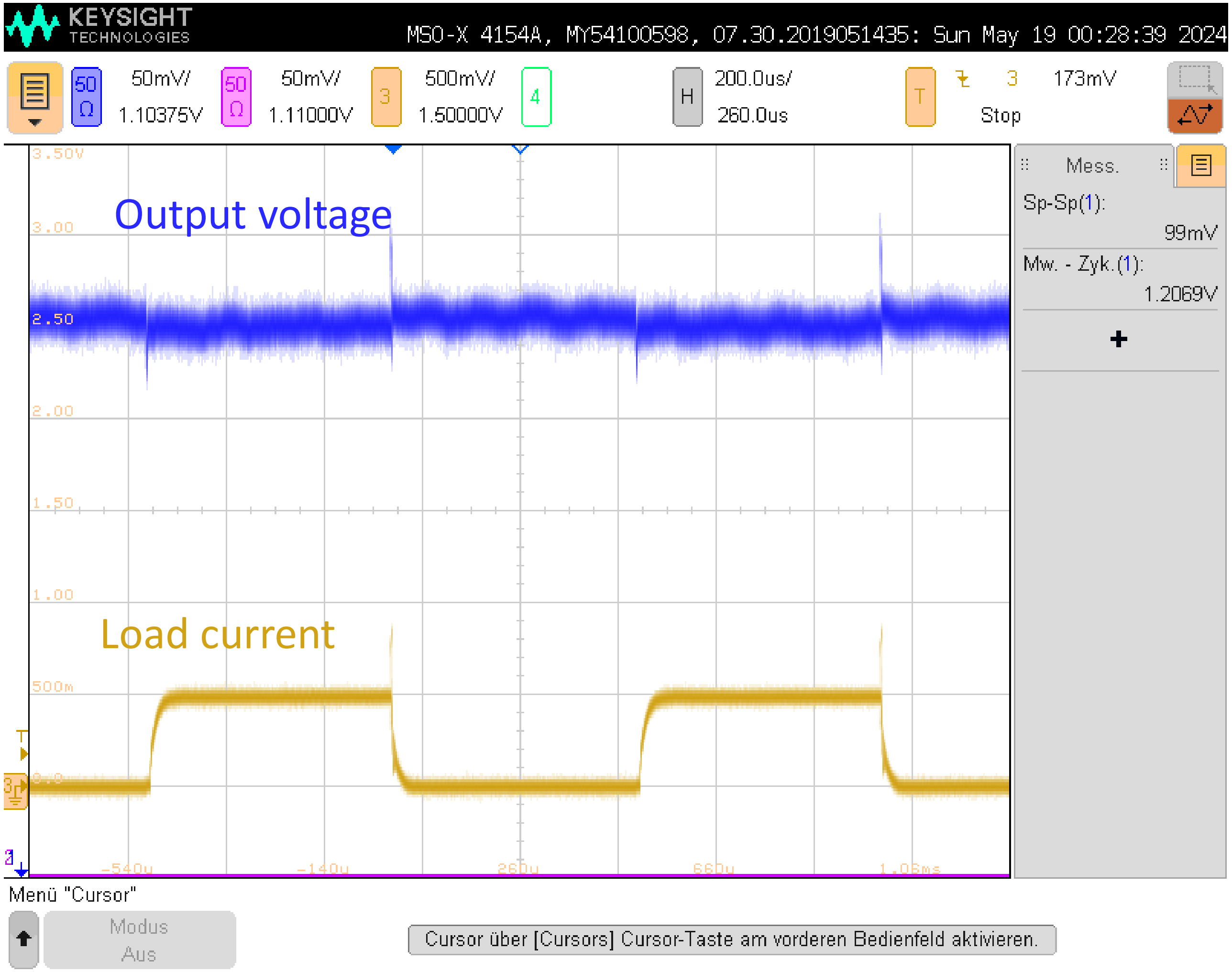
Freq.(1): 99.747MHz

Cursor über [Cursors] Cursor-Taste am vorderen Bedienfeld aktivieren.

Line Regulation



Transient Load Steps



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50 Ω 50mV/ 1.10375V

50 Ω 50mV/ 1.11000V

3 500mV/ 1.50000V

4

H 200.0us/ 260.0us

T 3 173mV Stop

Sp-Sp(1): 99mV

Mw. - Zyk.(1): 1.2069V

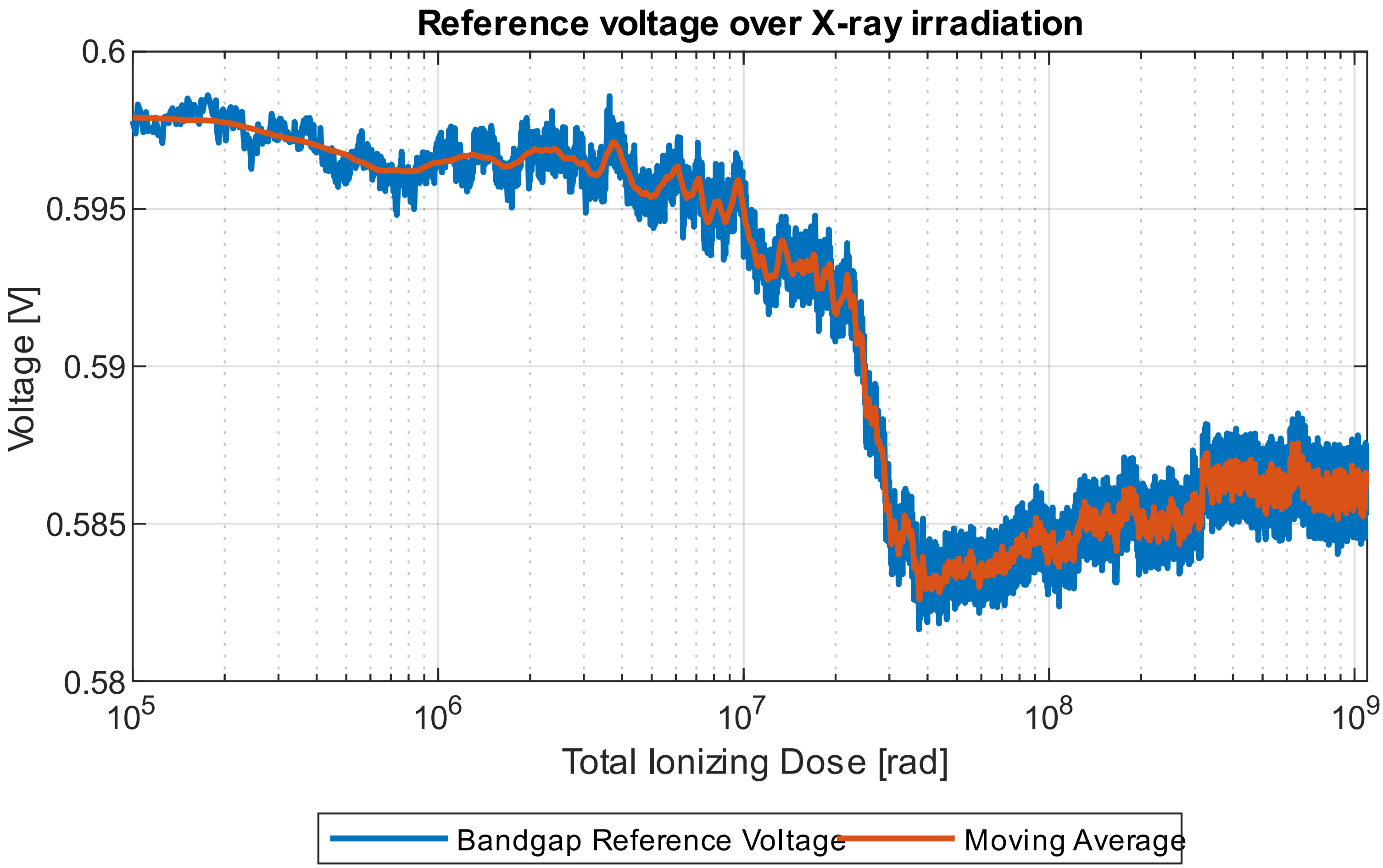
Cursor über [Cursors] Cursor-Taste am vorderen Bedienfeld aktivieren.

Settling time = 2µs

Irradiation Campaign

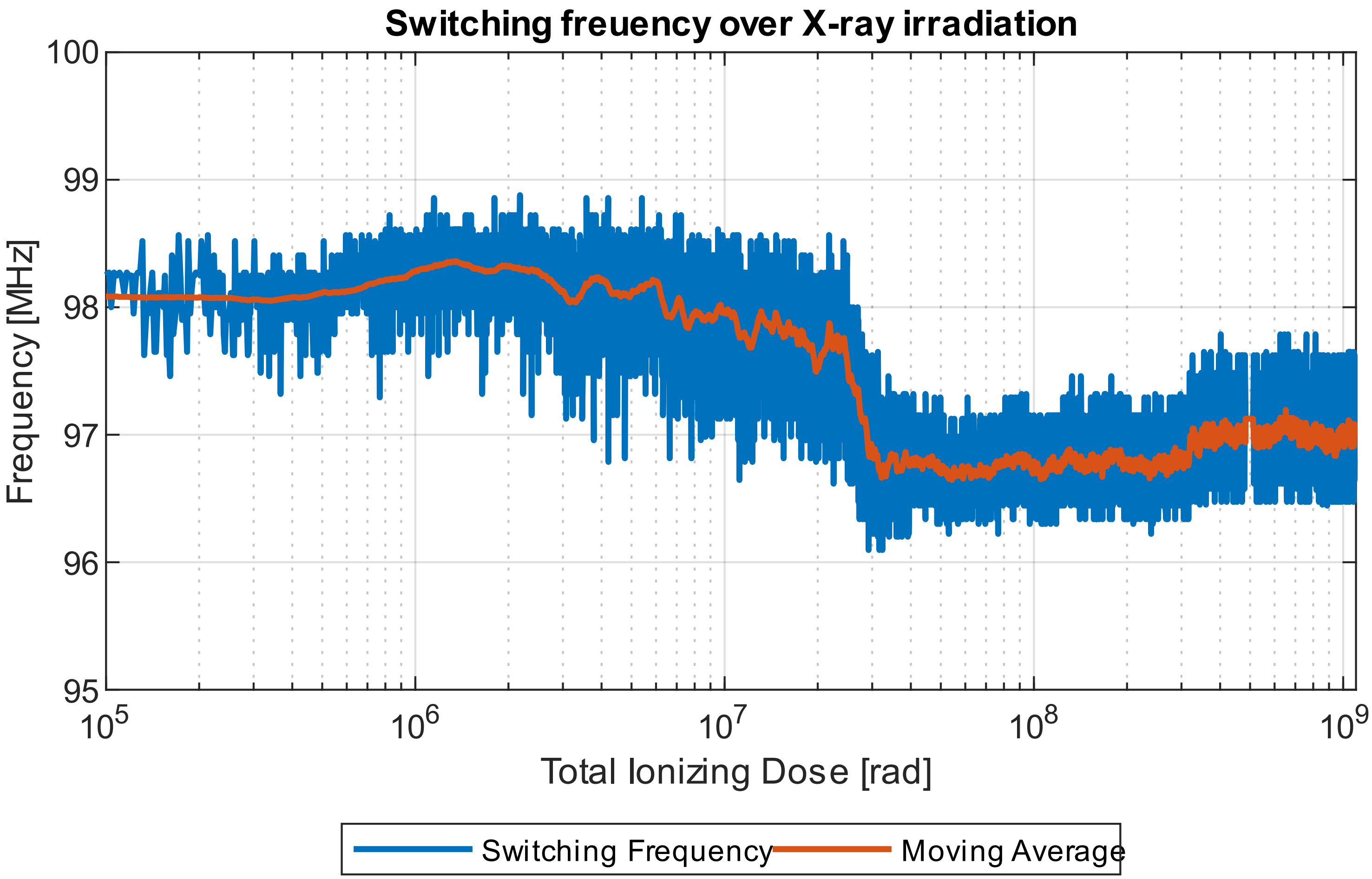
- Total Ionizing Dose (TID) tests performed at the Physics Department of the University of Bonn
- Tests were performed at a low temperature of -15°C
- Prototype irradiated with a dose rate of 2 Mrad/h
  - 3 weeks running time to achieve the radiation dose of 1 Gigarad
- Measured Variables:
  - Output voltage
  - Switching Frequency
  - Bandgap Reference Voltage
  - Efficiency

Bandgap reference voltage as function of TID



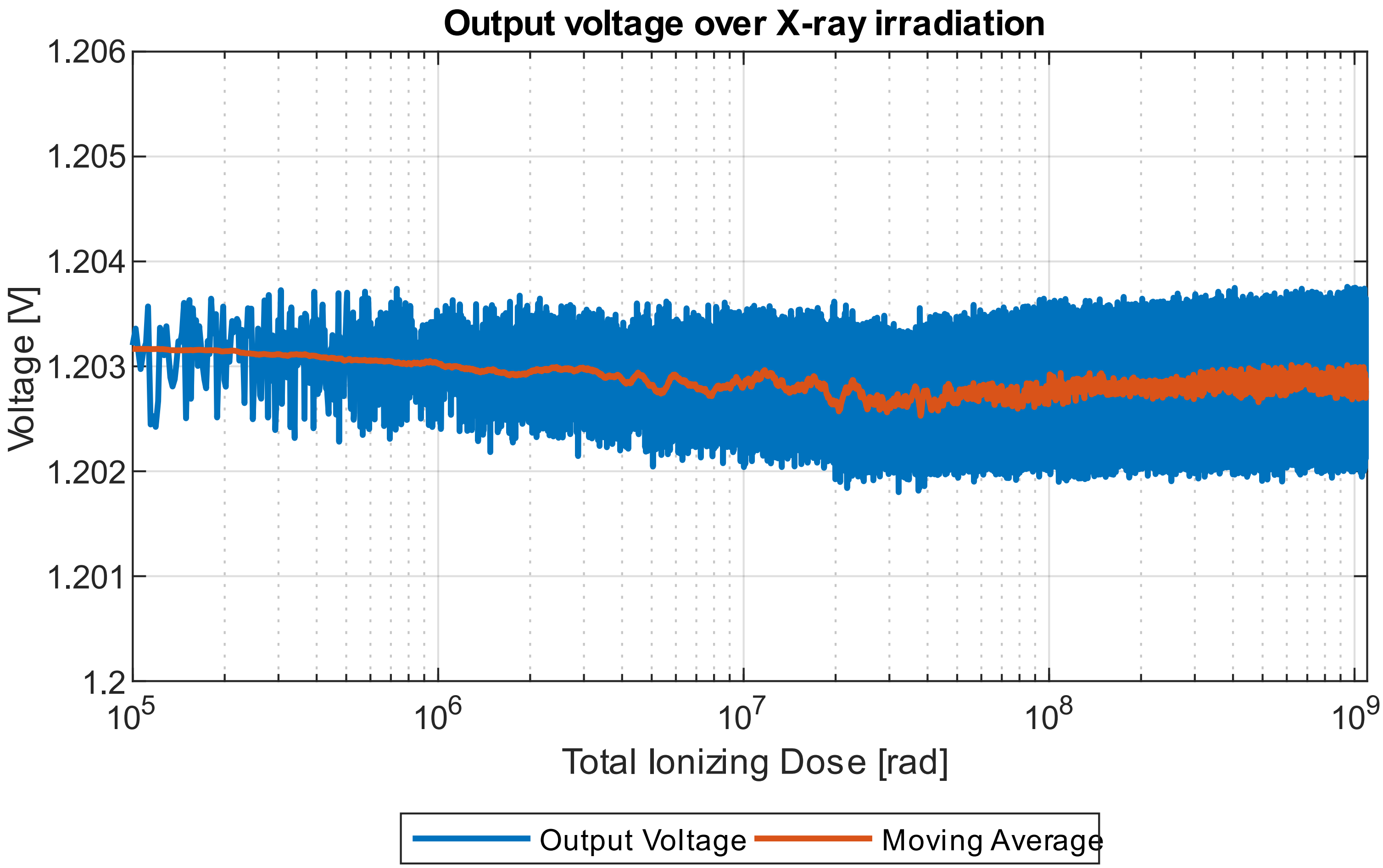
$$\Delta V_{ref} = 17.3\ mV$$

Switching frequency as function of TID



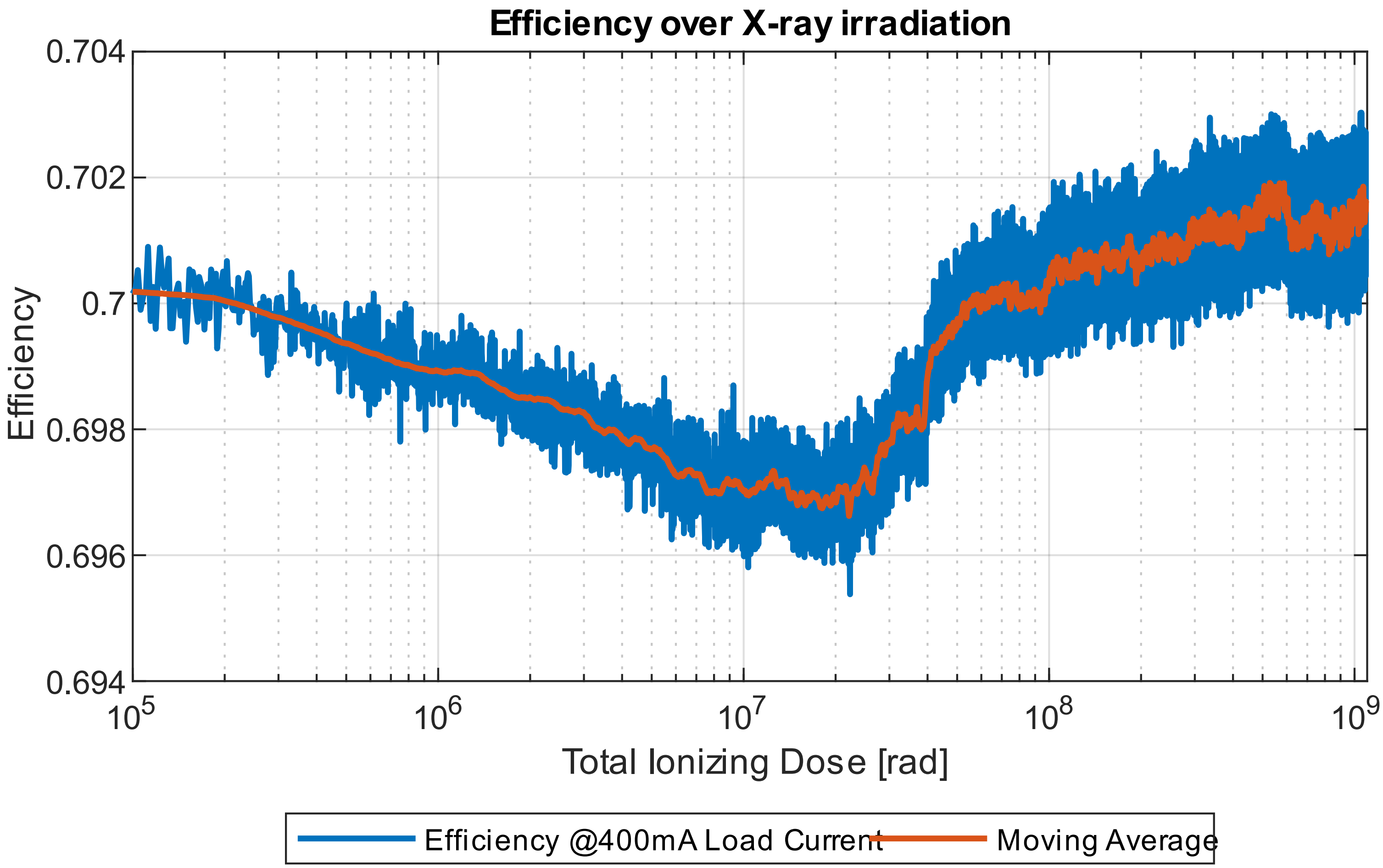
$$\Delta F_{sw} = 2.8\ MHz$$

Output voltage as function of TID



$$\Delta V_{out} = 2.1\ mV$$

Efficiency as function of TID



$$\Delta Efficiency = 0.77\ \%$$

Summary irradiation results

	Percentage change
ΔV_{ref}	2.88%
ΔF_{sw}	2.8%
ΔV_{out}	0.18%
$\Delta \mathrm{Eff}$	0.77%

Conclusion

- The DC/DC converter is designed for powering readout electronics in the innermost pixel detector layers
- Core transistors were stacked in the power stage
  - Allows the operation at high voltages and ultra high TID rates
- High switching frequencies are necessary to keep the passive components small
  - L = 22 nH
  - C = 100 nF
- Measurements have shown the reliability of the designed prototype
- TID investigations confirm the radiation hardness up to 1 Gigarad