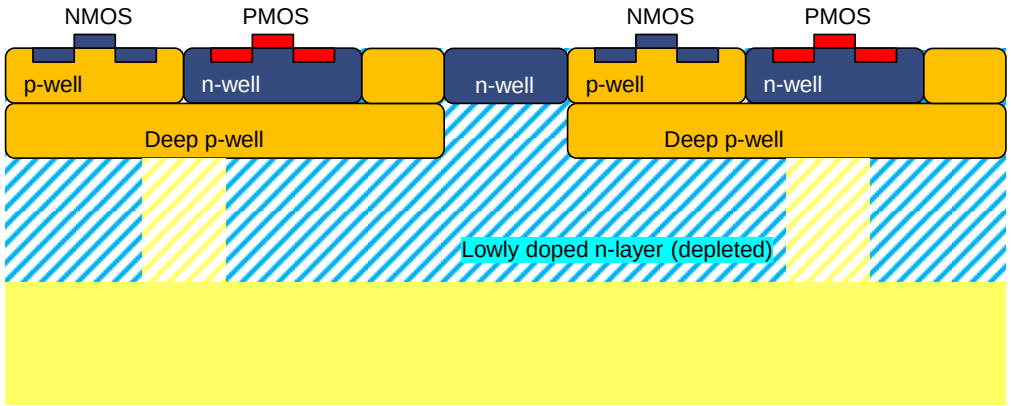
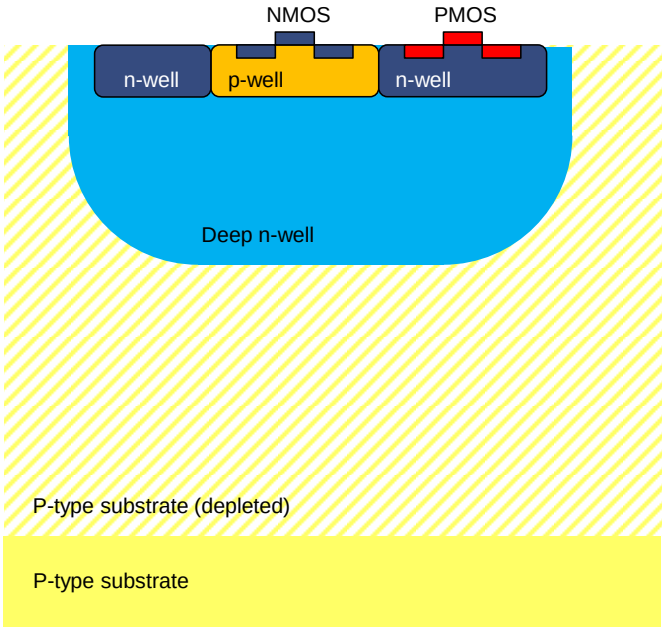
HV-MAPS developments at KIT

Ivan Peric

- Monolithic sensors for particle physics
- Third funding period
- Three monolithic structures were mostly used: MAPS with small charge collection electrode (InMAPS), HV-MAPS or HVCMOS sensors with large collection electrode. SOI sensors are the third technology
- Within this project we are designing the HVCMOS sensors



InMAPS with small charge collection electrode

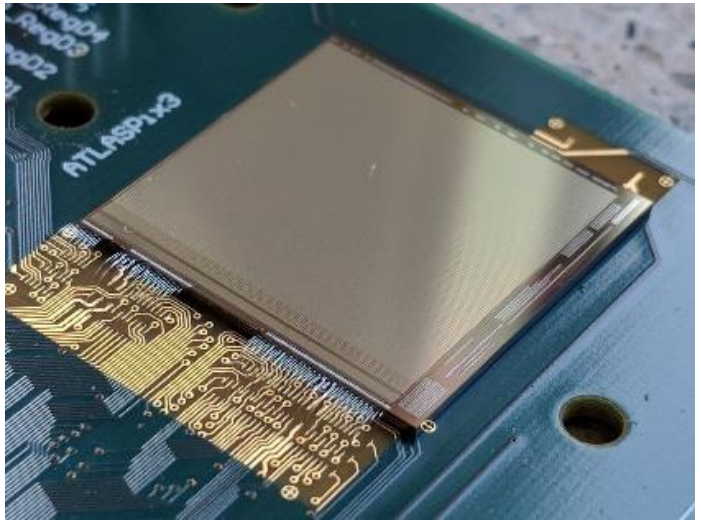


In the case of HVCMOS, the sensor diode is a deep n-well in p-substrate. Electronics is embedded inside n-well

Technologies

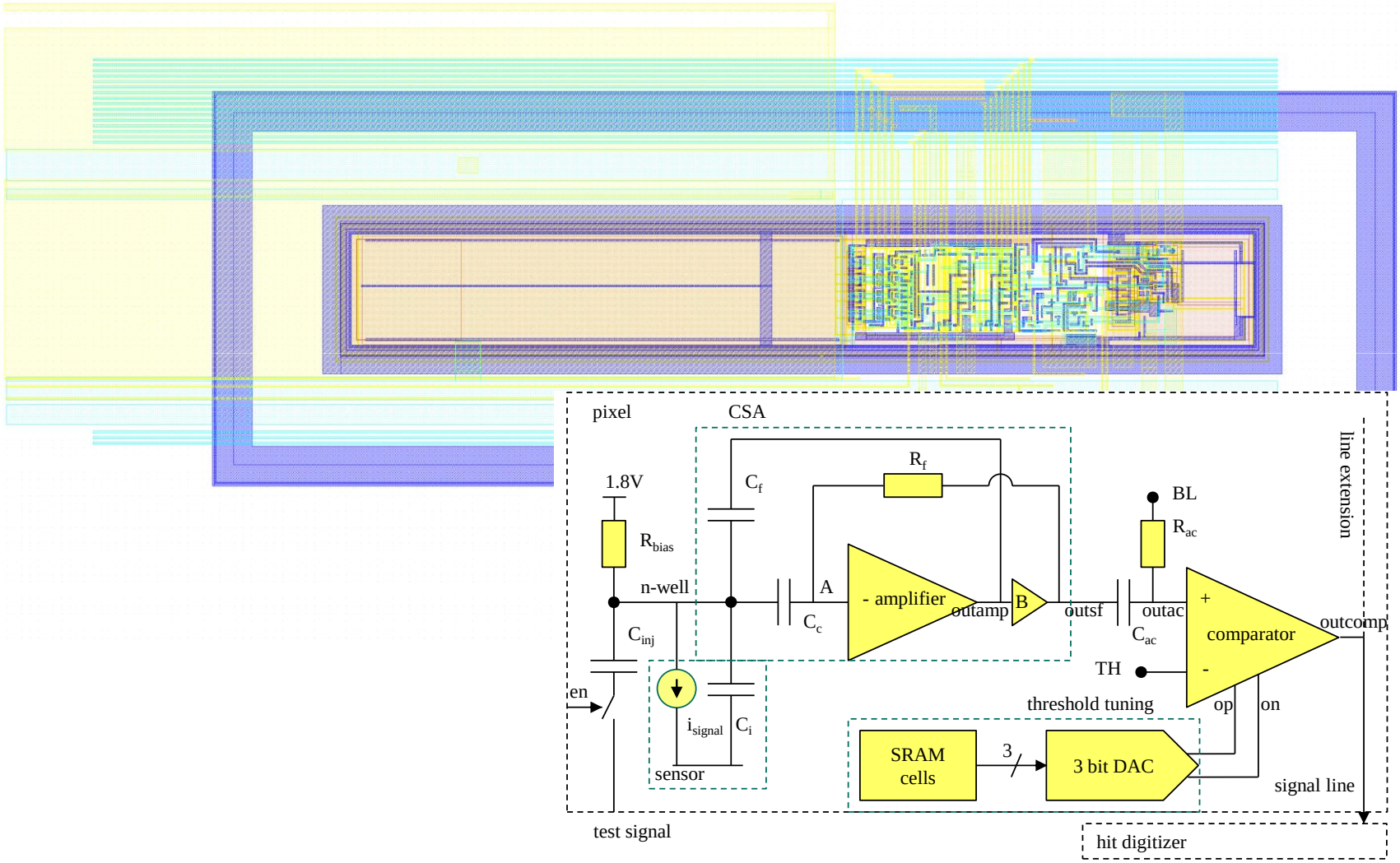
- HVCMOS sensors can be implemented in almost every CMOS process
- The sensor properties depend on substrate resistivity, substrate type (epi- or uniform), breakdown voltage between the deep n-well and substrate
- The most of our sensors have been implemented in hv7sf 180nm HVCMOS technology
  - In past offered by IBM, AMS and TSI, presently only supplier AMS
- 130nm SiGe BiCMOS process of IHP
- High speed HBTs with transit frequency >300GHz. Very fast circuits can be implemented
- HVCMOS sensors can benefit from these transistors. The rise time of the signal at the amplifier output depends on transistor transconductance. HBT can achieve larger transconductance for equal bias current as MOSFETs
- IHP is ready to add process modifications. High resistivity and epi-layer wafers can be used. LGAD structure has been successfully implemented in the IHP process. Deep p-well possible

- AtlasPix3 - the first reticle size HVCMOS sensor in 180nm HVCMOS technology
- High resistivity substrates of 300Ωcm
- Pixels of 50µm x 150µm
- Chip size 2.2 cm x 2.0 cm, matrix size 19.8 mm x 18.6 (132 x 372)

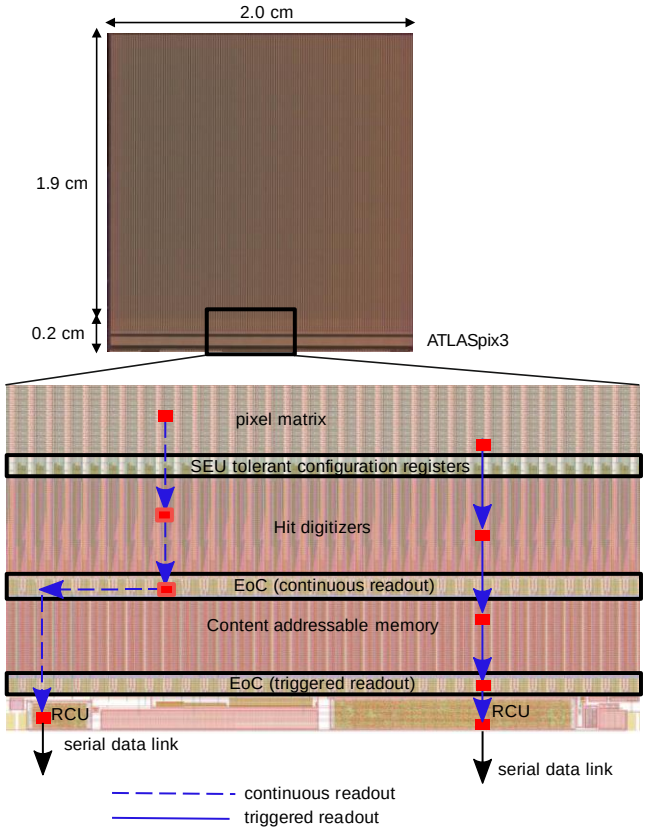


Pixel Layout (AtlasPix3)

- Pixels contain amplifiers and comparator with threshold tune circuit

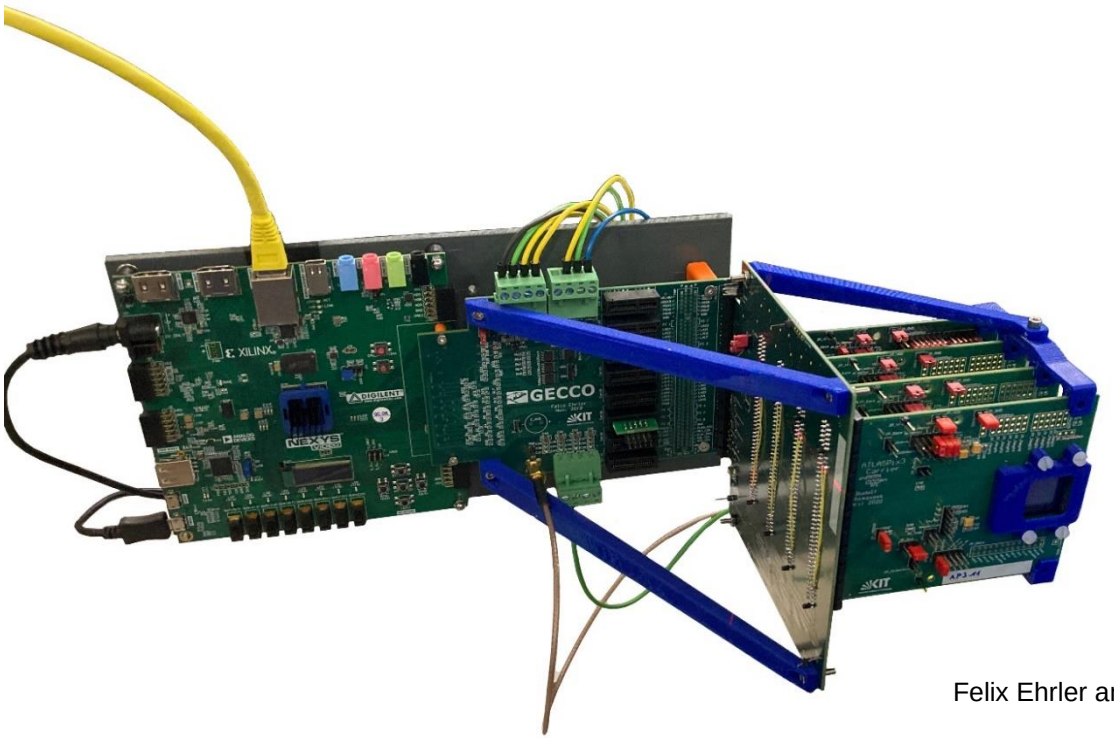


- Triggered and untriggered (continuous) readout



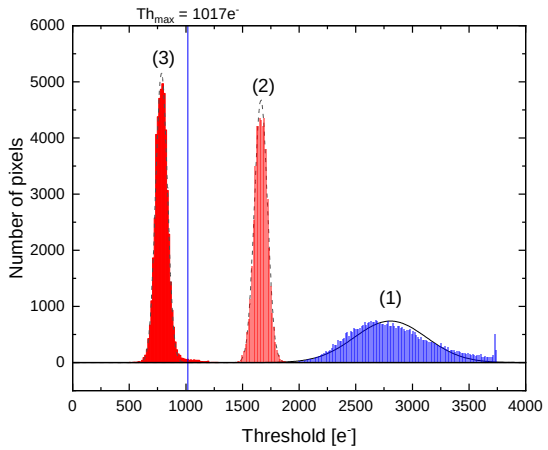
I. Peric et al, High-Voltage CMOS Active Pixel Sensor, IEEE Journal of Solid-State Circuits (Volume: 56, Issue: 8, Aug. 2021) https://doi.org/10.1109/JSSC.2021.3061760

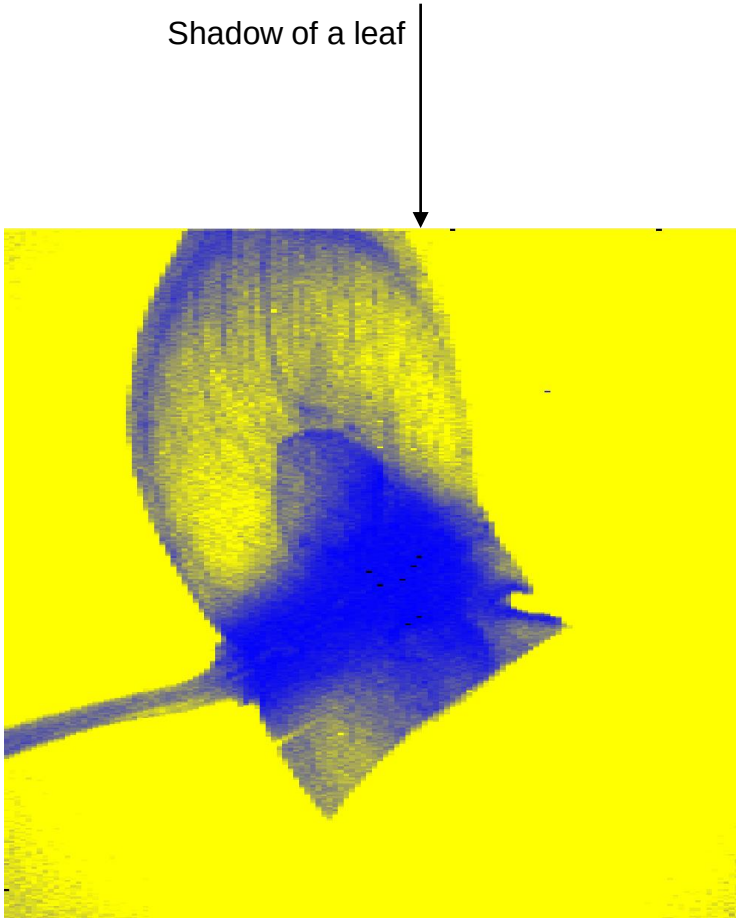
- For AtlasPix and other sensors, have developed a modular test system called Gecco that is based of several PCBs, commercial FPGA board and self-made software a firmware. The test system can be used for single chip tests and as beam telescope



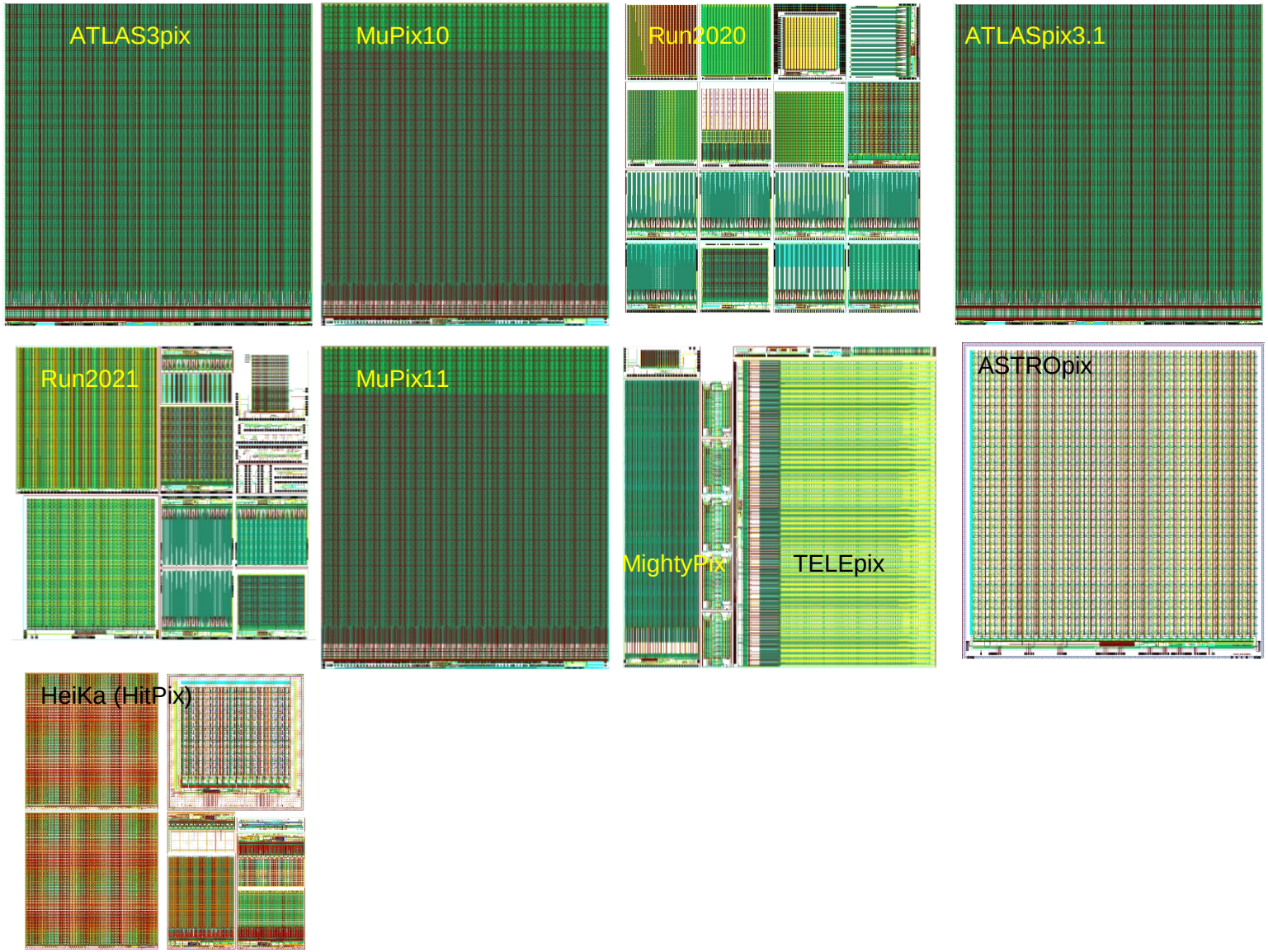
Felix Ehrler and Rudolf Schimassek

- Some results at KIT
- Threshold can be tuned to 800e, threshold dispersion 60e, noise around 70e
- Example: ^{55}Fe source measurement

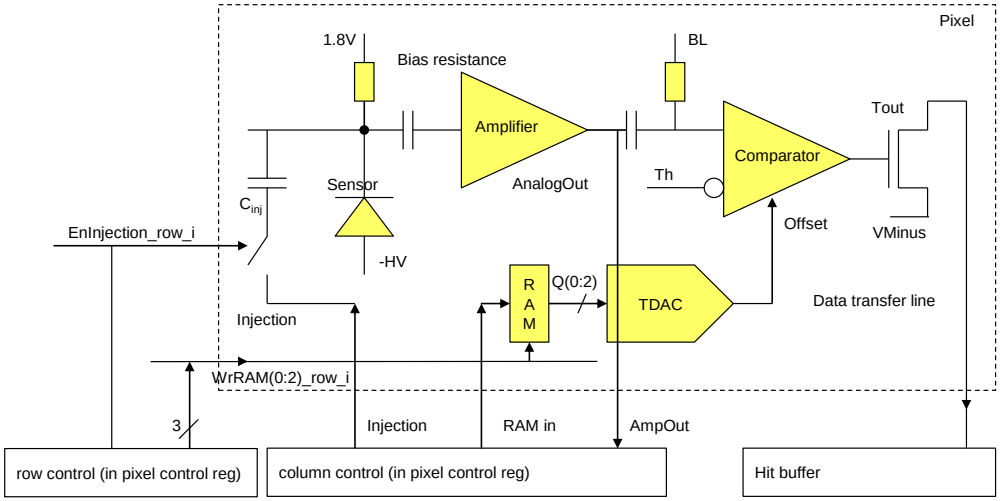


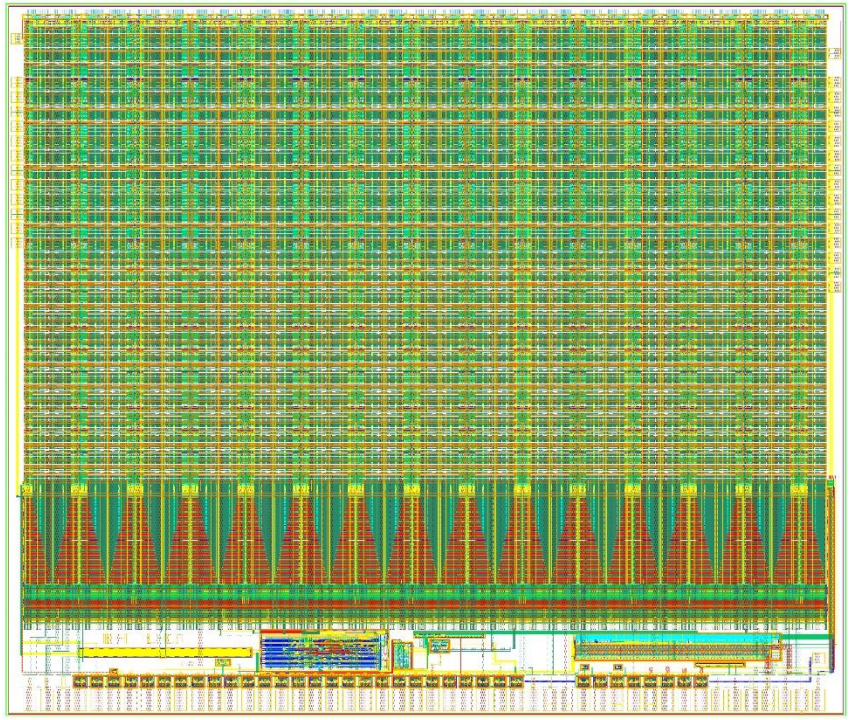


Engineering runs (2019-2023)



- Generic sensor structure

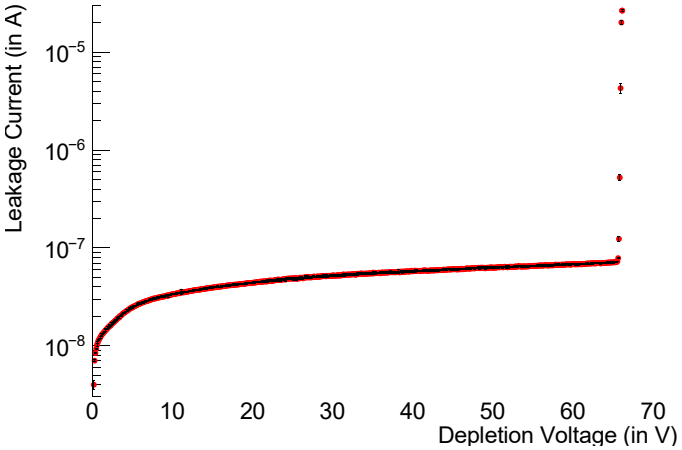


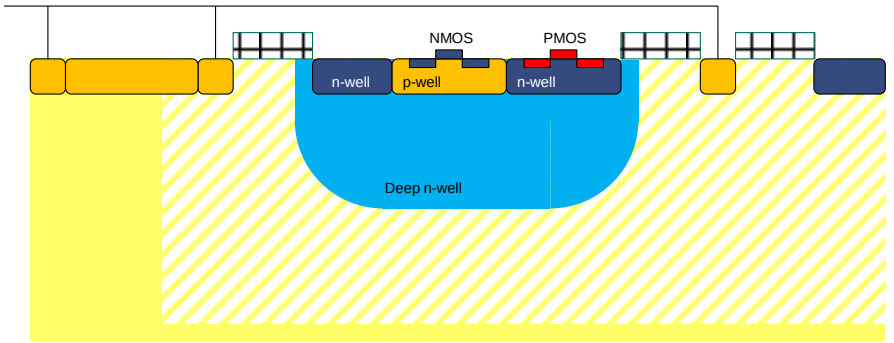


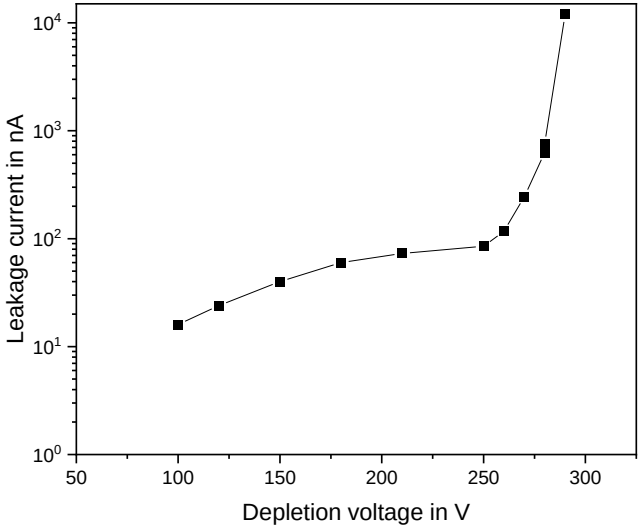
TECHNOLOGY IMPROVEMENTS

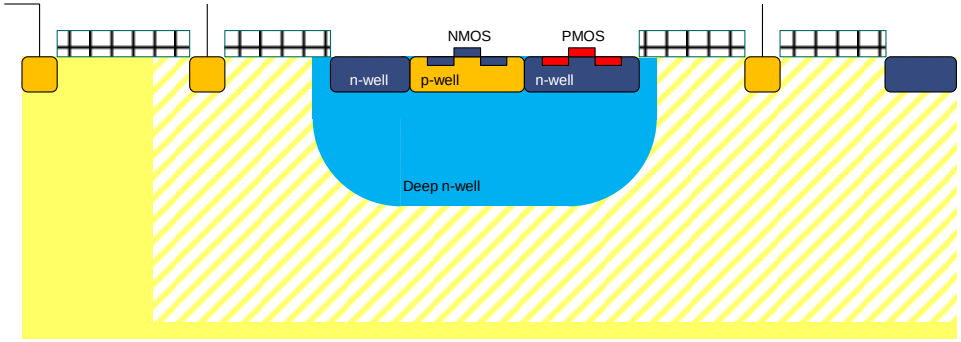
Breakdown voltage

- Breakdown from ~65V to > 200V





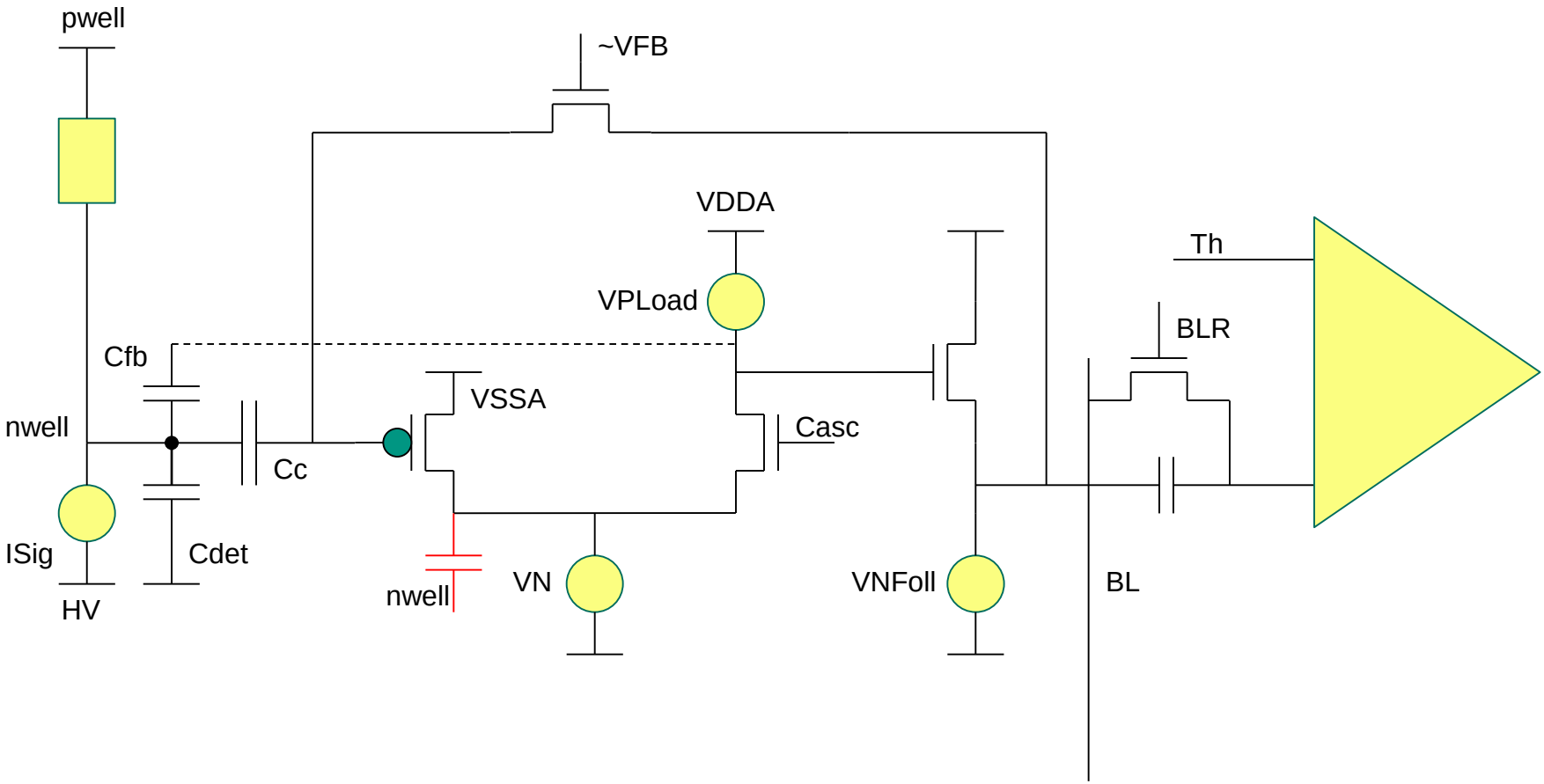




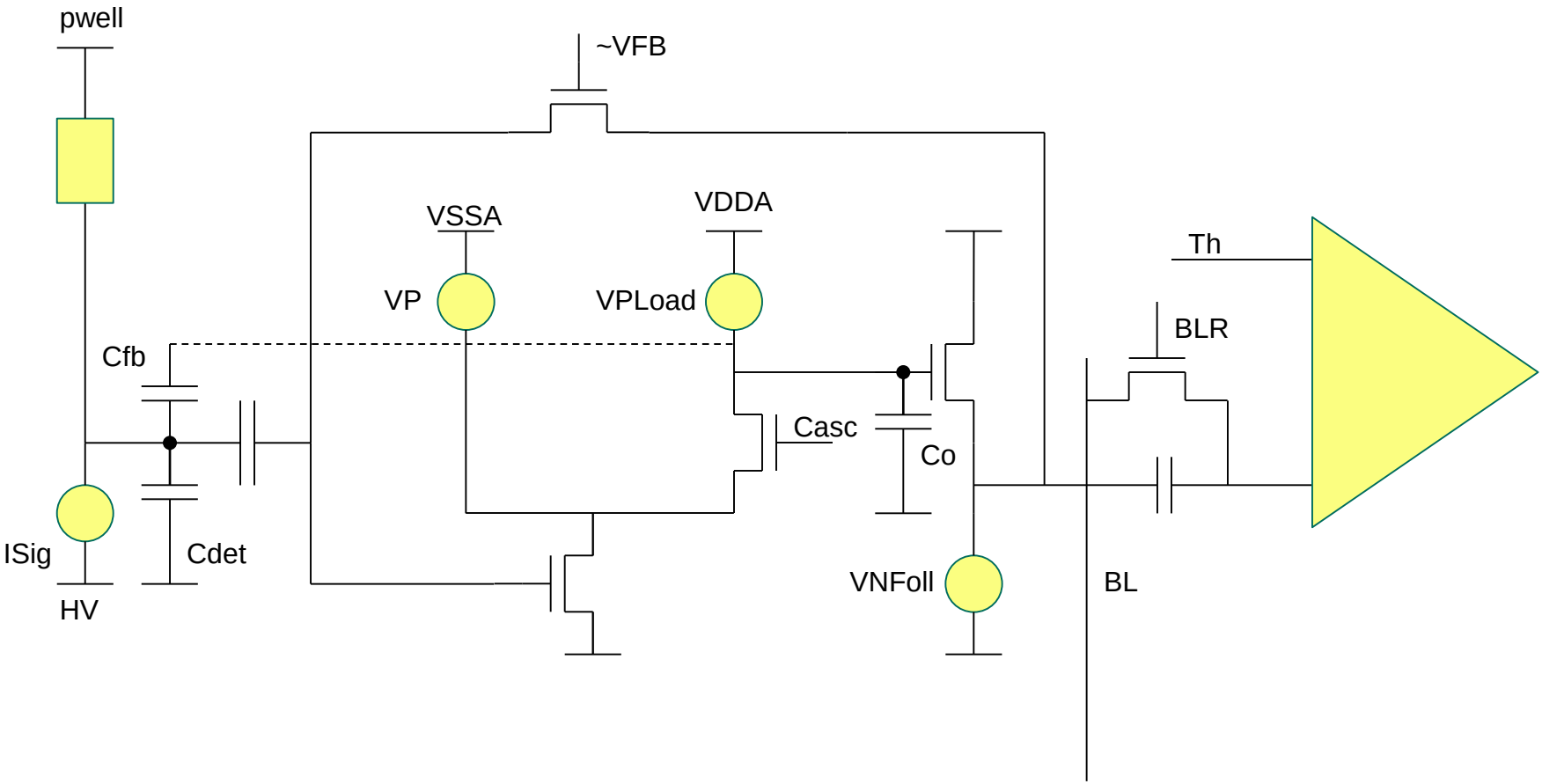
Pixel dimensions

- Pixel dimensions were reduced from 50µm (Atlaspix) to 25µm (“Telepix” chips)
- We have introduced new pixel-amplifier structures: from PMOS (Atlaspix) to faster NMOS and novel CMOS amplifier.

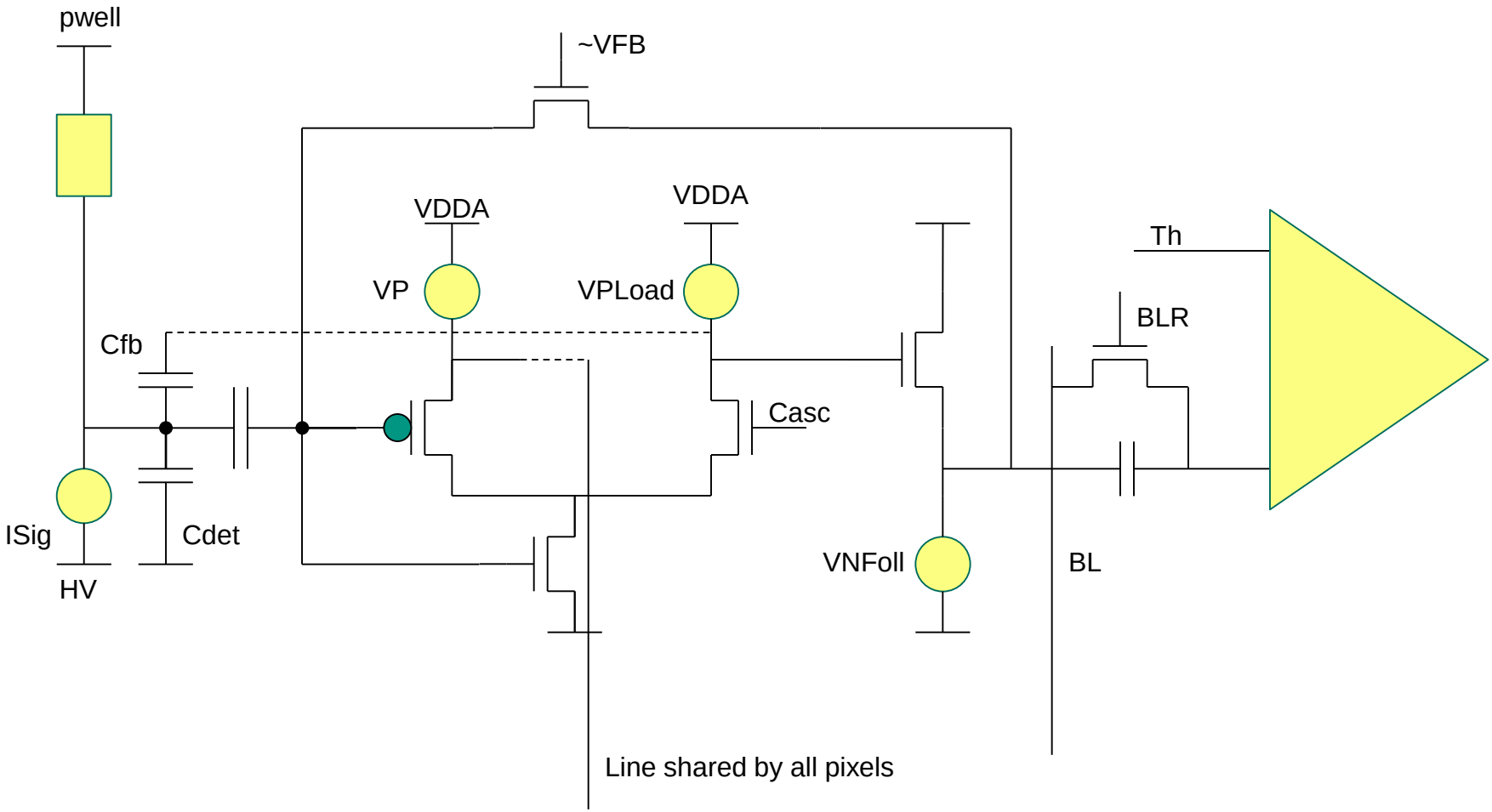
- PMOS amplifier
- Standard amplifier



- NMOS amplifier



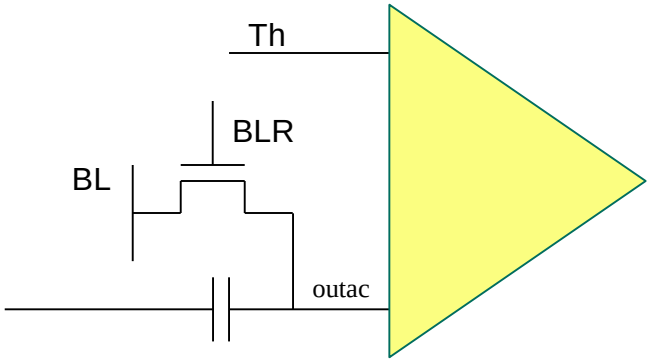
- CMOS amplifier
- Combination of both

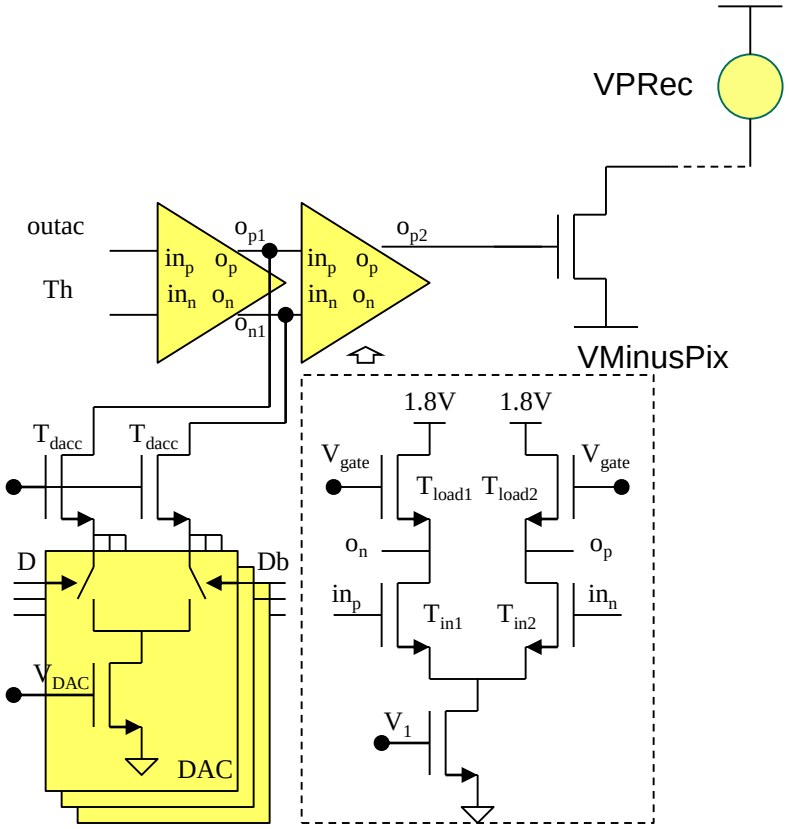


Comparator structures

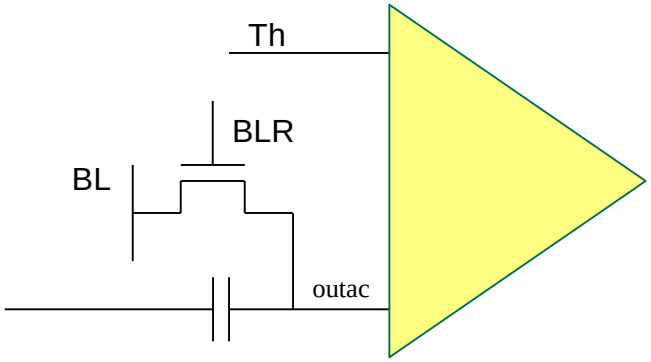
- New pixel-comparator designs were introduced: CMOS that requires isolated PMOS and “distributed” (split between pixels and periphery). The designs were tested and compared.
- All variations were tested, which was possible by connecting different matrices to same digital part

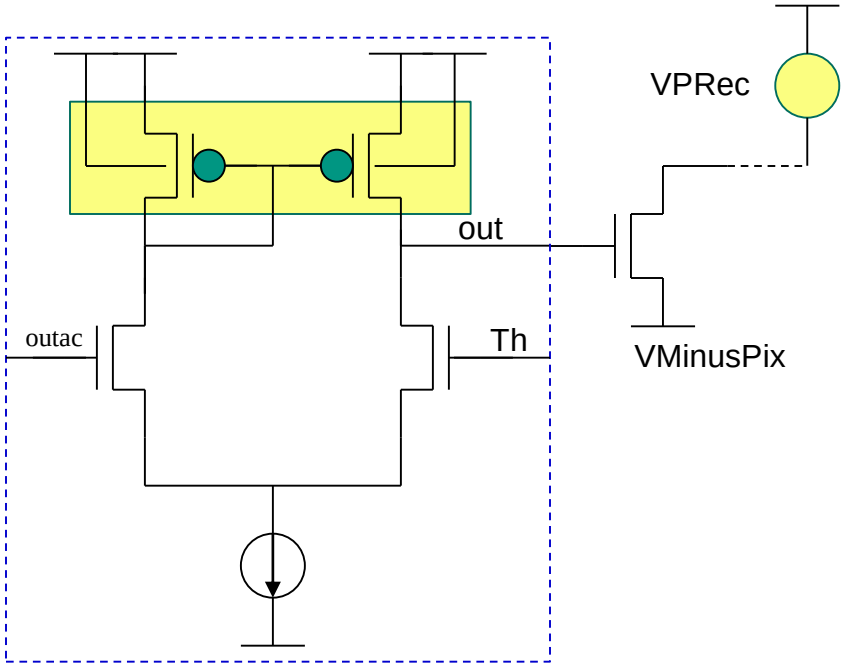
- NMOS comparator
- Standard – does not need deep p-well, used in Atlaspix3



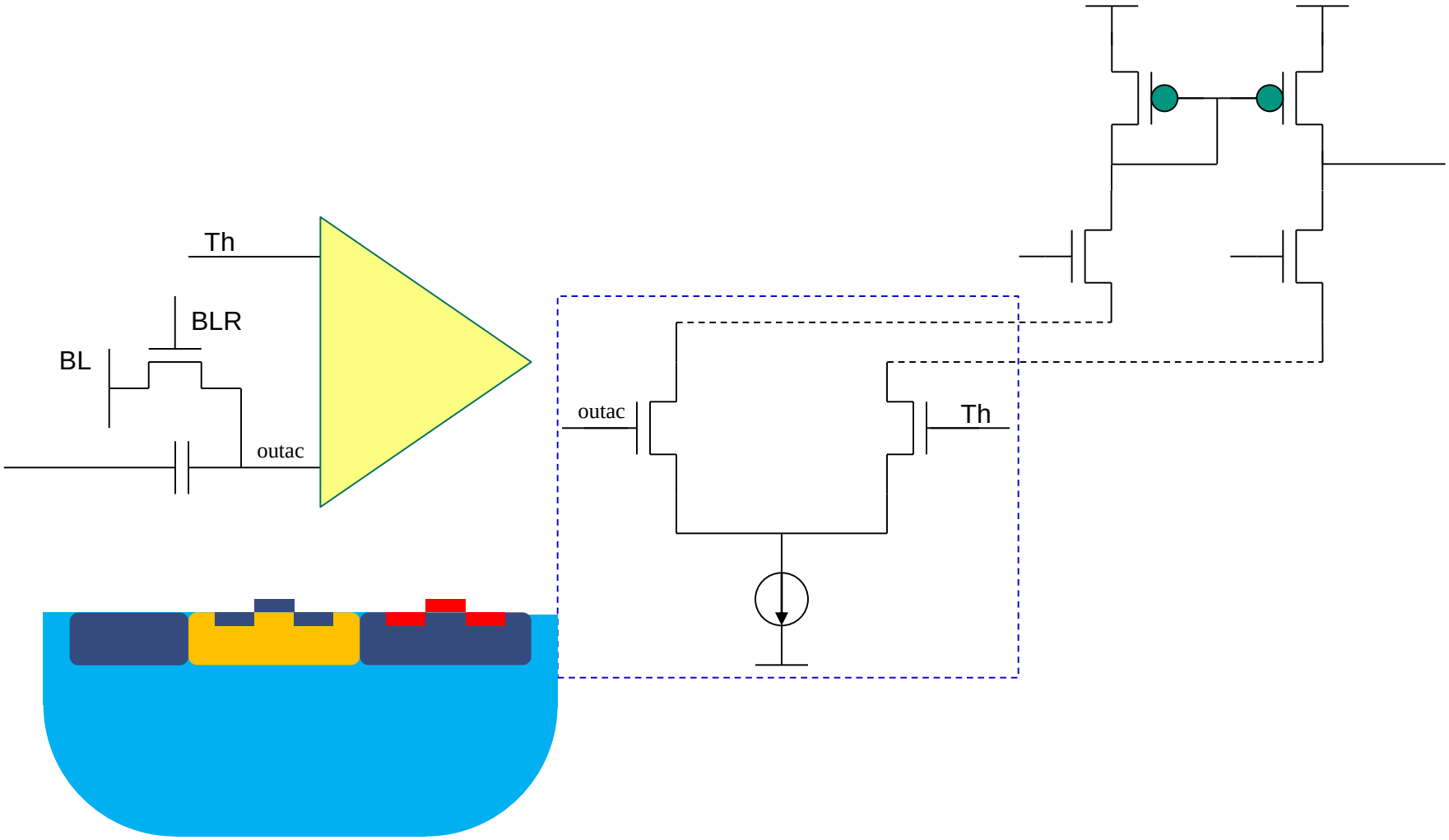


- CMOS comparator
- Needs deep p-well, should reduce delay dispersion





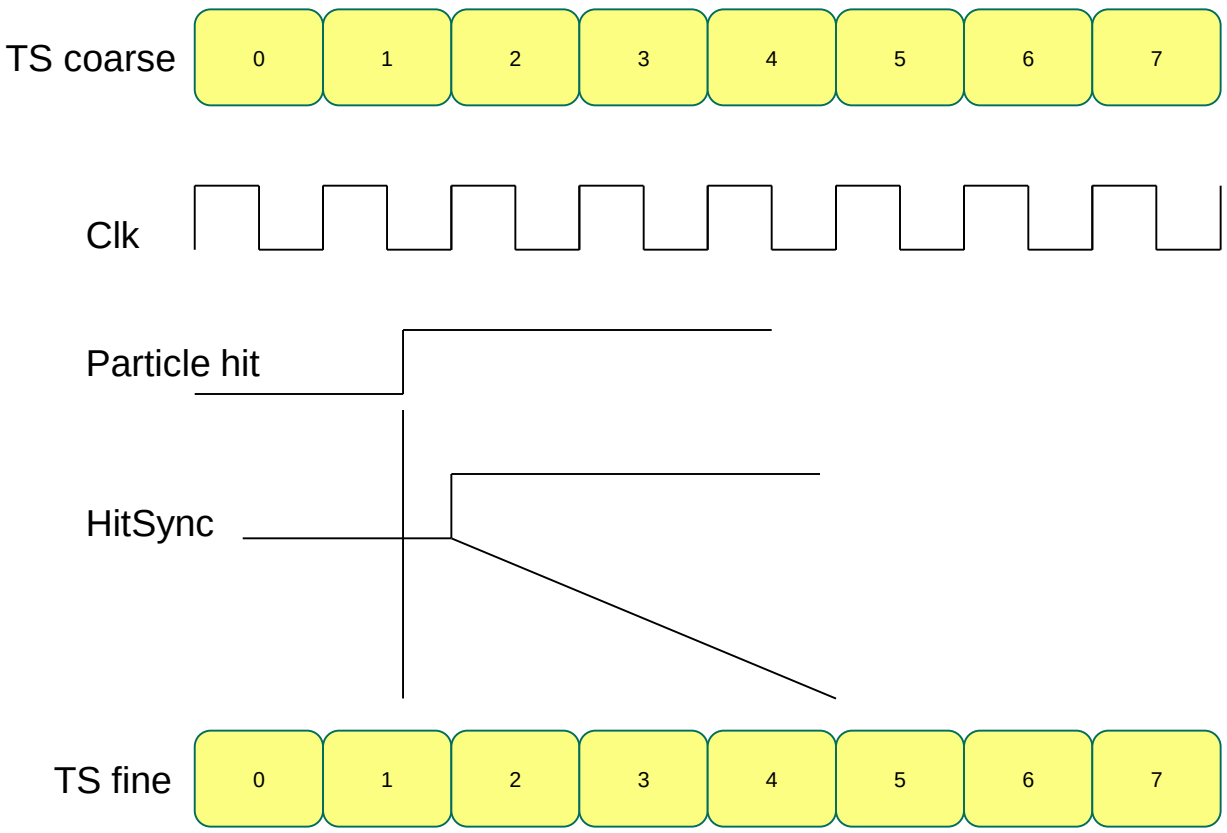
- Distributed comparator
- No crosstalk, little detector capacitance
- Needs two lines / pixel



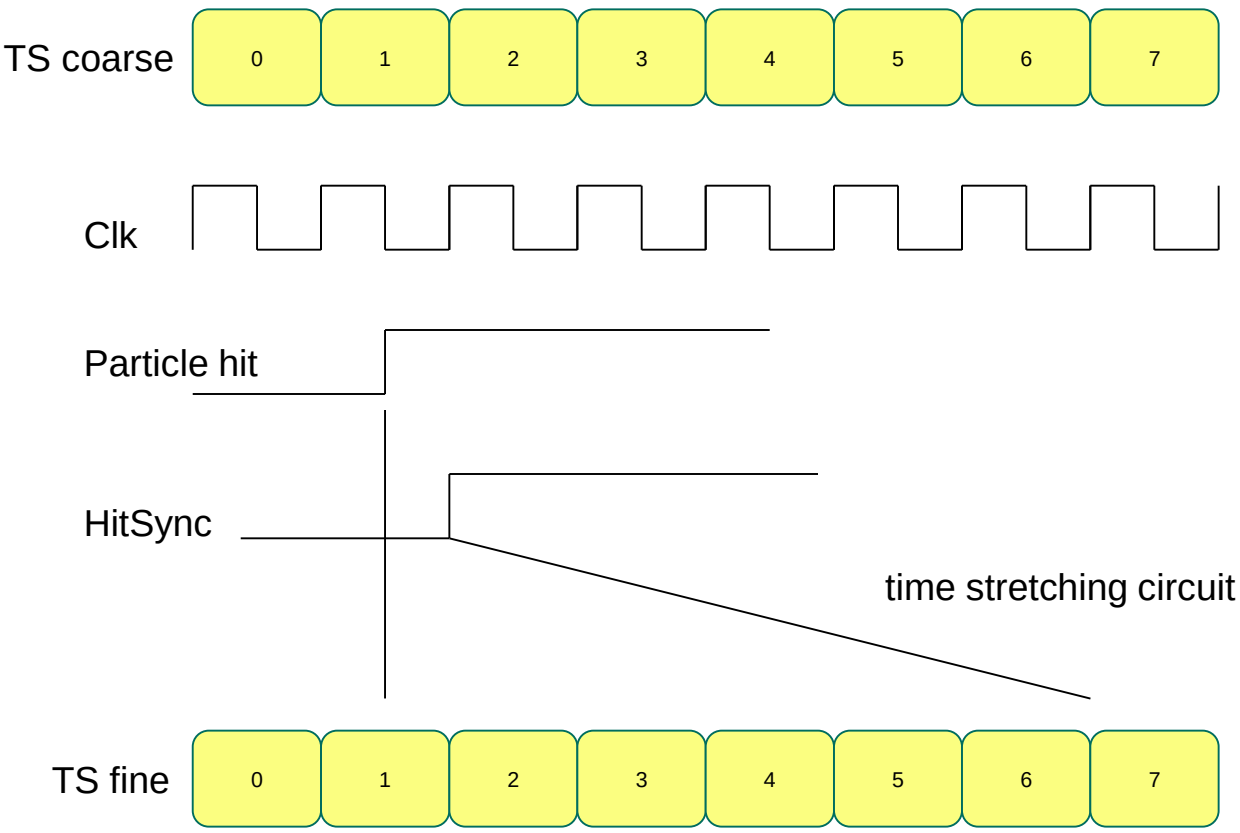
Time to digital converter

- We have also designed a TDC circuit that is small enough to be placed in every hit buffer. The TDC works as time stretching

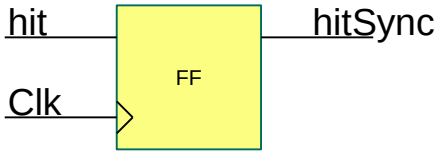
- The hit time is measured by storing two time stamp values

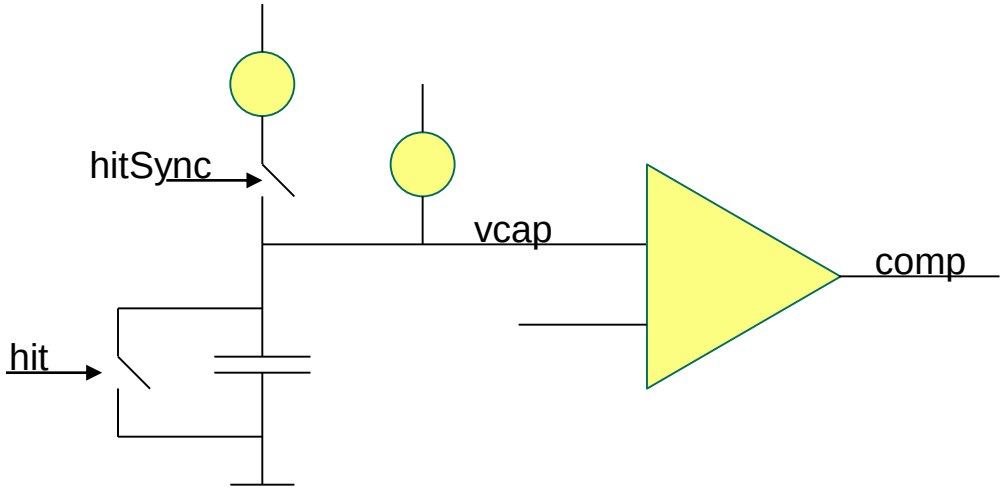


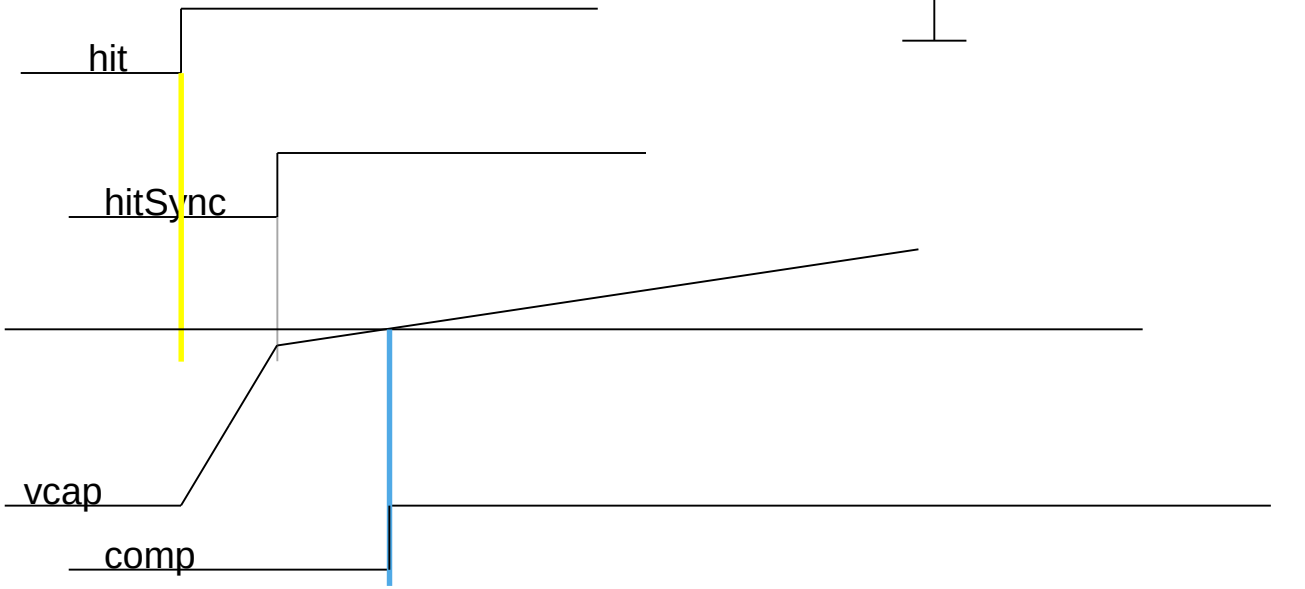
- The hit time is measured by storing two time stamp values

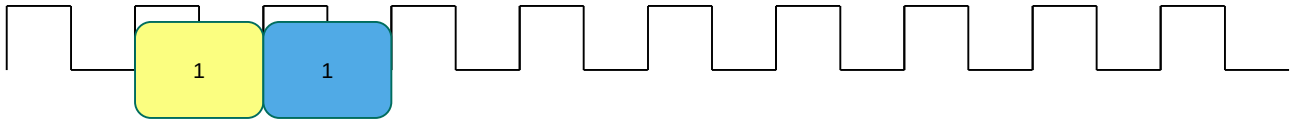


- …



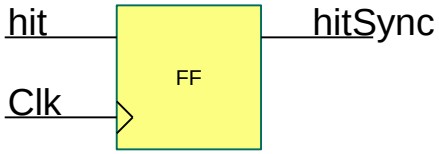


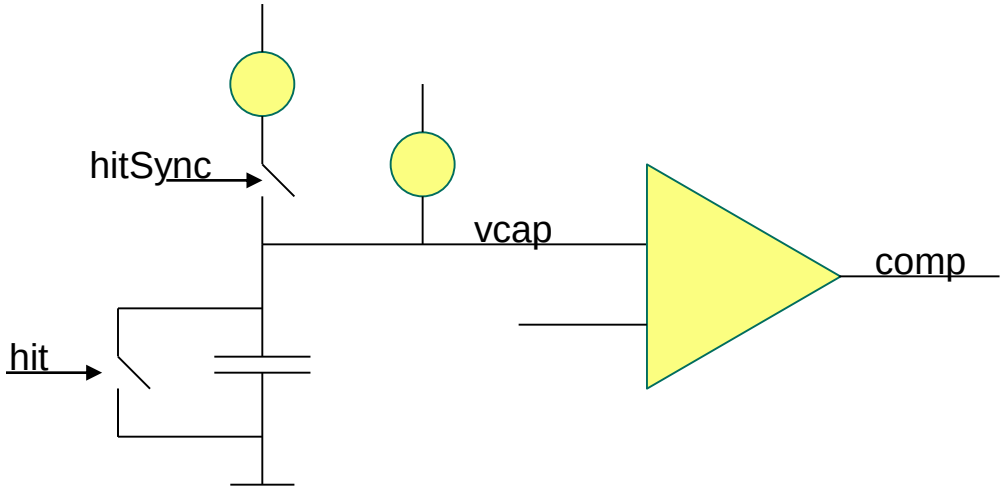


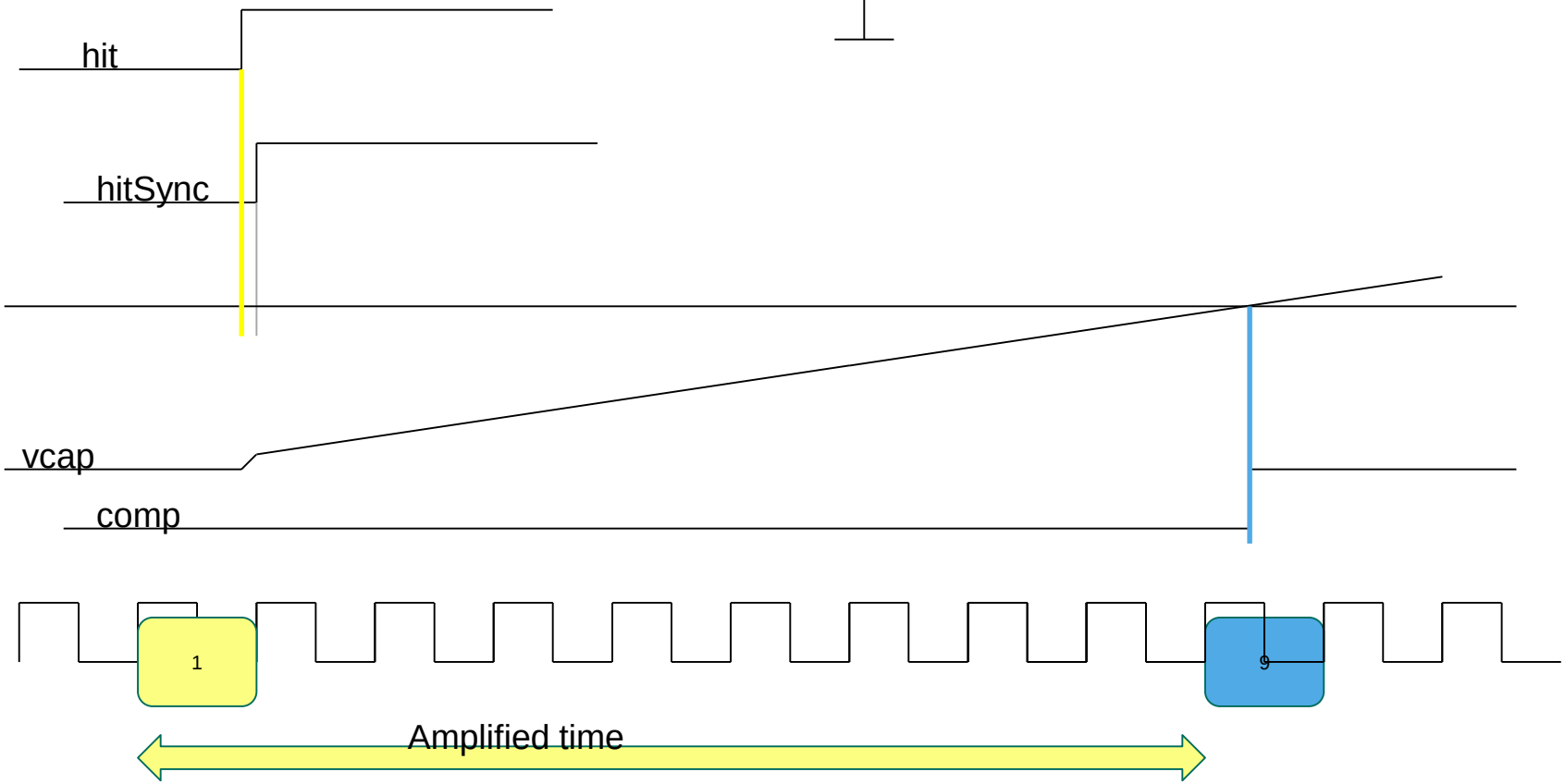


Amplified time

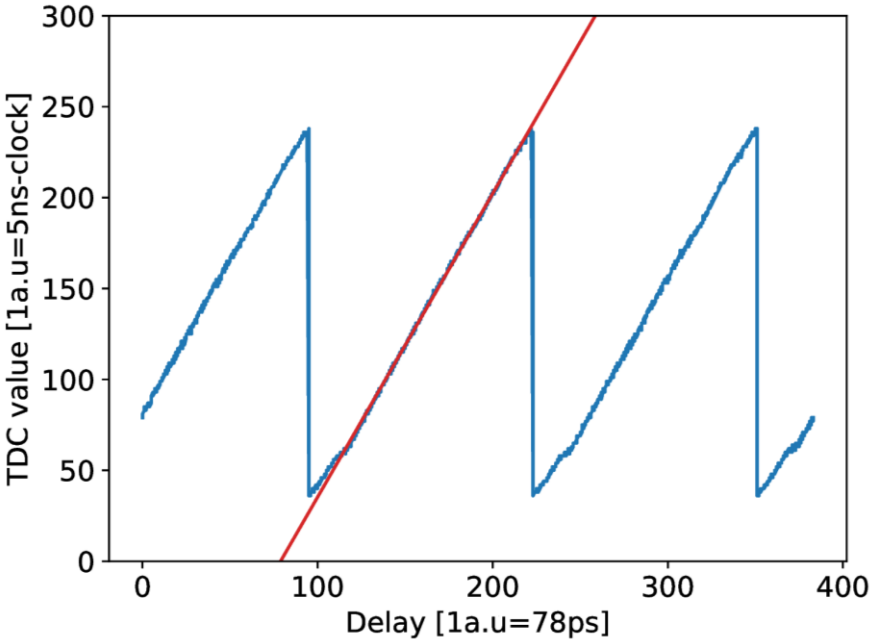
- …

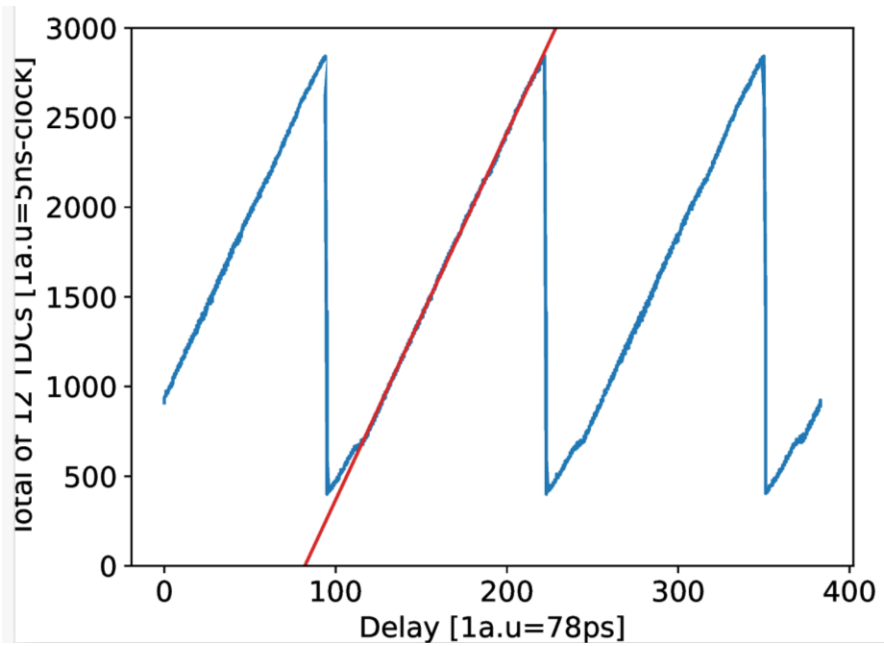

hit
Clk
FF
hitSync


hitSync
vcap
comp
hit

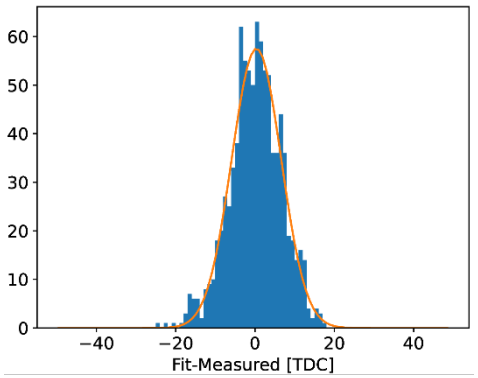

hit
hitSync
vcap
comp
1
9
Amplified time

- Intrinsic TDC time resolution is high (single TDC 56ps, with averaging 24ps rms, preliminary)
- Some issues with nonlinearity (probably crosstalk, can be tested in MuPix20)

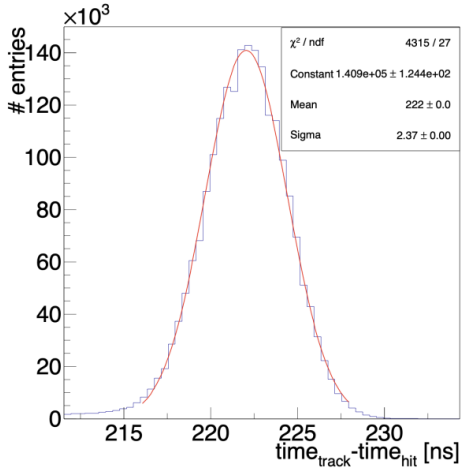




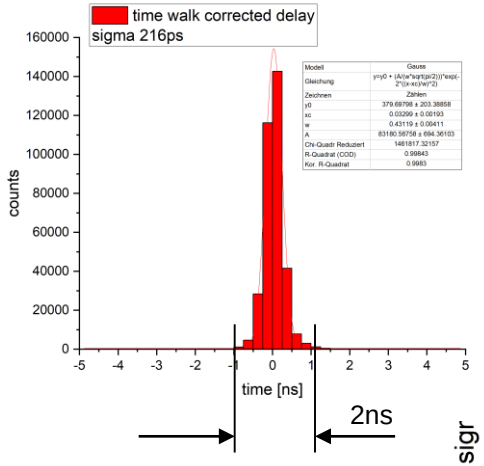
- 12 TDCs: Slope: 20.5, sigma difference from average: 6.23
- Resolution = 6.23/20.5 x 78ps = 23.7ps
- 1 TDC: Slope: 1.67, sigma difference from average: 1.19
- Resolution = 1.19/1.67 x 78ps = 55.6ps



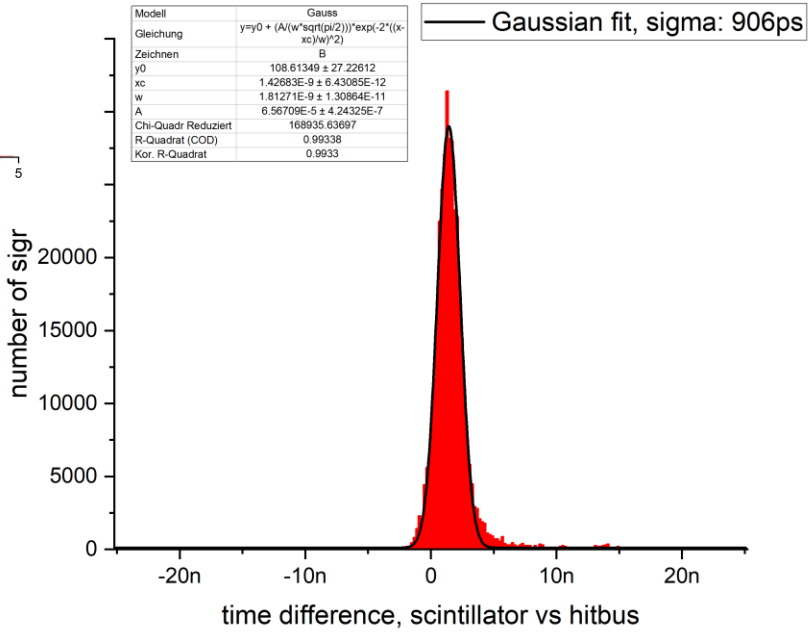
- We could improve the time resolution from about 4.5ns RMS (Atlaspix) to better than 2.4ns (Telepix chips). Further improvement should be possible with PandaPix which will be tested soon. With PicoPix sensors (that we develop for Mu3e), < ns was measured. Measurements are ongoing and preliminary



TelePix test chip time resolution 2.37ns



PicoPix - Time resolution measured with injection for signals > 3000e is 216ps



PicoPix - Time resolution measured with Sr-90 about 0.9ns

The main goals of funding period 21/24

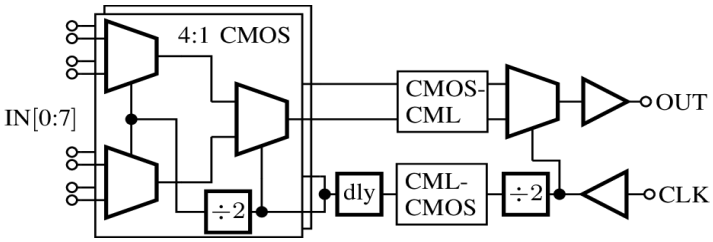
- VertexPix: Pixel sensor for vertex layers at future experiments in 130nm SiGe BiCMOS technology
- Goals: high time- and spatial-resolution, high rate capability, fast data transmission
- PandaPix: HV-CMOS pixel detector with high time and energy resolution in wide dynamic range for particle identification

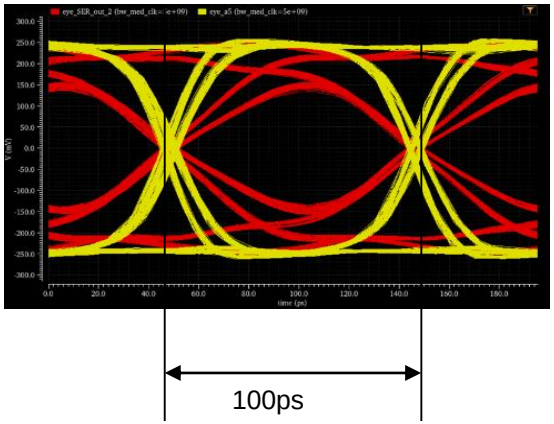
VERTEXPIX

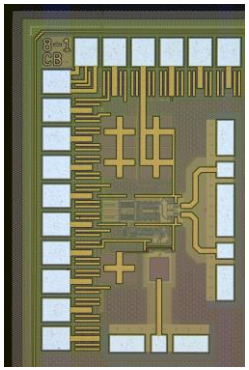
- Pixel sensor for vertex layers at HL-LHC in 130nm SiGe BiCMOS technology
- Specifications
- Particle rate 100/25 ns/cm^2
- Data transfer: 10Gb / link
- We have chosen the 130nm SiGe BiCMOS of IHP technology for this sensor development
- Fast SiGe bipolar transistors (HBT) and CMOS transistors that can be used in a pixel signal amplifier to improve time resolution
- 130nm gate-length
- Radiation-hard libraries
- The technology is used for particle physics experiments – FASER experiment
- Customized technology developments for HEP applications
- High resistivity substrates
- p-well isolation for HBTs
- Isolation for PMOS transistors (deep p-well)

- We have implemented test matrices, building blocks (TDC, DAC, Reference) and fast serializers.

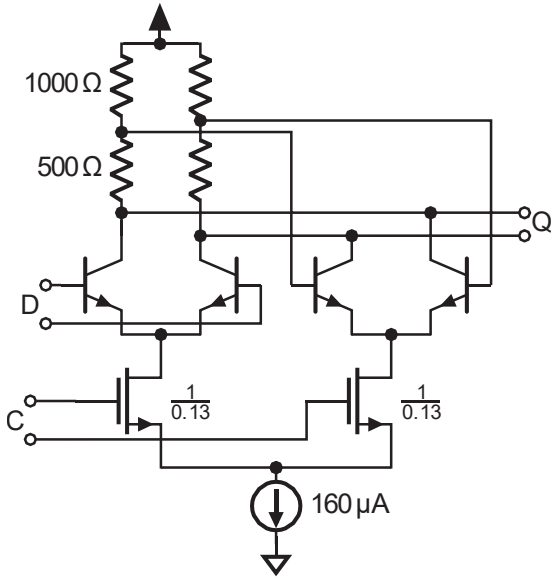
- Test chip with 8-1 multiplexer for 10Gbit/s data transmission





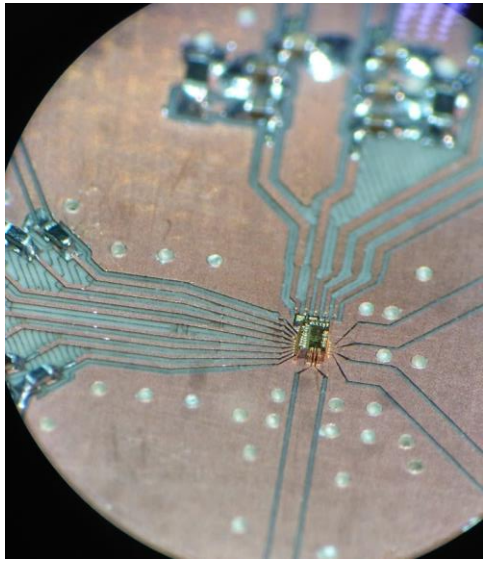


Test chip 500µm x 800µm

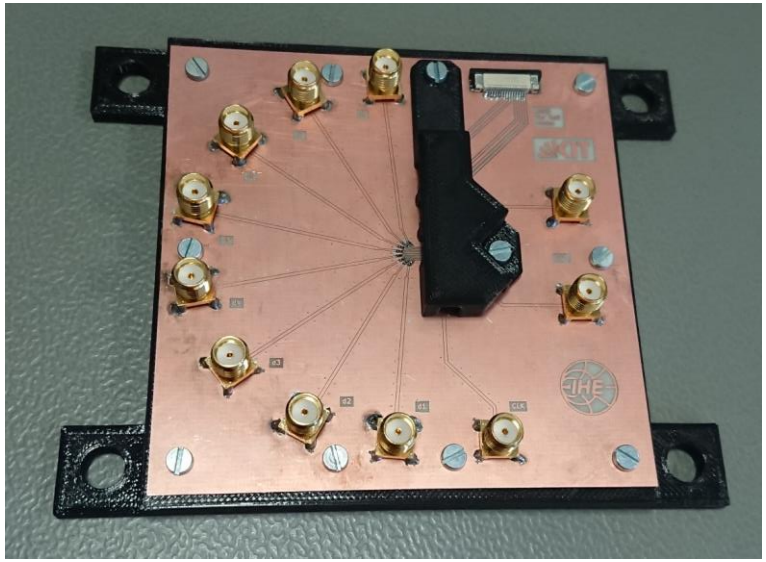


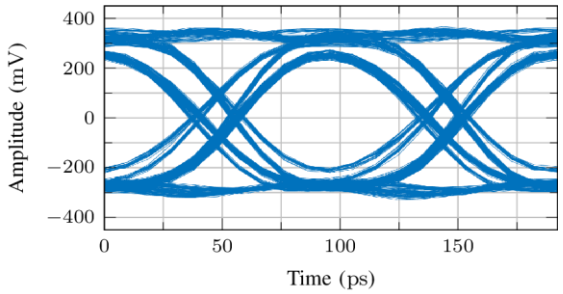
- Test setup
- Data transmission at 10Gbitps tested

PCB with Chip

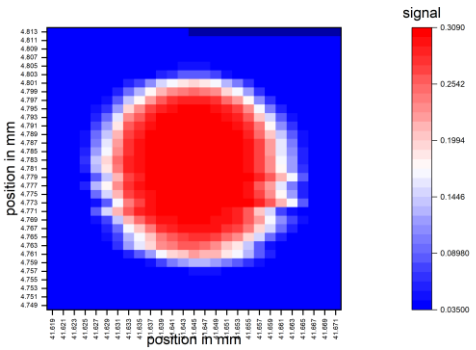


Bonded chip

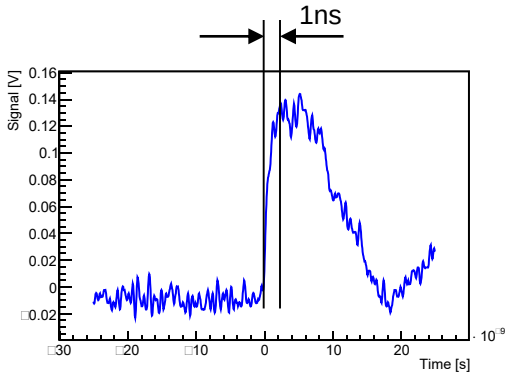




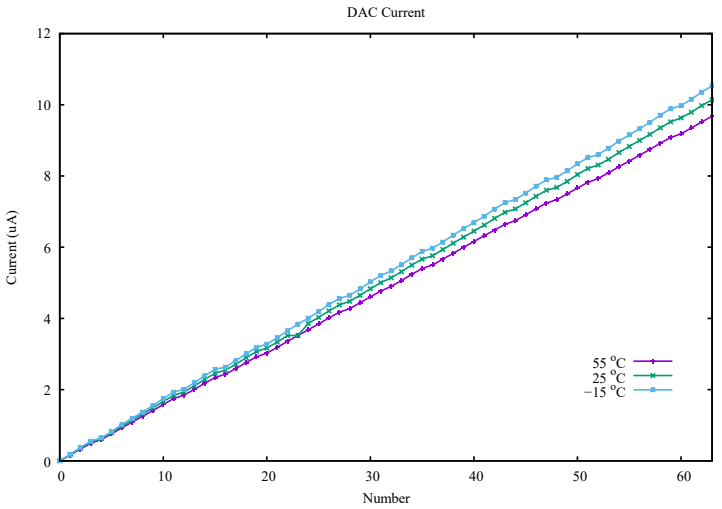
- Test matrix is rather simple (analoge readout). Timewalk is very small thanks to fast amplifiers. This promises high time resolution
- DACs and references were tested



Active pixel array, laser scan



Active pixel array, Sr-90 signal
Signal rise time ~ 1ns



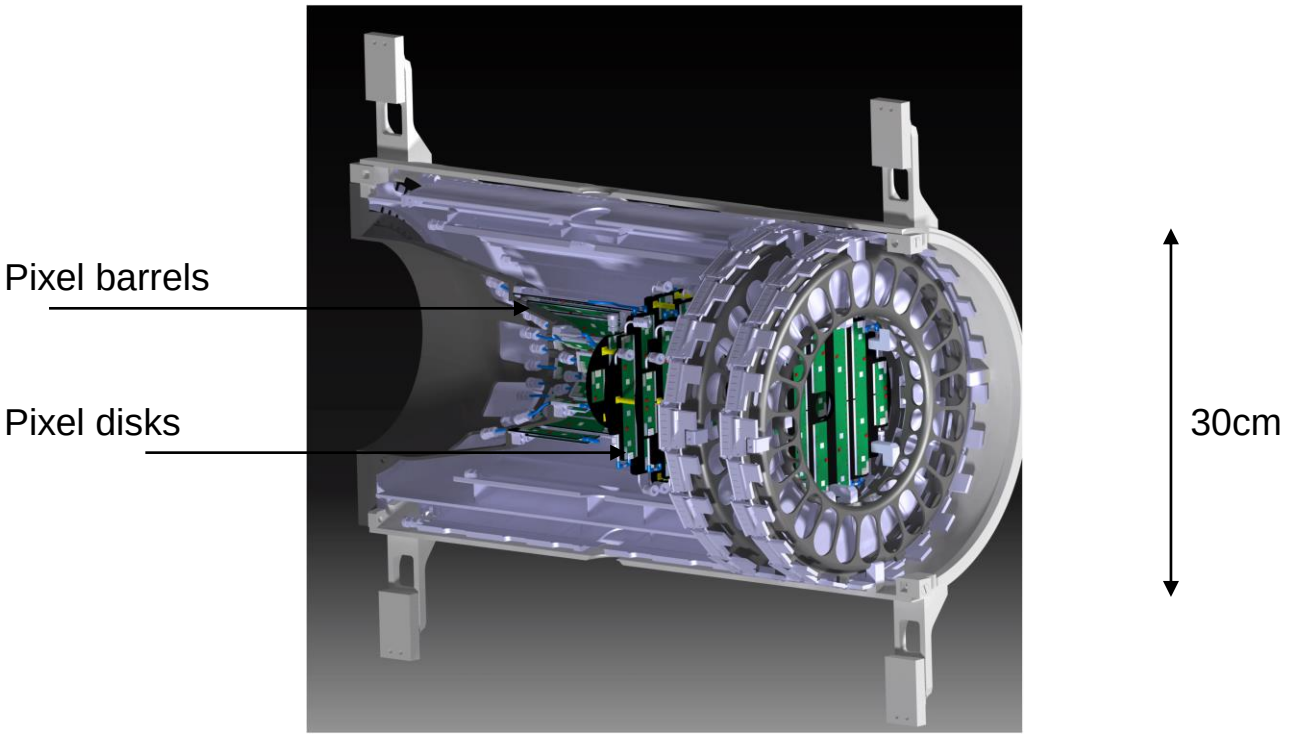
DAC and band gap reference test at different temperatures

VertexPix

- VertexPix submission in summer 2024
- Intended pixel size 50x50µm
- The pixel electronics will use HBTs
- Difficulty: HBT has base current (unlike MOSFETs with no gate current)
- New type of feedback circuit with leakage current compensation
- Pixel contains amplifier, feedback, comparator and TDAC
- CMOS comparator requires deep p-well isolation, which IHP added such to the process
- It requires change of the deep n-well energy (depth)
- Digital part contains hit buffers (to measure time and tot), EOC buffers, readout state machine serializer with 8b10b conversion and configuration registers
- The entire digital part will be synthesized

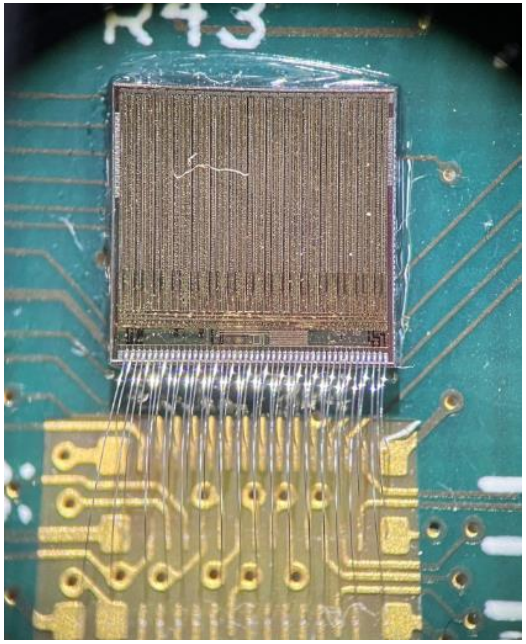
PANDAPIX

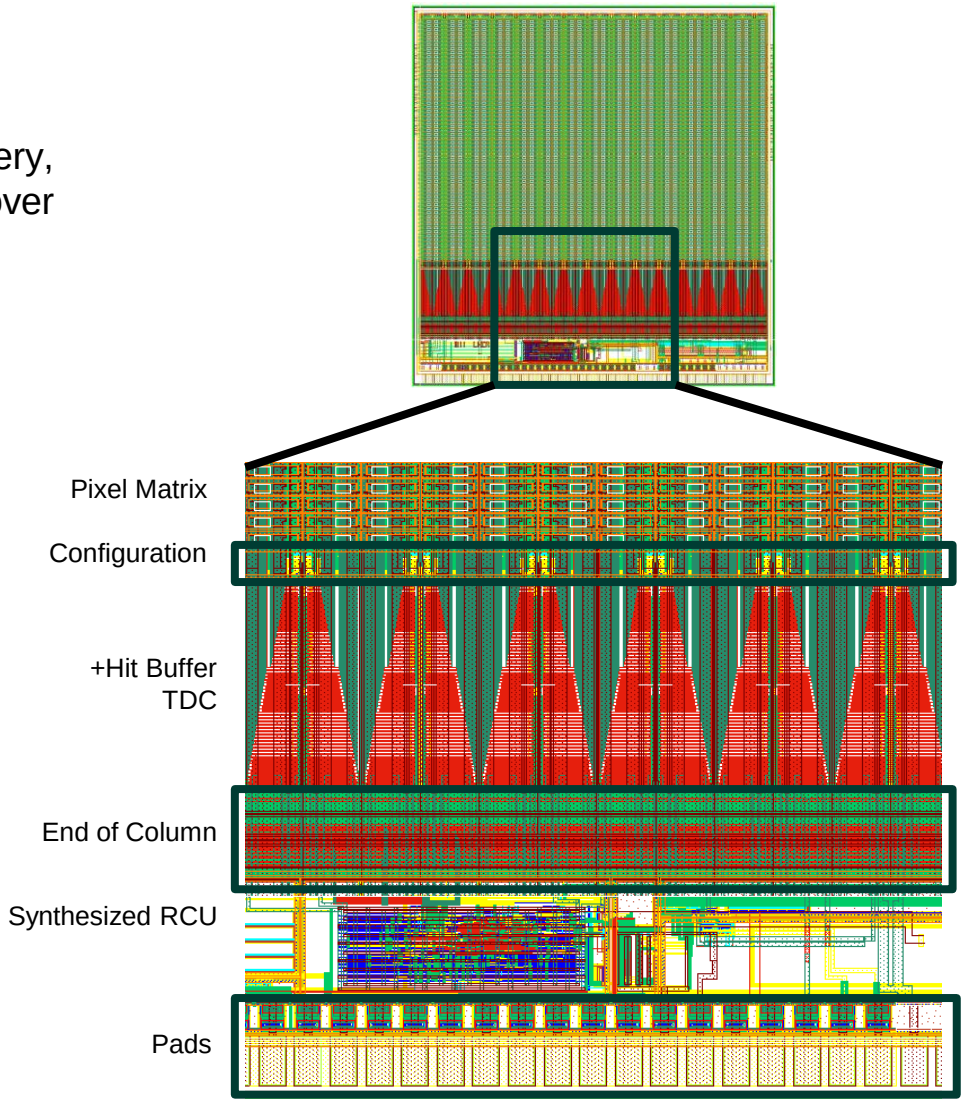
- High time resolution of 1ns RMS enables efficient track reconstruction and possibly particle identification by time of flight
- Energy resolution in wide dynamic range 100ke with 100e noise for dE/dX measurements and particle identification
- Goal: pixel size: 80 µm x 80 µm, chip size: 1 cm x 2 cm



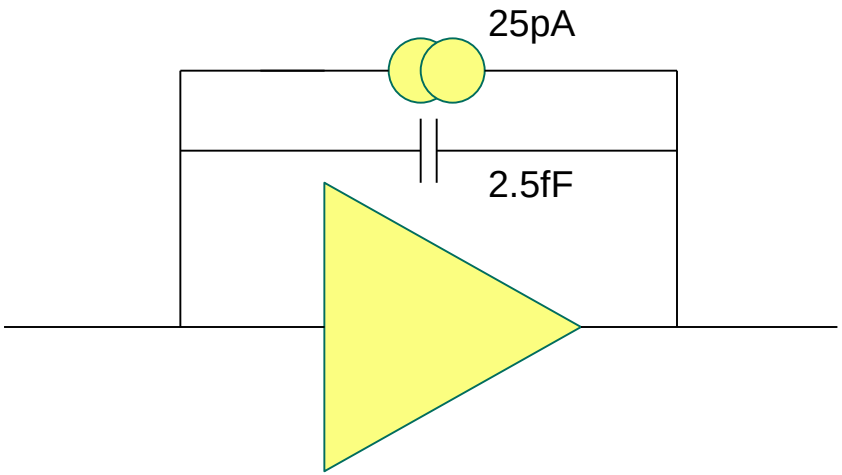
- ASICs
- PandaPix2020
- PandaPix2021
- PandaPix2023

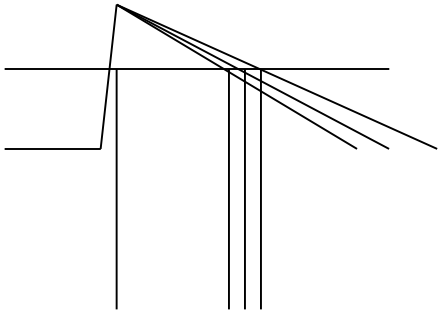
- Chip Size: ~ 5 mm x 5 mm
- Pixel Matrix: 29 columns x 62 rows
- Pixel Size: 50 µm x 165 µm
- Two comparators per pixel
- Each comparator one hit buffer in periphery, measures time of arrival and time over threshold. TDC in every hit buffer
- End of Column buffers
- Synthesized readout control unit
- Current and voltage DACs, registers



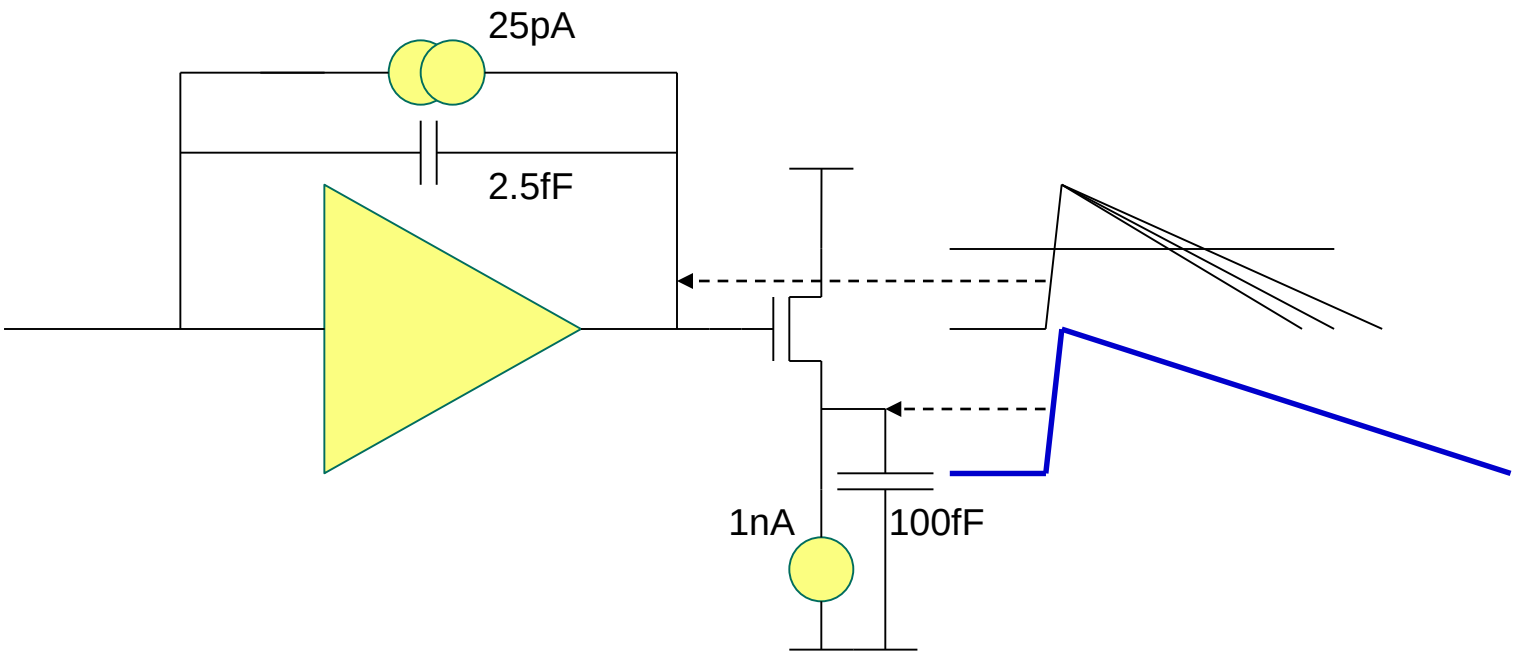


- Double measurement (peak detector)

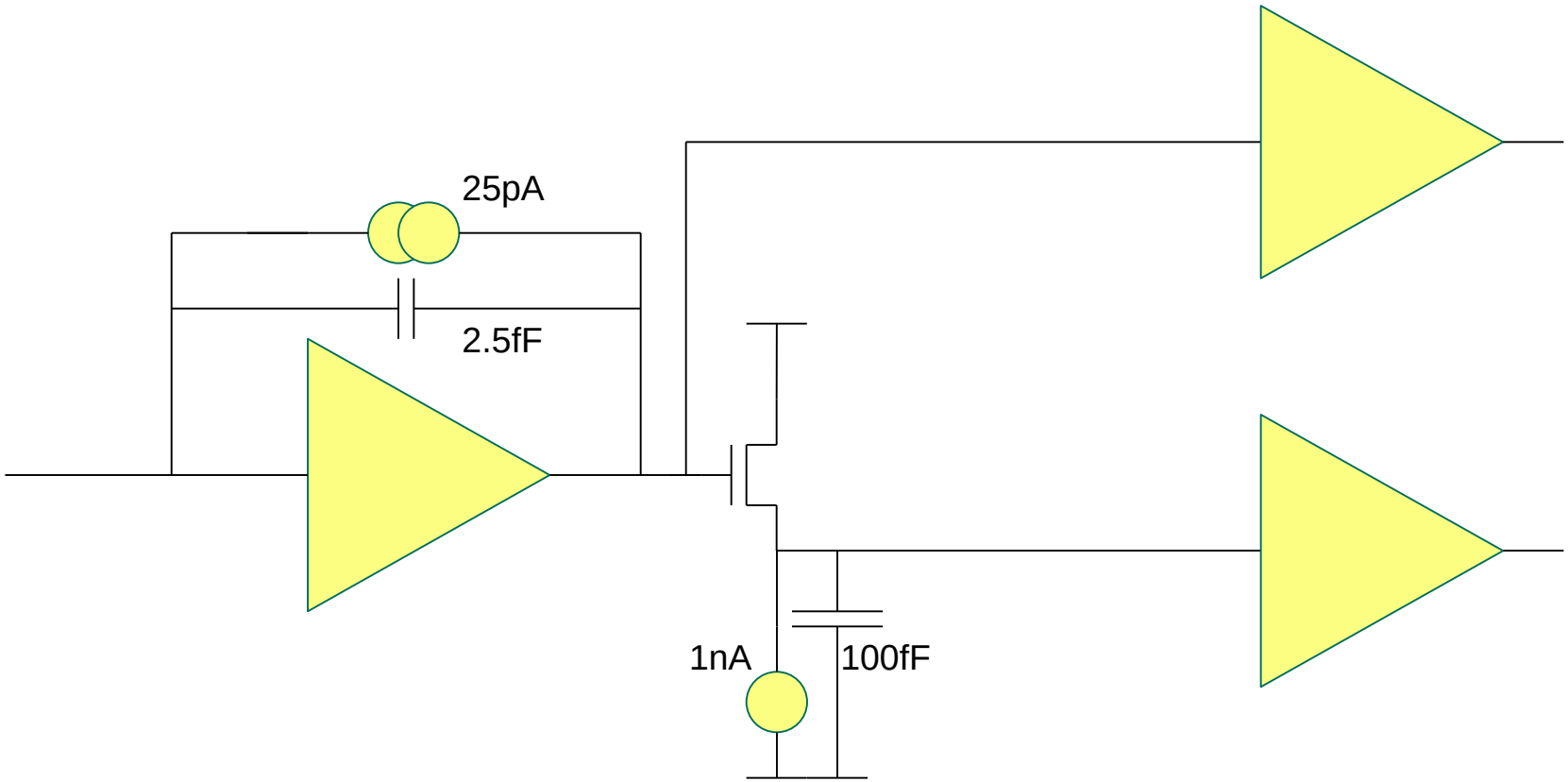




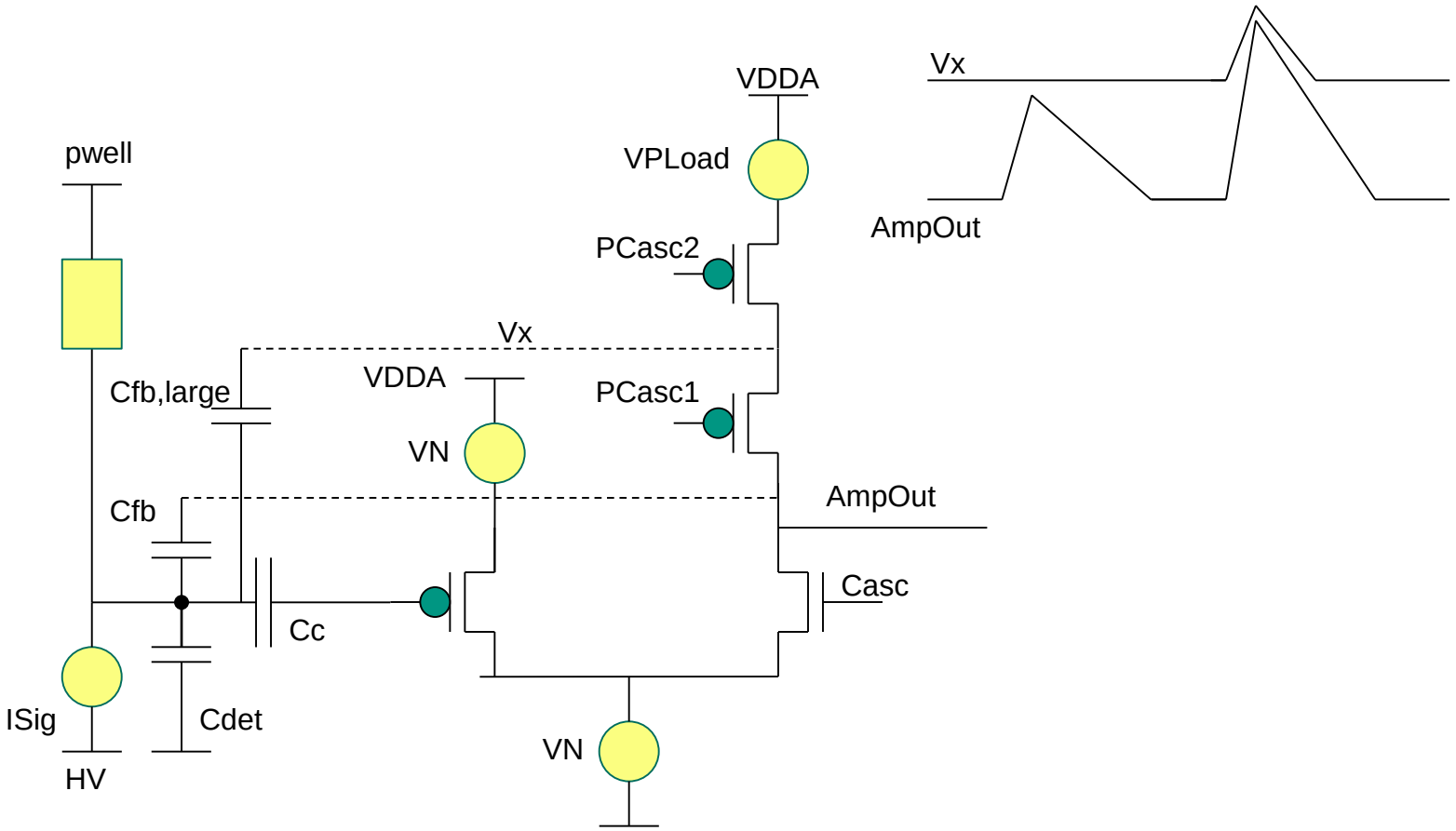
- Double measurement (peak detector)



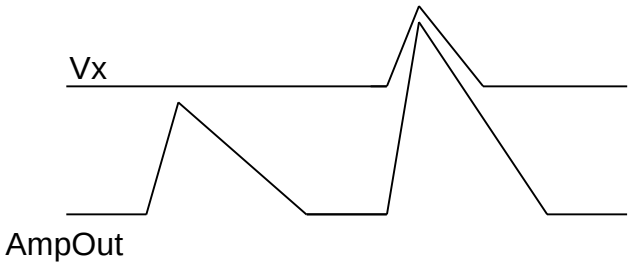
- Double measurement

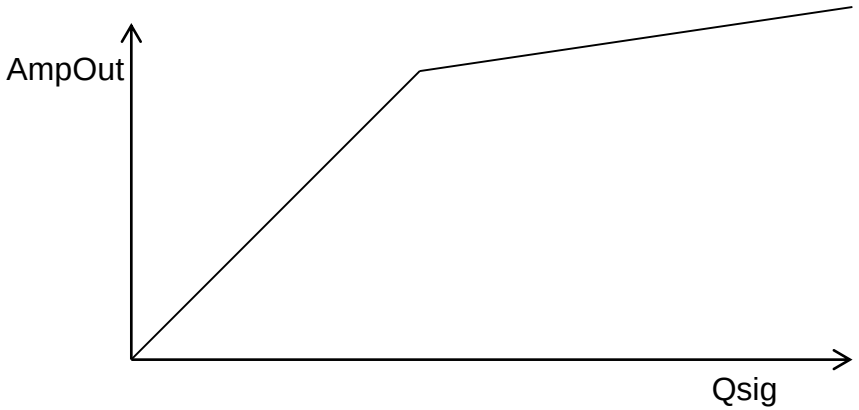


- High dynamic range

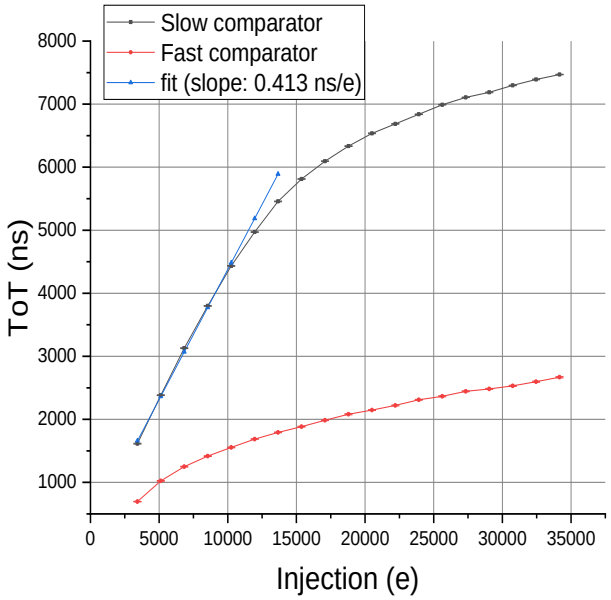


- High dynamic range



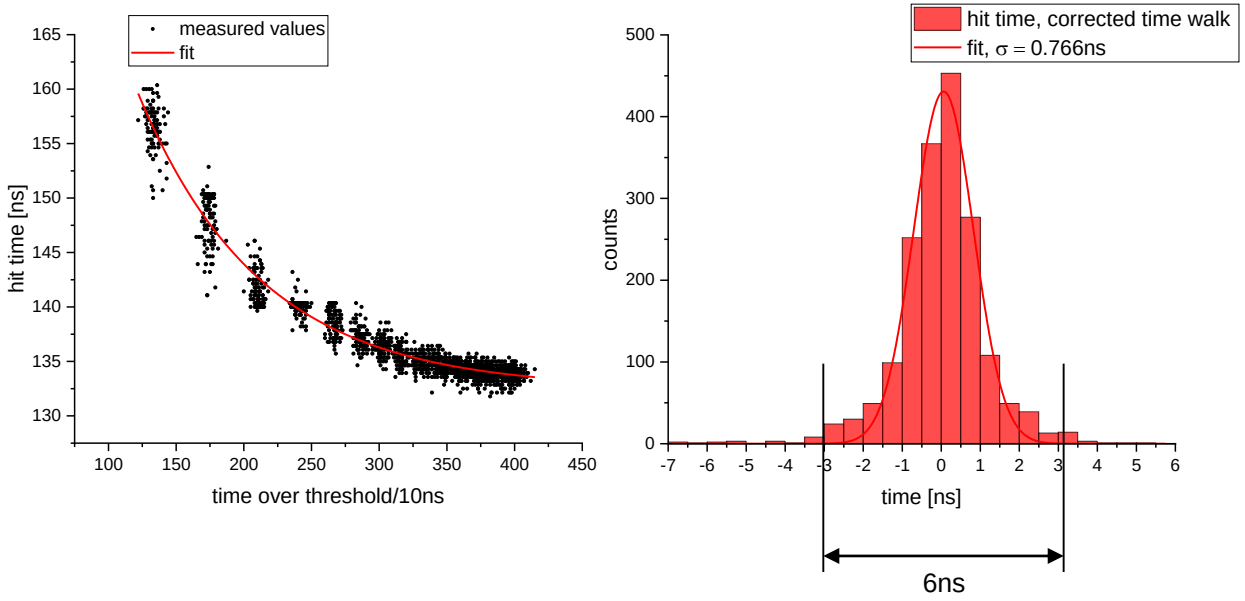


- Measurements on the PandaPix2021 test chip
- Energy resolution with SNR>1000 possible
- Better SNR on slow comparator

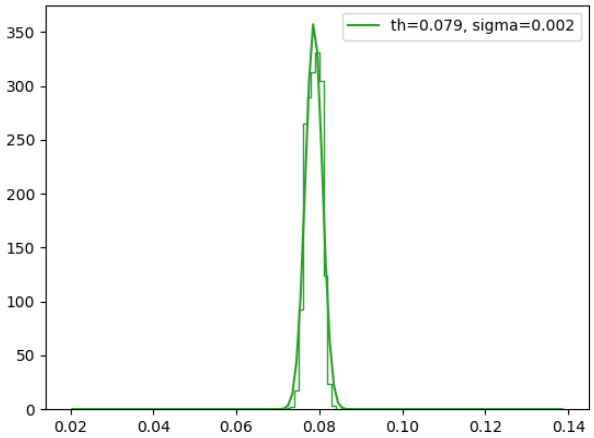


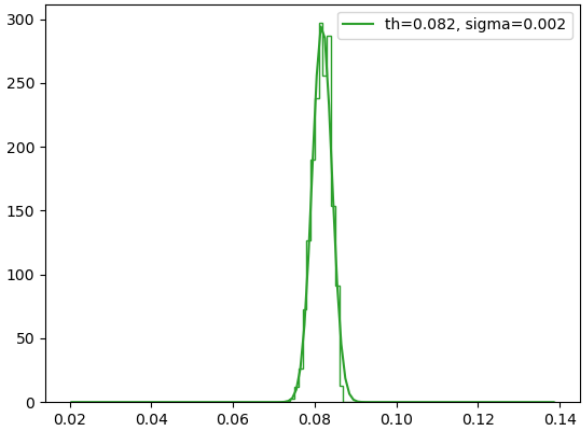
- For 32ke amplifier does not saturate, maximum signal limited by injection circuit
- The average ToT noise is about 48 ns for slow comparator. Its gain can be obtained by fit and it is 0.413 ns/e. If we divide the ToT by gain, we obtain the noise in electrons as 116 e.

- Time resolution <1ns should be possible
- Time walk is ~ 20ns for signals > 3000e but it can be compensated

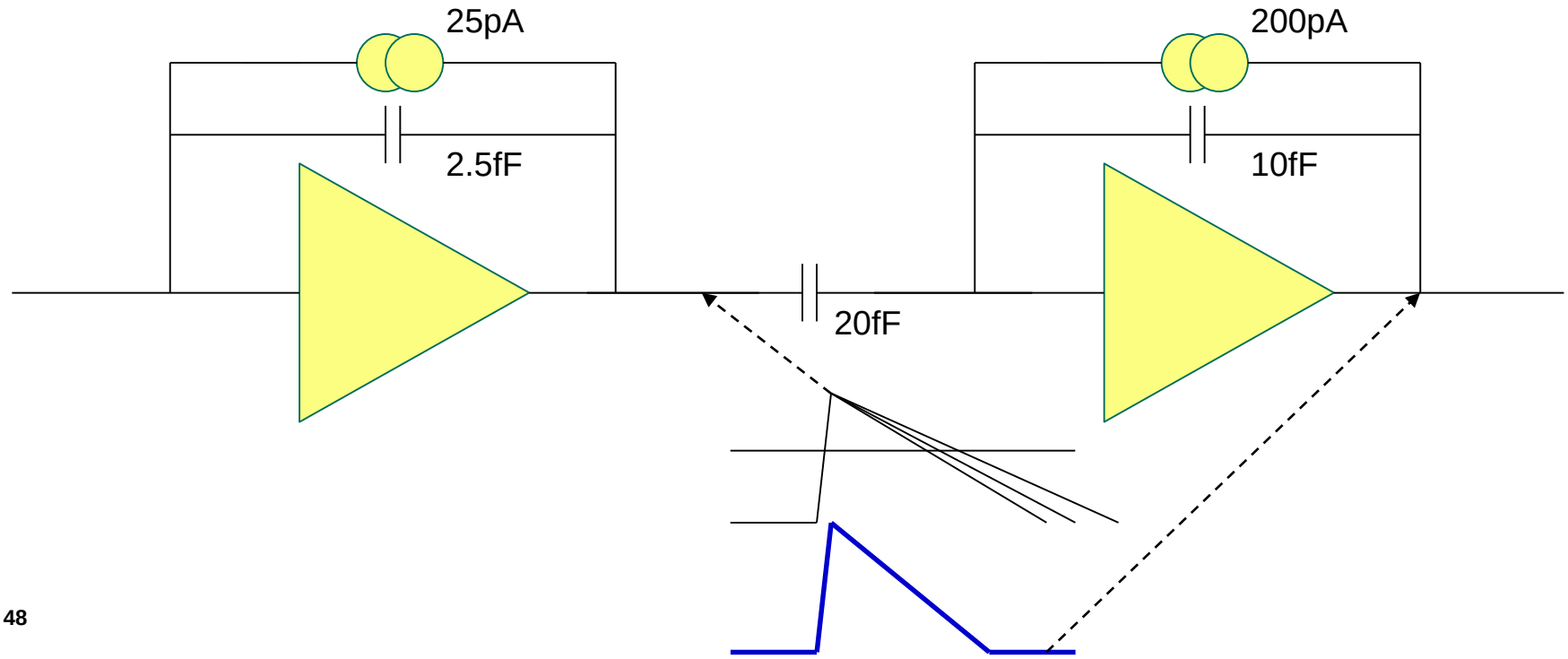


- Threshold dispersion is <60e, both comparators can be tuned





- PandaPix2023
- Uses two stage amplifier and one comparator
- Second amplifier improves energy resolution by TOT
- Pixel size 80µm x 80µm
- Uses deep p-well and isolated amplifier
- Test system ready, results soon



Summary

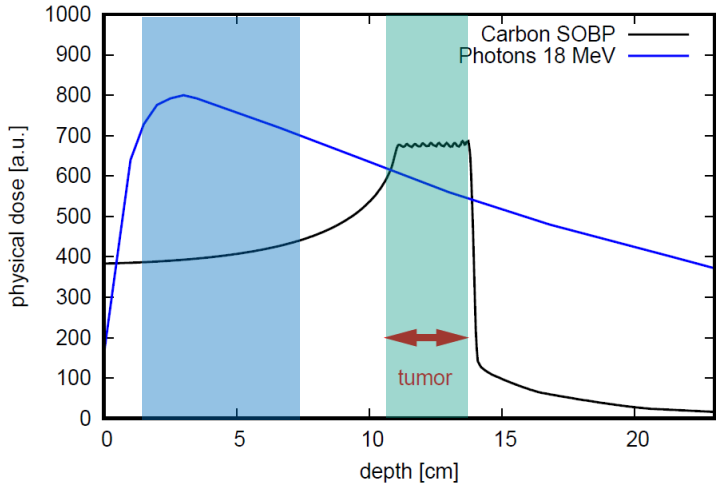
- We presented
- VertexPix: Pixel sensor for vertex layers at HL-LHC in 130nm SiGe BiCMOS technology
- Goals: high time- and spatial-resolution, high rate capability, fast data transmission
- PandaPix: HV-CMOS pixel detector for particle identification in 180nm HV-CMOS technology
- High time resolution and energy loss measurement with wide dynamic range
- Additional Activities in backup slides
- HITPix: HV-CMOS beam monitor
- MightyPix: Sensor for LHCb upgrade
- TelePix: Sensor for DESY telescope
- ASTROPix: Compton telescope
- PicoPix: Sensor for Mu3e timing layer

- Backup slides

BEAM MONITOR PROJECT

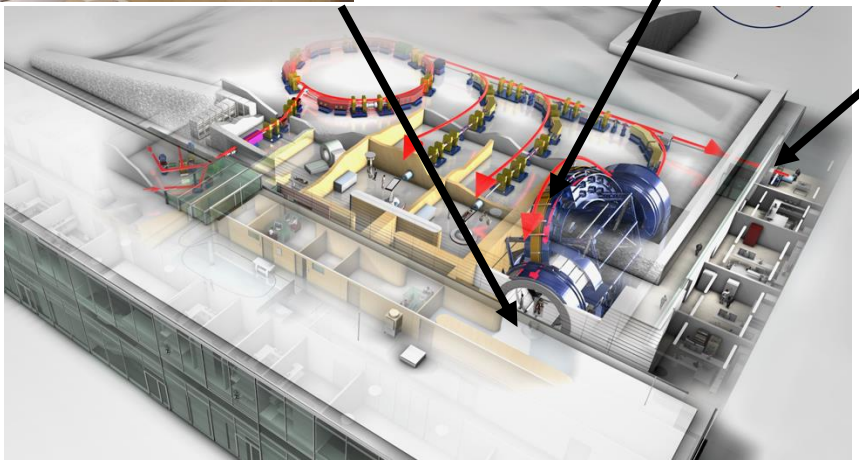
HIT beam monitor

- Heidelberg ion beam therapy facility (HIT)
- At HIT, cancer tissue is treated using proton and carbon ion beams
- Less radiation dose outside the target volume



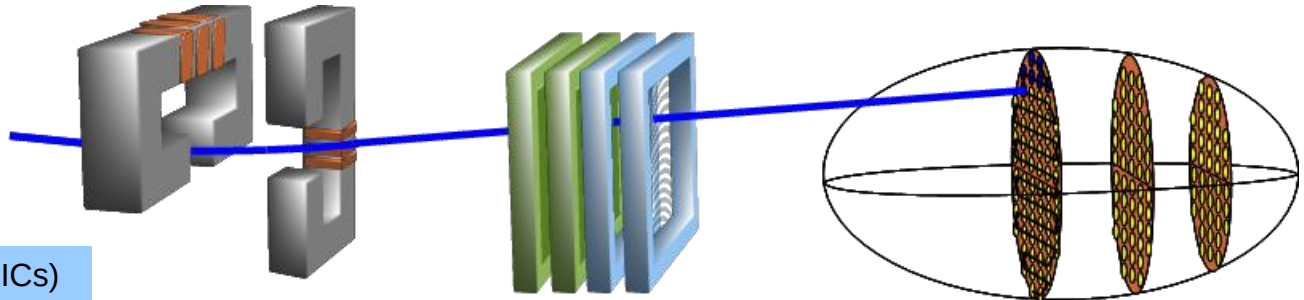
Gantry

Treatment room

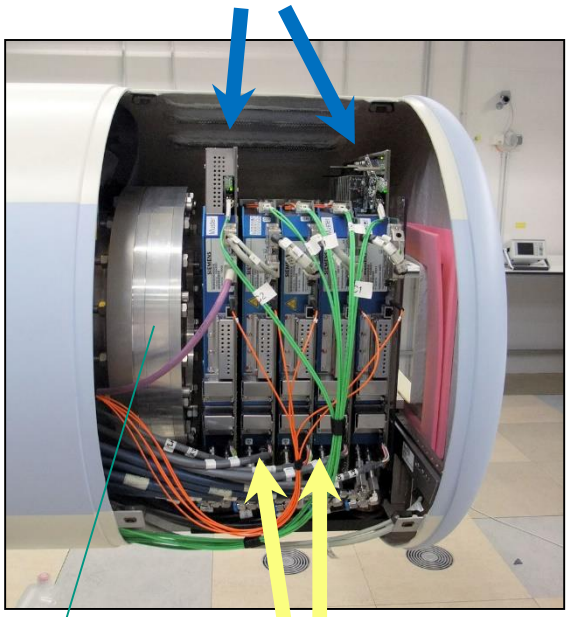


Beam monitor

- HIT aims MRT-compatible replacement/upgrade of the existing beam monitor



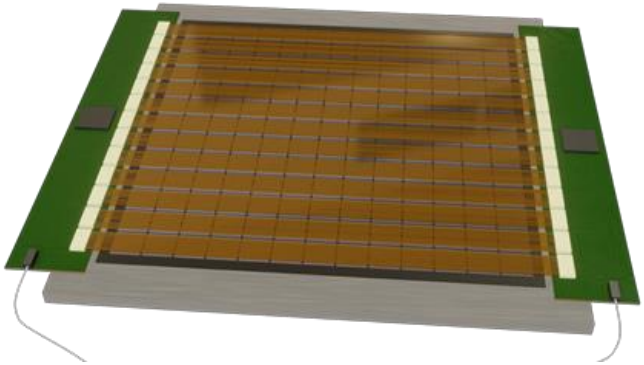
Multiwire chambers (MWICs) for position measurement

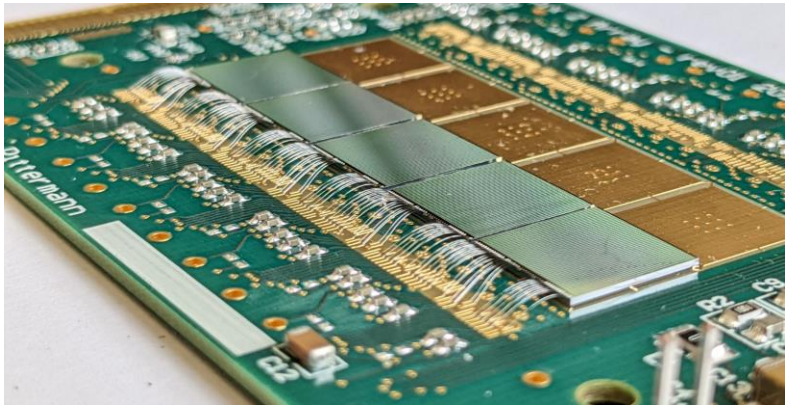


beam exit window

Ionization chambers (ICs) for dose measurement

- Our beam monitor would be based on HV-CMOS pixel sensors
- The detector would consist of sensors chips glued to the foil with printed connections

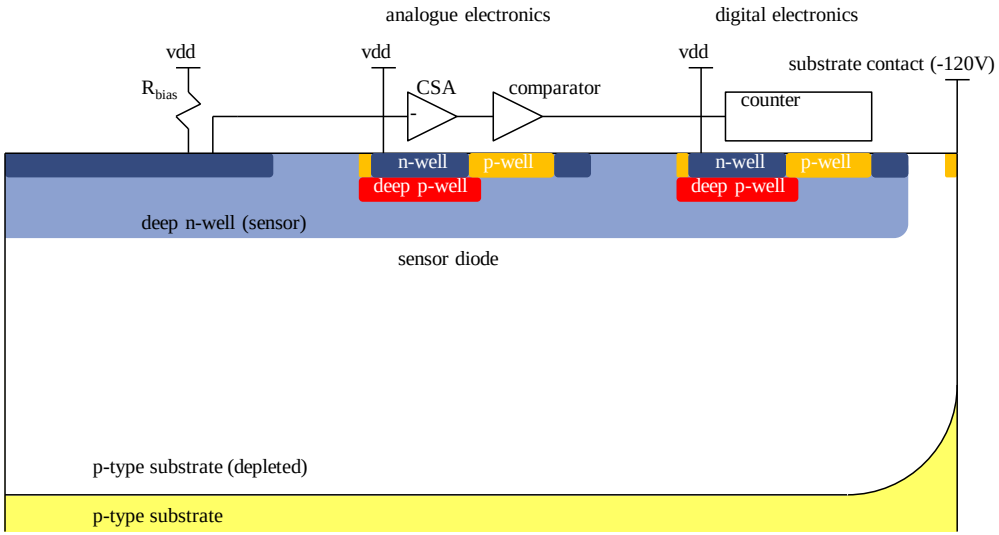


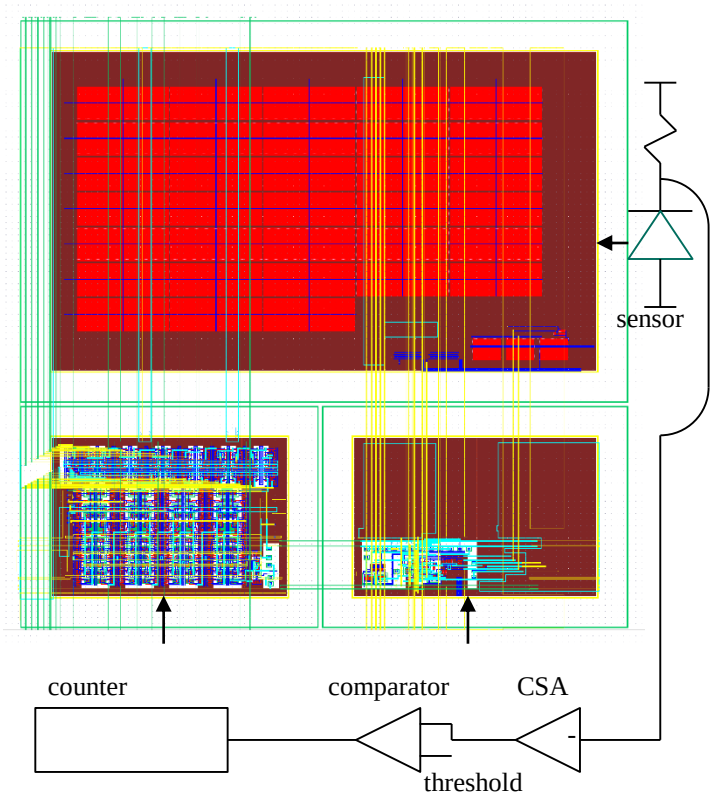


HIT beam monitor

- Sensor specifications are
- Detection of light ions (protons to oxygen)
- MR compatibility (magnetic field)
- Dose rates (example) $3x10^9$ protons/s for a beam spot of 33mm (FWHM)
- Beam spot 1mm - 13mm (carbon)/33mm (proton) FWHM
- Position measurement in ≤ 100µs
- Accuracy position ≤ 0.2mm
- Sensitive area ≥ 25x25 cm
- Radiation tolerance to 10^{15} particles (protons and carbon, different energies) at the innermost cm^2 per year
- Thickness ≤ 1mm (all layers)

- We have designedseveral 5x5mm^2 test chips and two 1cm^2 prototypes
- The pixel electronics is rather complex
- Amplifier, comparator, 8 bit counter and adder
- High-rate capability implemented by using counters





The digital cells generate fast 1.8V signals and a lot of noise
To shield the sensor electrode from noise, we have added an additional layer – the deep p-well.

- Experimental results

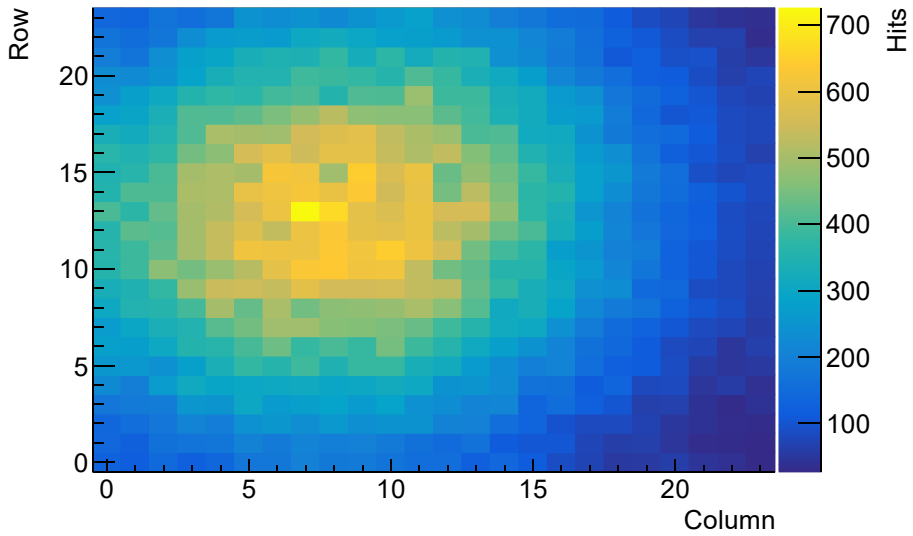
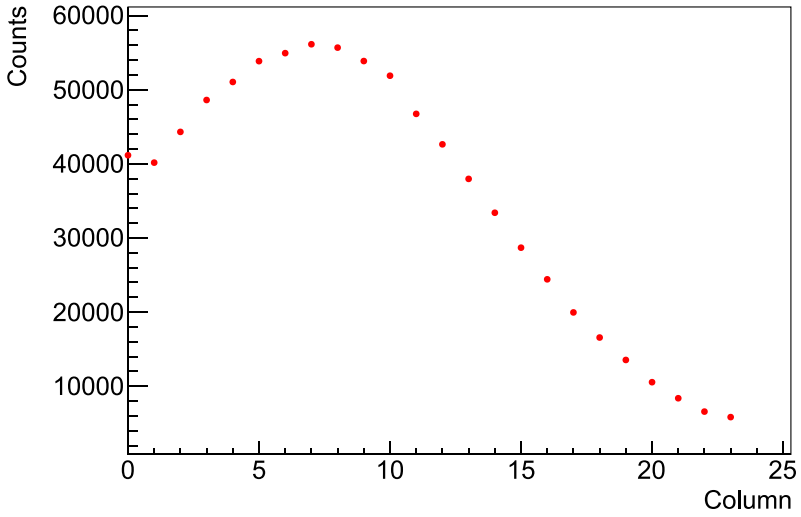
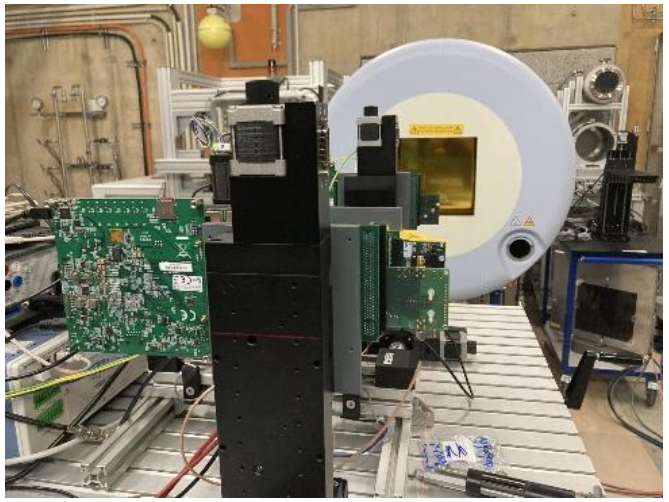


Image of the carbon beam obtained with counters

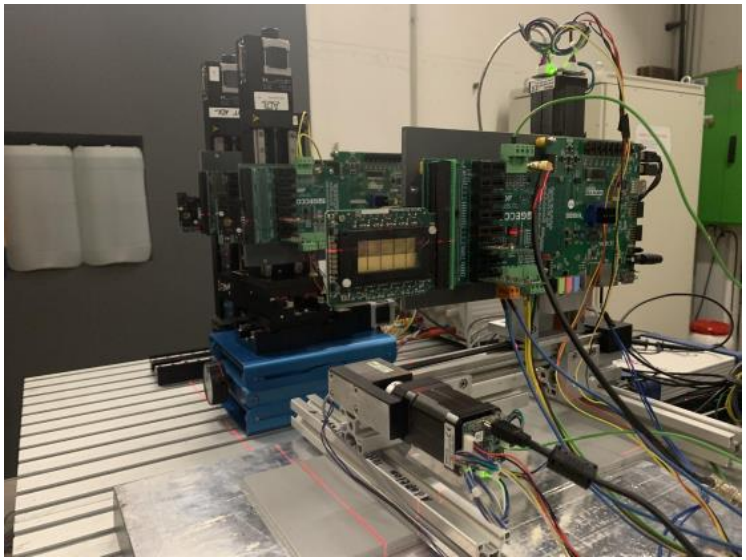


The adders of at the end of each column allow measurement of the beam projection. The beam intensity was 2×10^6 carbon ions/s at an energy of 423.44 MeV/u.

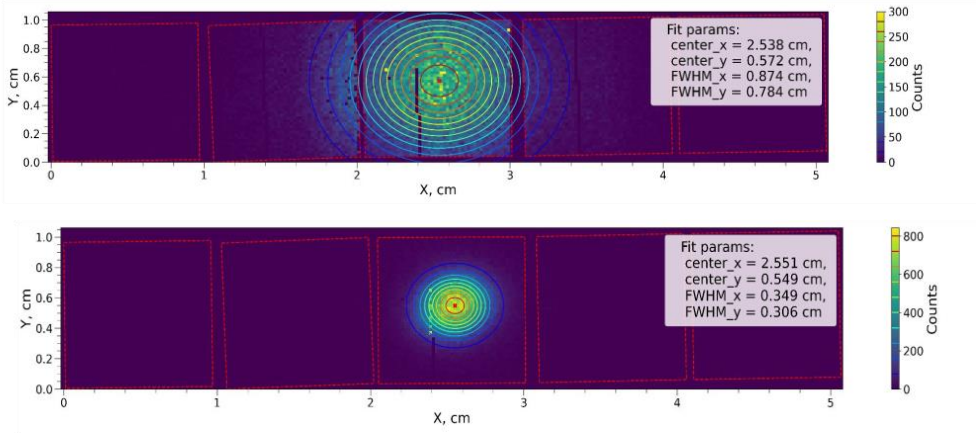
- Tests in magnetic field have been performed



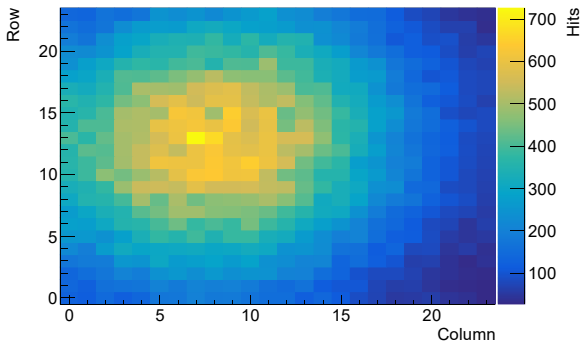
- Multichip modules have been built
- Better resolution with new chips

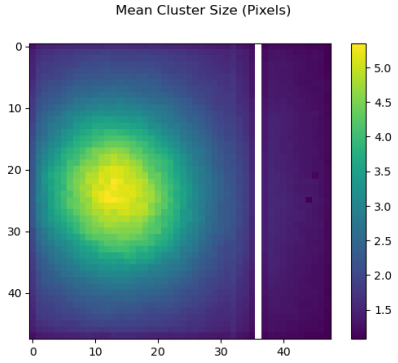


Proton beam



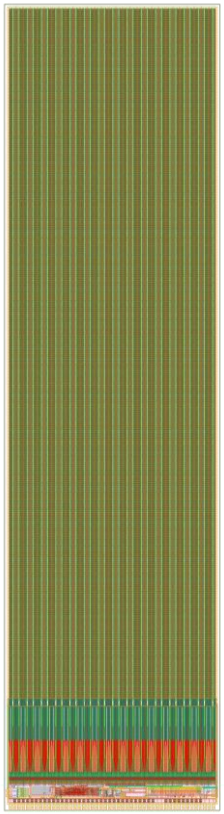
Beam scan

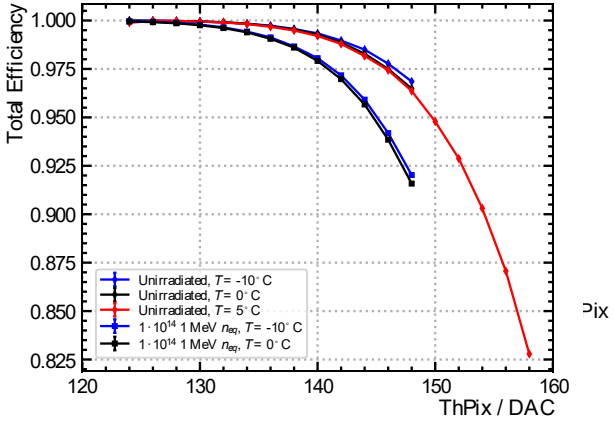




OTHER PROJECTS

- Further developments
- MightyPix
- Sensor chip for tracking detector upgrade at LHCb
- The Mighty Tracker is the planned upgrade of the downstream tracking system. It is a hybrid detector making use of both scintillating fibres (SciFi) and HV-MAPS technology.
- In total over 46000 silicon sensors should cover an area of 18 m^2

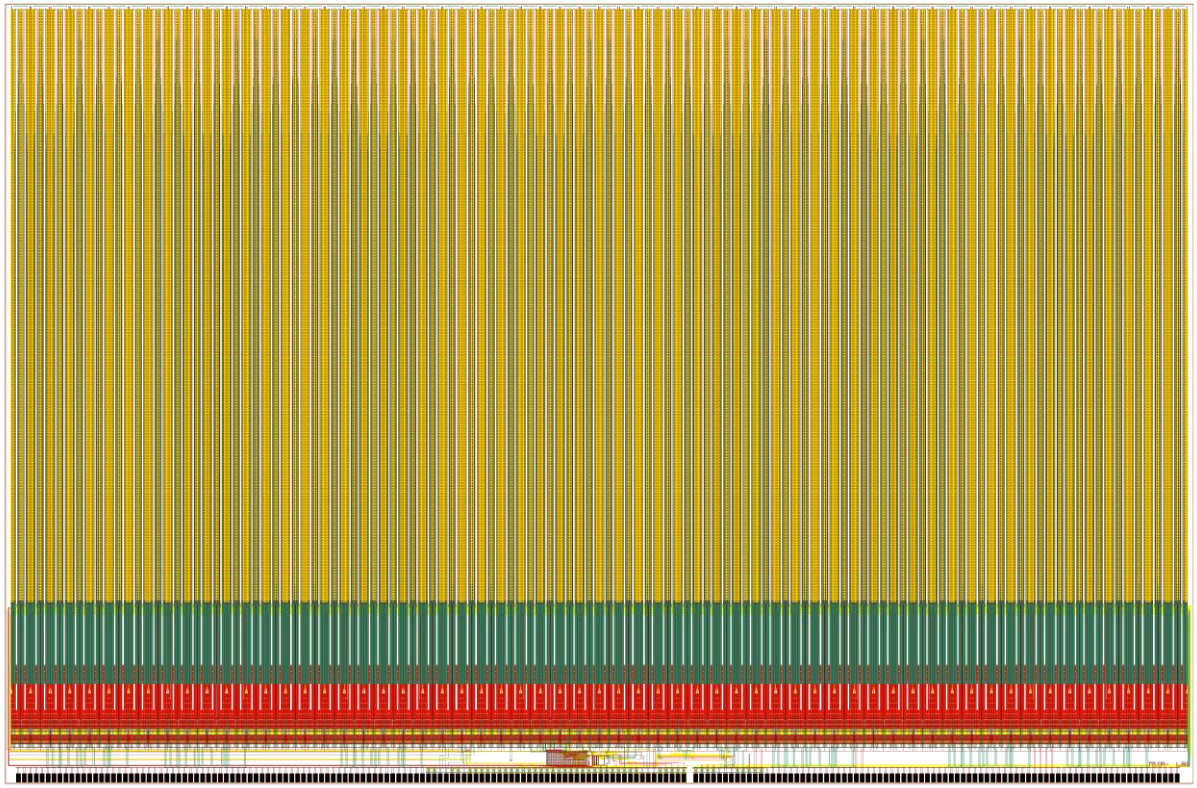


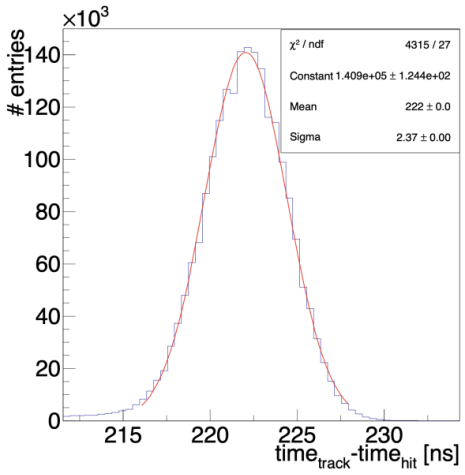


As preparation work, in 2022 we performed tests with a large HV-CMOS sensor – ATLASPIX

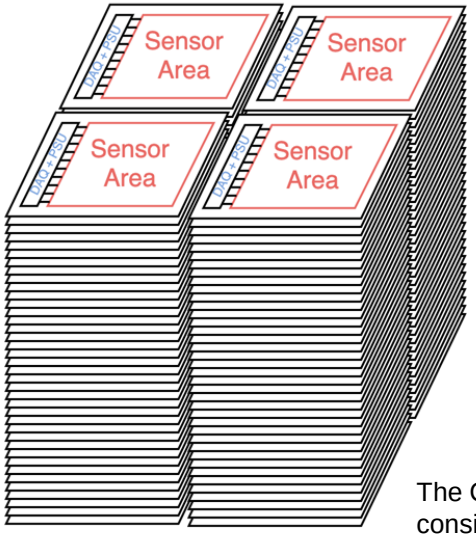
First prototype MightyPix1 has been designed and submitted within the "TELEPIX" engineering run

- TelePix - large HVCMOS sensor (sensor area 1cm x 2cm) for DESY telescope upgrade. The pixel width is 25µm. Produced in an engineering run in 180 nm HVCMOS technology by TSI.
- Uses deep p-well and CMOS comparator
- TDC in every hit buffer
- Time resolution of 3.45ns measured with large chip

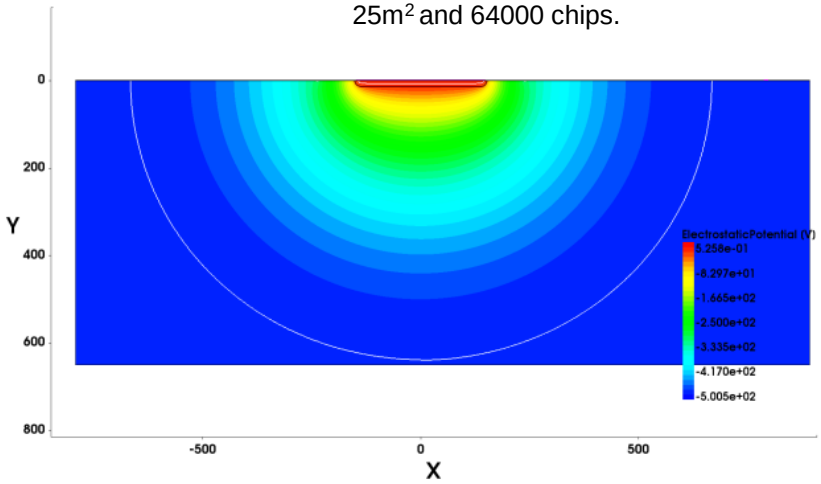




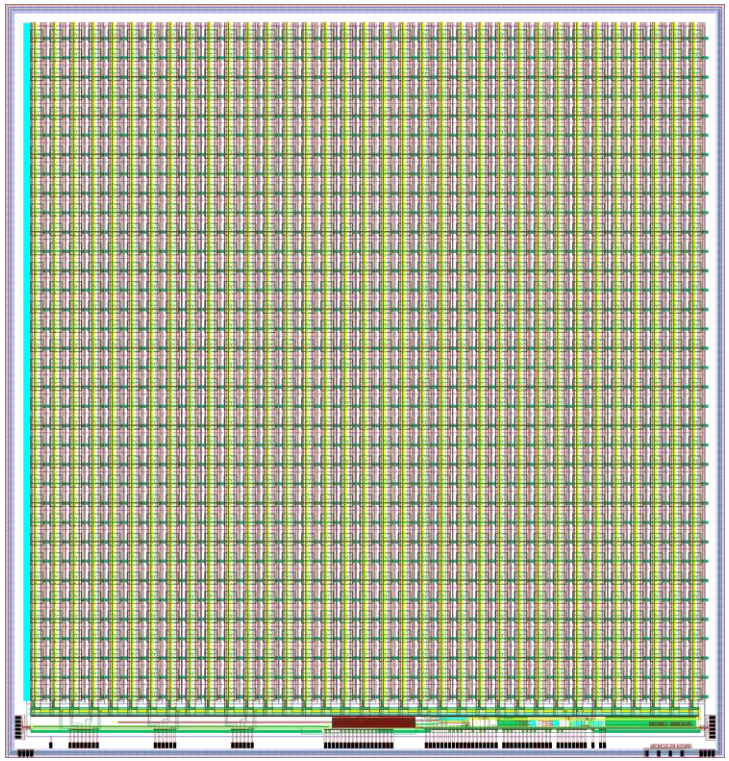
- ASTROPIX will be a HV-CMOS monolithic sensor with very low power consumption and fully depleted substrate.
- Sensor for Compton telescope



The Compton telescope would consist of 40 layers, with total area of 25m^2 and 64000 chips.

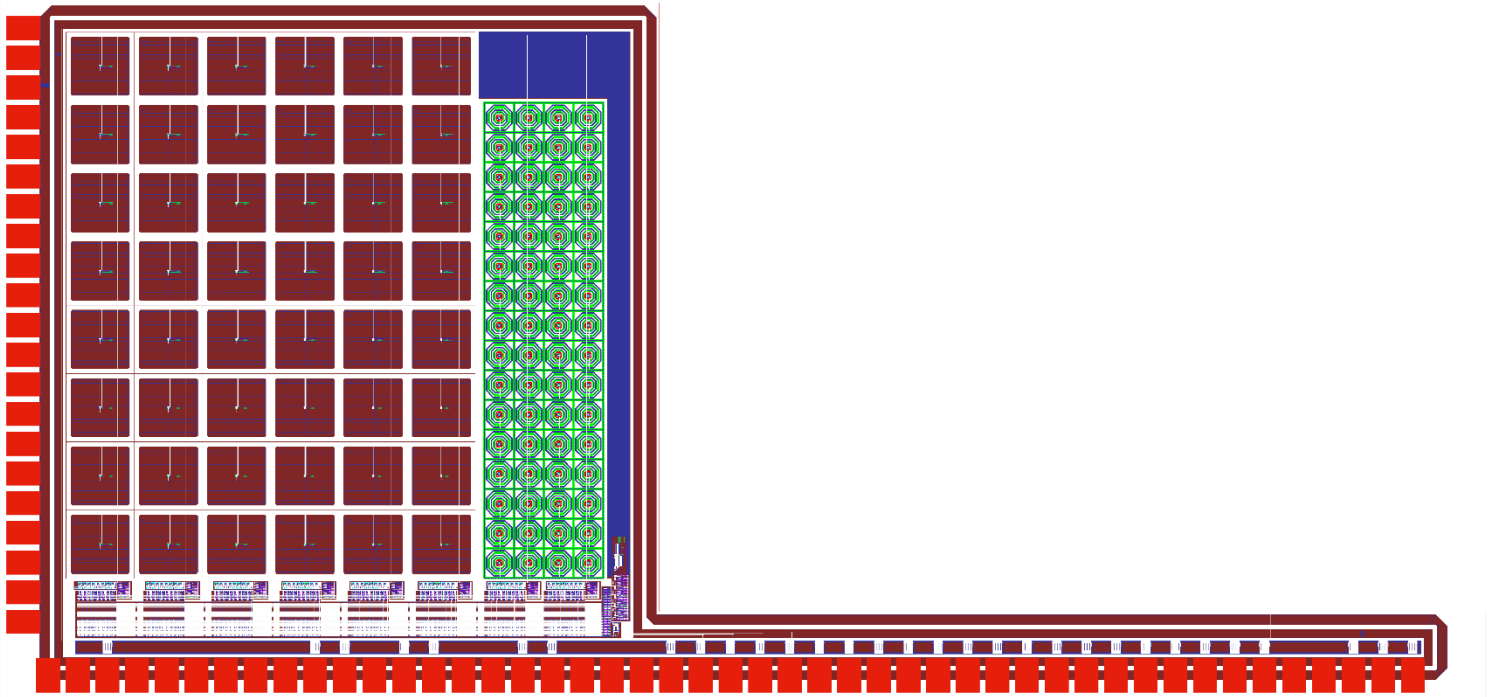


Simulation of full depletion

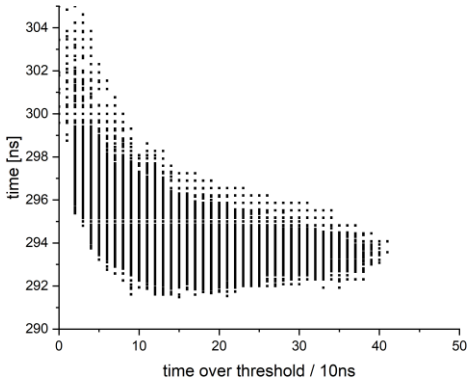


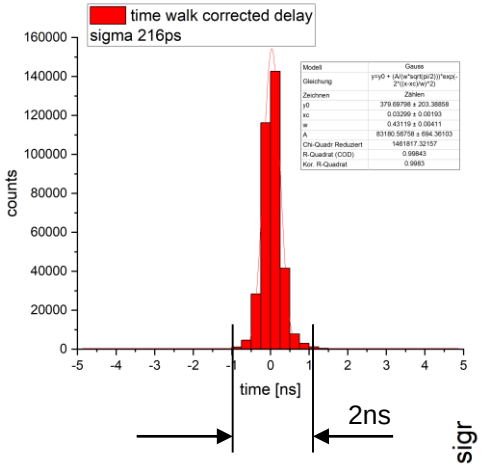
A full reticle prototype ASTROPIX3 (area 4cm^2)

- PicoPix in SiGe BiCMOS
- Sensor for Mu3e-upgrade timing layer
- Goal: 100ps time resolution



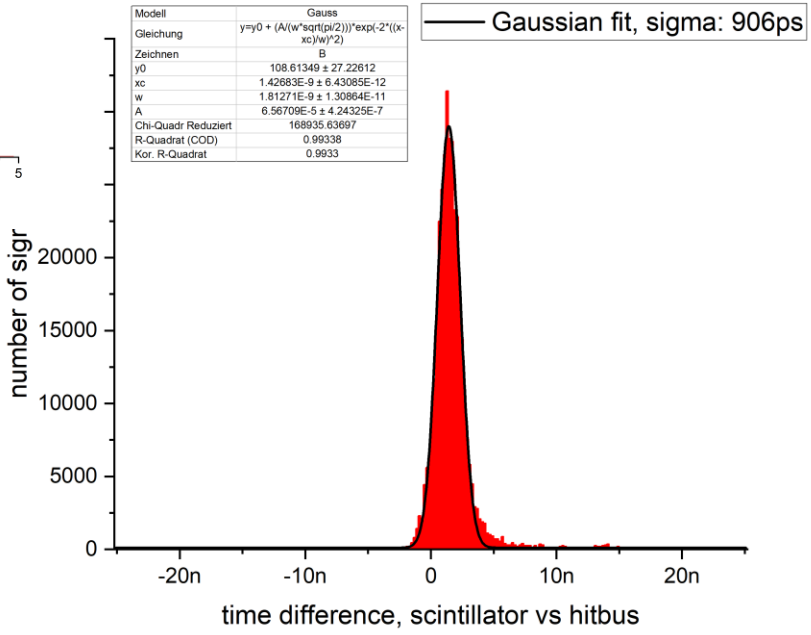
- CMOS-alternative: PicoPix in TSI HV-CMOS 180nm technology
- Pixel size 165µ x 165µm
- Novel voltage amplifier





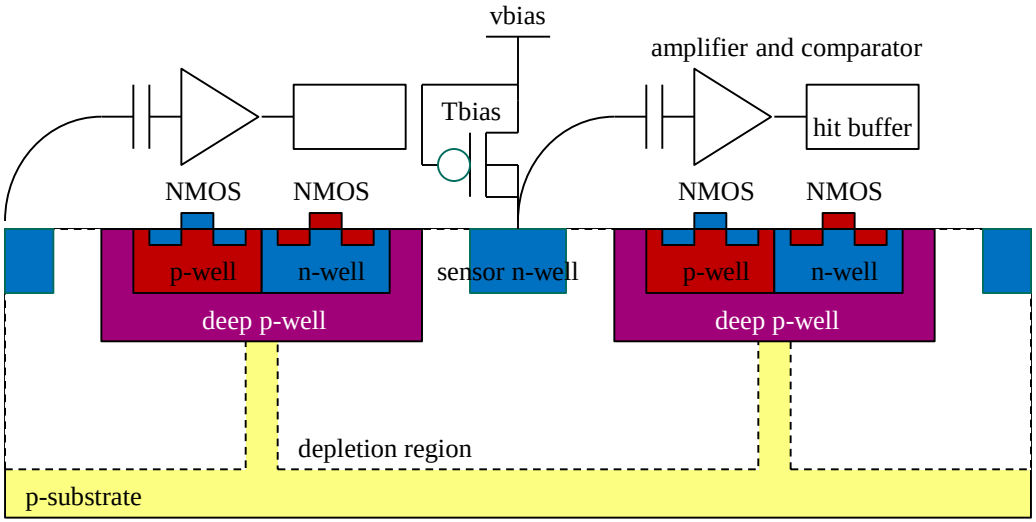
Time walk of a few ns can be corrected

=> Time resolution measured with injection for signals > 3000e is 216ps

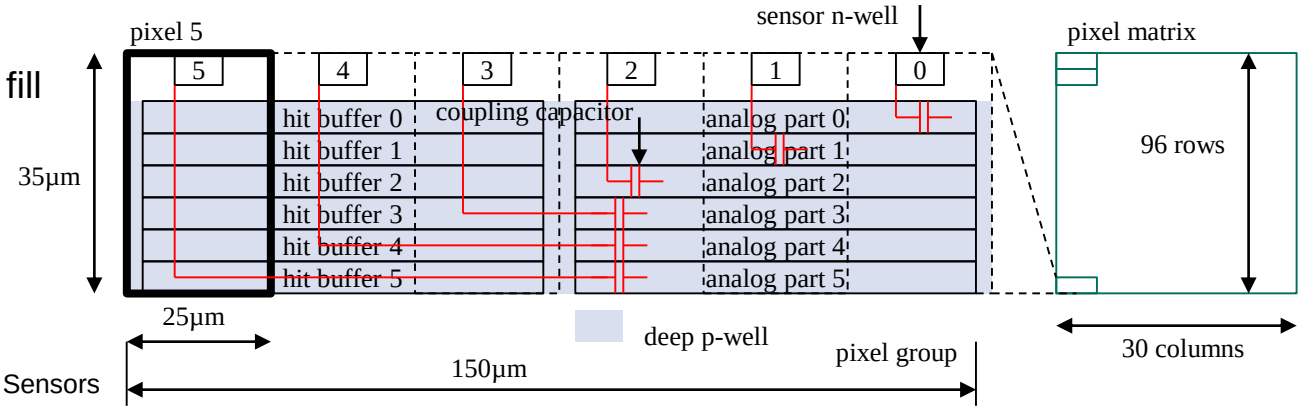


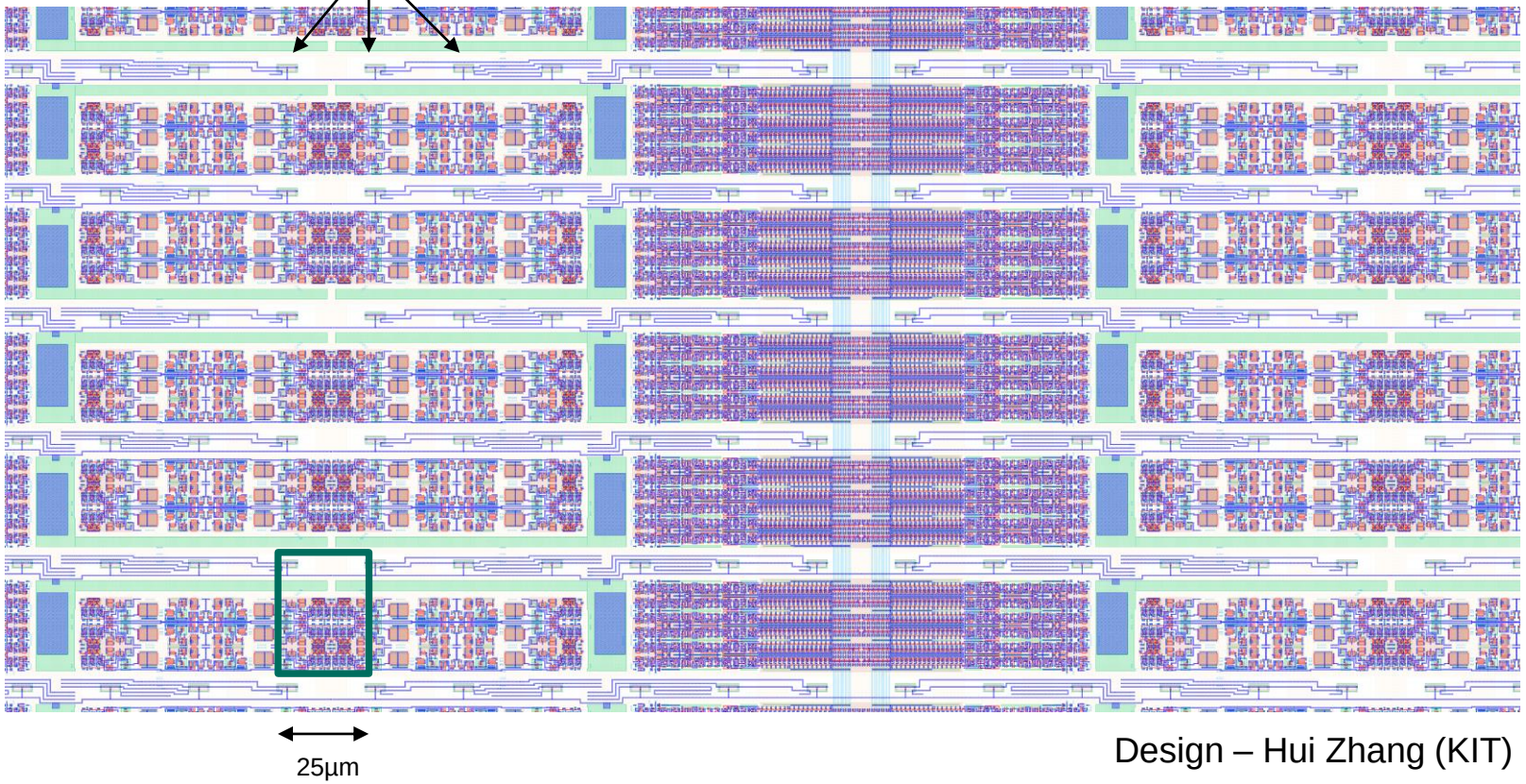
Time resolution measured with Sr-90 about 0.9ns

- H25: A test matrix with DMAPS-like pixels (low fill factor) that use deep p-well. The pixel size is 35µm x 25µm



- H25: A test matrix with DMAPS-like pixels (low fill factor) that use deep p-well. The pixel size is 35µm x 25µm





Design – Hui Zhang (KIT)