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Ultra-thin hybrid pixel detectors

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Dortmund

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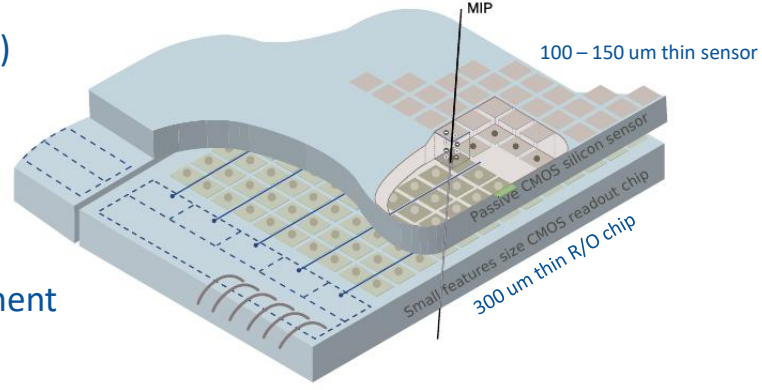
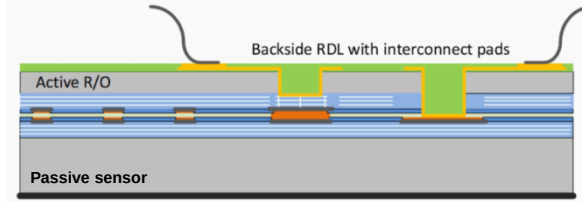
ULTRA-THIN HYBRID PIXEL DETECTORS

- Main idea: reduce material budget, i.e. detector thickness as much as possible while keeping benefits of hybrid approach
  - Separate development of two entities (sensor + R/O electronics)
  - Fine-pitch interconnection between R/O channels and sensor channels
  - Thinning of R/O chip and sensor to minimum
- Goal: Ultra-thin hybrid pixel detector -> for future tracking experiment
  - 50 – 100 um thin pixel sensor
  - ~20 um thinned R/O chip
- Need of different bonding technique

Standard hybrid pixel detector



Ultra-thin hybrid pixel detector



WAFER-TO-WAFER BONDING

- Special technique required to realise ultra-thin hybrid pixel detectors -> **Wafer-to-wafer bonding**
  - Allows for fine pitch bonding (down to a few micrometer)
  - Thin sensor-chip stacks
- Important: Requires „matching“ wafers for sensor and R/O chip
  - Same wafer diameter -> typically 200/300 mm wafers
  - Same wafer arrangement of structures

  ➔ Timepix3 as readout chip

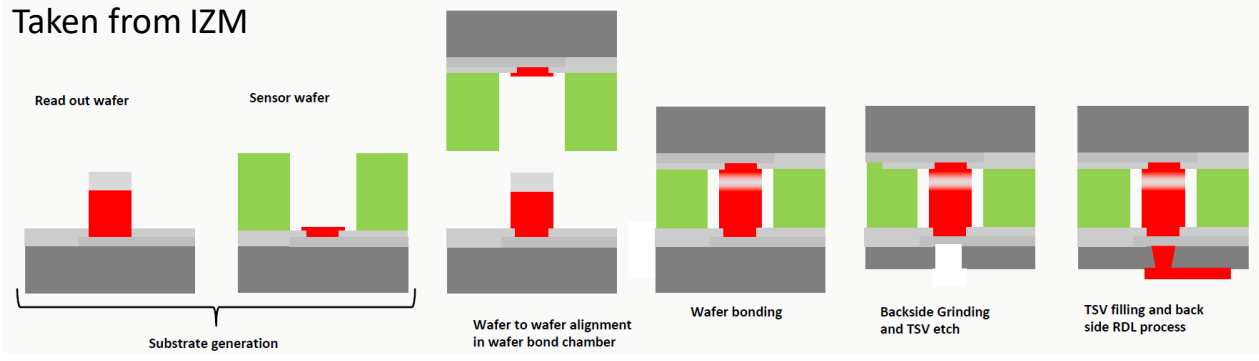
  ➔ Dedicated submission of passive CMOS LFoundry sensors matching the Timepix3 layout

W2W BONDING – PROCESS FLOW

- Process developement currently done by IZM (including thinning)
- Readout chip wafer with Cu/SnAg pillars (red)
- Cu/Sn bonds will be supported by spin coated, photo-structured polymer layer (green) applied to sensor wafer

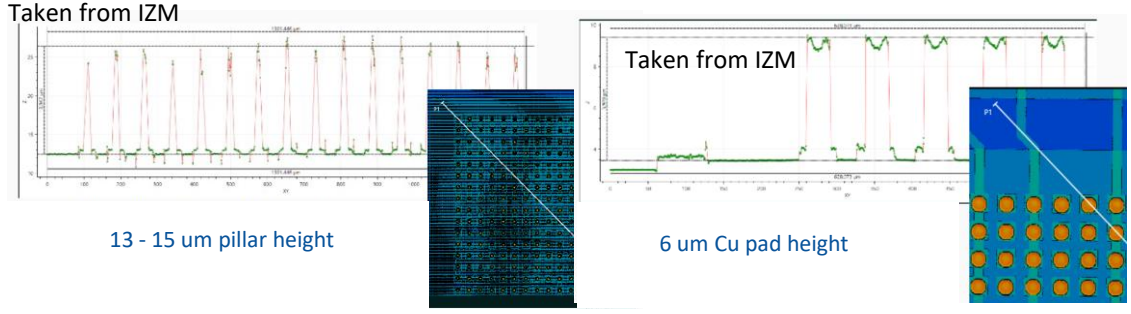
-> polymer hybrid wafer bonding

- Bonding (simplified): wafers joined by applying pressure and thermal curing



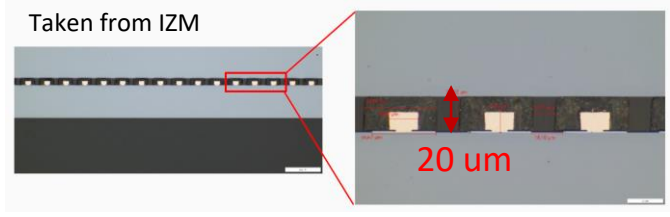
W2W BONDING – PROCESS EVALUATION

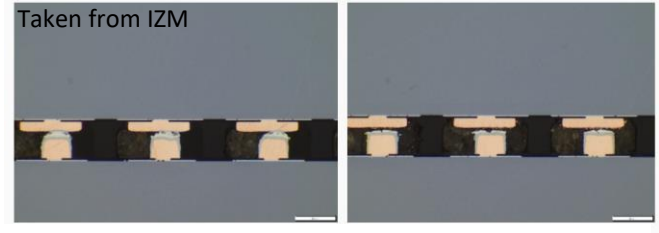
- Many process parameters to optimise:
  - Type of polymer
  - Bond layer thickness
  - Planarity
  - Curing temperature
  - Pressure
  - …..
- Preliminary process results:
  - 20 um polymer layer thickness
  - 13 - 15 um pillar height (across wafer)
  - 4 – 6 um Cu pad height
  - Good solder transfer from CuSnAg-pillar to Cu pad, but some are not connected



13 - 15 um pillar height

6 um Cu pad height

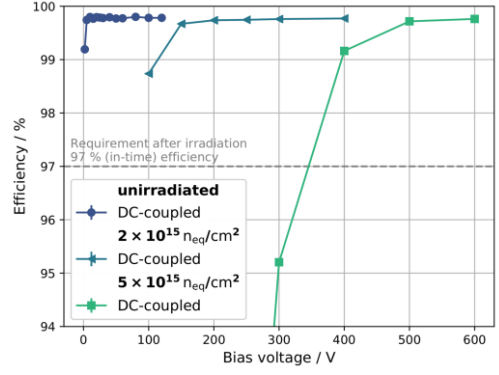


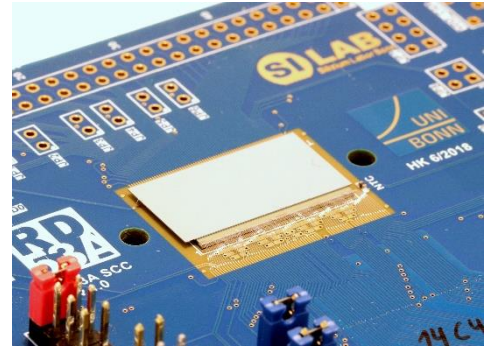


connected not-connected

CMOS PIXEL SENSOR - RECAP

- Starting point for sensor: passive CMOS sensors developed in LFoundry 150 nm technology
- Radiation tolerant n-in-p pixel design in 150 nm CMOS technology
- CMOS fabrication process offers 200 mm wafers -> fit to Timepix3 wafers
- Towards „thin hybrid sensor“:
  - Copy layout from former submissions
  - Adjust pixel size to Timepix3
  - Dedicated wafer layout matched to Timepix3 wafer



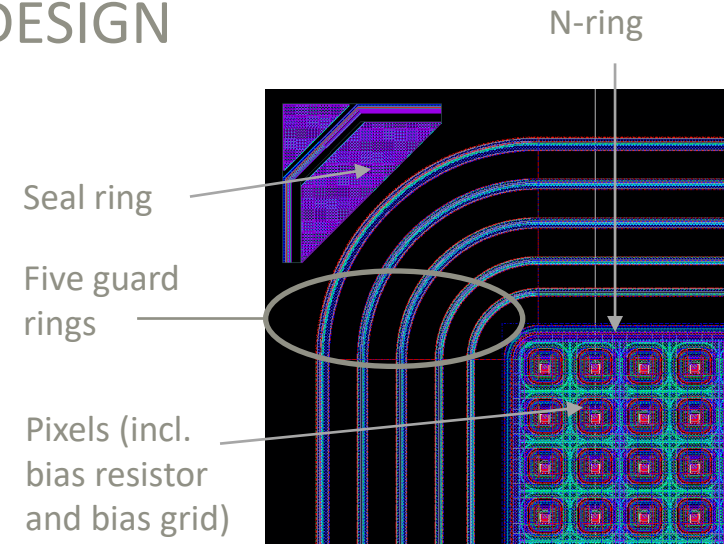


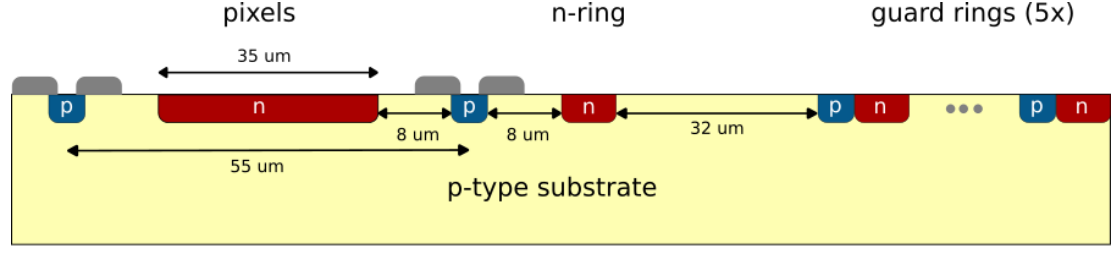
More information about passive CMOS sensors:

“Development and Characterisation of Passive CMOS Sensors for Pixel Detectors in High Radiation Environments”, Y. Dieter

CMOS PIXEL SENSOR - DESIGN

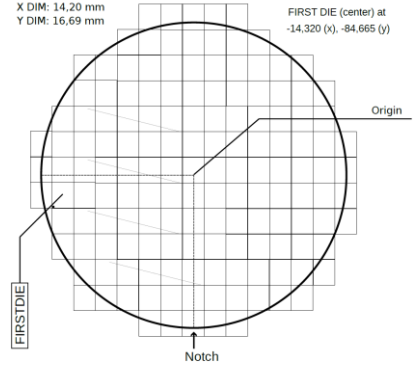
- Strategy: „copy“ layout from former passive CMOS submissions in LFoundry
  - Match pixel size with timepix3 pixel size -> 55 um pixels
  - Increase n-well size to 35 um -> keep 8 um spacing between n-well and p-stop
  - Poly-silicon bias resistor implemented (and bias grid)
  - N-ring surrounding the pixel matrix -> 32 um spacing between n-ring and p-well (from 1st guard ring)
  - Five n+p guard rings

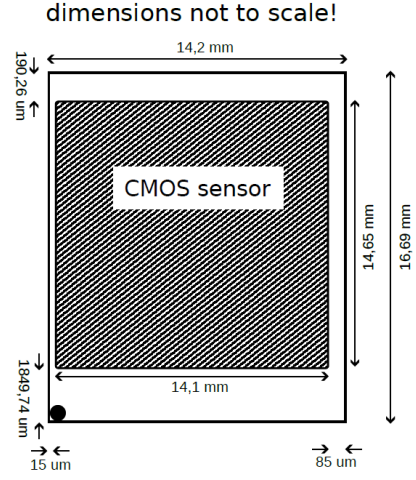




CMOS PIXEL SENSOR - SUBMISSION

- Full engineering run at LFoundry
  - Wafer2wafer bonding requires custom wafer layout
  - Reticle has to match with Timepix3 for proper overlay
- Will get 25 wafers on high-resistivity Cz-Si and 150 um thickness
- Final details to be discussed with LFoundry
- Aim to start engineering run end of June





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SUMMARY

- Goal of AIDA project is ultra-thin hybrid pixel detector using wafer-to-wafer bonding technique
  - 50 – 100 um thin sensor (passive CMOS sensor)
  - ~20 um thin readout chip (Timepix3)
- Wafer-to-wafer bonding technique currently established at IZM
- Dedicated submission of passive CMOS sensors in 150 nm LFoundry process on the way

Thank you for your contribution to the
submission of the passive CMOS sensors!

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BACKUP

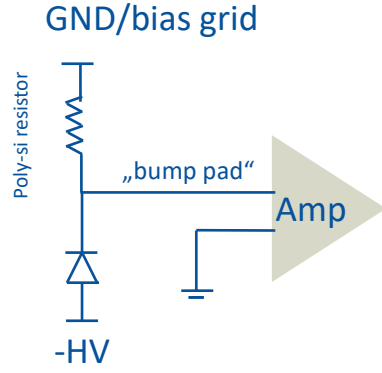
LAYOUT VERIFACTION

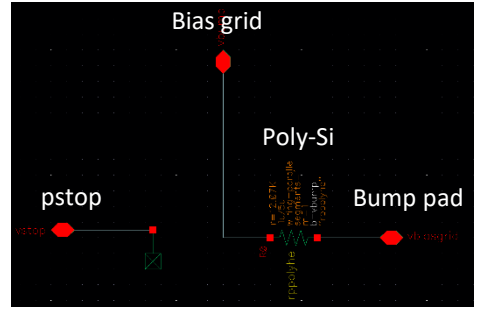
- Design rule checks (DRC)
  - Checks if spacings, width, ovelaps, etc. of various layers are ok to ensure proper production of layout
  - „Geometrical“ check

  ➔ Found a few DRC violations in design which should have been also present in former submissions (to be discussed with foundry)

- Layout vs schematic (LVS) -> thanks Ned for helping me!!
  - Checks if (drawn) layout is equal to schematic
  - „Connectivity“ check

  ➔ LVS is clean





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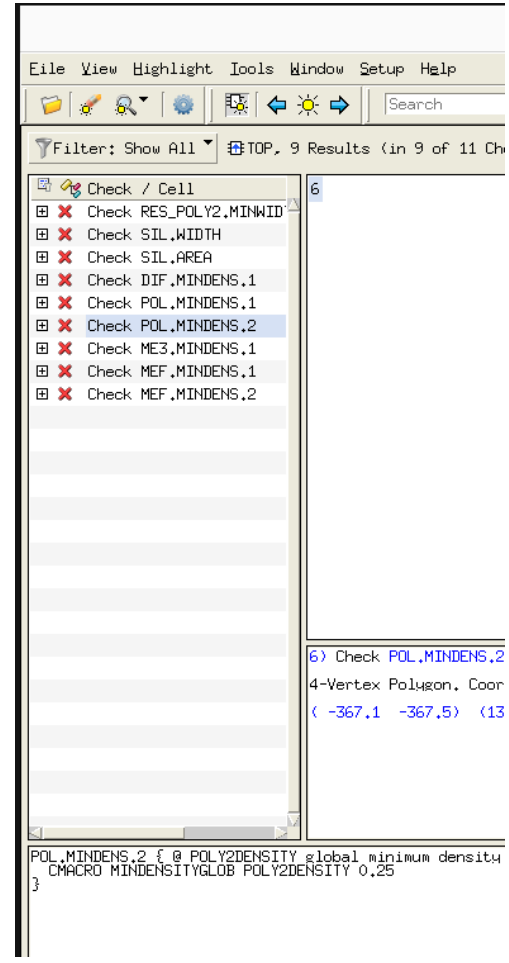
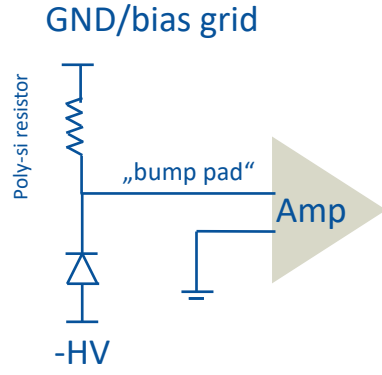
DRC

- A few DRC violations
- RES_POLY2.MINWIDTH:
  - poly-silicon bias resistor width is 0.15 um (< 1.0 um)
  - done in the same way as in former submissions -> okay?
- SIL.WIDTH/AREA:
  - passivation opening of pads too small (12 x 12 um octagon)
  - done in the same way as in former submissions -> okay?
- Various density checks on DIFF, POLY2 ME3/F



LAYOUT VS SCHEMATIC

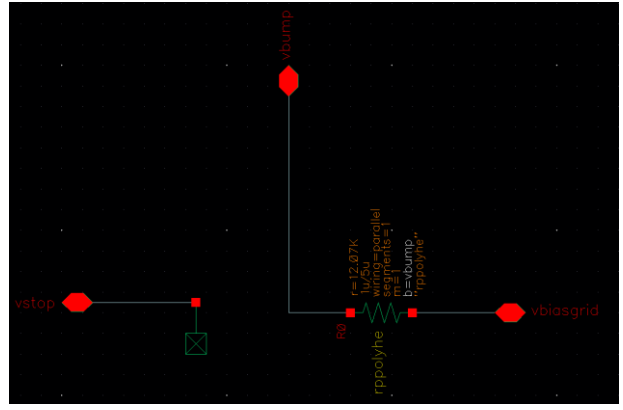
- Check if physical layout corresponds to schematic of „pixel“
- LVS run on single pixel and top layout to check „wiring“ of pixels:
  - Bias grid
  - Polysilicon bias resistor
  - Bump pads
  - Floating pstop

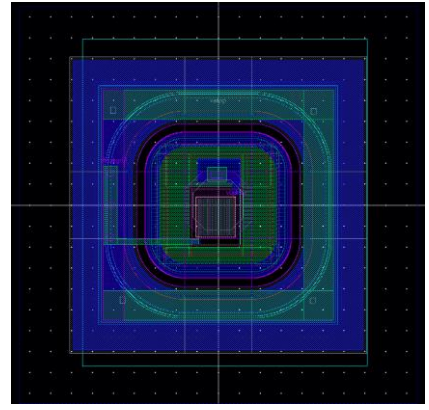


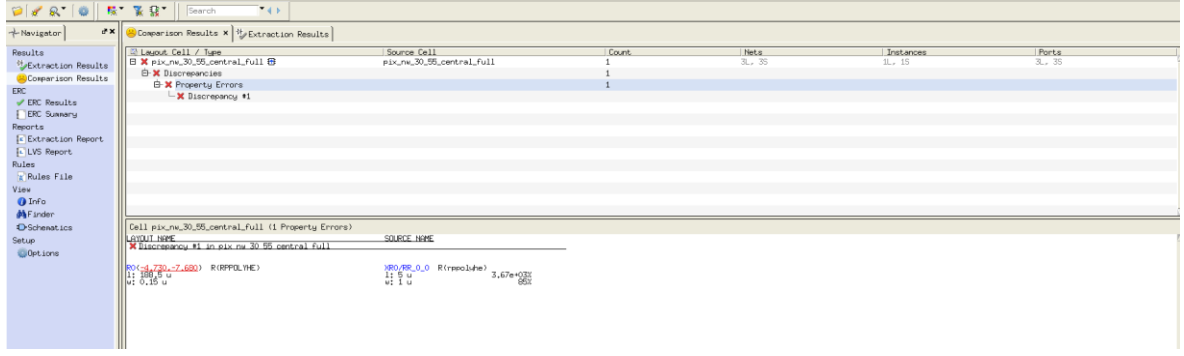
LVS – SINGLE PIXEL

- Created complete single pixel:
  - Implantations, pstop, ….
  - Bias resistors and „bias grid“
  - Bump pad
- Pins:
  - Connection to bias grid: vbiasgrid (M_F)
  - Connection to bump: vbump (M_F)
  - Connection to pstop: vpstop (M2)

-> „clean“ LVS (except polysilicon discprepancy in L/W, but expected)

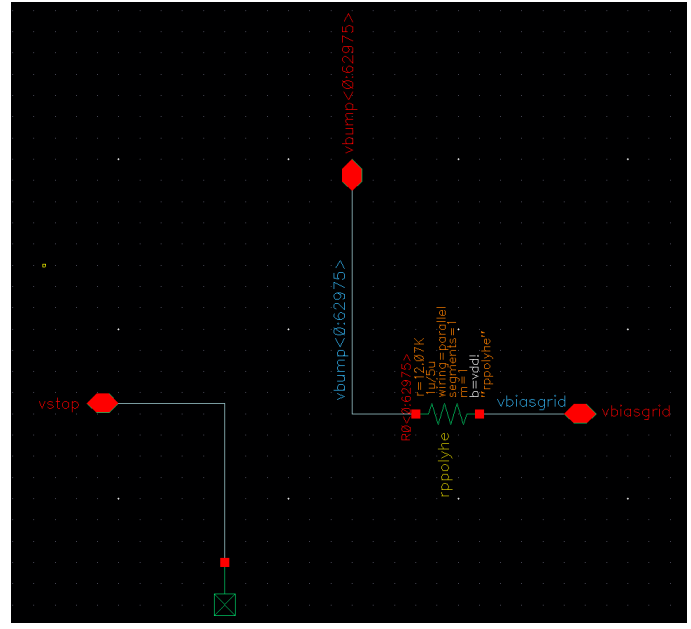






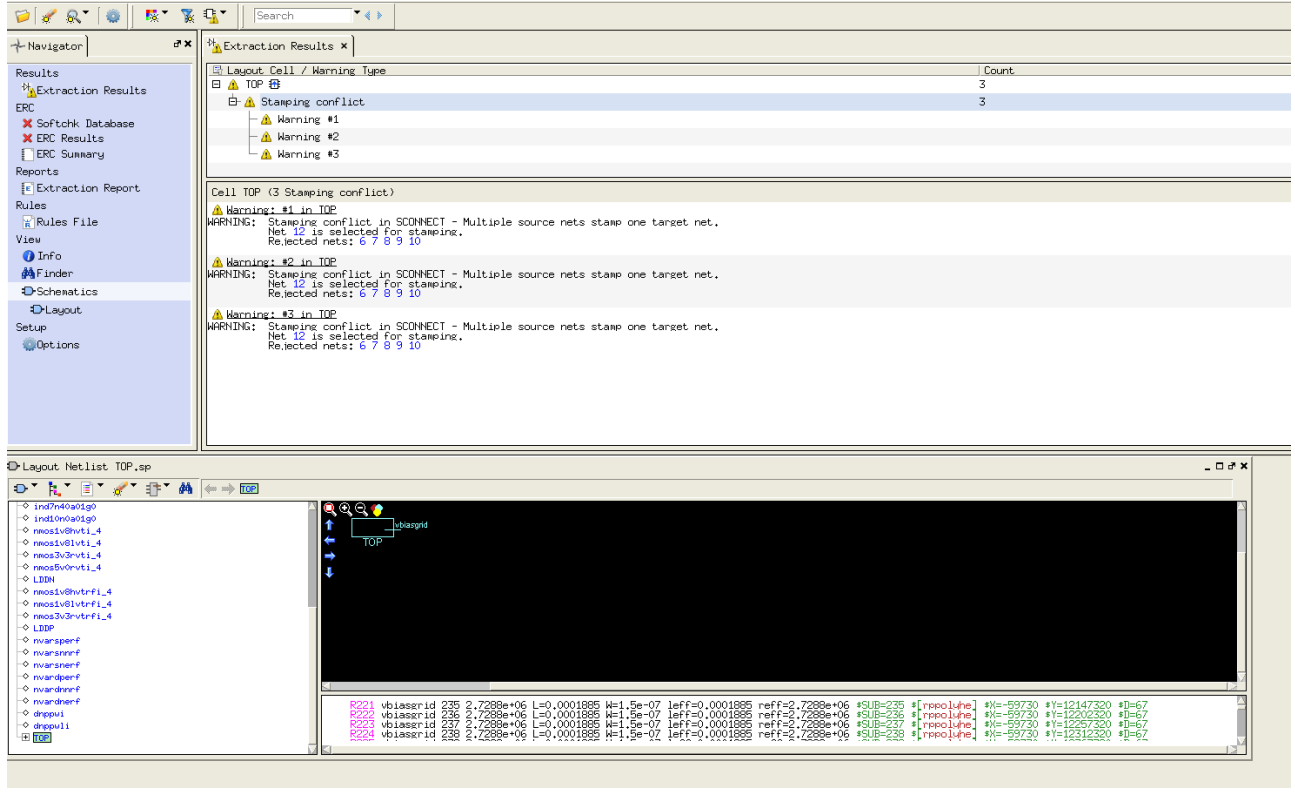
LVS - FULL PIXEL ARRAY (1)

- Full pixel array: 256 x 246 pixels (62976 pixels)
- Schematic:
  - Bias grid connected via 62976 polysilicon bias resistors to 62976 bump pads
  - Floating pstop (not connected)
- Pins:
  - 2x bias grid probing pad (check if those are properly wired): vbiasgrid
  - 62976x bump pad: vbump



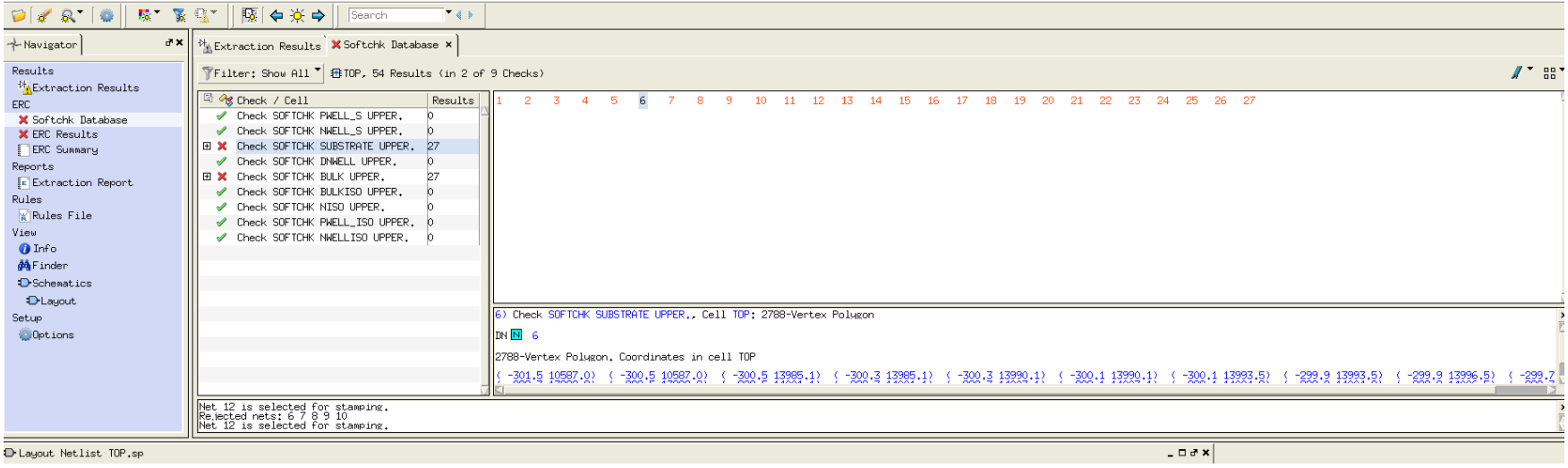
LVS - FULL PIXEL ARRAY (2)

- Warning is actually good
- We created two labels of „vbiasgrid“ (bottom and top probing pad)
- „Stamping conflict“ tells us that the two labels are on the same net, i.e are connected



LVS - FULL PIXEL ARRAY (3)

- Soft connectivity check



LVS - FULL PIXEL ARRAY (4)

- Electrical rule checks