

Ultra-thin hybrid pixel detectors

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Dortmund

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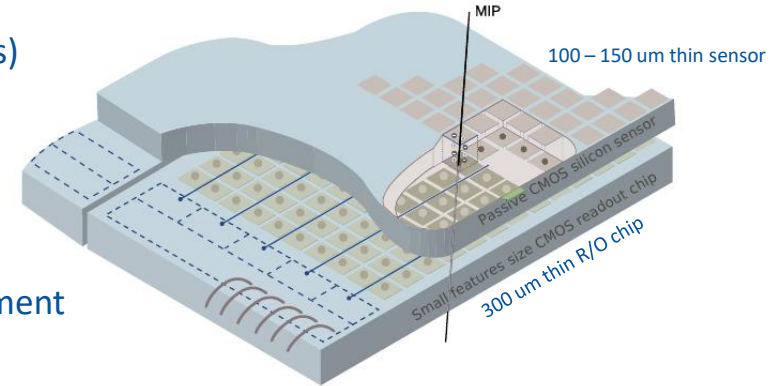


ULTRA-THIN HYBRID PIXEL DETECTORS

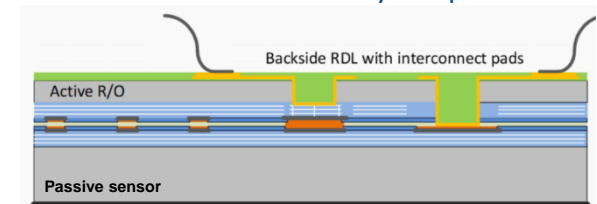


- Main idea: reduce material budget, i.e. detector thickness as much as possible while keeping benefits of hybrid approach
 - Separate development of two entities (sensor + R/O electronics)
 - Fine-pitch interconnection between R/O channels and sensor channels
 - Thinning of R/O chip and sensor to minimum
- Goal: Ultra-thin hybrid pixel detector -> for future tracking experiment
 - 50 – 100 um thin pixel sensor
 - ~20 um thinned R/O chip
- Need of different bonding technique

Standard hybrid pixel detector



Ultra-thin hybrid pixel detector

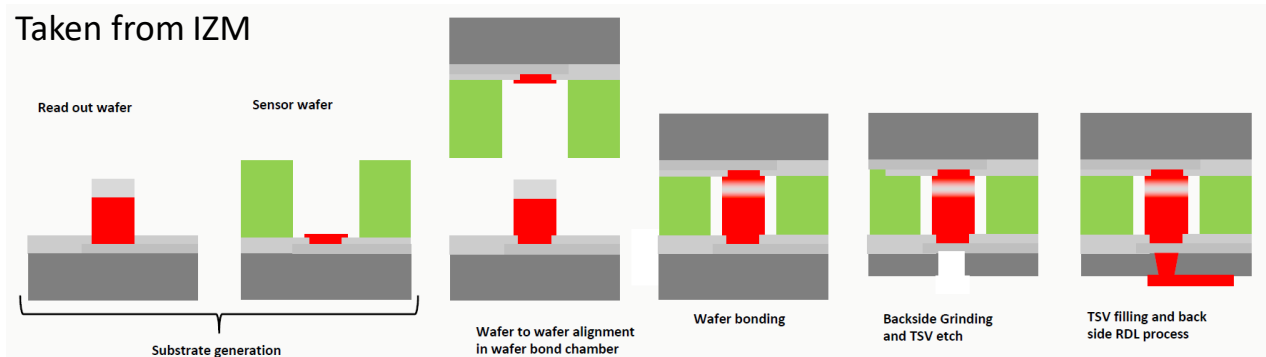


WAFER-TO-WAFER BONDING

- Special technique required to realise ultra-thin hybrid pixel detectors -> **Wafer-to-wafer bonding**
 - Allows for fine pitch bonding (down to a few micrometer)
 - Thin sensor-chip stacks
- Important: Requires „matching“ wafers for sensor and R/O chip
 - Same wafer diameter -> typically 200/300 mm wafers
 - Same wafer arrangement of structures
 - ➔ Timepix3 as readout chip
 - ➔ Dedicated submission of passive CMOS LFoundry sensors matching the Timepix3 layout

W2W BONDING – PROCESS FLOW

- Process development currently done by IZM (including thinning)
 - Readout chip wafer with Cu/SnAg pillars (red)
 - Cu/Sn bonds will be supported by spin coated, photo-structured polymer layer (green) applied to sensor wafer
- > polymer hybrid wafer bonding
- Bonding (simplified): wafers joined by applying pressure and thermal curing



W2W BONDING – PROCESS EVALUATION

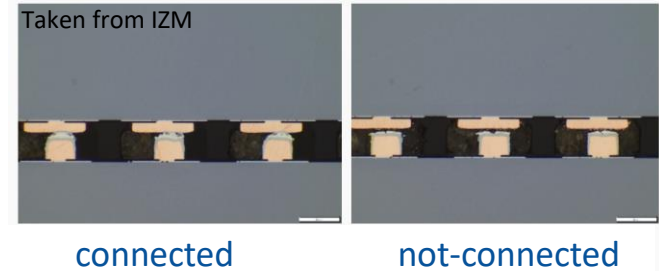
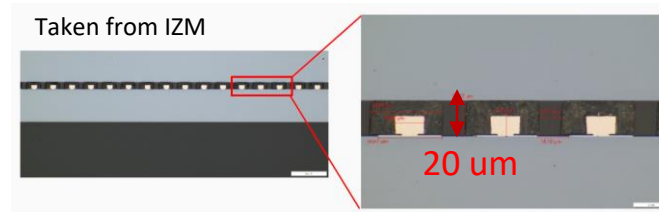
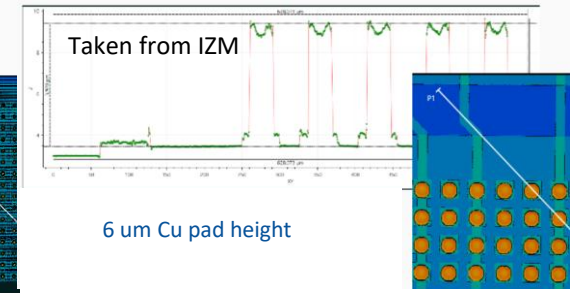
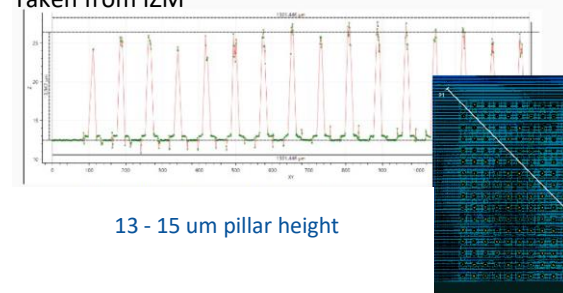
- Many process parameters to optimise:

- Type of polymer
- Bond layer thickness
- Planarity
- Curing temperature
- Pressure
-

- Preliminary process results:

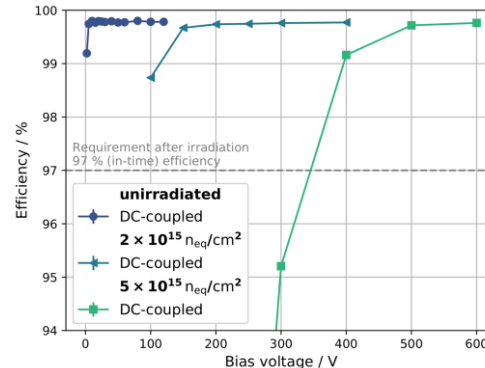
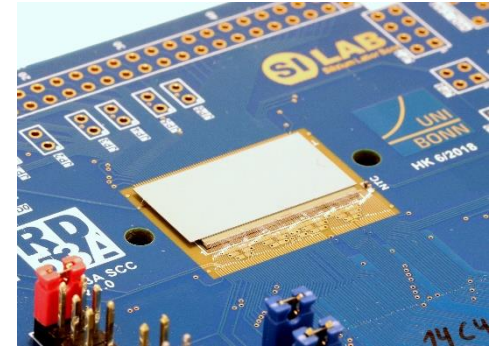
- 20 μm polymer layer thickness
- 13 - 15 μm pillar height (across wafer)
- 4 – 6 μm Cu pad height
- Good solder transfer from CuSnAg-pillar to Cu pad, but some are not connected

Taken from IZM



CMOS PIXEL SENSOR - RECAP

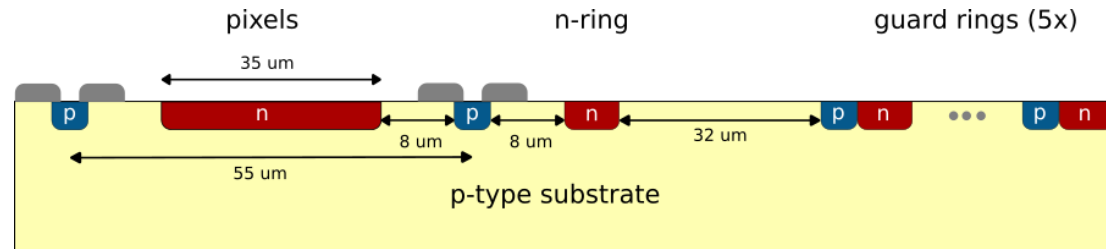
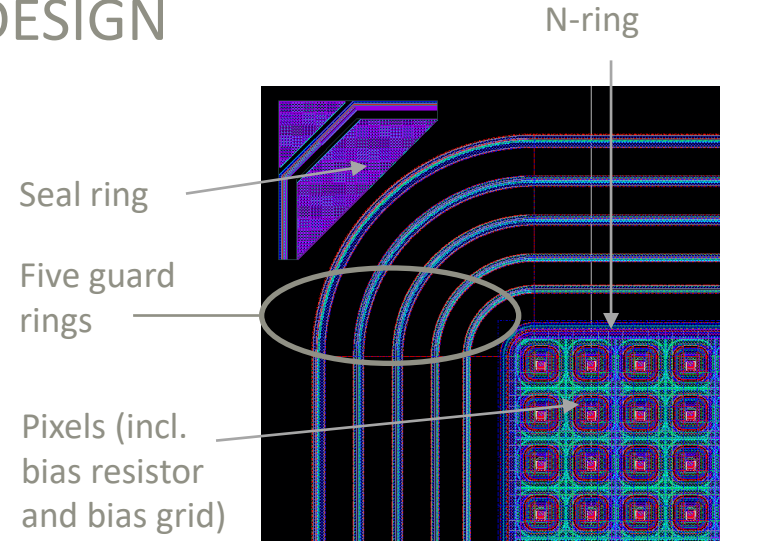
- Starting point for sensor: passive CMOS sensors developed in LFoundry 150 nm technology
- Radiation tolerant n-in-p pixel design in 150 nm CMOS technology
- CMOS fabrication process offers 200 mm wafers -> fit to Timepix3 wafers
- Towards „thin hybrid sensor“:
 - Copy layout from former submissions
 - Adjust pixel size to Timepix3
 - Dedicated wafer layout matched to Timepix3 wafer



More information about passive CMOS sensors: [“Development and Characterisation of Passive CMOS Sensors for Pixel Detectors in High Radiation Environments”, Y. Dieter](#)

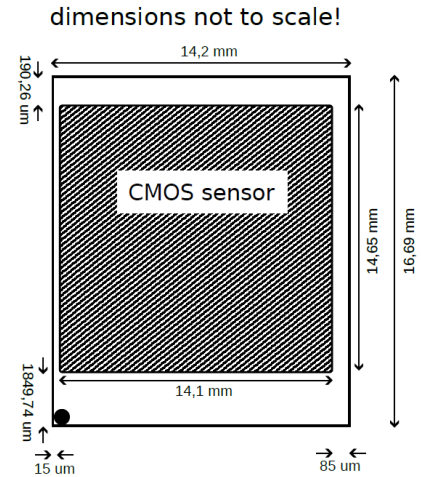
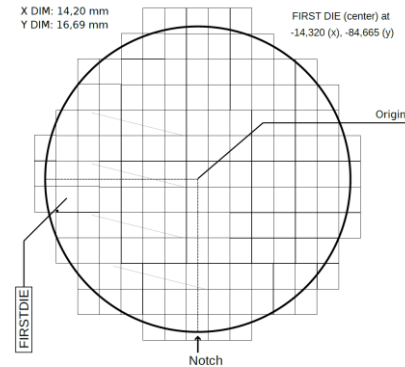
CMOS PIXEL SENSOR - DESIGN

- Strategy: „copy“ layout from former passive CMOS submissions in LFoundry
 - Match pixel size with timepix3 pixel size -> 55 um pixels
 - Increase n-well size to 35 um -> keep 8 um spacing between n-well and p-stop
 - Poly-silicon bias resistor implemented (and bias grid)
 - N-ring surrounding the pixel matrix -> 32 um spacing between n-ring and p-well (from 1st guard ring)
 - Five n+p guard rings



CMOS PIXEL SENSOR - SUBMISSION

- Full engineering run at LFoundry
 - Wafer2wafer bonding requires custom wafer layout
 - Reticle has to match with Timepix3 for proper overlay
- Will get 25 wafers on high-resistivity Cz-Si and 150 μm thickness
- Final details to be discussed with LFoundry
- Aim to start engineering run end of June



SUMMARY

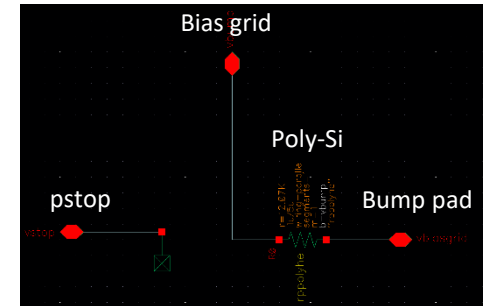
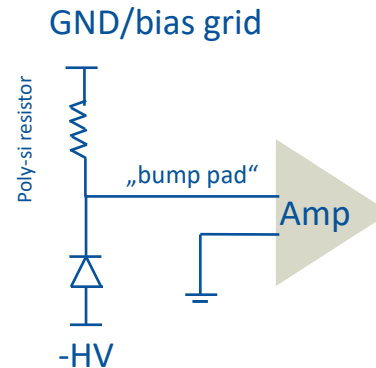
- Goal of AIDA project is ultra-thin hybrid pixel detector using wafer-to-wafer bonding technique
 - 50 – 100 um thin sensor (passive CMOS sensor)
 - ~20 um thin readout chip (Timepix3)
- Wafer-to-wafer bonding technique currently established at IZM
- Dedicated submission of passive CMOS sensors in 150 nm LFoundry process on the way

Thank you for your contribution to the
submission of the passive CMOS sensors!

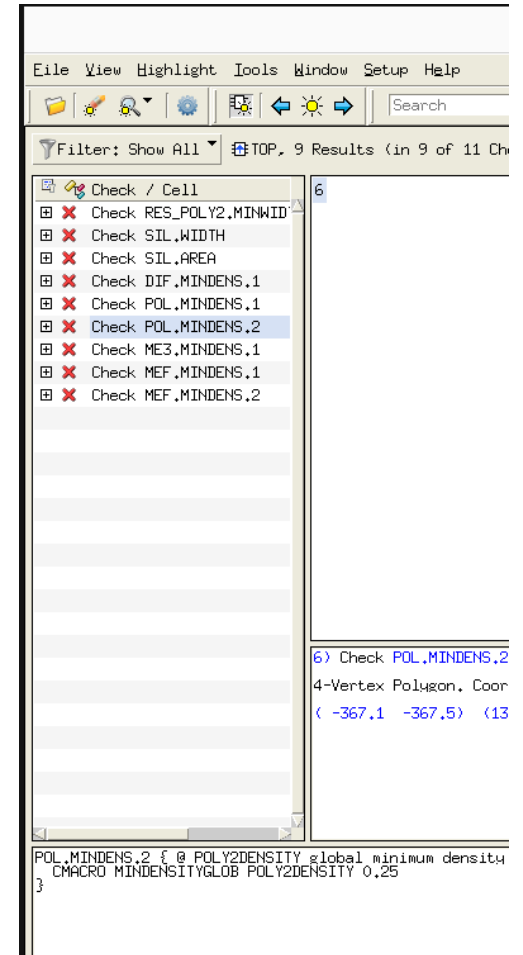
BACKUP

- Design rule checks (DRC)
 - Checks if spacings, width, overlaps, etc. of various layers are ok to ensure proper production of layout
 - „Geometrical“ check
 - ➔ Found a few DRC violations in design which should have been also present in former submissions (to be discussed with foundry)

- Layout vs schematic (LVS) -> thanks Ned for helping me!!
 - Checks if (drawn) layout is equal to schematic
 - „Connectivity“ check
 - ➔ LVS is clean

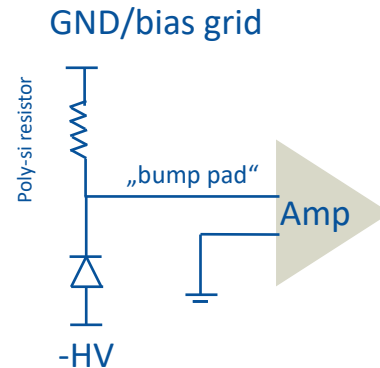


- A few DRC violations
- RES_POLY2.MINWIDTH:
 - poly-silicon bias resistor width is 0.15 μm ($< 1.0 \mu\text{m}$)
 - done in the same way as in former submissions -> okay?
- SIL.WIDTH/AREA:
 - passivation opening of pads too small (12 x 12 μm octagon)
 - done in the same way as in former submissions -> okay?
- Various density checks on DIFF, POLY2 ME3/F



LAYOUT VS SCHEMATIC

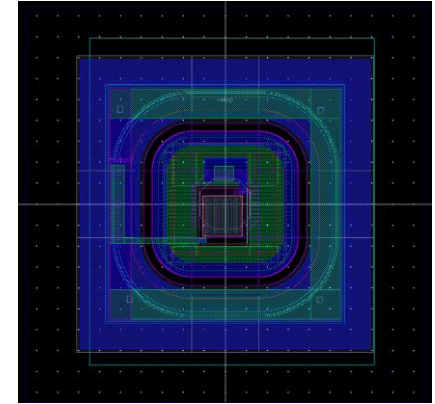
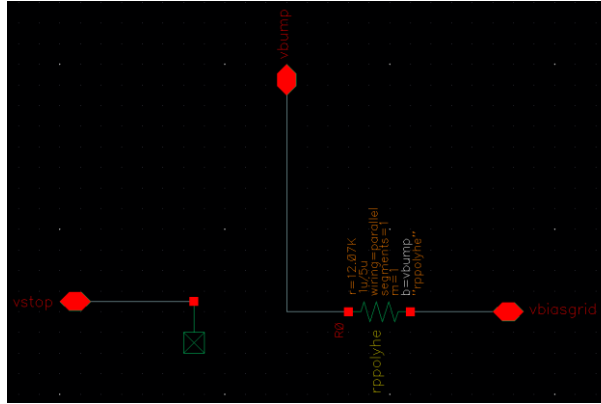
- Check if physical layout corresponds to schematic of „pixel“
- LVS run on single pixel and top layout to check „wiring“ of pixels:
 - Bias grid
 - Polysilicon bias resistor
 - Bump pads
 - Floating pstop



LVS – SINGLE PIXEL

- Created complete single pixel:
 - Implantations, pstop,
 - Bias resistors and „bias grid“
 - Bump pad
- Pins:
 - Connection to bias grid: vbiasgrid (M_F)
 - Connection to bump: vbump (M_F)
 - Connection to pstop: vpstop (M2)

-> „clean“ LVS (except polysilicon discrepancy in L/W, but expected)

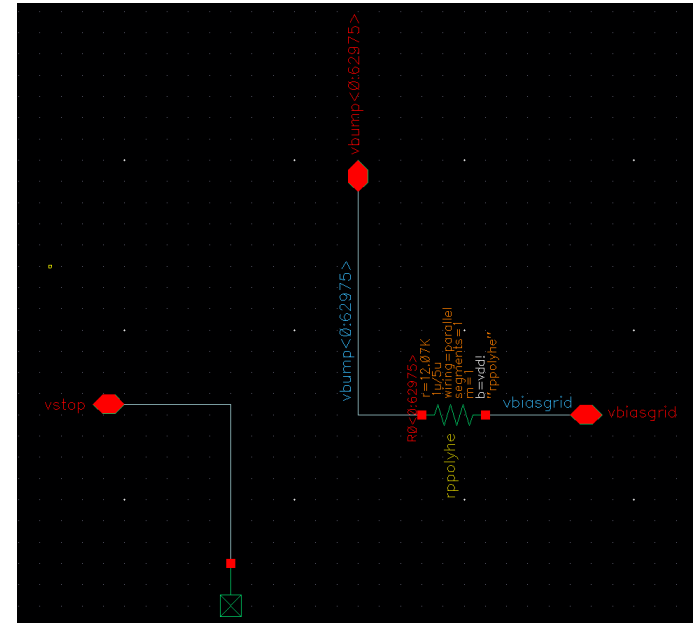


Layer	Cell	Source Cell	Count	Meta	Instances	Ports
polysil	pix_rw_30_55_central_full	pix_rw_30_55_central_full	1	SL_35	SL_15	SL_35
Discrepancies						
Property Errors						
Discrepancy #1						

CELL NAME	SOURCE NAME
Discrepancy #1 in pix_rw_30_55_central_full	
R30<-1.720e-7.600> R(RPOLYNE)	R30<-1.720e-7.600> R(RPOLYNE)
L1 0.15 u"	L1 0.15 u"
W1 0.15 u"	W1 0.15 u"
	R30<-1.720e-7.600> R(RPOLYNE)
	L1 0.15 u"
	W1 0.15 u"
	SL_35
	SL_15
	SL_35

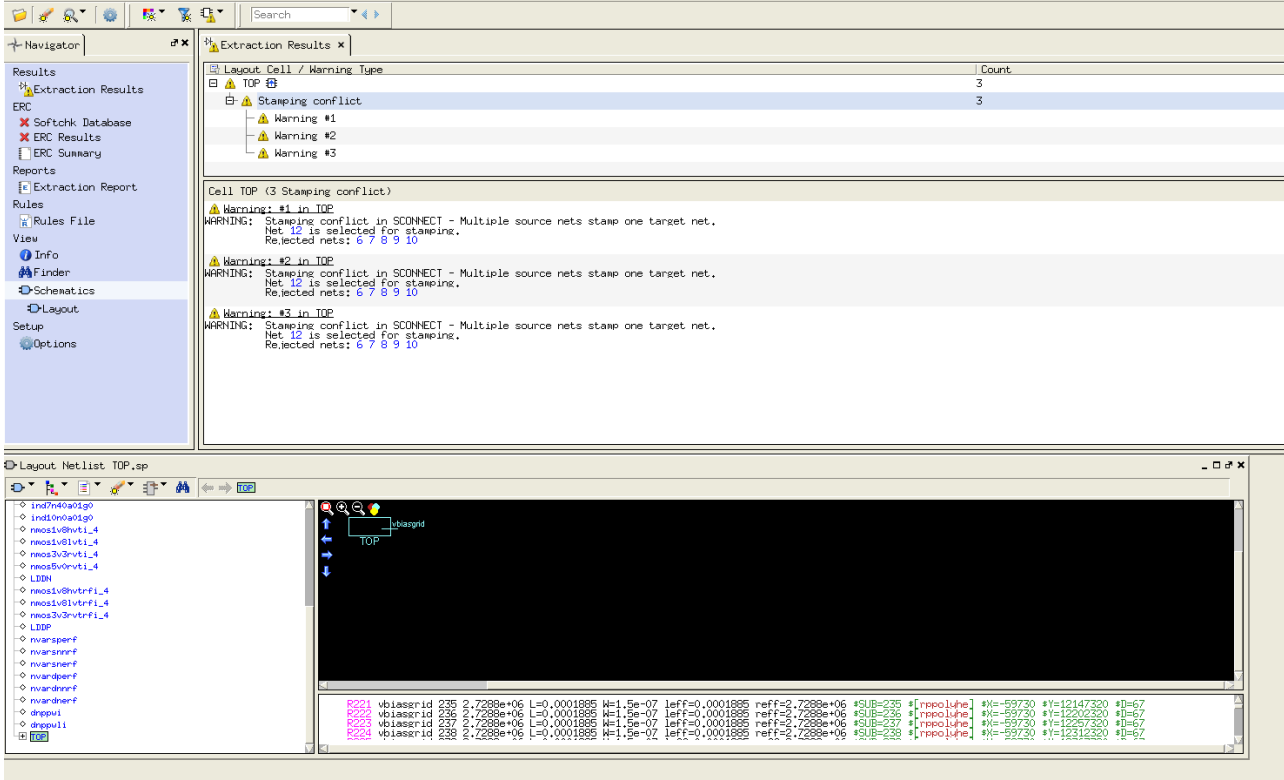
LVS - FULL PIXEL ARRAY (1)

- Full pixel array: 256 x 246 pixels (62976 pixels)
- Schematic:
 - Bias grid connected via 62976 polysilicon bias resistors to 62976 bump pads
 - Floating pstop (not connected)
- Pins:
 - 2x bias grid probing pad (check if those are properly wired): vbiasgrid
 - 62976x bump pad: vbump



LVS - FULL PIXEL ARRAY (2)

- Warning is actually good
- We created two labels of „vbiassgrid“ (bottom and top probing pad)
- „Stamping conflict“ tells us that the two labels are on the same net, i.e. are connected



The screenshot shows the LVS software interface. The top window, 'Extraction Results', displays a summary of warnings:

Layout Cell / Warning Type	Count
TOP B3	3
Stamping conflict	3
Warning #1	
Warning #2	
Warning #3	

The bottom window, 'Layout Netlist TOP.sp', shows a list of components and their properties. The netlist includes:

```

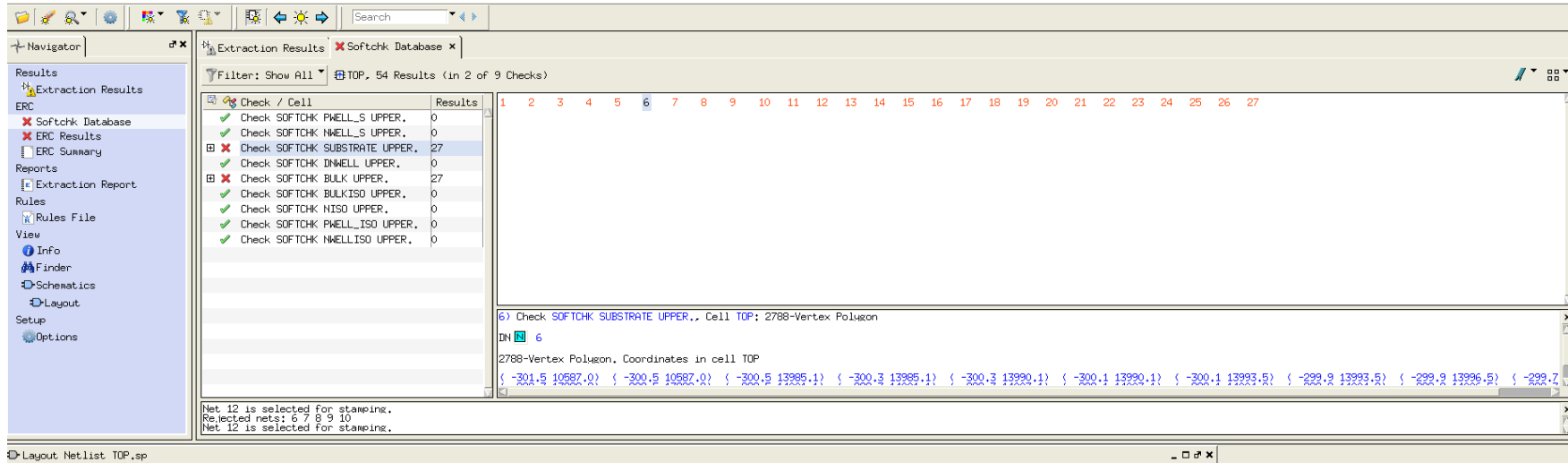
ind7nd0a01g0
ind7nd0a01g0
nm0siv8vti_4
nm0siv8vti_4
nm0siv8vti_4
nm0siv8vti_4
nm0siv8vti_4
LID01
nm0siv8vtrfi_4
nm0siv8vtrfi_4
nm0siv8vtrfi_4
LIDP
nvansperf
nvansrnf
nvansrnf
nvandperf
nvandrfnf
nvandrfnf
dngsu1
dngsu1
TOP
  
```

The netlist also shows detailed properties for several components, such as:

```

222 vbiassrid 235 2.2288e+06 L=0.0001885 W=1.5e-07 leff=0.0001885 ref=2.2288e+06 #SUB=235 #L[ppol]u# #X=-59730 #Y=12147320 #B=67
222 vbiassrid 236 2.2288e+06 L=0.0001885 W=1.5e-07 leff=0.0001885 ref=2.2288e+06 #SUB=236 #L[ppol]u# #X=-59730 #Y=12202320 #B=67
222 vbiassrid 237 2.2288e+06 L=0.0001885 W=1.5e-07 leff=0.0001885 ref=2.2288e+06 #SUB=237 #L[ppol]u# #X=-59730 #Y=12257320 #B=67
222 vbiassrid 238 2.2288e+06 L=0.0001885 W=1.5e-07 leff=0.0001885 ref=2.2288e+06 #SUB=238 #L[ppol]u# #X=-59730 #Y=12312320 #B=67
  
```


- Soft connectivity check



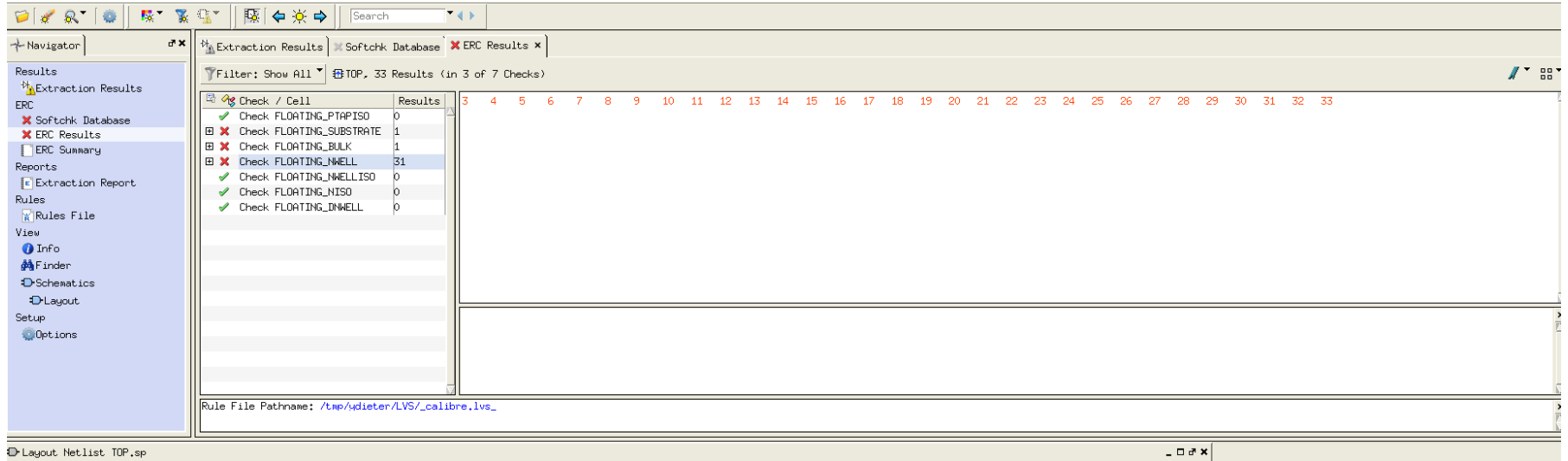
The screenshot shows a software interface with a 'Navigator' on the left and a main workspace. The workspace displays 'Extraction Results' for 'Softchk Database'. A table lists various checks and their results for cell 'TOP'. Check 6, 'SOFTCHK SUBSTRATE UPPER', is highlighted in red, indicating a failure. Below the table, a detailed view of check 6 shows coordinates for a vertex polygon in cell TOP.

Check / Cell	Results
✓ Check SOFTCHK PWELL_S UPPER.	0
✓ Check SOFTCHK PWELL_S UPPER.	0
✗ Check SOFTCHK SUBSTRATE UPPER.	27
✓ Check SOFTCHK INWELL UPPER.	0
✗ Check SOFTCHK BULK UPPER.	27
✓ Check SOFTCHK BULKISO UPPER.	0
✓ Check SOFTCHK NISO UPPER.	0
✓ Check SOFTCHK PWELL_ISO UPPER.	0
✓ Check SOFTCHK PWELLISO UPPER.	0

6) Check: SOFTCHK SUBSTRATE UPPER., Cell TOP: 2788-Vertex Polygon
 IN 6
 2788-Vertex Polygon, Coordinates in cell TOP
 { -201.5 10587.0 } { -300.5 10587.0 } { -300.5 13995.1 } { -300.3 13995.1 } { -300.3 13990.1 } { -300.1 13990.1 } { -300.1 13993.5 } { -299.9 13993.5 } { -299.9 13996.5 } { -299.7 13996.5 } { -299.5 13996.5 } { -299.5 13993.5 } { -299.3 13993.5 } { -299.3 13990.1 } { -299.1 13990.1 } { -299.1 10587.0 } { -299.3 10587.0 } { -299.5 10587.0 } { -299.5 10587.0 }

Net 12 is selected for stamping.
 Rejected nets: 6 7 8 9 10
 Net 12 is selected for stamping.

- Electrical rule checks



Filter: Show All | TOP, 33 Results (in 3 of 7 Checks)

Check / Cell	Results	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
✓ Check / Cell																																
✓ Check FLOATING_PTAPISO	0																															
✗ Check FLOATING_SUBSTRATE	1																															
✗ Check FLOATING_BULK	1																															
✗ Check FLOATING_NWELL	31																															
✓ Check FLOATING_NWELLISO	0																															
✓ Check FLOATING_NISO	0																															
✓ Check FLOATING_INWELL	0																															

Rule File Pathname: /tmp/udieter/LVS/_calibre.lvs_

Layout Netlist TOP.sp