

Plans Active CMOS Strips

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Next submission plans

- ▶ smaller testchip with 30 strips with regular design $75.5\mu\text{m}$
 - ▶ May be $25\mu\text{m}$
- ▶ Strip length to match reasonable reticle size (money + handling constrains)
- ▶ keep: P type FZ material $150\mu\text{m}$ thick with resistivity $2\text{k}\Omega\text{cm}$
- ▶ No metal on top of pstop
- ▶ Wirebond pads at the passive end of strips to increase capacitance equivalent to longer strips
 - ▶ or connect longer external strips

Active electronics

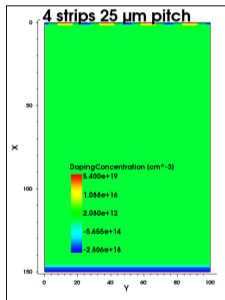
- ▶ Configuration on chip:
 - ▶ global register: n-bit, to set global DAC values
 - ▶ shift register to address individual strips → “strip register”
 - ▶ have local n-bit register per strip
 - ▶ mask bit (disconnect comparator from readout)
 - ▶ FDAC and TDAC values
 - ▶ feedback capacity select bit
 - ▶ hitbus enable bit (OR for enabled channels to create trigger?)
- ▶ Readout:
 - ▶ discriminator output buffered to wirebond pad, asynchronous
 - ▶ hit serialization external
- ▶ Target DAQ: Caribou on ZCU102
 - ▶ ZCU102 in hand in Dortmund, Freiburg and DESY?
 - ▶ still need carr boards

Performance Target

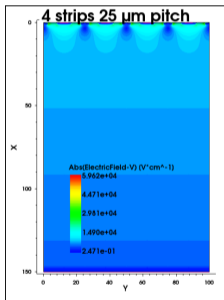
Parameter	HEP application	MedPhys application
Charge injection	10bit, 0-50ke (FE-I4)	10bit, 20ke-200ke (300ke)
Range threshold	1ke	~ 30ke
Noise	try for 100 - 300e	
ToT resolution	doesn't really matter (need to be able to do c.o.g. clustering)	few ke at 40ke-300ke
Best operating point	low charge (high efficiency after irradiation) → low threshold, ToT max for 15ke (above max expected charge)	close to Bragg peak → threshold 50-100ke, ToT max for 350ke
Tests	different strip lengths (via wirebonding more strips) → performance of the amplifier (noise, timing)	
Charge deposition (maximum)	12ke before irradiation	300ke ($150\mu\text{m} \cdot 6\text{keV}/\mu\text{m} / 3.6\text{eV per e/h pair}$)
Charge deposition (minimum)	~7ke after irradiation	41ke ($150\mu\text{m} \cdot 1\text{keV}/\mu\text{m} / 3.6\text{eV per e/h pair}$) for 150 MeV protons

25 μm strip pitch option

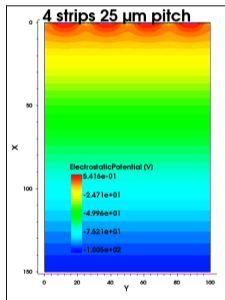
- ▶ initial simulation done
- ▶ 4 strips parallel, scaled to 2.1cm long



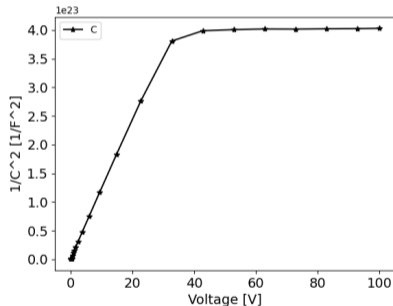
Doping



E-Field

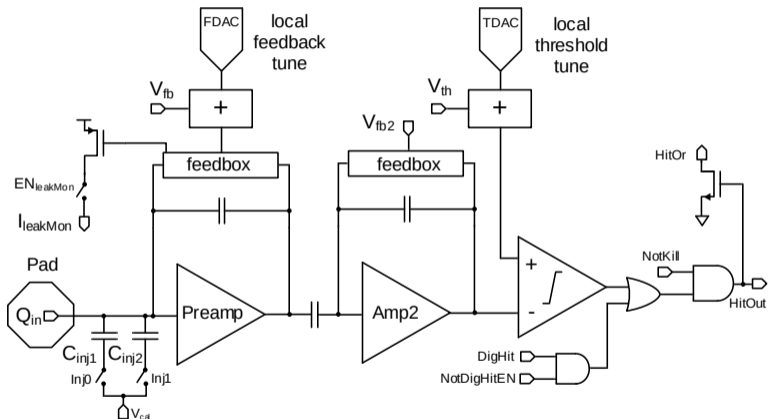


E-Potential

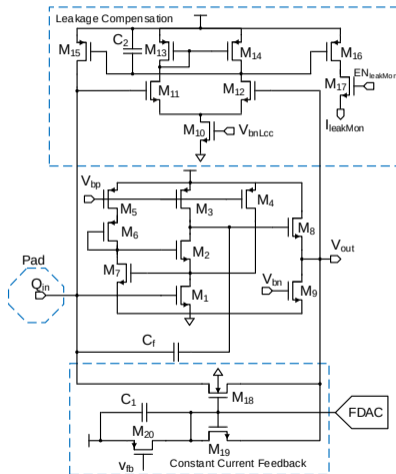


C-V

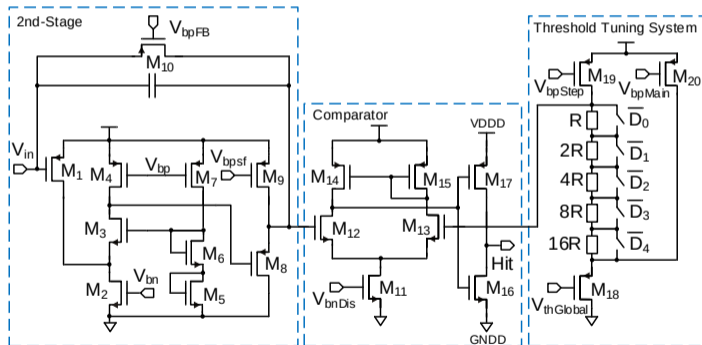
Front-End Architecture of FE-I4



Preamplifier Schematic



2nd-Stage and Comparator



Submission options

- ▶ Initial Plan MPW directly at LFoundry (~~May 2024~~/May 2025)
- ▶ Engeneering run with MLM with tiny reticle
- ▶ Also an option to do joint DRD3 community submission of the MLM 1x3