DAQ Pilot User Project
New Firmware Architecture
Caribou Boreal
DRD3/MPW-Caribou-CERN-University of Seville

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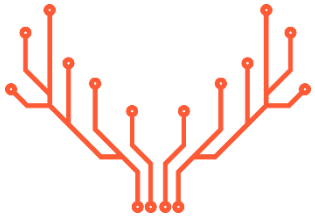
DRD3-WG1 Internal Meeting
June 6 - 2024

DRD3



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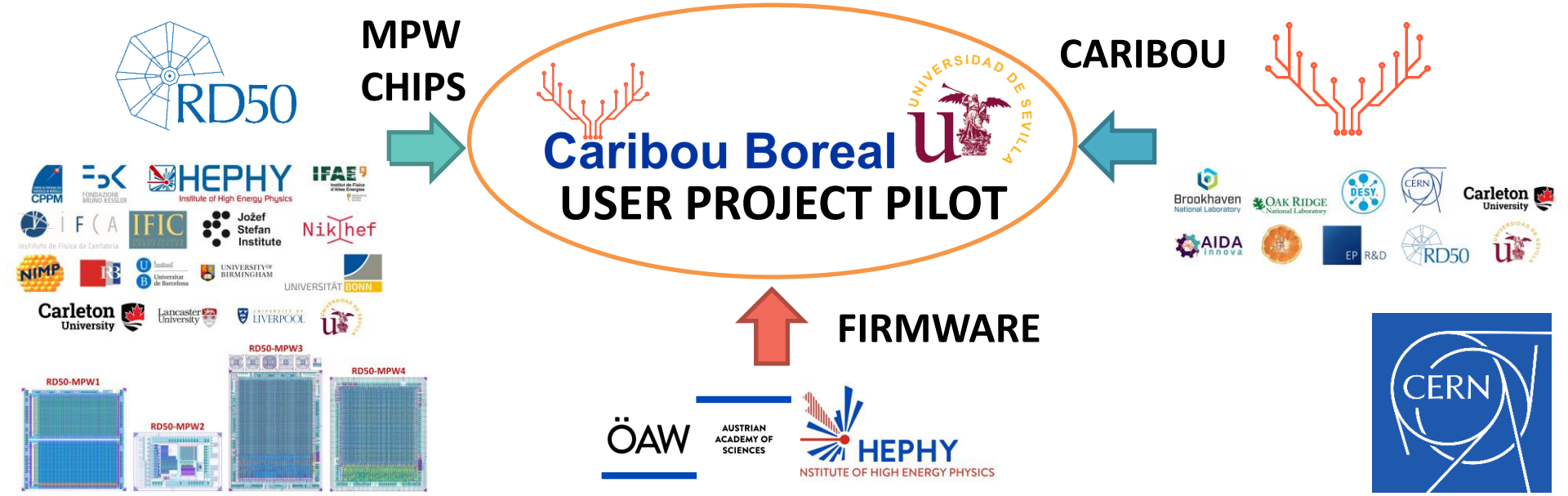
1. INTRODUCTION

Pilot project New Boreal modular architecture from DAQ Caribou using MPWx chips

- The objective of this pilot project is to modularize and adapt the **firmware MPW4 developed by HEPHY** in the user part of **Caribou's new Boreal firmware architecture** with Peary software integration.
- This project is presented as a **collaboration** between the following institutions:



Caribou Boreal

A unified, modular and configurable firmware

**Younes Otarid - Caribou Developers Meeting – 14.05.2024*

Currently:

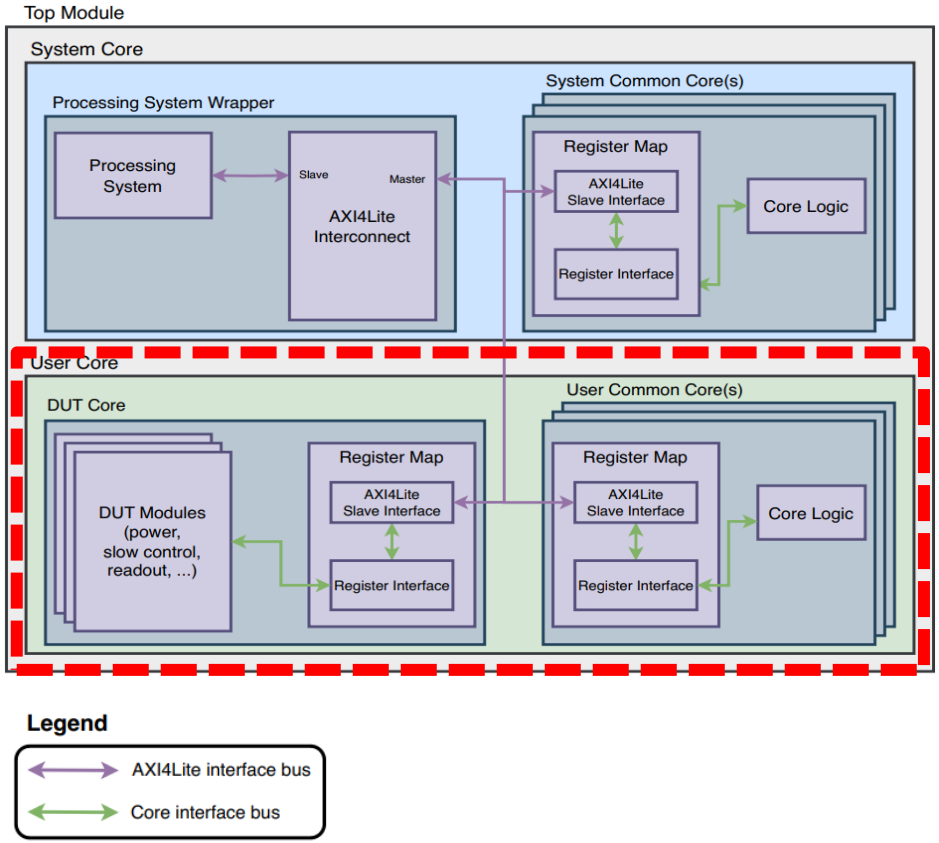
- Block design recreated and reconfigured for each project (GIT repository for each chip integrated with Caribou)
- Common IPs (Git repository with common IPs), sometimes copied and modified locally
- No HDL simulation/verification
- No CI/CD workflow and without documentation

Objective:

- **Optimized Workflow: Design of common blocks and IPs along with a base architecture (microprocessor, common blocks and AXI interface).**
- **Starting from the base architecture, integration into the single project of the specific user block for each chip.**
- **A single Git project for all devices**
- **Enhanced HDL simulation/verification**
- **Optimized CI/CD workflow and documented code**

Caribou Boreal Firmware

**Younes Otarid - Caribou Developers Meeting – 14.05.2024*



Processing System wrapper:

- Processing System and Reset IP (VHDL file)
- Pre-configured for the Caribou Zynq board (ZC706)
- One AXI4Lite interface per block (system/user core) with a unique address
- System evolution and features extension (ZCU102 UltraScale+)

System common core(s):

- Common cores/IPs related to the system (Zynq board, CaR board) features

DUT core:

- User core including device-specific control and readout logic

User common core(s):

- Common cores/IPs related to external or user functionalities

Caribou Boreal Firmware

**Younes Otarid - Caribou Developers Meeting – 14.05.2024*

Project Configuration

- Through Constants in the VHDL: supported SoC, supported devices and AXI interface

```
--Board type constant
type board_type is (ZC706, ZCU102);
constant BOARD : board_type := ZC706;
```

```
-- Project type constant
type project_type is (BLINK_LED);
constant PROJECT           : project_type := BLINK_LED;
```

User Core

```
architecture behavioral of zc706_usr_core is

begin

  -- LED blinking block instantiation
  blink_led_gen : if PROJECT = BLINK_LED generate
    blink_led_inst : entity work.blink_led
```

```
# Check condition
if {$project == "BLINK_LED"} {
  # ZC706 constraints
  if {$board == "ZC706"} {
}

# ZCU102 constraints
if {$board == "ZCU102"} {
```

XDC file

Simulation

- Cocotb (VHDL and SystemVerilog RTL using Python) and Questa simulator

Caribou Boreal Firmware

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Boreal Manager

- Python Script: Create Vivado, Configure the Vivado Project (chose SoC and device) and Build (Synthesis + Implementation + bitstream generation)

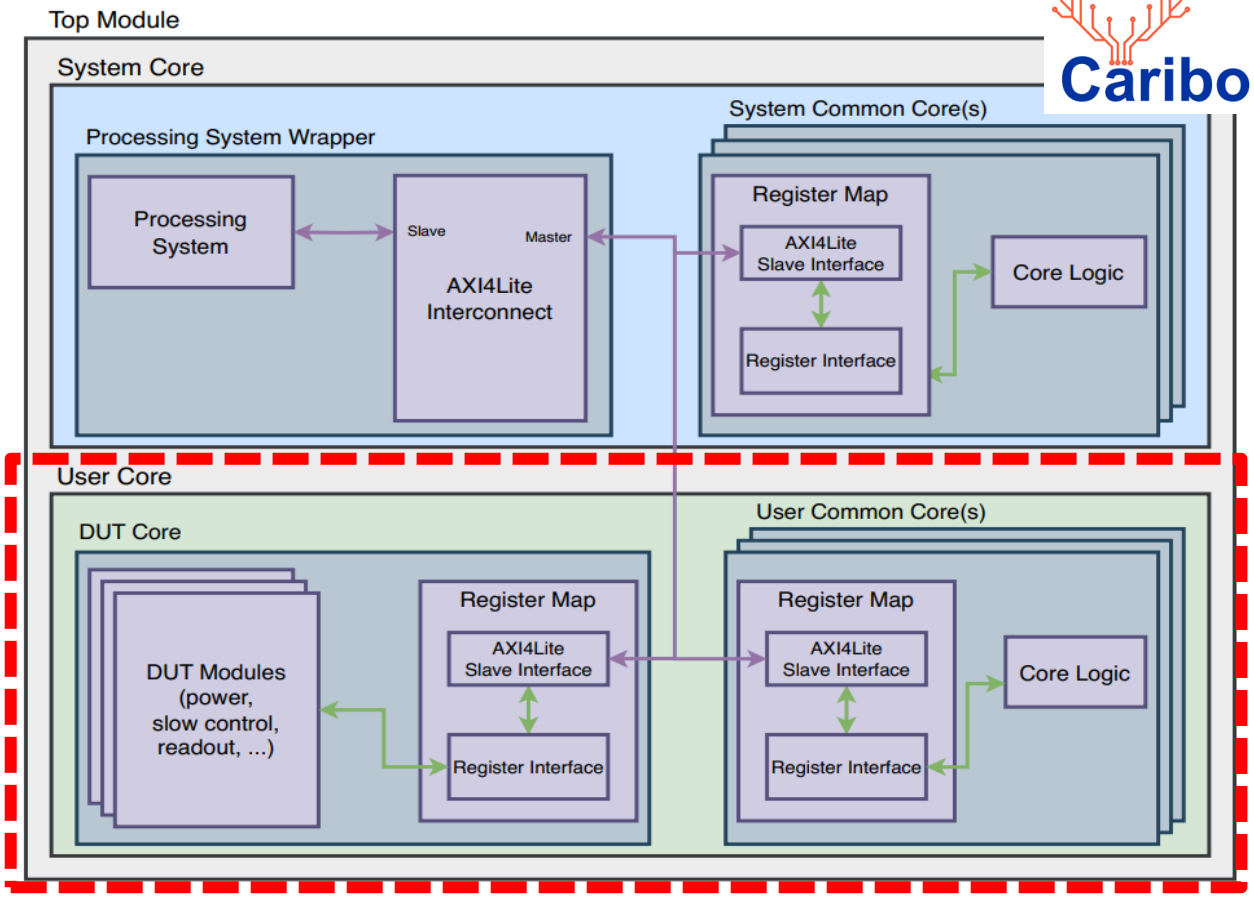
```
Boreal Vivado project manager

optional arguments:
  -h, --help            show this help message and exit
  --create              Create Vivado project
  --configure           Configure Vivado project
  --board {ZC706,ZCU102}
                        Board to be used
  --project {BLINK_LED}
                        Device project to be used
  --synth               Run synthesis
  --impl                Run implementation
```

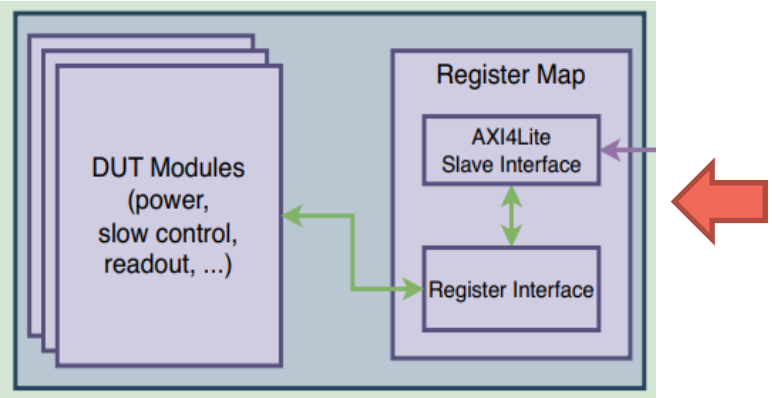
CI/CD Workflow

- Single instance of project creation
- Code linting using vhdl-linter and verible-format
- Cocotb simulation of all cores
- Bitstream generation for all supported devices and for all supported boards

Caribou Boreal Firmware - Project Pilot (MPW4)



Caribou Boreal Firmware - DUT Core Project Pilot (MPW4)



Modular Blocks – DUT Core:

- ❑ Register map accessible via AXI interface, with configurable number of registers
- ❑ Core logic connected to register map and to the core IO interface

Starting from the original MPW3/4 firmware provided by HEPHY, ADAPT AND MODULARIZE BLOCKS for each of the tasks:

- MPW4 Slow Control
- MPW4 Slow Readout (SoC)
- MPW4 Fast Readout (GBE-SFP)
- TLU Control

Caribou Boreal – Integration and Software

Project Configuration

- Integrate the necessary constants and configuration into the vHDL for the integration of the MPW4 device into the project.

Simulation

- Simulation of the different modular blocks of MPW4 separately and in conjunction with Cocotb.

CI/CD Workflow

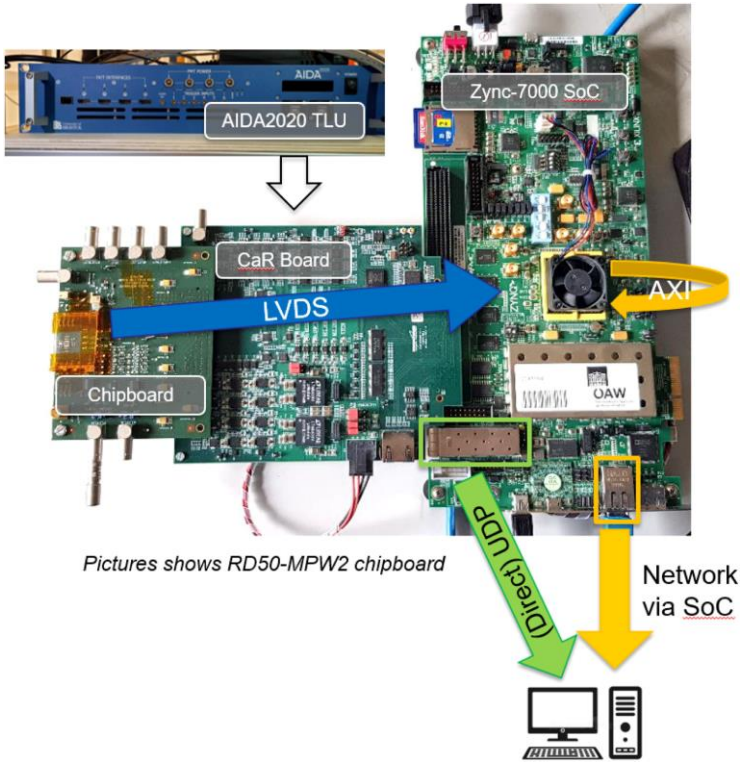
- Add the simulation of the MPW4 blocks and verify in the workflow the code linting and construction with MPW4 in the global project.

Peary Modular Software

- Configuration of the Caribou feeds necessary for the MPW4.
- Integrate libraries in the new version of peary modular software for the MPW4 device.

Caribou Boreal – Verification

Test the complete system on both the ZC706 board and the ZCU102 board (UltraScale+)



Pictures shows RD50-MPW2 chipboard

4. PHASES

Phase 0: Study, analyze, and divide the original HEPHY firmware code into functional components.

Phase 1: example base Boreal architecture (blink LED developed by Younes) and integrate the slow control of MPW4 chip.

Phase 2: Cocotb Simulation and CI workflow of slow control MPW4 chip.

Phase 3: Slow control and configure the Caribou power supplies in the Peary software. Verify the slow control with the system and MPW4.

Phase 4: Integrate module firmware TLU control and readout MPW4 chip.

Phase 5: Cocotb Simulation and CI workflow of TLU an readout MPW4 chip.

Phase 6: Integrate the libraries for readout and TLU Peary software

.

Phase 7: Conduct a test with the complete systems (ZC706 and ZCU102).

5. CONCLUSIONS

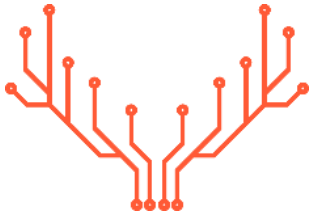
- The new Boreal firmware architecture allows, based on a single, modularized and configurable base architecture, to simplify the integration of chips in the Caribou system.

- This project involves using the MPW4 as the first chip in the new Boreal architecture.

- For the above objectives, **this pilot project aims to modularize and adapt the MPW4 firmware developed by HEPHY into the user part of Caribou's new Boreal firmware architecture.** Additionally, the following tasks will be carried out:
  - ❖ Add Automation in the Boreal project Vivado configuration
  - ❖ Simulations with Cocotb and Questa of the modular blocks.
  - ❖ Integration in CI Workflow
  - ❖ Adaptation of Peray software libraries for the use of MPW4 in Boreal.
  - ❖ Verification in ZC706 and the UltraScale+ ZCU102.

6. ACKNOWLEDGMENT

- **Caribou Collaboration**



- **Institute of High Energy Physics**

- **DRD3(RD50)-MPW Collaboration**

DRD3

Thank you for your attention

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