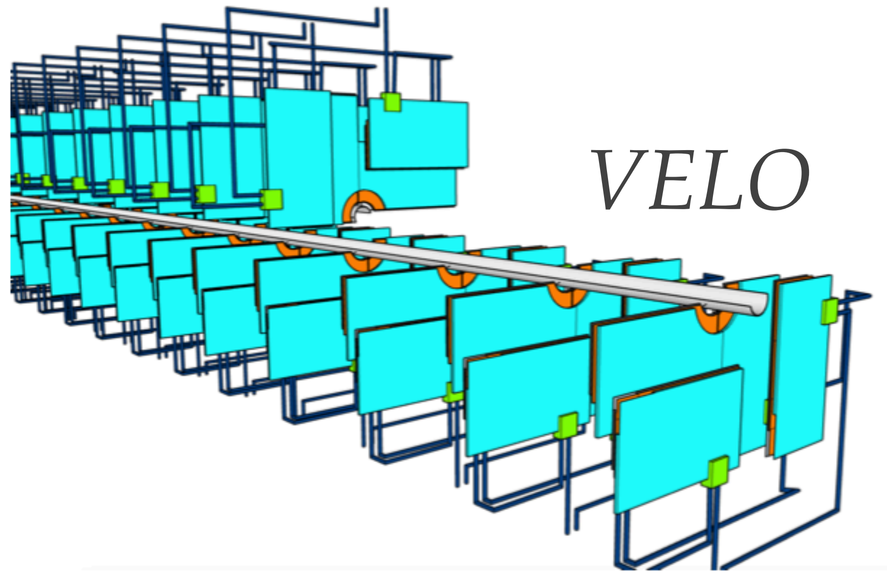
HEAVY-ION PHYSICS AT LHCB - CONTRIBUTION OF IRFU TO LHCB TRACKING UPGRADE

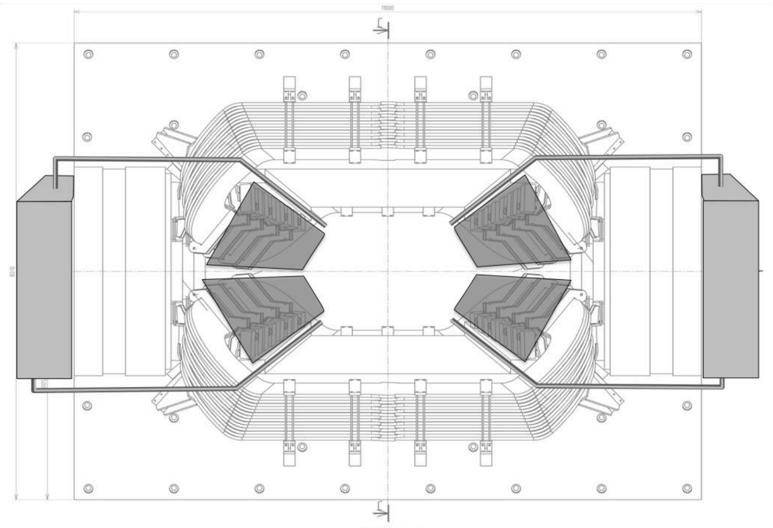
BENJAMIN AUDURIER FOR THE LQGP GROUP - CSTD DPHN - 12/06/24

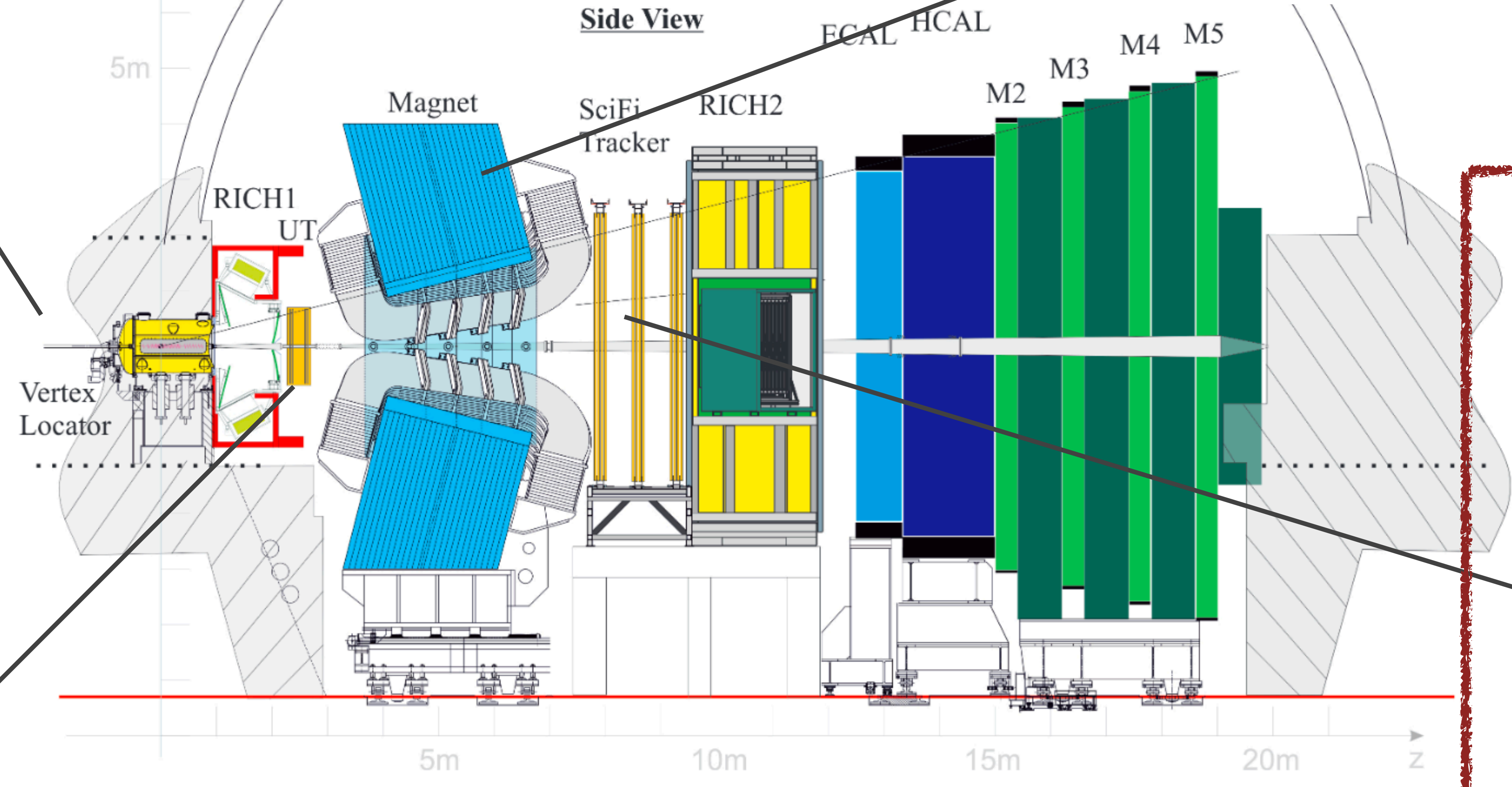
Presentation of the detector

VELO

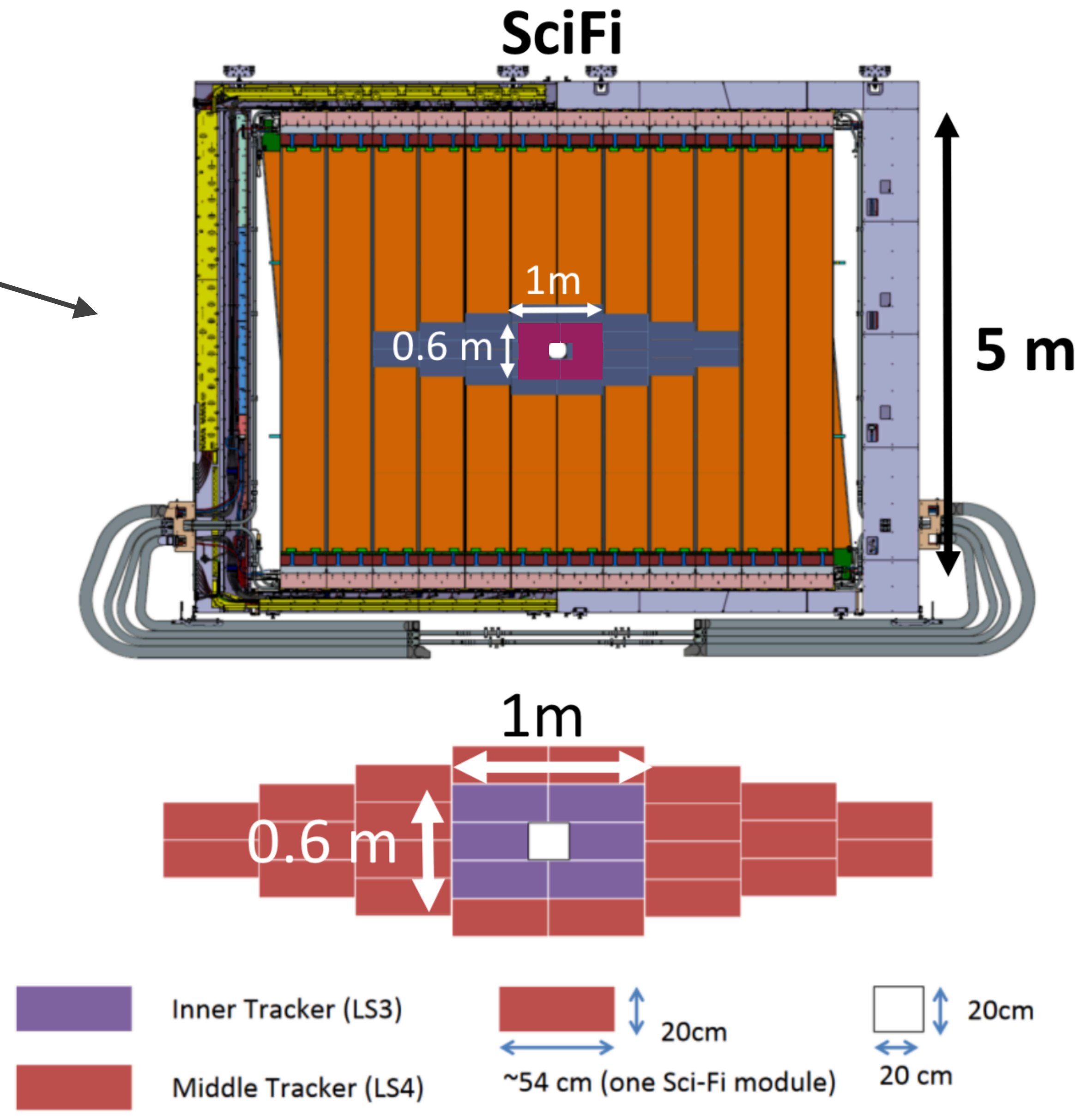


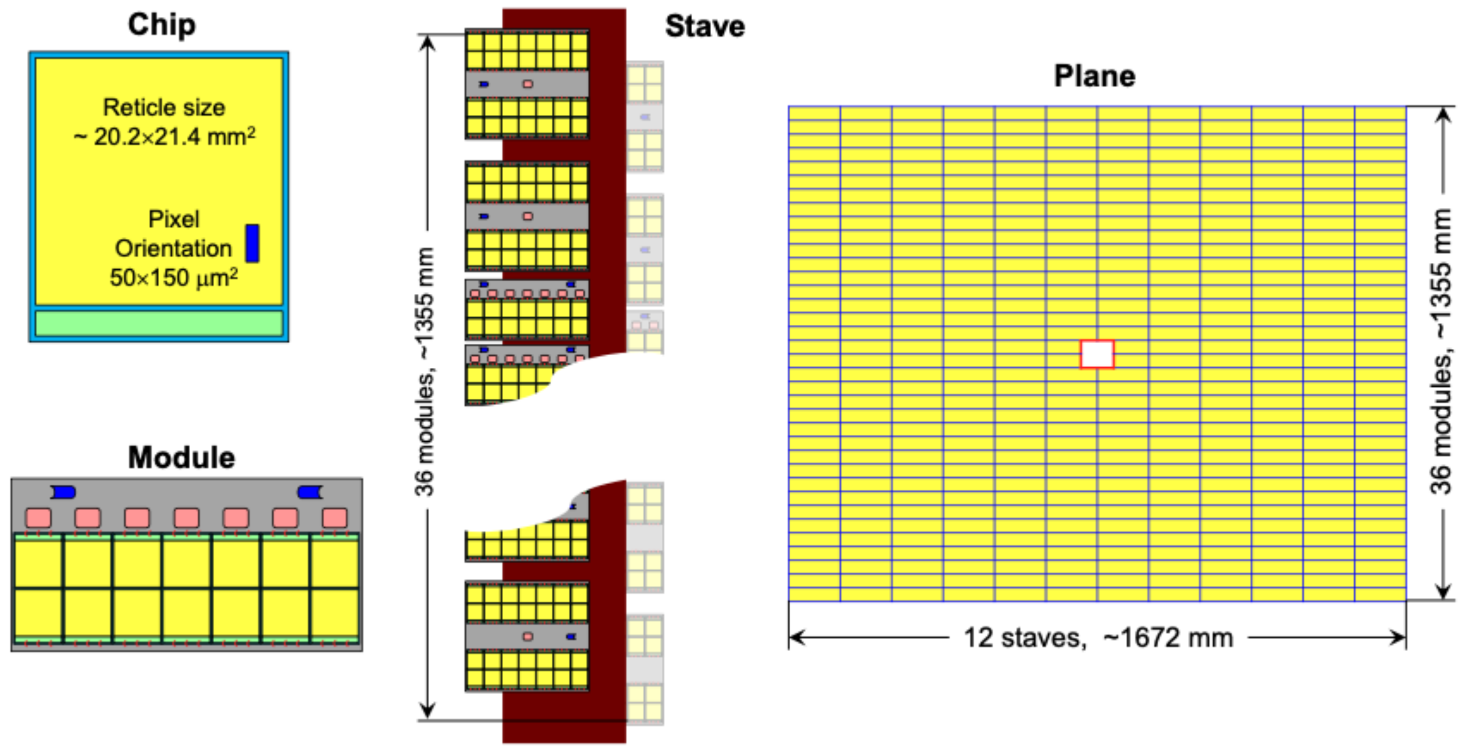
Magnet Stations





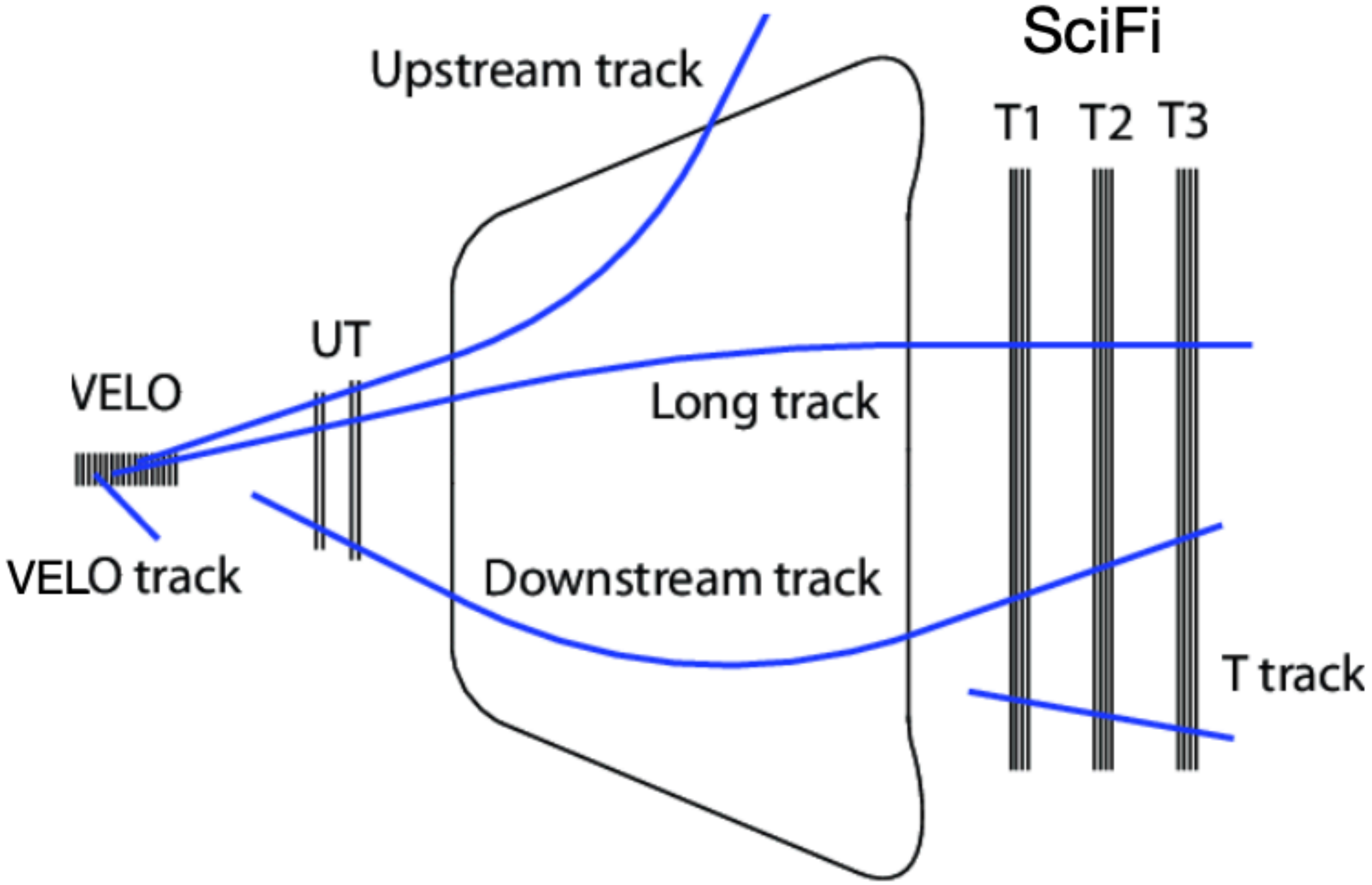
Mighty Tracker

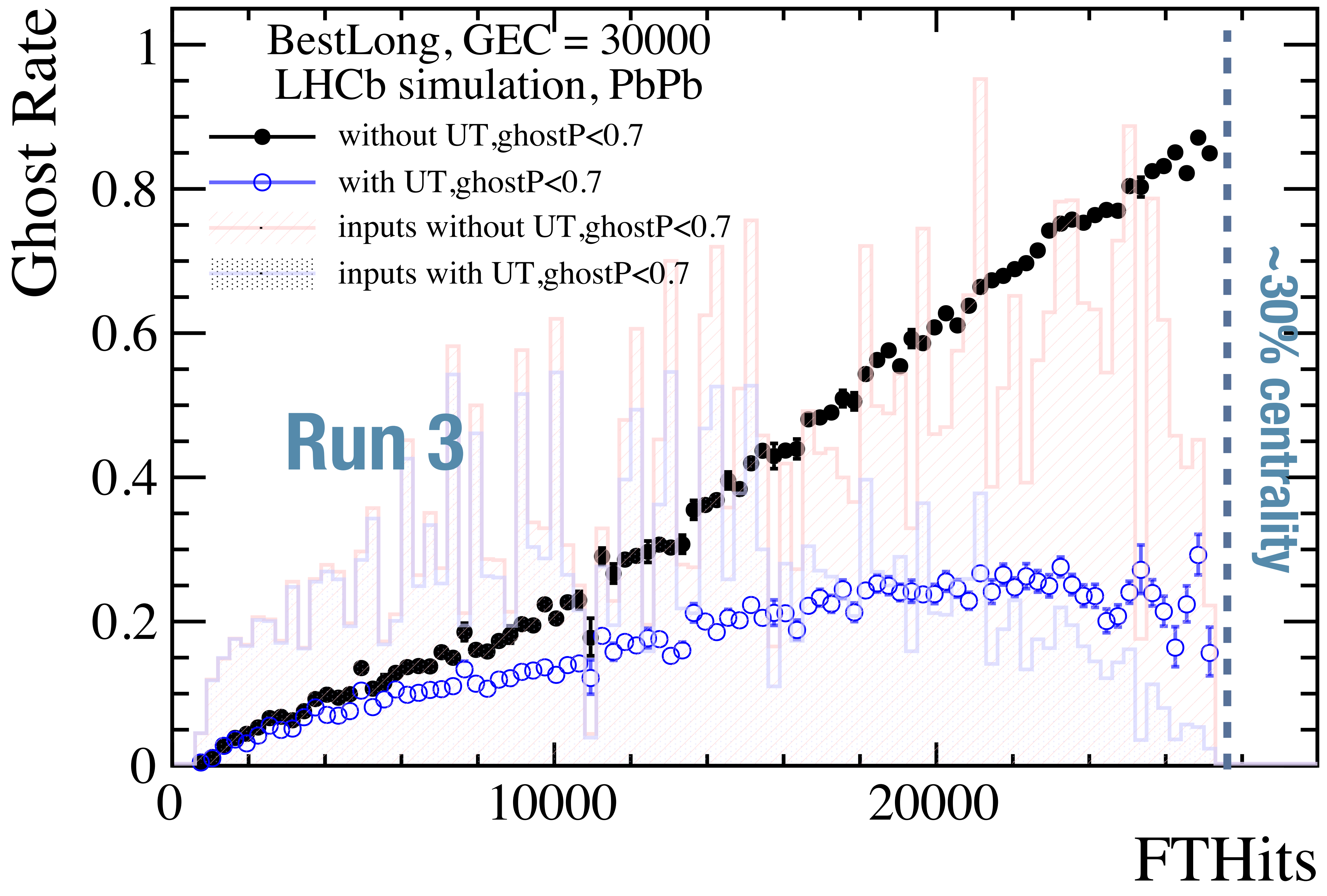




Upstream Tracker (UT)

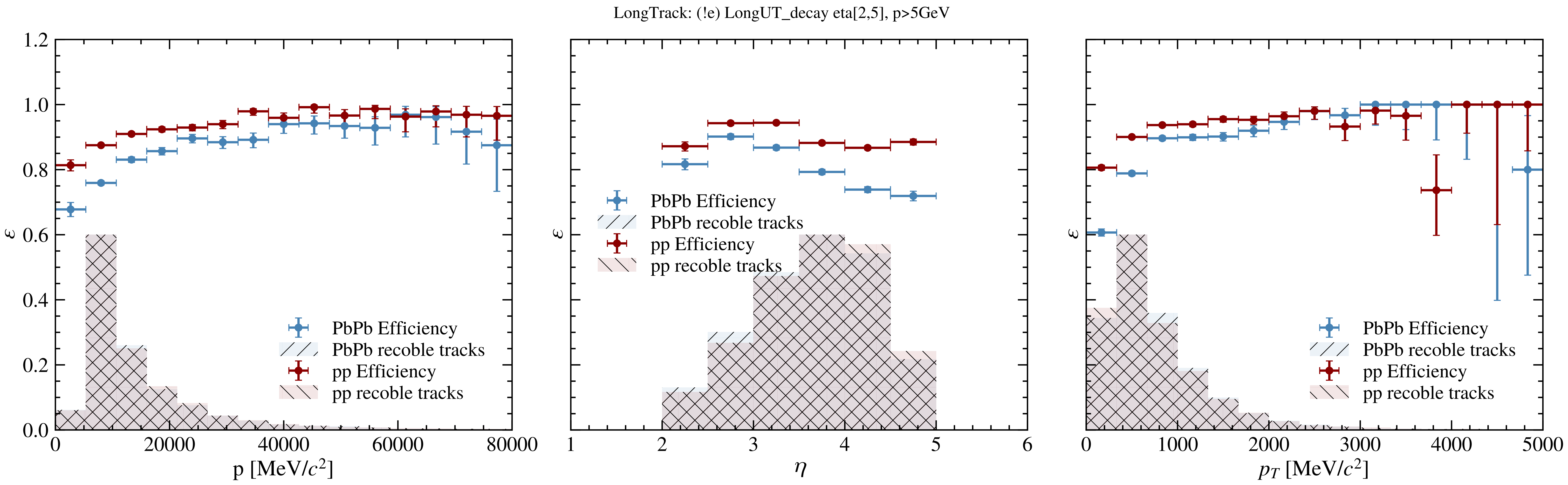
UT and the tracking system





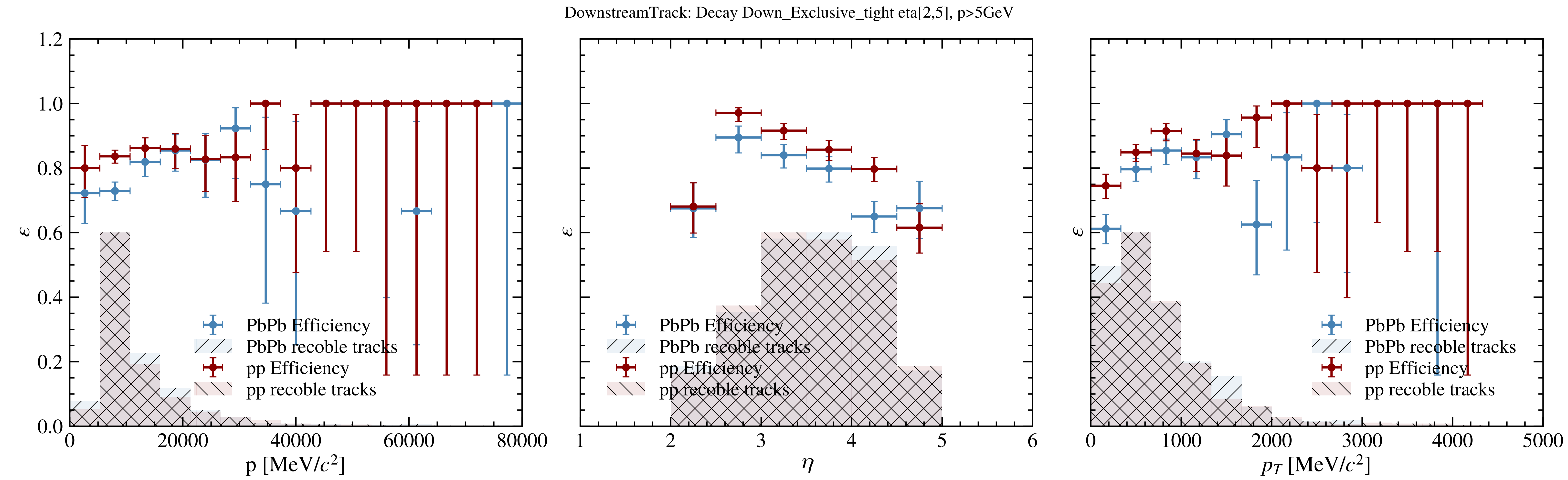
- UT in the tracking system:
  - Mandatory to tackle **the ghost rate**
  - Mandatory for **all** tracks

Preliminary results for Run 5 PbPb



LongTrack Efficiency

	Efficiency	Ghost rate
pp	90 %	24 %
PbPb (Central)	80 %	39 %

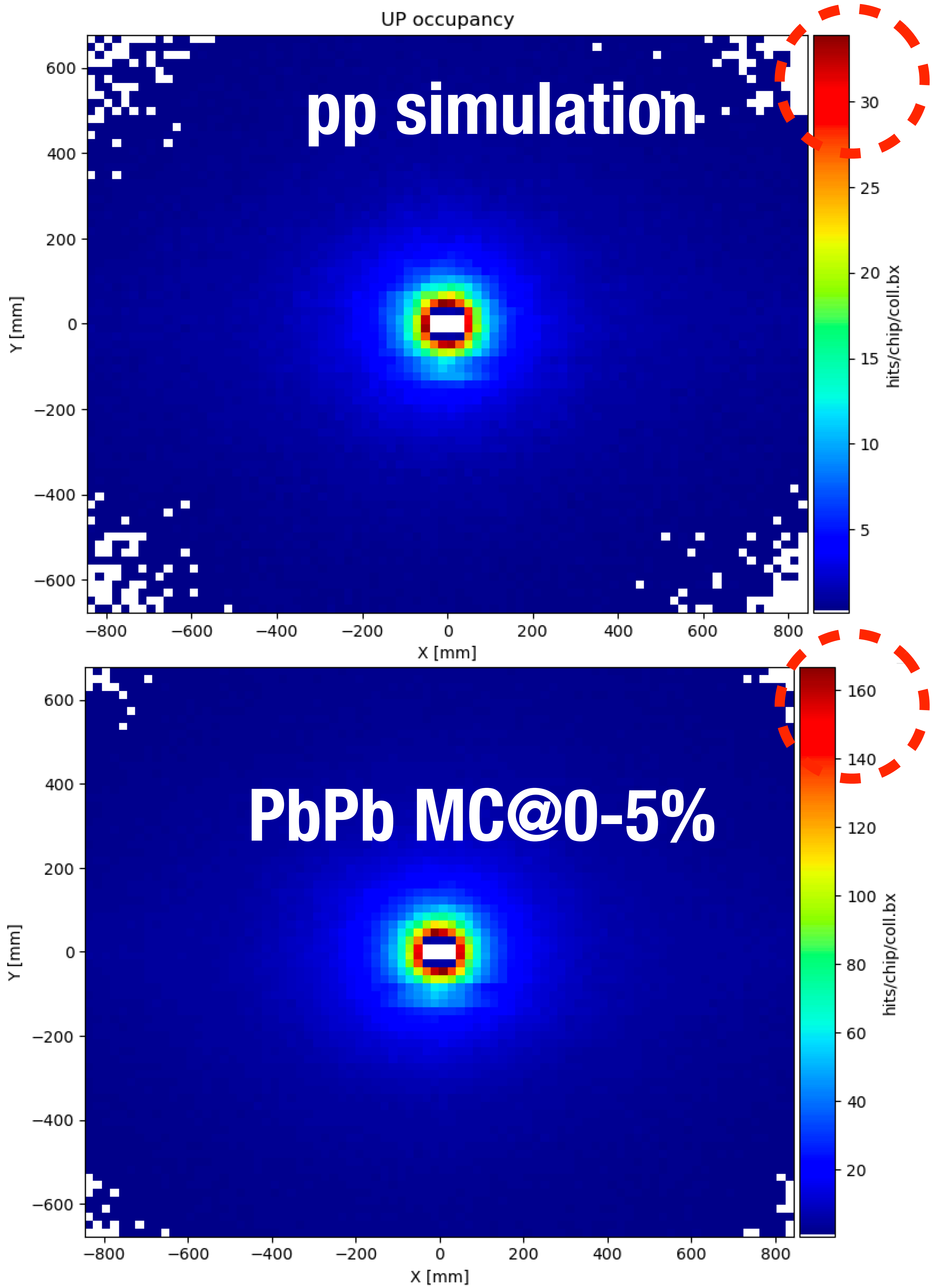


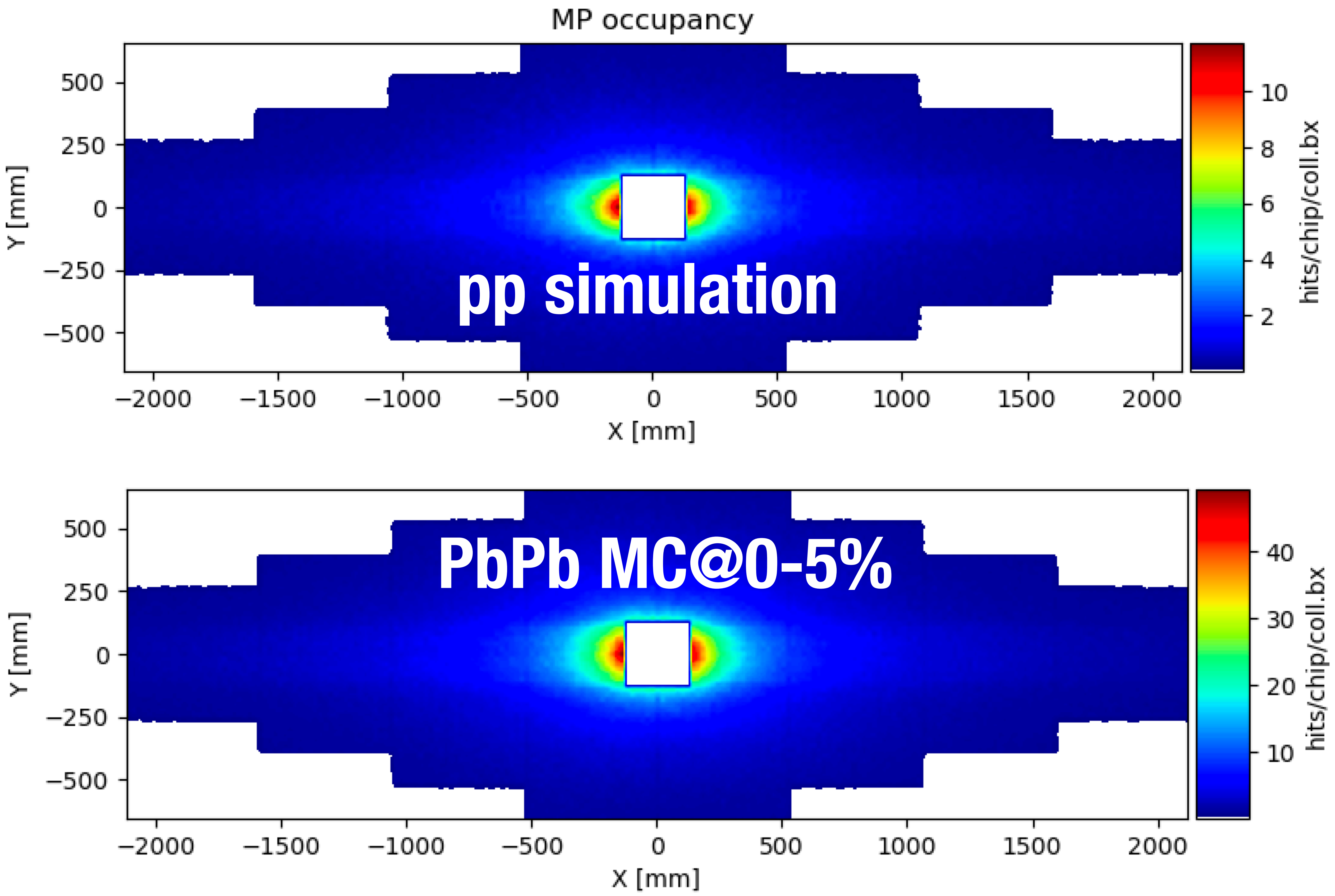
Downstream Efficiency

	Efficiency	Ghost rate
pp	85 %	27 %
PbPb (Central)	78 %	38 %

Simplest model possible, to be improved

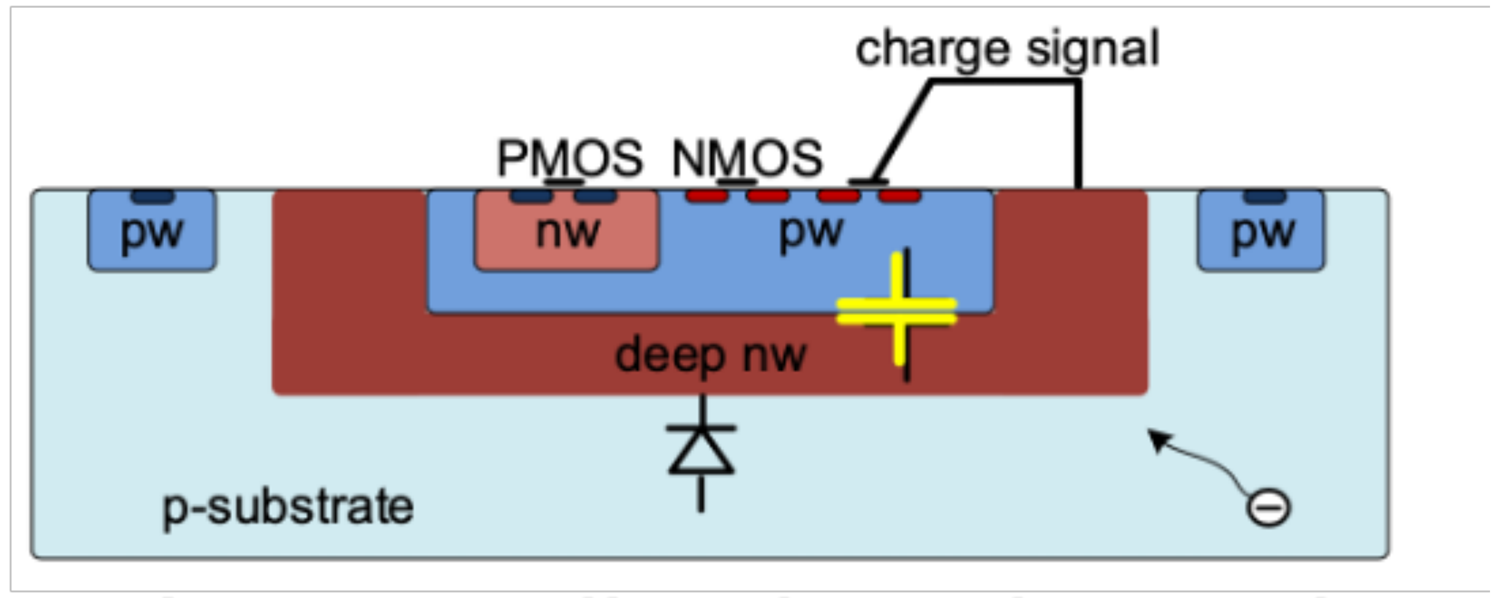
Specifications for pixels





Space resolution	5 μm	< 10 μm
In-time efficiency	> 99% within 25 ns	> 99% within 25 ns
Time resolution	O(1 ns) for BX tagging	few ns for BX tagging
Radiation dose	3.10^{15} 1 MeV n_{eq}/cm^2, 240 Mrad	6.10^{14} 1 MeV n_{eq}/cm^2
Maximum data rate	4.5 Gb/s (without ToT in data) 160 MHz/cm^2 (6 hits/BX/cm^2 in pp)	2 Gb/s (with ToT in data)
Power consumption	100-300 mW/cm^2	< 150 mW/cm^2

Options for the pixels

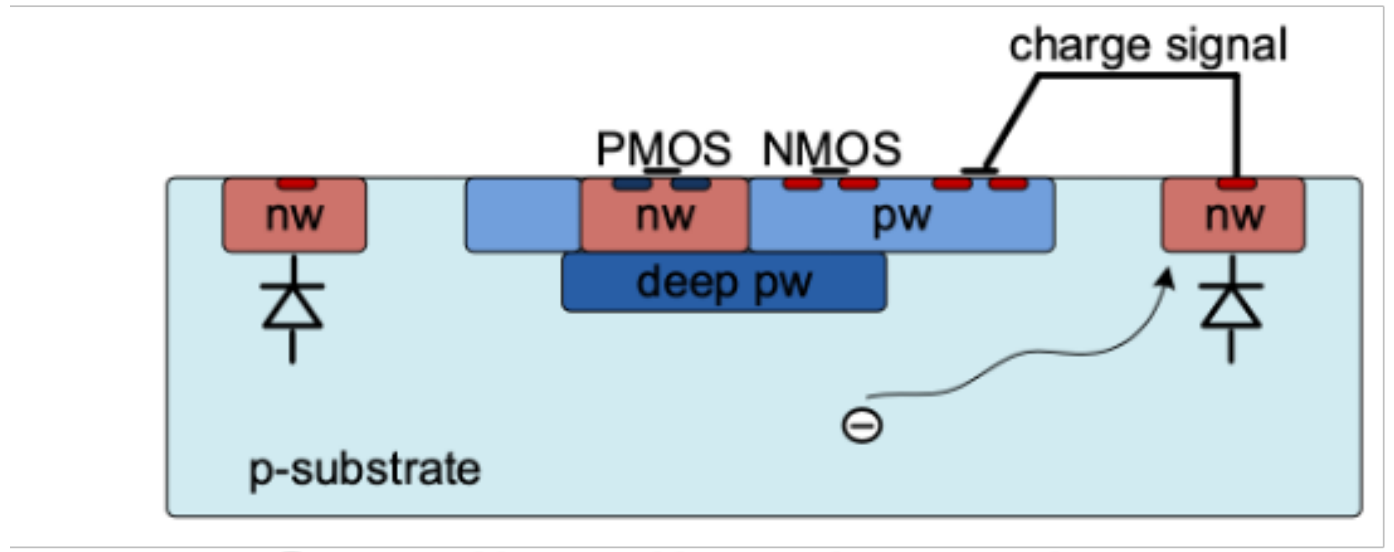


Large collection electrode

- Typical pixel size: 50 x 150 μm^2
- Circuitry inside the collection well (requires high field: “HV-CMOS”)
- High radiation hardness
- Higher noise (high capacitance)
- Higher power consumption
- Possible cross-talk (digital to sensor)

Technology	Sensor
AMS/TSI 180 nm	MightyPix
SMIC 55 nm	COFFEE

Technology	Sensor
LF 150 nm	MonoPix

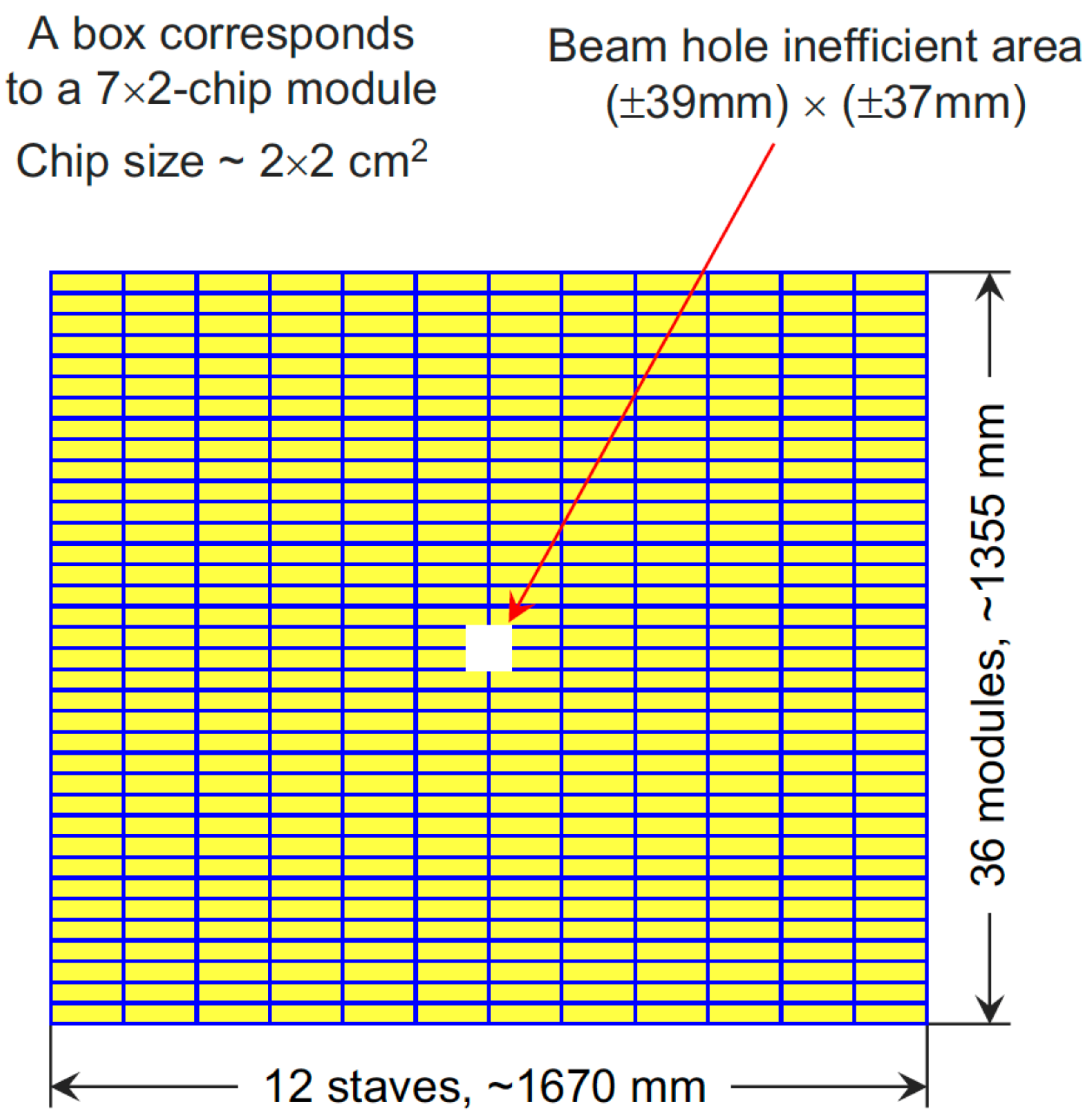


Small collection electrode

- Typical pixel size: 30 x 30 μm^2
- Circuitry outside the collection well (requires low/moderate field: “LV-CMOS”)
- High radiation hardness thanks to process modification (increase of depletion zone)
- Lower noise (low capacitance)
- Lower power consumption
- Less sensitive to cross-talk

Technology	Sensor
TowerJazz 180 nm	MALTA
TPSCo 65 nm	SPARC

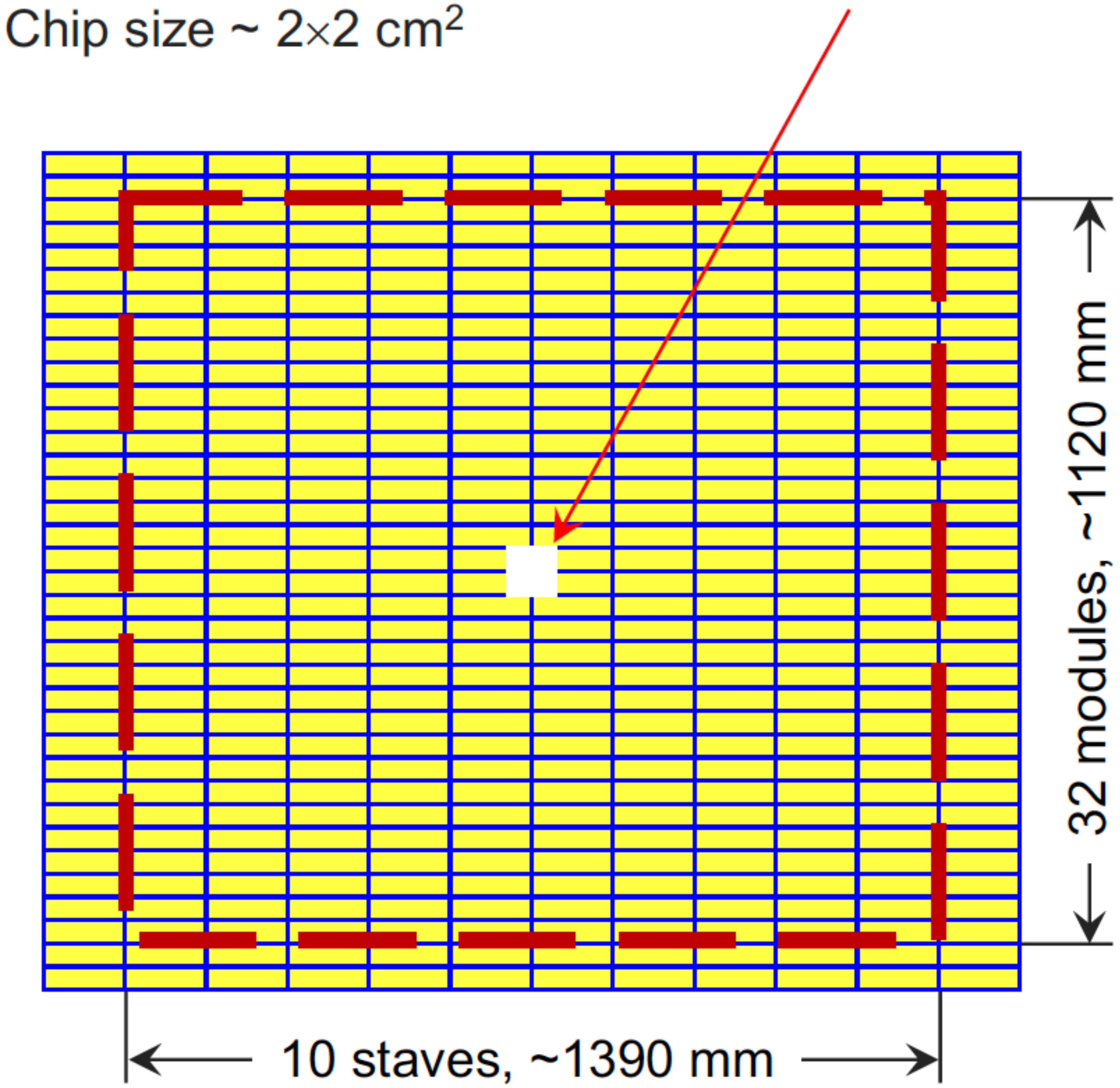
Original baseline



4 planes, 48 staves, 1728 modules, 24128 sensor chips

- **Preliminary design**:
  - 4 detector planes, at Z positions similar to the current UT
  - Each plane is composed by 12 staves, covering ~1672 mm in X, with 2 mm overlap
  - Each stave is composed by 36 modules, covering ~1355 mm in Y
  - Each module is composed by 2x7 sensor chips of ~ 2x2 cm2
    - In the outer regions of each plane, dual modules are used
  - Central hole (beam pipe) of (±39mm)x(±37mm)

New baseline



A box corresponds to a 7×2-chip module

Chip size ~ 2×2 cm^2

Beam hole inefficient area (±39mm) × (±37mm)

32 modules, ~1120 mm

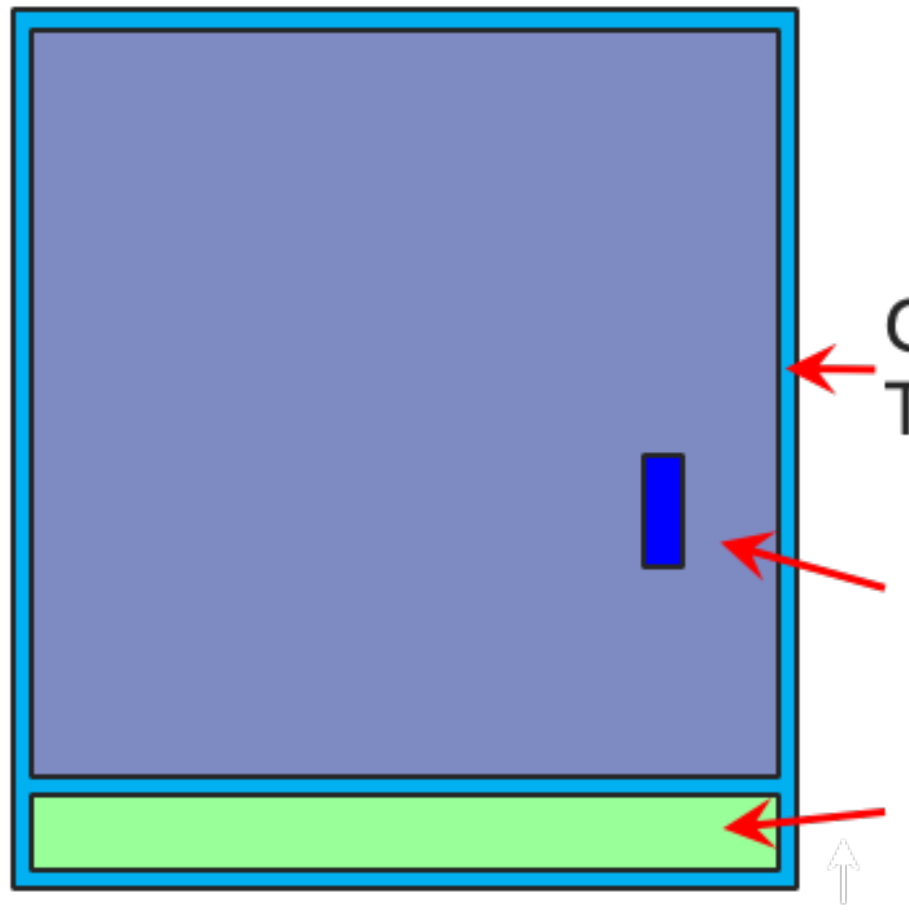
10 staves, ~1390 mm

4 planes, 40 staves, 1280 modules, 17920 sensor chips

- **Preliminary design**:
  - 4 detector planes, at Z positions similar to the current UT
  - Each plane is composed by 10 staves, covering ~1672 mm in X, with 2 mm overlap
  - Each stave is composed by 32 modules, covering ~1355 mm in Y
  - Each module is composed by 2x7 sensor chips of ~ 2´2 cm2
    - In the outer regions of each plane, dual modules are used
  - Central hole (beam pipe) of (±39mm)x(±37mm)

Conceptual design

Chip (HV-CMOS)



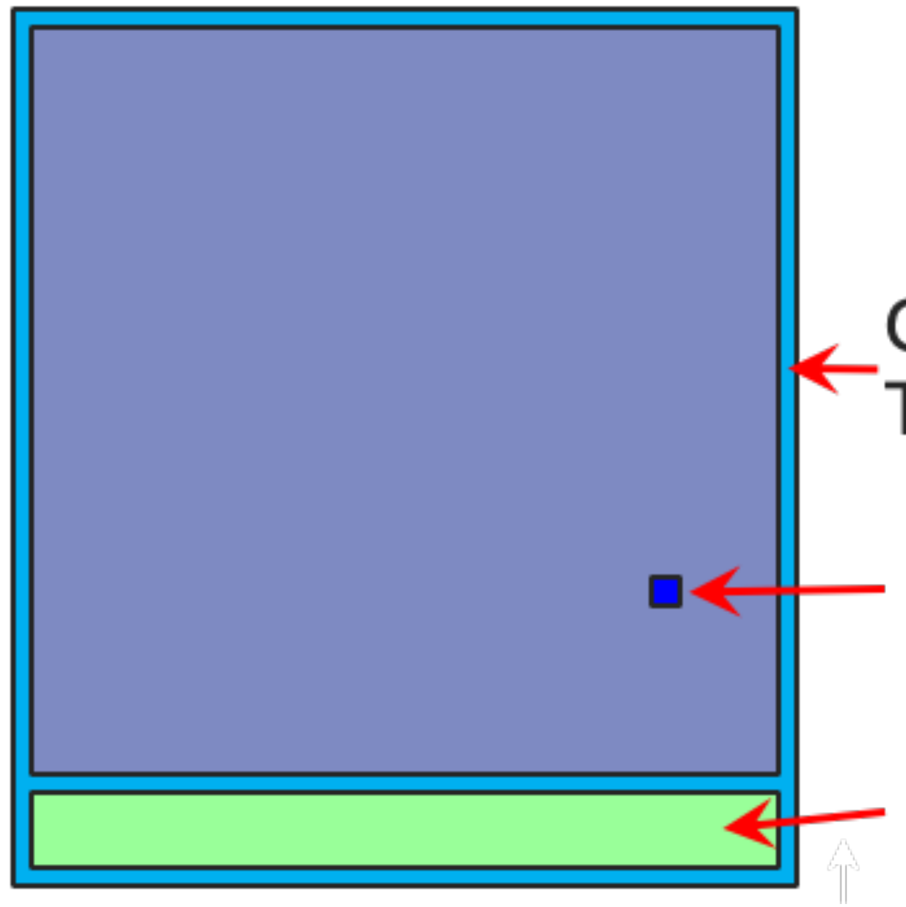
Reticle size
~ 20.2×21.4 mm^2

Guard ring = 80 μm
Tolerances ~20-40 μm

Pixel = 50×150 μm
Matrix = 400×128

Periphery ~ 2 mm

Chip (LV-CMOS)



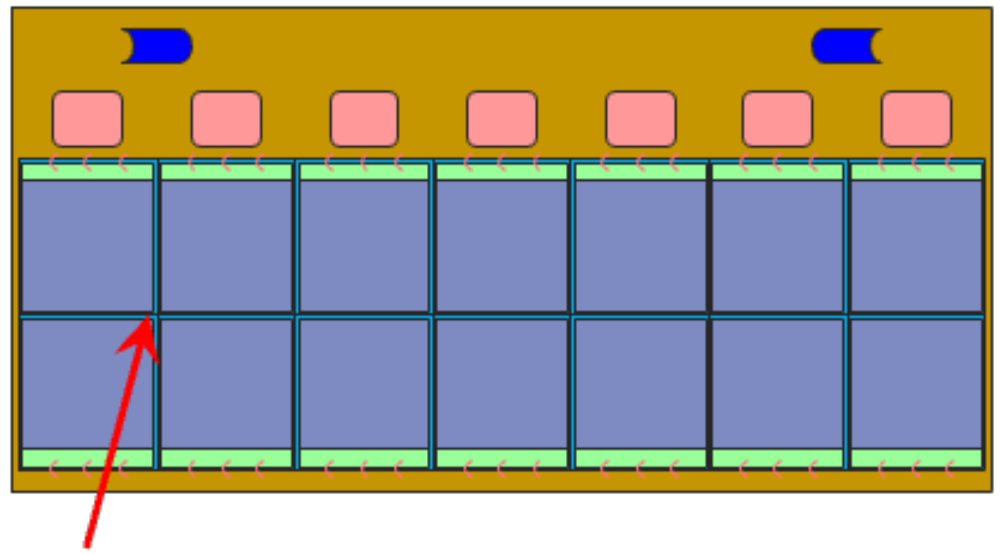
Reticle size
~ 18.6×19.8 mm^2

Guard ring = 80 μm
Tolerances ~20-40 μm

Pixel = 36.4×36.4 μm
Matrix = 512×544

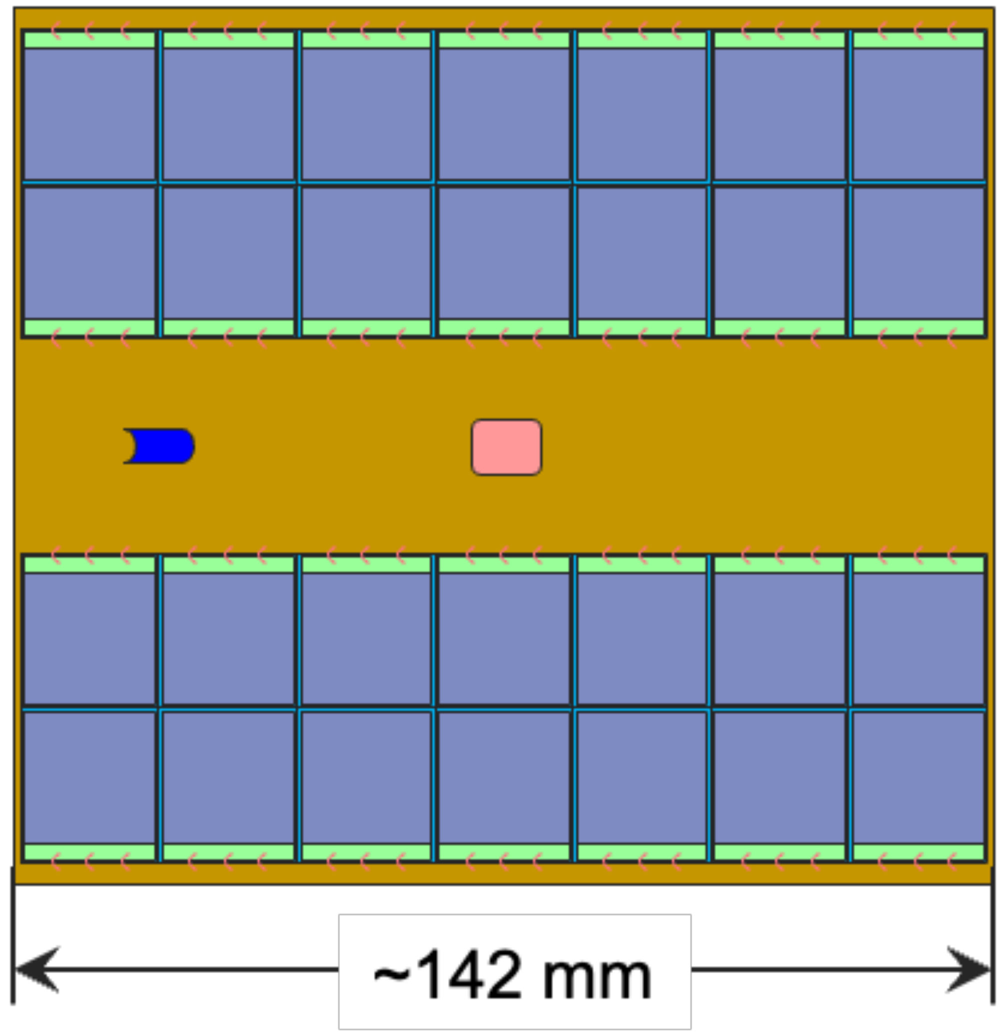
Periphery ~ 2 mm

Module



Dead space ~ 200 μm

Dual-Module

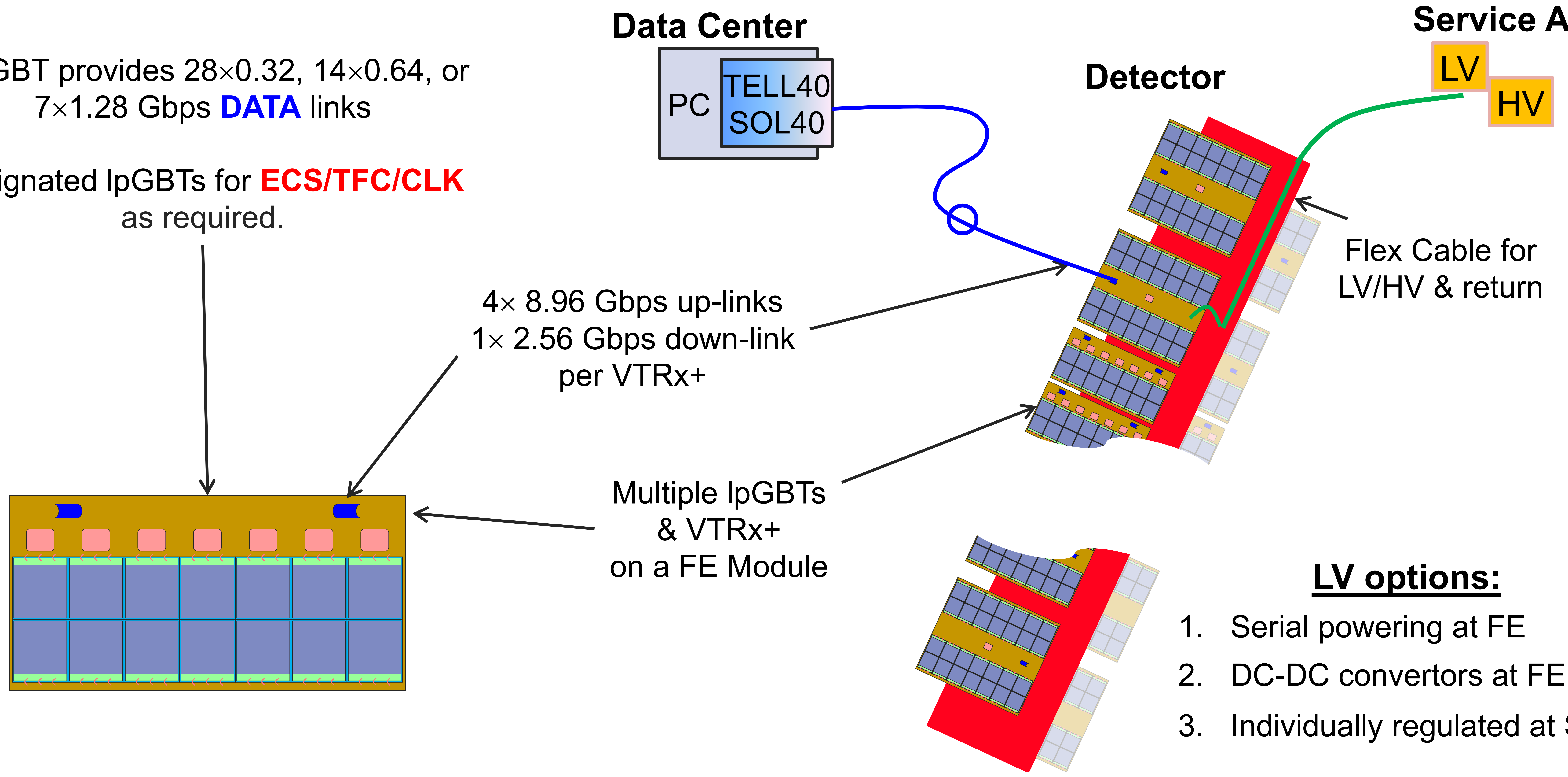


Stave

Readout scheme

1 lpGBT provides 28×0.32, 14×0.64, or 7×1.28 Gbps **DATA** links

Designated lpGBTs for **ECS/TFC/CLK** as required.



Flex Cable for LV/HV & return

4× 8.96 Gbps up-links
1× 2.56 Gbps down-link
per VTRx+

Multiple lpGBTs
& VTRx+
on a FE Module

LV options:

1. Serial powering at FE
2. DC-DC convertors at FE
3. Individually regulated at SBC

Current detector modeling

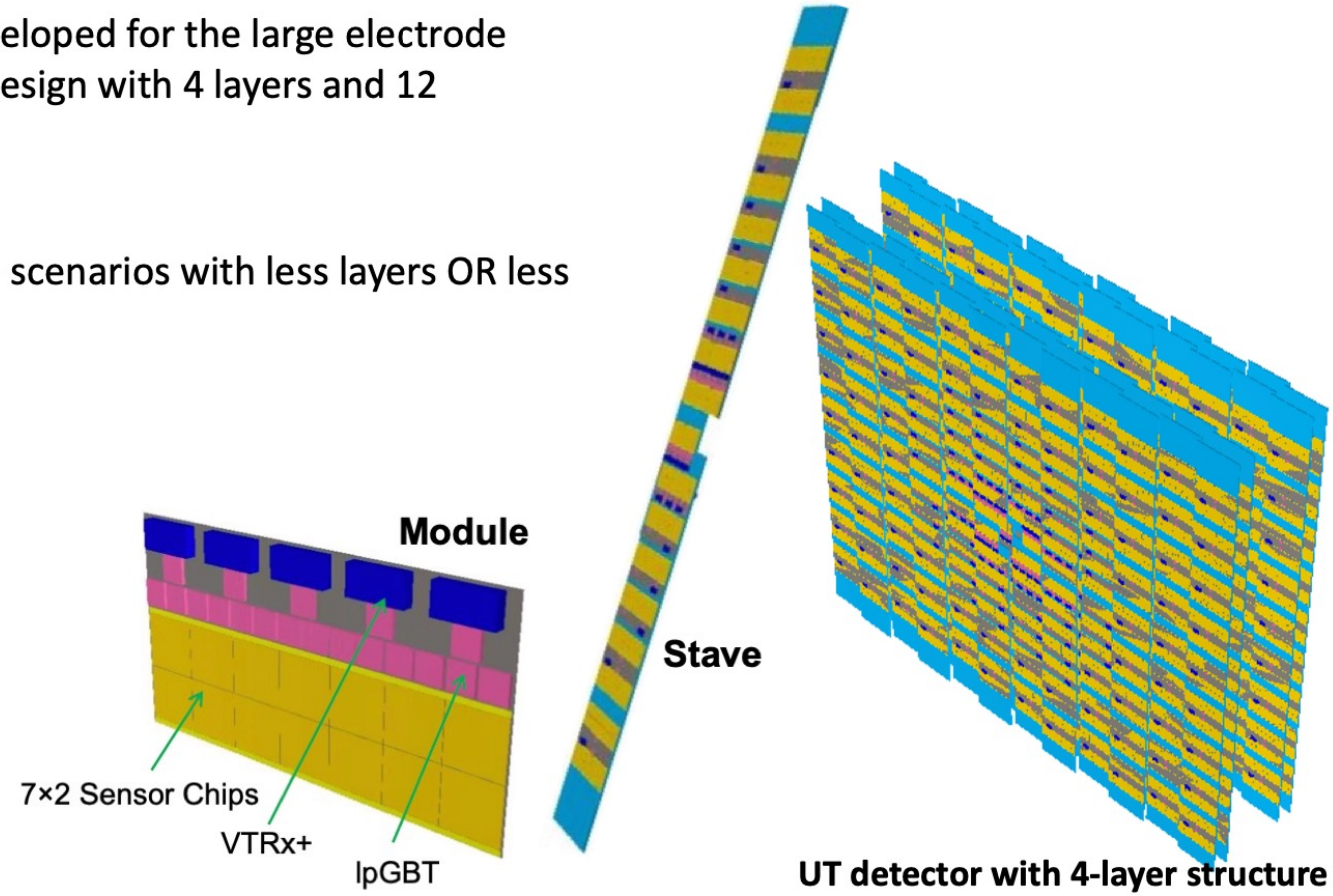
Detector description has been developed for the large electrode solution (HV-CMOS). The default design with 4 layers and 12 stave/layer applied

For scoping document studies, the scenarios with less layers OR less staves also ready

- 3-layers design
- 10-stave design

For the small electrode solution, development ongoing

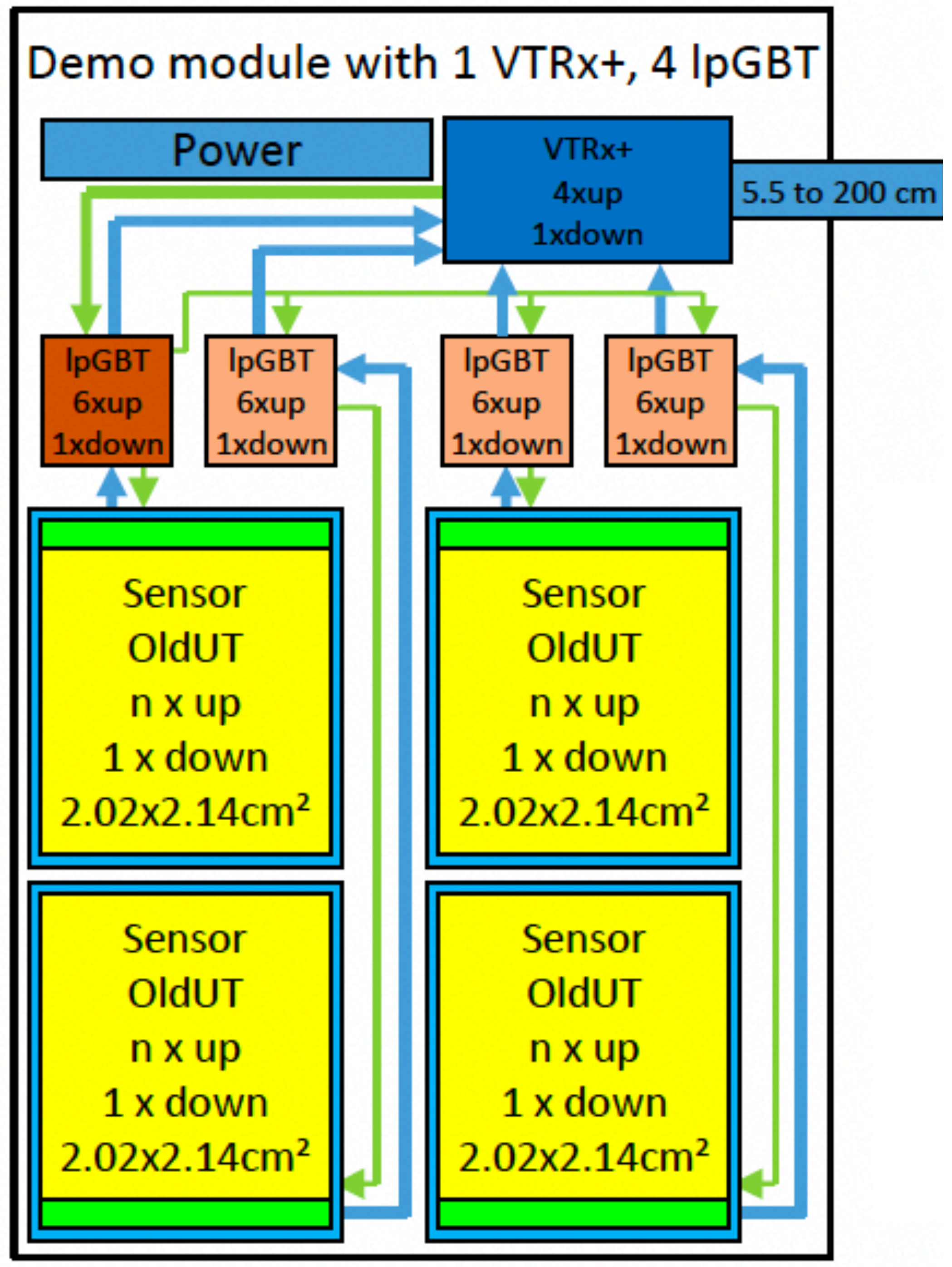
Simulation used for the tracking studies

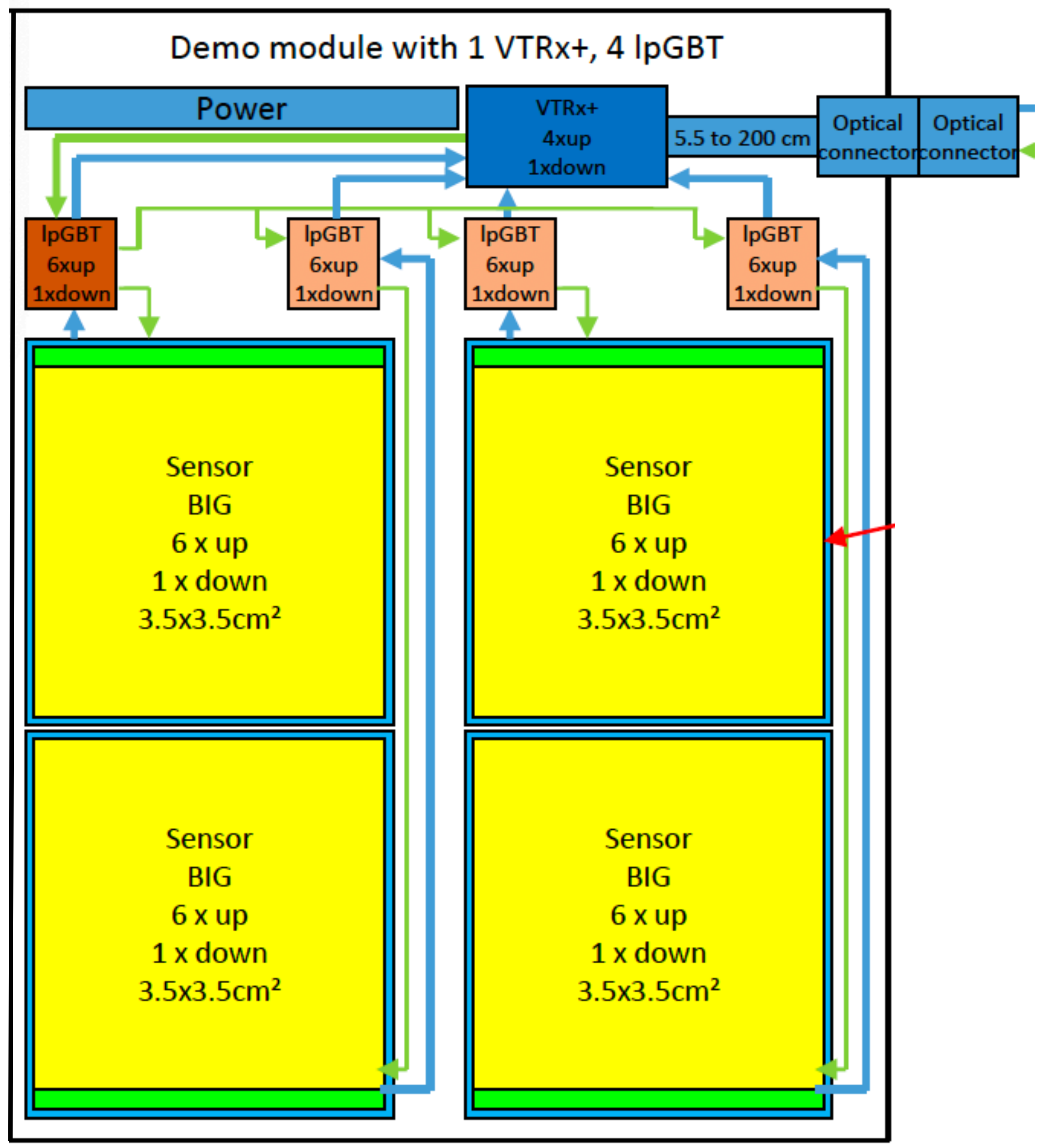


Module design and material budget

Target budget: 1%X_0 per plane

Different module designs





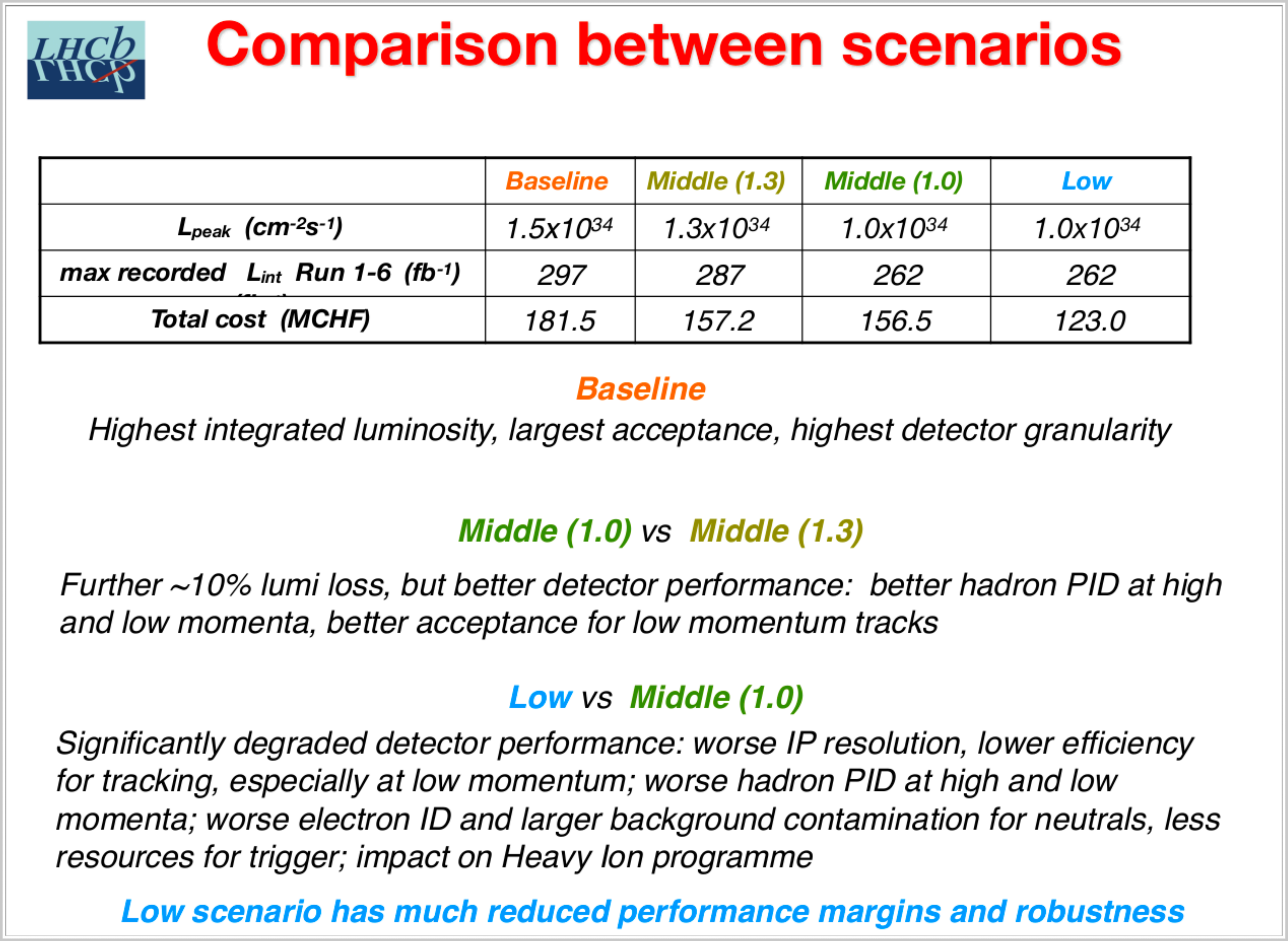
Scenario (Thickness 200µm)	%X_0/plane
Optimise lpGBT e-links	0.77
No VTRx+ in modules	0.63
No lpGPT nor VTRx+	0.46

Scenario (No lpGPT + VTRx+)	%X_0/plane
Thickness 200µm	0.46
Thickness 100µm	0.41
Thickness 50µm	0.38

© SUBATECH, Nantes

Does not include the cooling + UT box

UT and LHCb's scoping document



Comparison between scenarios

	Baseline	Middle (1.3)	Middle (1.0)	Low
L_{peak} ($cm^{-2}s^{-1}$)	1.5×10^{34}	1.3×10^{34}	1.0×10^{34}	1.0×10^{34}
max recorded L_{int} Run 1-6 (fb^{-1})	297	287	262	262
Total cost (MCHF)	181.5	157.2	156.5	123.0

Baseline

Highest integrated luminosity, largest acceptance, highest detector granularity

Middle (1.0) vs **Middle (1.3)**

Further ~10% lumi loss, but better detector performance: better hadron PID at high and low momenta, better acceptance for low momentum tracks

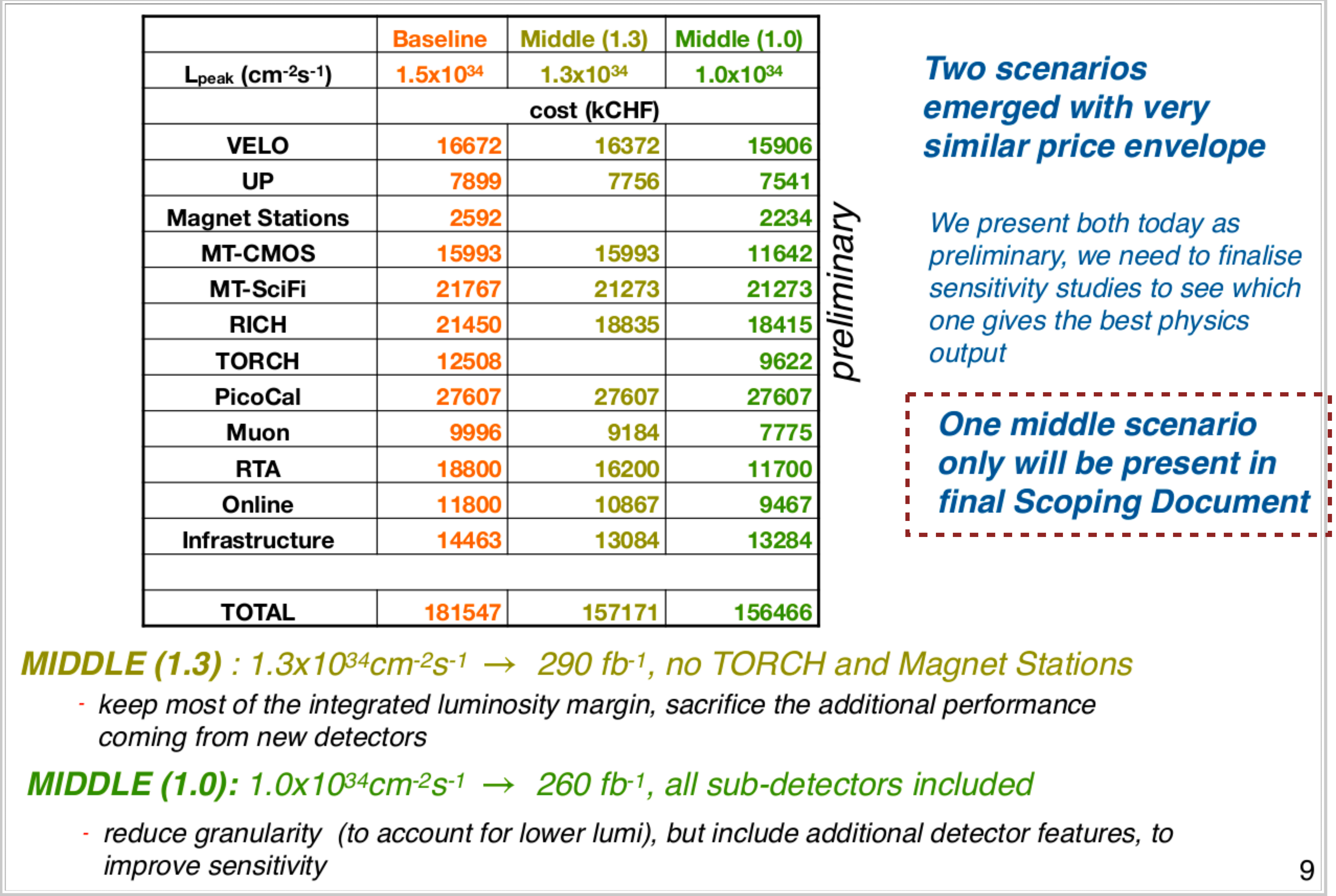
Low vs **Middle (1.0)**

Significantly degraded detector performance: worse IP resolution, lower efficiency for tracking, especially at low momentum; worse hadron PID at high and low momenta; worse electron ID and larger background contamination for neutrals, less resources for trigger; impact on Heavy Ion programme

Low scenario has much reduced performance margins and robustness

Slides from the Ressource Review Board (CERN review)

UT and LHCb's scoping document



	Baseline	Middle (1.3)	Middle (1.0)
L_{peak} ($cm^{-2}s^{-1}$)	$1.5\text{x}10^{34}$	$1.3\text{x}10^{34}$	$1.0\text{x}10^{34}$
	cost (kCHF)		
VELO	16672	16372	15906
UP	7899	7756	7541
Magnet Stations	2592		2234
MT-CMOS	15993	15993	11642
MT-SciFi	21767	21273	21273
RICH	21450	18835	18415
TORCH	12508		9622
PicoCal	27607	27607	27607
Muon	9996	9184	7775
RTA	18800	16200	11700
Online	11800	10867	9467
Infrastructure	14463	13084	13284
TOTAL	181547	157171	156466

preliminary

Two scenarios emerged with very similar price envelope

We present both today as preliminary, we need to finalise sensitivity studies to see which one gives the best physics output

One middle scenario only will be present in final Scoping Document

MIDDLE (1.3) *: $1.3\text{x}10^{34} cm^{-2}s^{-1}$ → 290 fb^{-1}, no TORCH and Magnet Stations*

- *keep most of the integrated luminosity margin, sacrifice the additional performance coming from new detectors*

MIDDLE (1.0): *$1.0\text{x}10^{34} cm^{-2}s^{-1}$ → 260 fb^{-1}, all sub-detectors included*

- *reduce granularity (to account for lower lumi), but include additional detector features, to improve sensitivity*

Slides from the Ressource Review Board (CERN review)

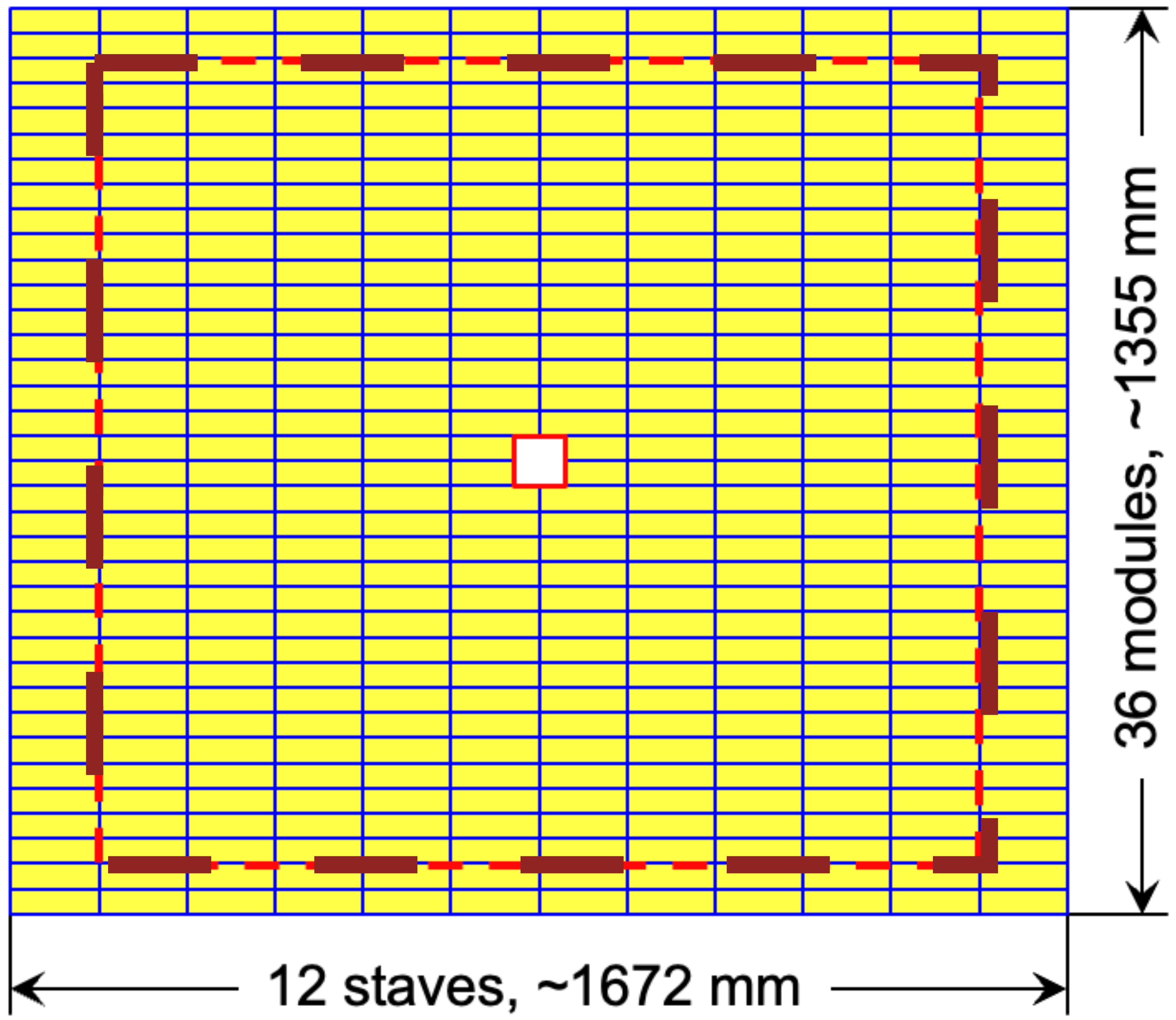
UT scoping scenario

1) Reduced coverage: **(12→10)** staves × **(36→32)** modules
   - Reduce 26% detection area at the outer ring
   - The overall budget decreases from 9.6 MCHF to 7.9 MCHF by this de-scoping alone

Already implemented in the new baseline

2) Reduced peak luminosity (**1.5→1.3→1.0**)×10^{34} cm^{-2} s^{-1}
   - Designs of sensor chip & detector module are less difficult, even though the cost reduction is not very significant
   - Save 156 kCHF for (**1.5→1.3**)×10^{34} cm^{-2} s^{-1}, or 143 kCHF on top of the coverage reduction
   - Save 389 kCHF for (**1.5→1.0**)×10^{34} cm^{-2} s^{-1}, or 358 kCHF on top of the coverage reduction

3) Improve the yield of sensor chip: **(40→60)%**
   - It may be feasible to optimize the sensor chip production and wafer test procedure and improve the yield
   - It could reduce the baseline budget by ~10%

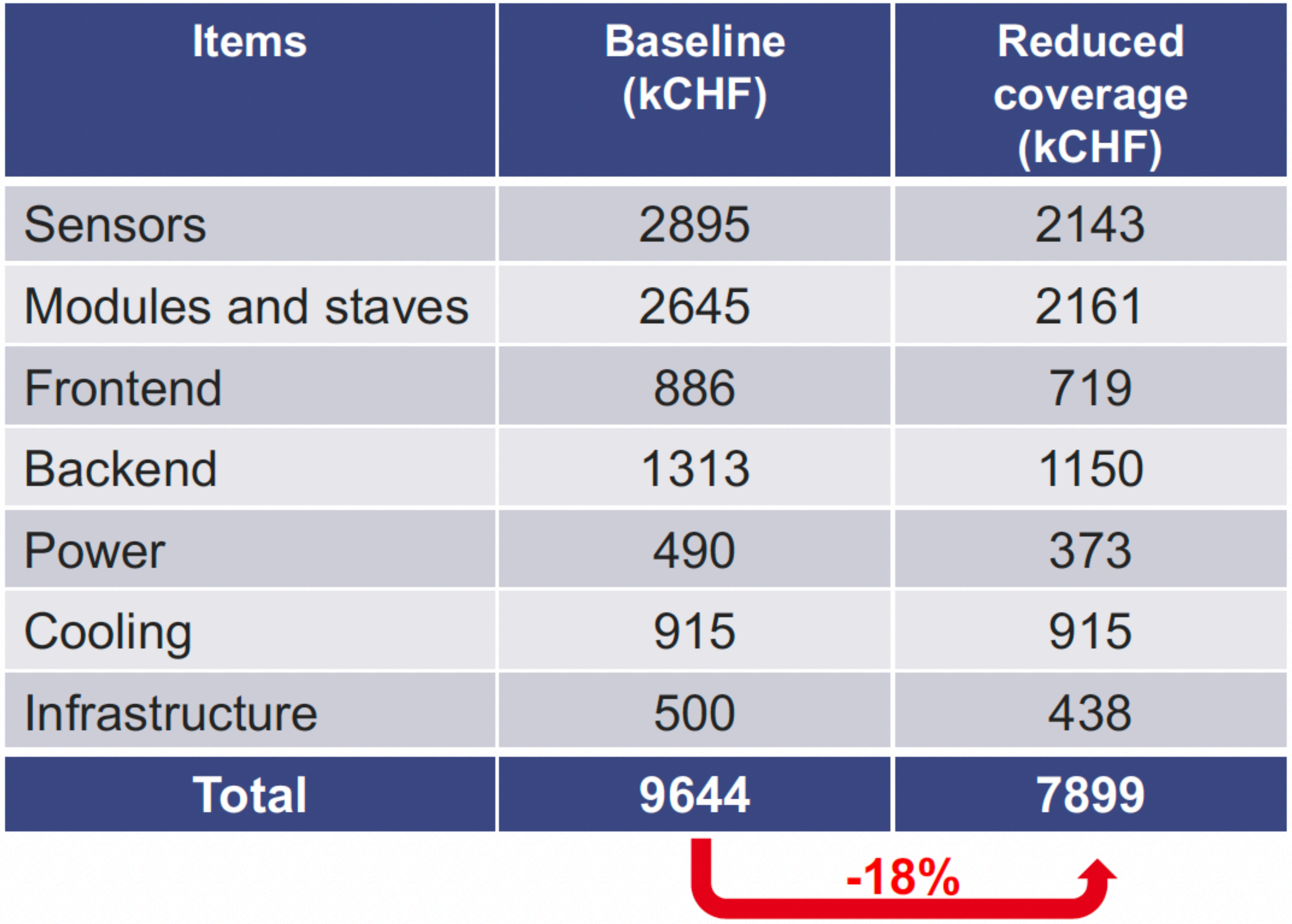


Other options studied but discarded in the cost descoping:

➡Reduce the number of planes $(4 \rightarrow 3)$

➡Increase central hole $(\eta: \ 4.8 \rightarrow 4.5)$

Scoping scenarios



Items	Baseline (kCHF)	Reduced coverage (kCHF)
Sensors	2895	2143
Modules and staves	2645	2161
Frontend	886	719
Backend	1313	1150
Power	490	373
Cooling	915	915
Infrastructure	500	438
Total	**9644**	**7899**

-18%

Scoping scenarios

Items	Baseline (kCHF)	New baseline (kCHF)	Reduced luminosity (kCHF)	Reductions + incr. yield (kCHF)
Sensors	2895	2143	2143	1436
Modules and staves	2645	2161	2119	2119
Frontend	886	719	661	661
Backend	1313	1150	892	892
Power	490	373	373	373
Cooling	915	915	915	915
Infrastructure	500	438	438	438
Total	**9644**	**7899**	**7541**	**6834**

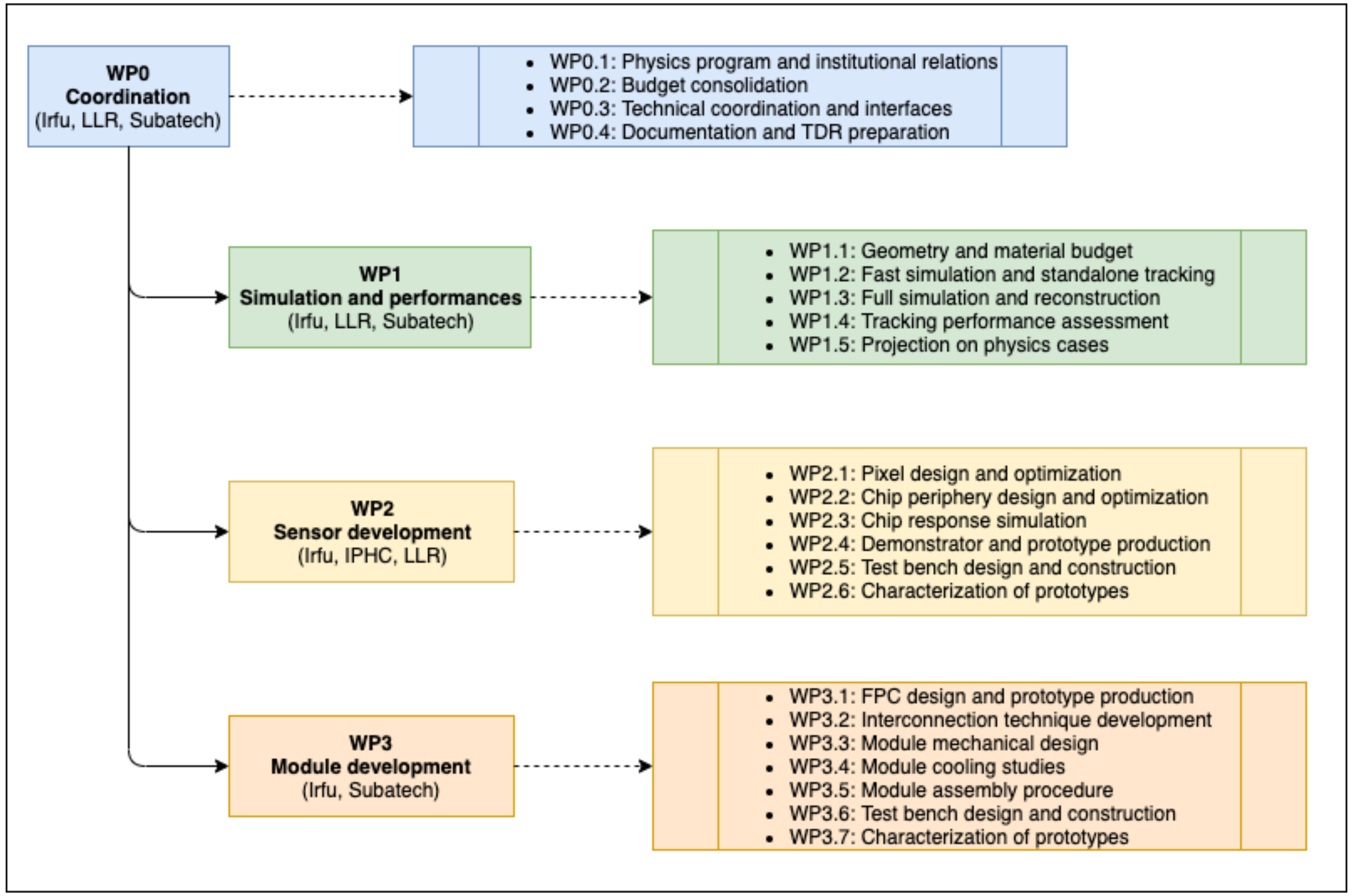
-5%

-14%

Project organisation

- Organization of the UT project is under construction:
  - Partners:
  - Steering of the proto-collaboration:
    - Jianchun Wang (IHEP, Beijing), Stefano M. Panebianco (Irfu)
  - Definition of the Work Packages and preparation of subtasks

WP	Name	Coordinators
0	Project Management	Jianchun Wang (IHEP, Beijing) **Stefano Panebianco (Irfu)**
1	Simulation, reconstruction and performance studies	**Benjamin Audurier (Irfu)** Xuhao Yuan (IHEP, Beijing)
2	Sensor chip design and characterization	Yiming Li (IHEP, Beijing) **Fabrice Guilloux (Irfu)** Franck Gastaldi (LLR)
3	Stave and module design and characterization	Jiesheng Yiu (HNU, Hunan) **Charlotte Riccio (Irfu)**
4	Mechanics, integration and services	Manuel Guittière (Subatech)
5	Readout architecture and integration into LHCb DAQ	Kai Liu (LZU, Lanzhou)



WP0
Coordination
(Irfu, LLR, Subatech)

- WP0.1: Physics program and institutional relations
- WP0.2: Budget consolidation
- WP0.3: Technical coordination and interfaces
- WP0.4: Documentation and TDR preparation

WP1
Simulation and performances
(Irfu, LLR, Subatech)

- WP1.1: Geometry and material budget
- WP1.2: Fast simulation and standalone tracking
- WP1.3: Full simulation and reconstruction
- WP1.4: Tracking performance assessment
- WP1.5: Projection on physics cases

WP2
Sensor development
(Irfu, IPHC, LLR)

- WP2.1: Pixel design and optimization
- WP2.2: Chip periphery design and optimization
- WP2.3: Chip response simulation
- WP2.4: Demonstrator and prototype production
- WP2.5: Test bench design and construction
- WP2.6: Characterization of prototypes

WP3
Module development
(Irfu, Subatech)

- WP3.1: FPC design and prototype production
- WP3.2: Interconnection technique development
- WP3.3: Module mechanical design
- WP3.4: Module cooling studies
- WP3.5: Module assembly procedure
- WP3.6: Test bench design and construction
- WP3.7: Characterization of prototypes

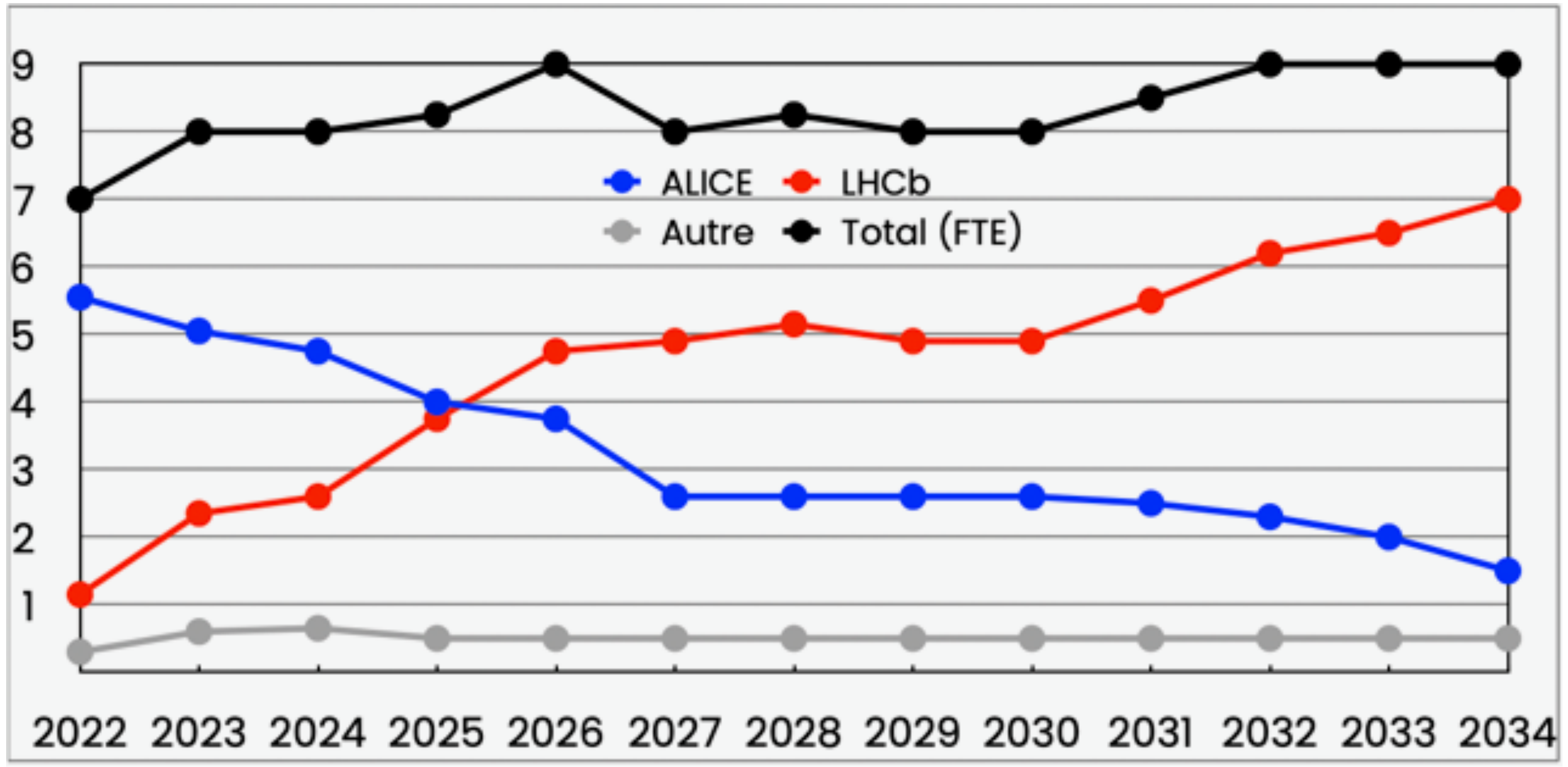
R&D Plan

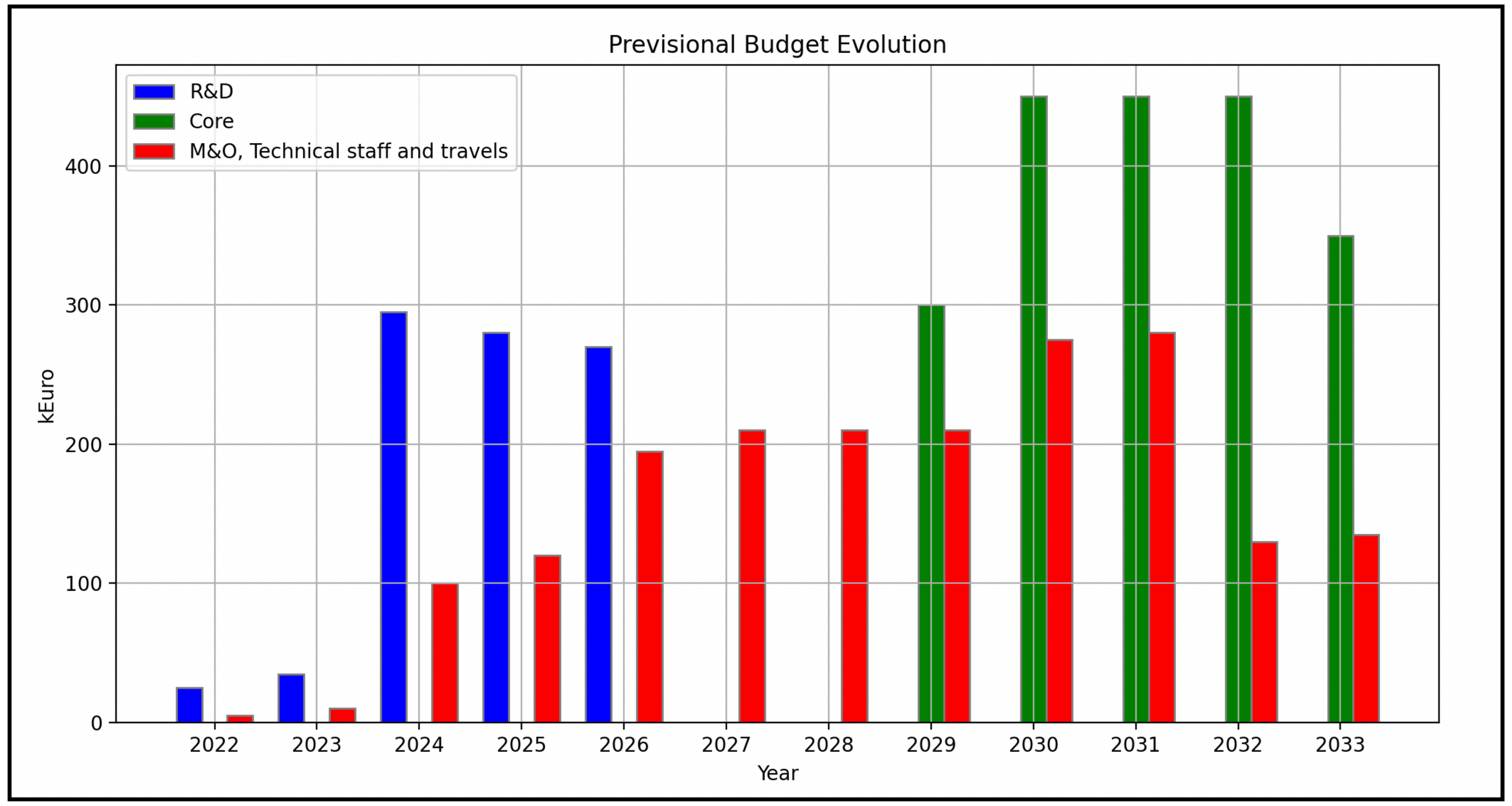
	2024				2025				2026				2027			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
WP1 **Simulation and performances**	Optimization of geometry and material budget	🟩	🟩	🟩												
		Fast simulations	🟩	🟩												
					Consolidation on detailed specifications	🟩	🟩									
			First version of standalone tracking	🟩	🟩											
						Full simulations	🟩	🟩								
				First version of global tracking	🟩	🟩										
									Optimization of tracking performances	🟩	🟩	🟩				
										Application to chosen physcs cases	🟩	🟩	🟩			
												Finalisation of TDR	🟩			
														Implementation of reco algorithm	🟩	🟩
WP2 **Sensor**	Qualification of MALTA3	🟨	🟨	🟨												
				Design of MALTA4	🟨	🟨										
							Submission of MALTA4 ER	🟨								
									Qualification of MALTA4	🟨	🟨	🟨				
	SPARC design finalization	🟨														
			Submission or SPARC ER	🟨												
					Qualification of SPARC	🟨	🟨	🟨								
							Submission of MPR2	🟨								
									Qualification of MPR2	🟨	🟨	🟨				
												Finalisation of TDR	🟨			
														Pre-prod of chosen sensor	🟨	🟨
WP3 **Module**	Cooling preliminary studies	🟧														
	Readout preliminary studies	🟧														
		Module design studies	🟧													
				Prototypes production	🟧	🟧										
						Prototypes qualification	🟧	🟧								
								Design optimization	🟧							
										Full scale demo production	🟧					
												Full scale demo qualification	🟧			
												Finalisation of TDR	🟧			
														Pre-prod of first modules	🟧	🟧

Reminder of the Irfu investment

- **Total investment profile**
  - R&D up to 2026: consider two parallel axes on CMOS R&D (in 2023–2024)
    - Expected total contribution of ~900k€
  - Construction (CORE) 2027–2031 => only chip production is envisaged
    - Core cost includes 20% margin with respect to surface-scaled MFT cost
    - Eventual saving from MT-UT convergency in one single project is not taken into account
    - Expected total contribution between 1-2M€
  - Installation in 2033. Start of data taking 2035
    - Start of M&O-B payment in Run 4

Person-power DPhN

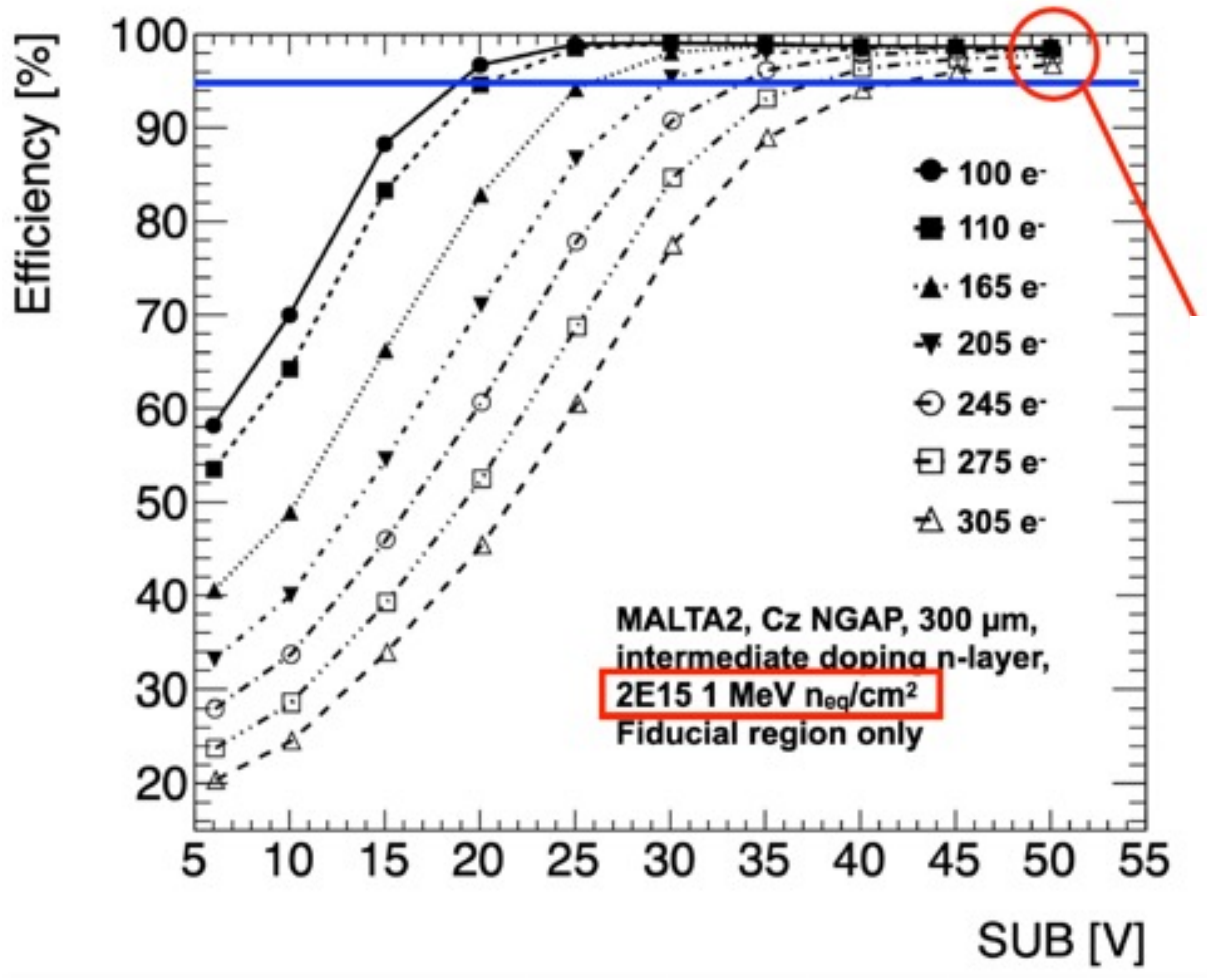


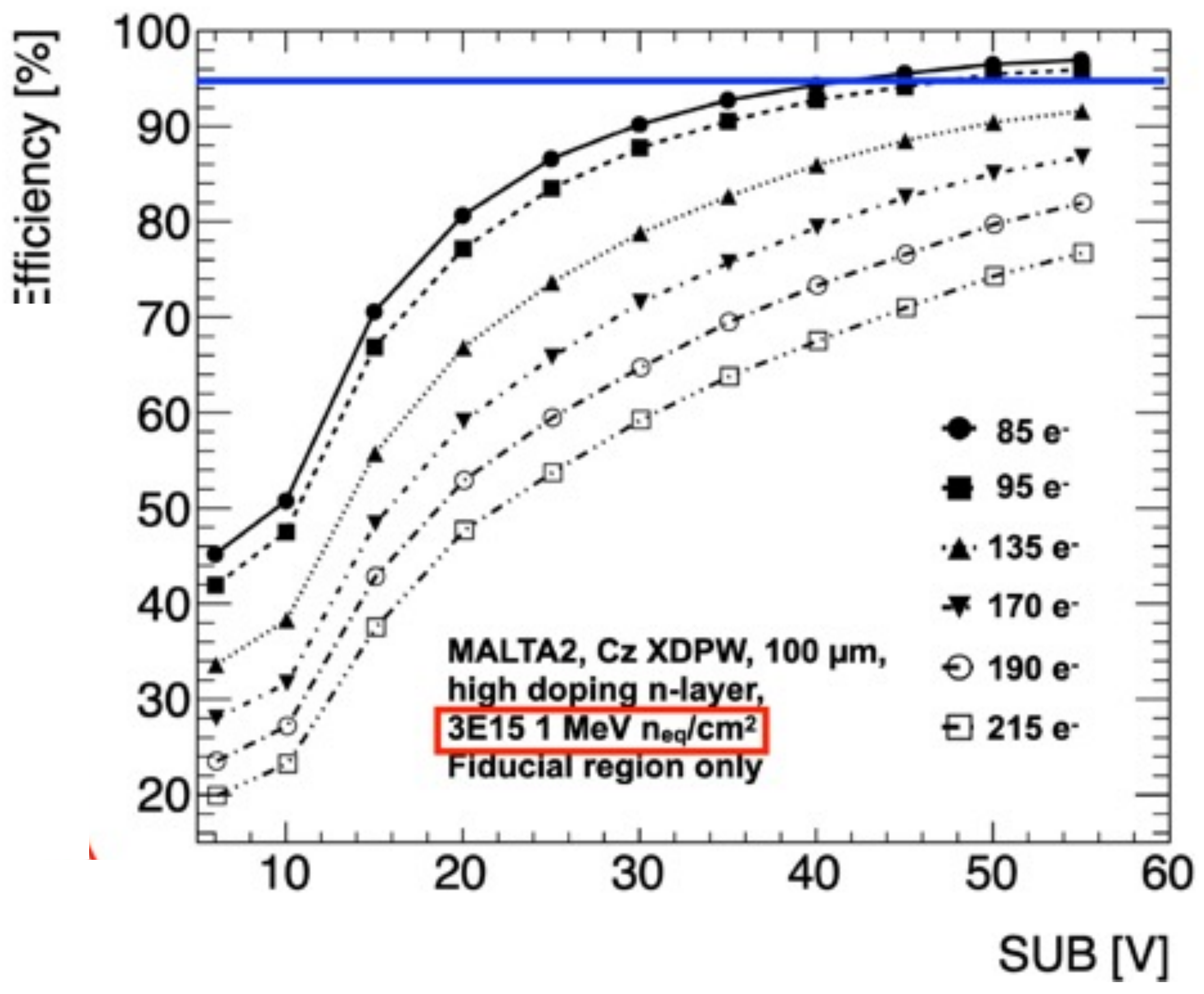


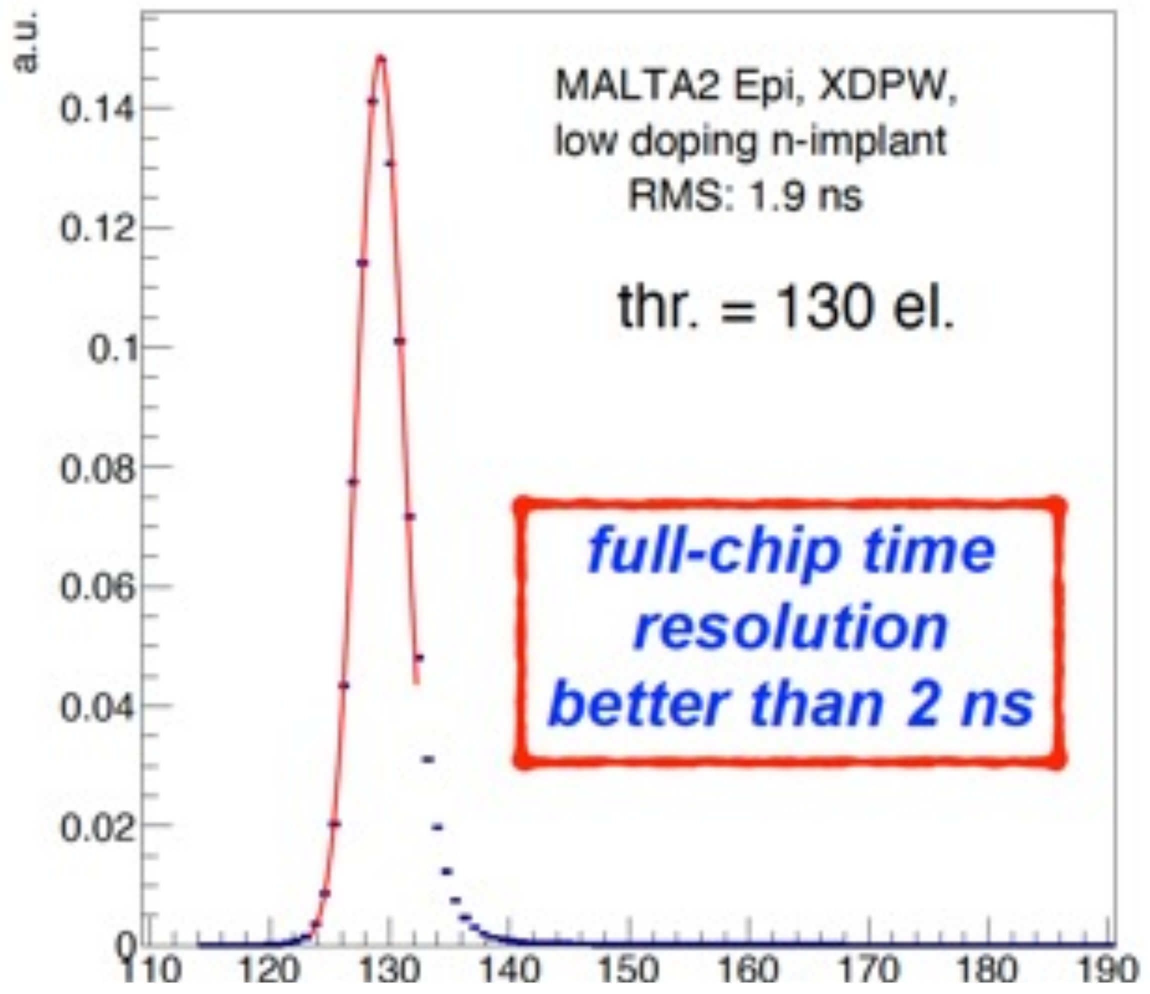
BACK-UP

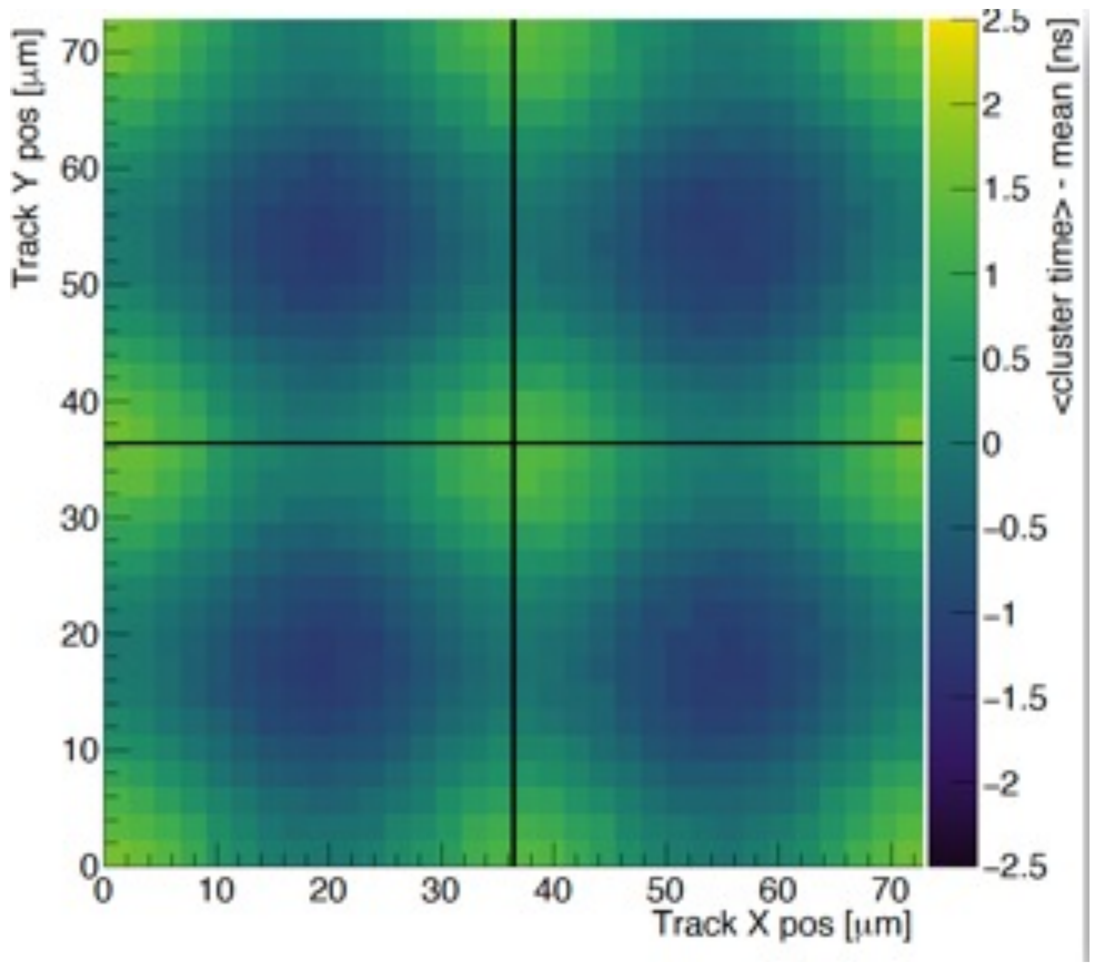
MALTA – TJ180

- Existing chip in well proved technology and extensively qualified
- Present version is MALTA3
  - Ongoing chip testing and qualification (in lab and on test beams for irradiated and not irradiated chips)
- Present performances:
  - Position resolution: ~ 5 μm
  - Time tagging (without ToT): fully efficient in 25 ns
  - Power consumption: ~ 90 mW/cm^2
  - High efficiency (>95%) for a dose rate of 3x10^{15} 1 MeV n$_{eq}$/cm^2 (but cooled down to -20 °C)
- Development of LHCb-oriented readout periphery blocs to cope with the high data rate
  - Virtual pixel: cluster or group of pixels
  - Creation of the building blocks of a generic data compressor



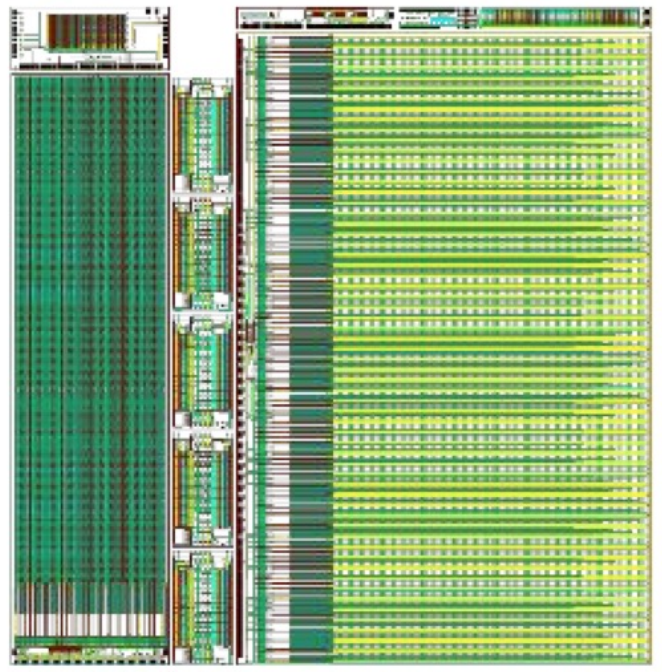




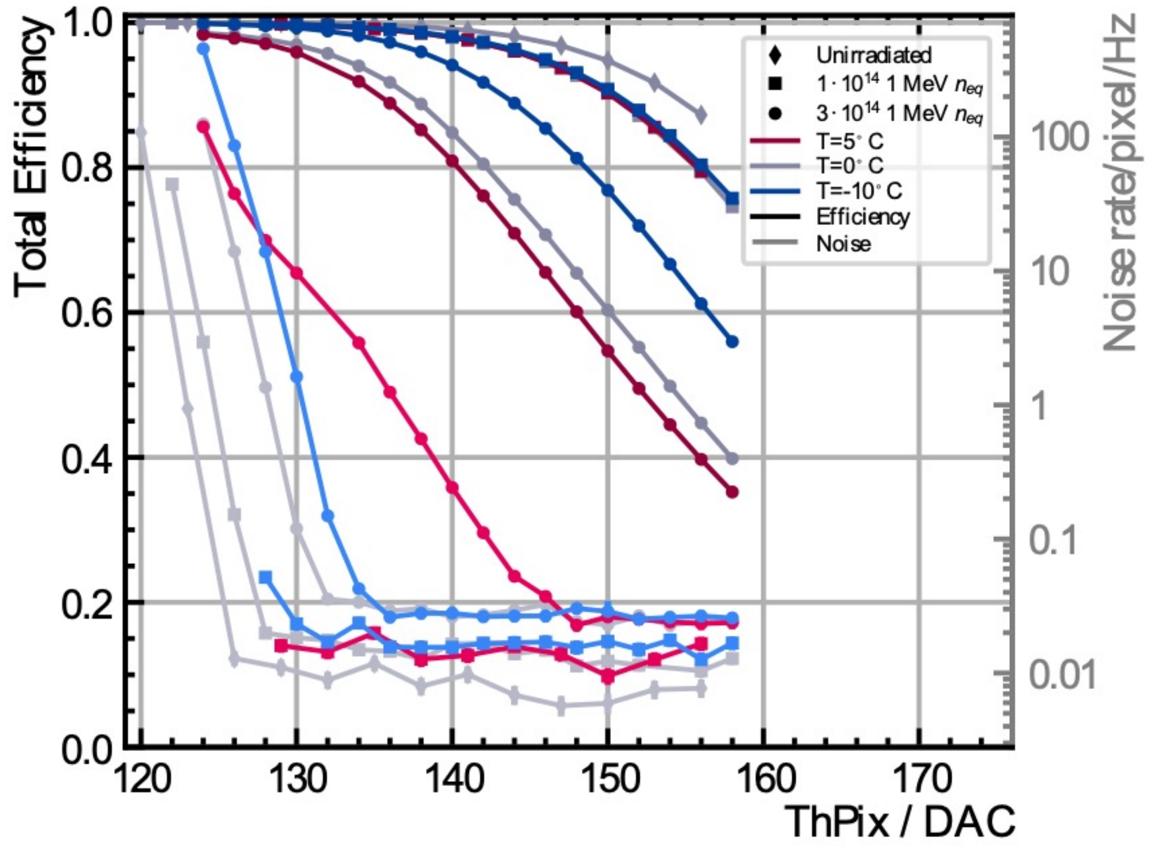


MightyPix – AMS180

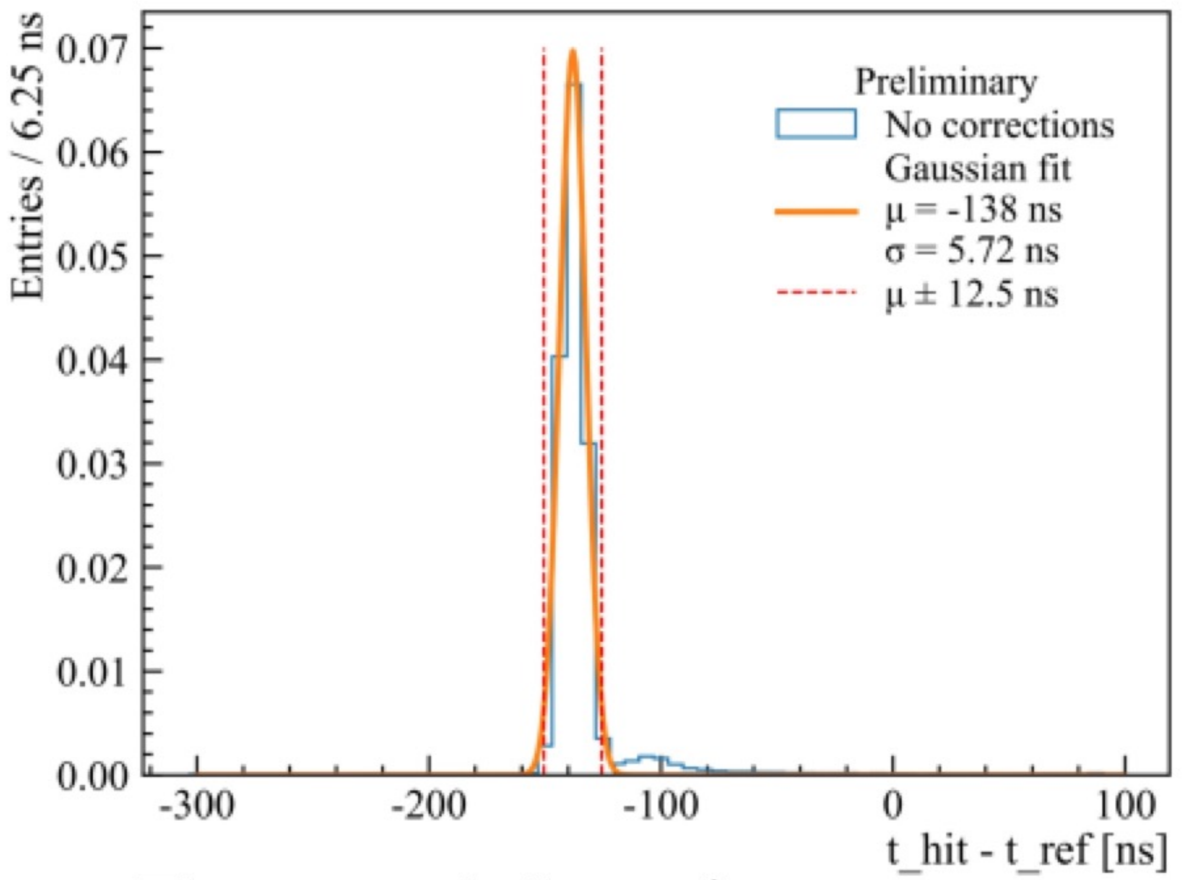
- Existing chip in well proved technology and extensively qualified
- Present qualified version is MightyPix1
  - Production in TSI180 is stopped
  - Redesign in AMS180
  - Possible design in LF150
- Very encouraging results from MightyPix1
  - Position and time resolution
  - Power consumption: 56 mW/cm^2
- The present design does not meet the UT specs in terms of data rate and radiation dose



MightyPix1



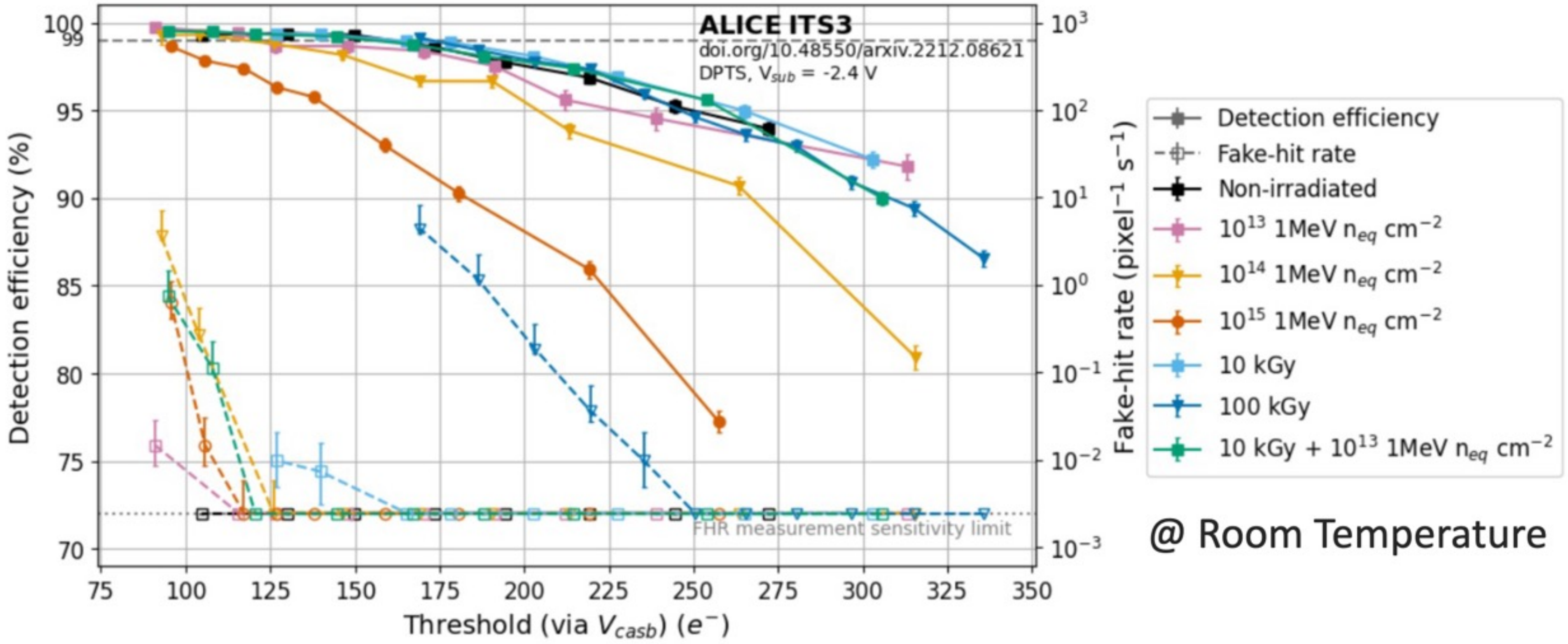
Radiation hardness tests



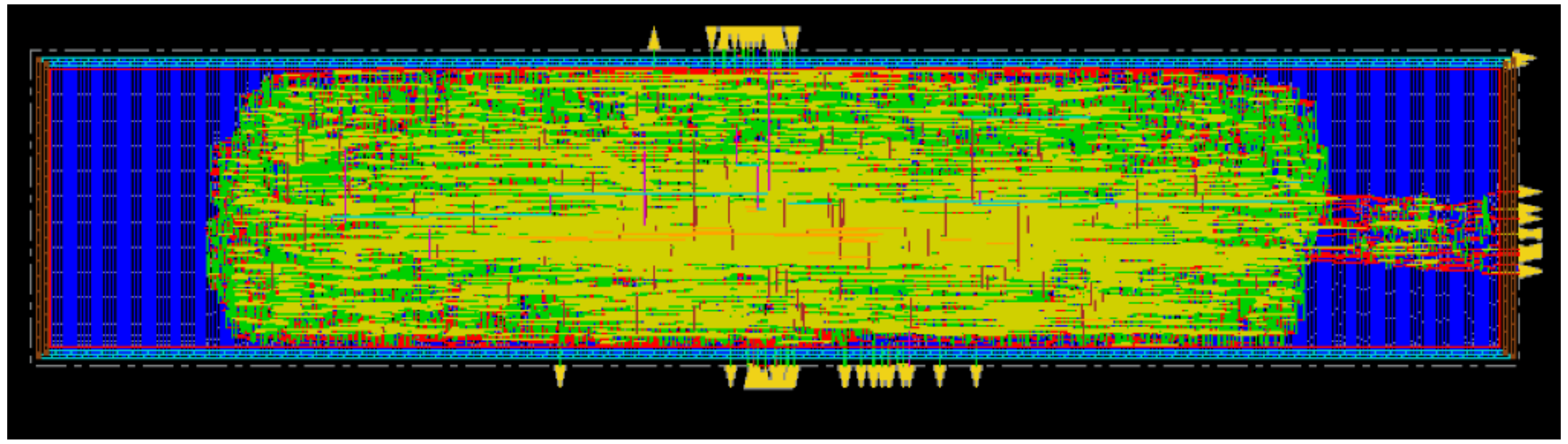
Time resolution of MightyPix1 (preliminary)

SPARC – TPSCo65

- New and challenging technology for MAPS
- Very encouraging results within ALICE-ITS3 project
  - High efficiency (>95%) for a dose rate of several 10^{15} 1 MeV n_{eq}/cm^2 (at room temperature!)
- Ongoing collaboration between IPHC (Strasbourg) and Irfu (Saclay) on the development of digital blocks of readout periphery (as for MALTA)
- Development of a TV for ER2 (2024) to assess TPSCo 65nm radiation hardness + in-chip time tagging investigation
- MLR2 for a second prototype in 2025.



@ Room Temperature

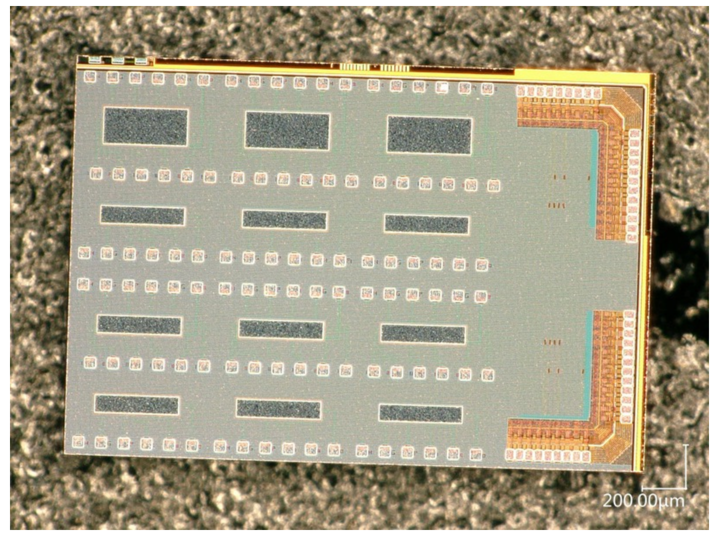


FIFO memory in 65 nm designed at Irfu for SPARC

COFFEE – SMIC55

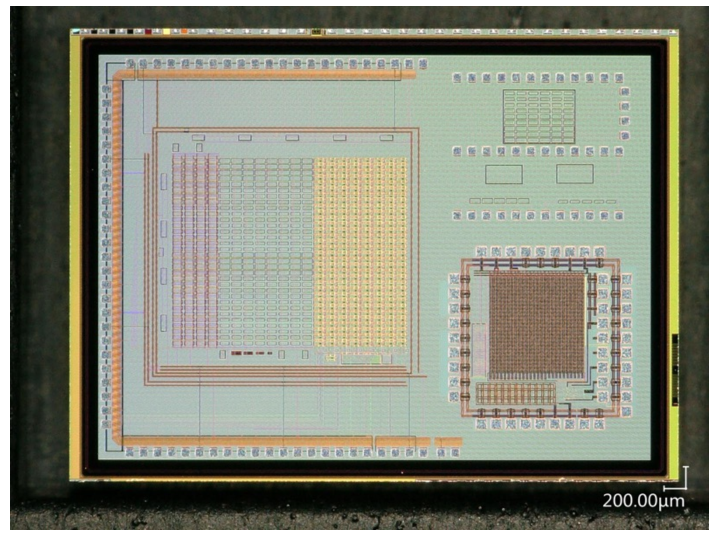
SMIC 55nm Low-Leakage process

- Not HV, yet with a similar deep n-well structure
- MPW submitted in Oct 2022 in normal wafer
- COFFEE1 received in Apr 2023



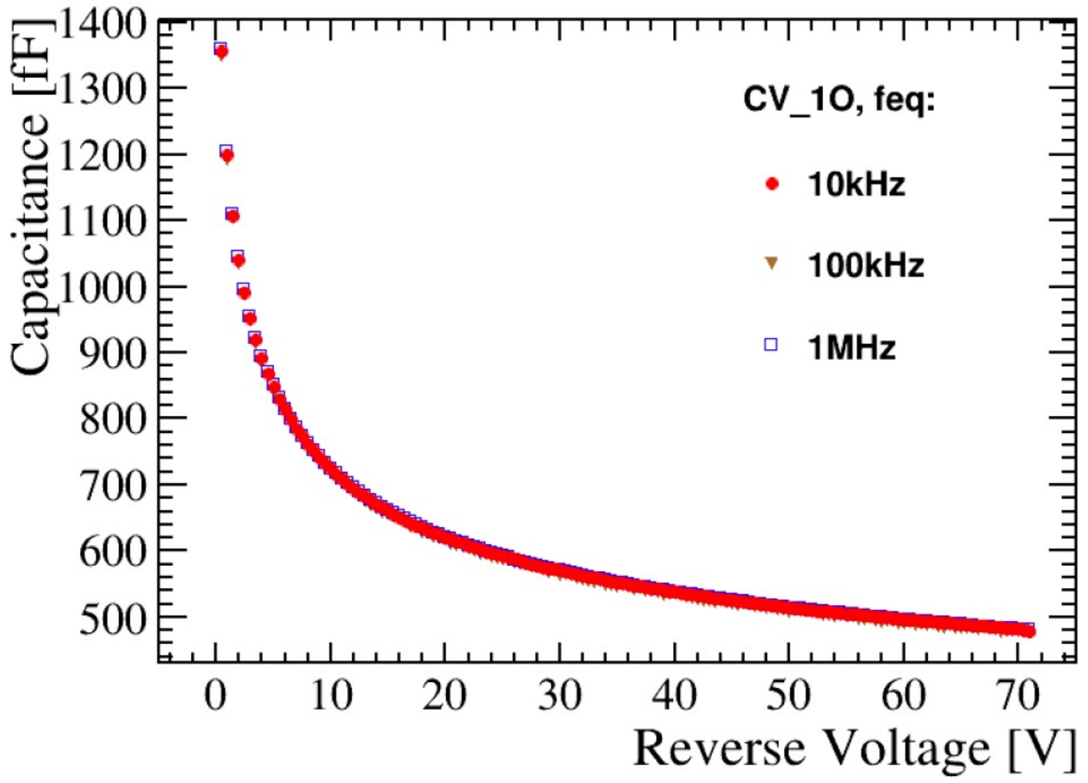
SMIC 55nm HVCMOS process

- HVCMOS process, with 1kΩ ·cm wafer
- MPW submitted in Aug 2023
- COFFEE2 received in Dec 2024

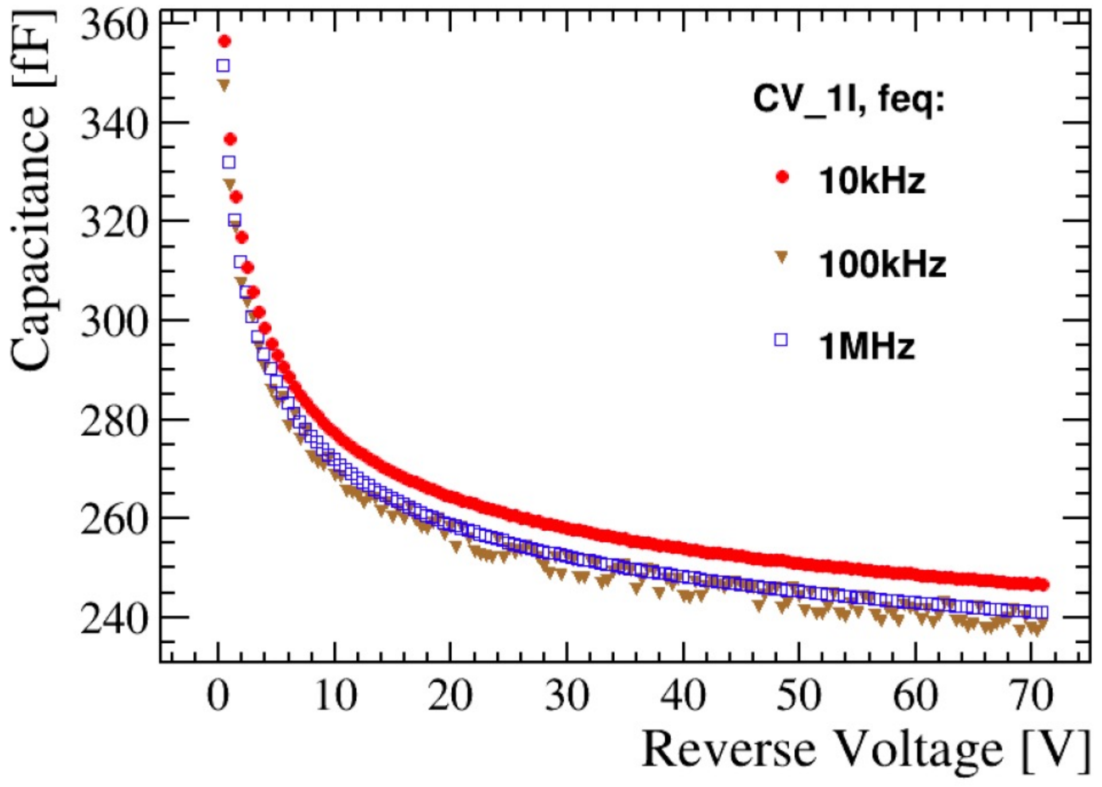


MPW with SMIC HV 55nm

- High-res wafer of 1k or 2k Ωcm available
- Real validation of the sensor!
- 4mm * 3mm in area
- Passive arrays similar as COFFEE1
- Two-pixel arrays with in-pixel amplifier and more digital design
- Submitted in Aug 2023
- Received in Dec 2024
- Test started



CV of 8-pixel connected
C(8) = 8*C0 + offset?



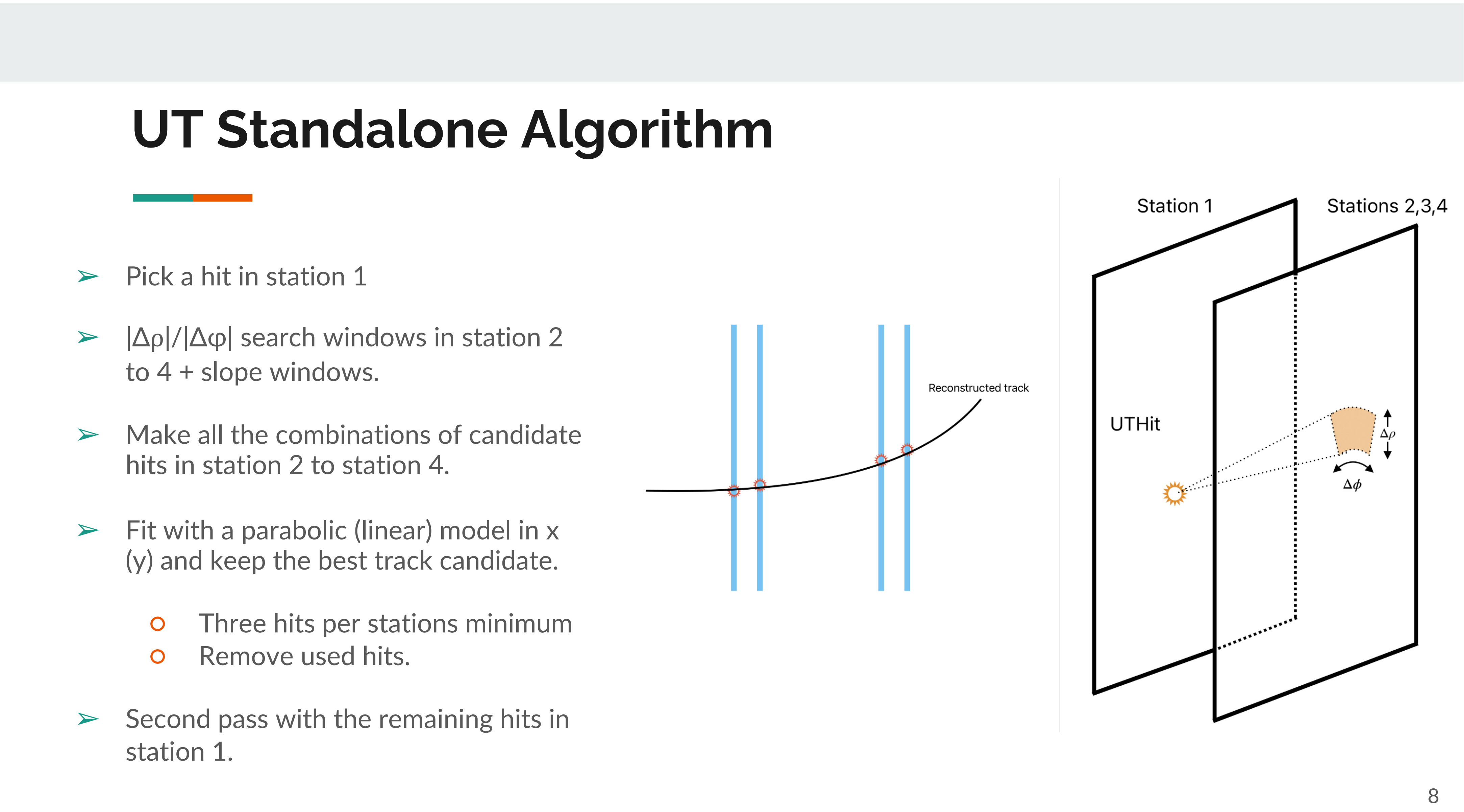
CV of a single pixel
C(1) =1*C0 + offset?

Breakdown voltage up to – 70V

Capacitance (with offset subtracted) scales with sensor area

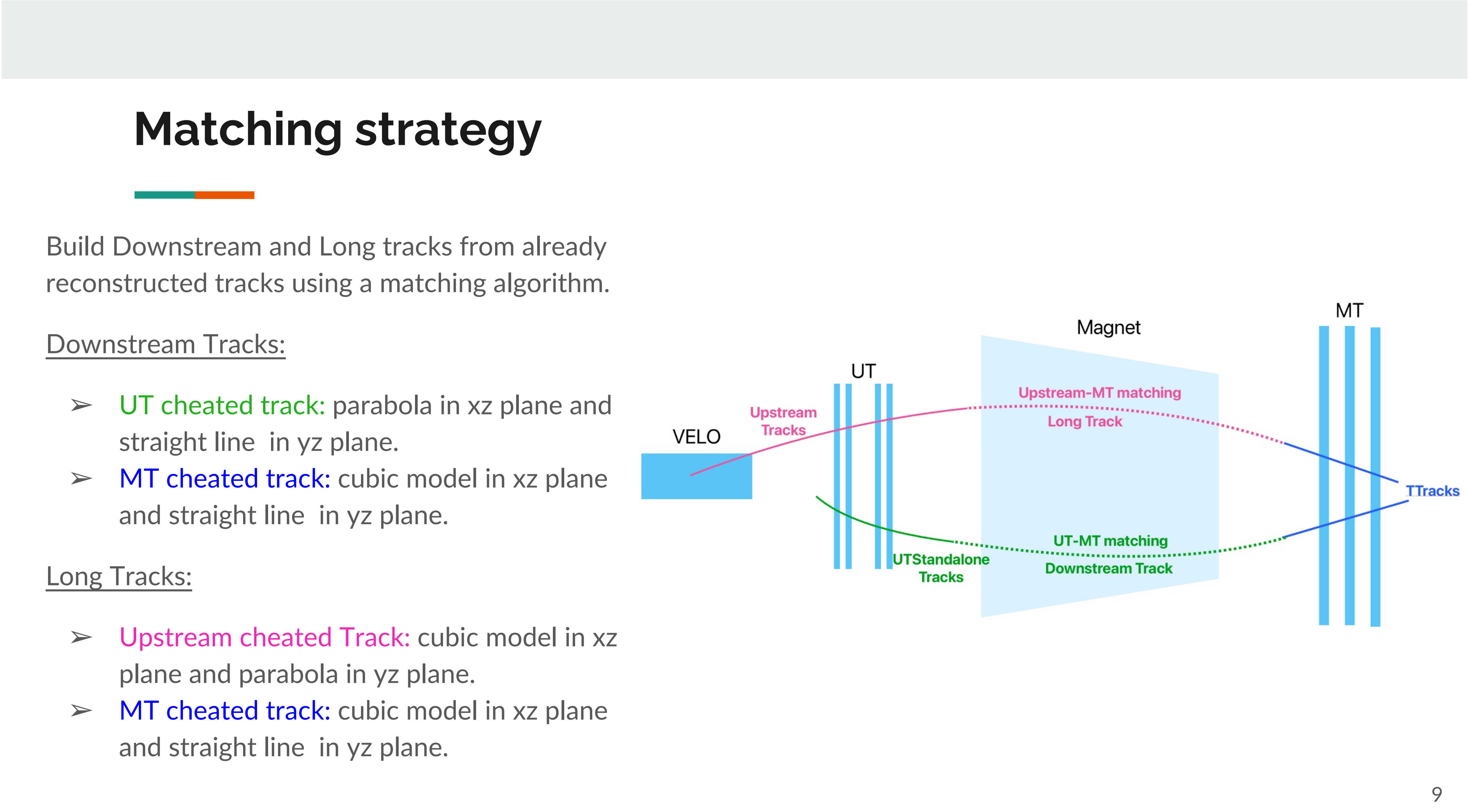
Tracking studies status

- Studies done using the py_pattern_reco framework.
- Three algorithms tested so far:
  - UT standalone.
  - « Cheated Matching Dowstream » and « Cheated Matching LongTrack » algorithms.
    - For the « cheated matching LongTrack », a layer of Machine Learning is added to remove the ghosts.



UT Standalone Algorithm

- Pick a hit in station 1
- |Δρ|/|Δφ| search windows in station 2 to 4 + slope windows.
- Make all the combinations of candidate hits in station 2 to station 4.
- Fit with a parabolic (linear) model in x (y) and keep the best track candidate.
  - Three hits per stations minimum
  - Remove used hits.
- Second pass with the remaining hits in station 1.



Matching strategy

Build Downstream and Long tracks from already reconstructed tracks using a matching algorithm.

Downstream Tracks:

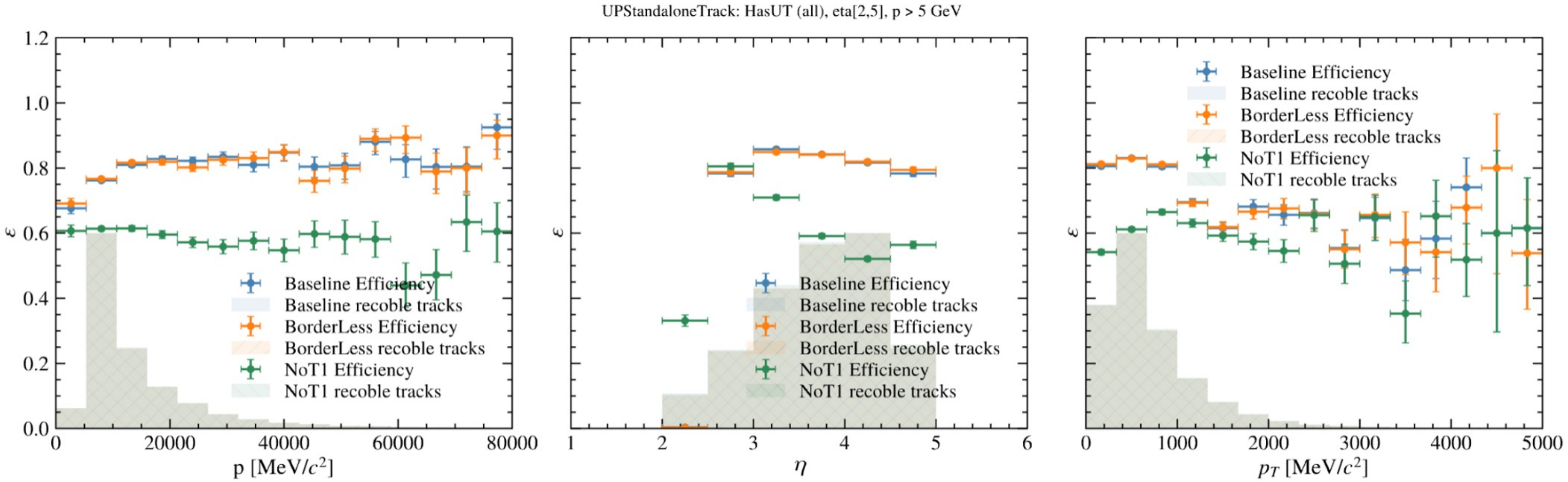
- UT cheated track: parabola in xz plane and straight line in yz plane.
- MT cheated track: cubic model in xz plane and straight line in yz plane.

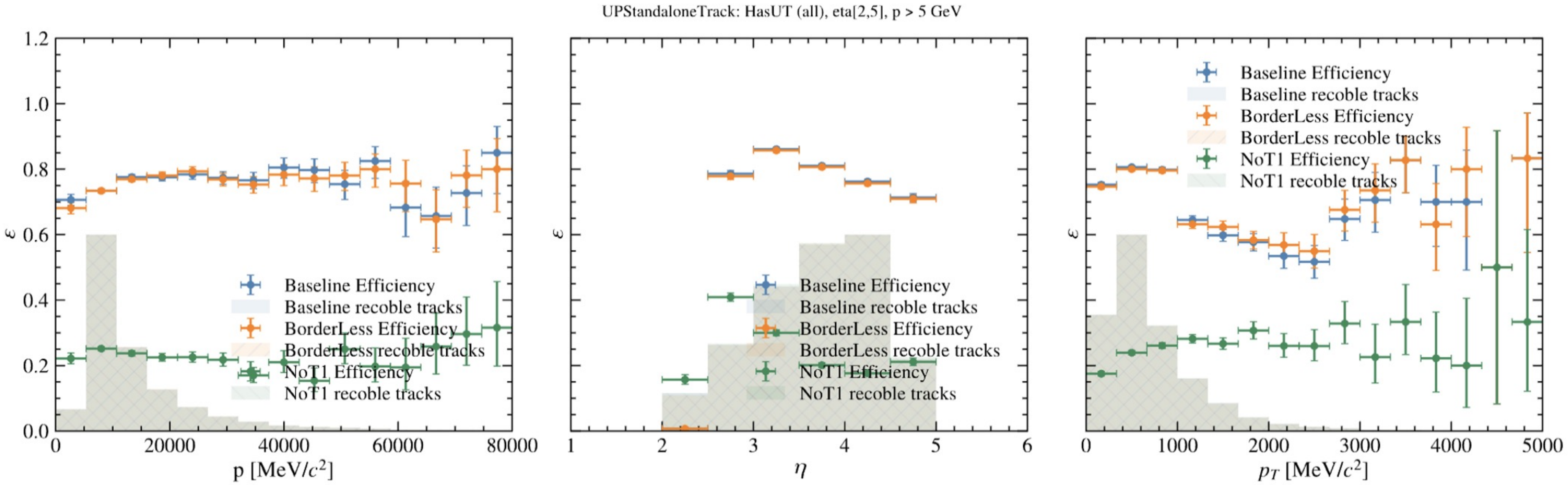
Long Tracks:

- Upstream cheated Track: cubic model in xz plane and parabola in yz plane.
- MT cheated track: cubic model in xz plane and straight line in yz plane.

Preliminary results

UT standalone Tracks Results (Preliminary)


UPStandaloneTrack: HasUT (all), eta[2,5], p > 5 GeV


UPStandaloneTrack: HasUT (all), eta[2,5], p > 5 GeV

ε	Baseline	Borderless	NoT1
pp	78 %	78 %	60%
PbPb	75%	75%	24%

- ➢ Very similar results in baseline and borderless cases.
- ➢ Drastic drop of the efficiencies when remove the first station.
- ➢ Results in pp and PbPb are very close.