KiCad Status 2024

Version 8 and beyond

Roberto Fernandez Bautista 14/06/2024

CERN electronics forum



Common Improvements

Properties Panel in all editors

Pro	perties	×						
Te	t Box							
=	Basic Properties	50 C	×					
	Start X	7250 mils		Nich 16.P5	This darings was beend in the v3.0 daring			
	Start Y	6543 mils			The Vides/-15.PS rails are studdent of reafford and the divert on the right. If paralises the following components: Rea, 3-0123 in left flowing and the Vides/-	en RESET is pailed kny, tals functi like functions by is net required to sail, read 12, to, this way pin 3 a little		
	End X	11550 mils						
	End Y	7243 mils						
	Line Width	0 mils						
	Line Style	Solid						
	Line Color							
	Filled					977877877		
	Fill Color			wee not bested yet, in GLO	the rd33 and -1.8 mile vive restan	wing LHQ4913, which		
9	Text Properties			as (assisted by the matter) is shorting the comparison the SIT physical the short in the a functionality is not required on not papalate the companies (16, 15, 199, 817).				
	Text	This design was not tested yet. In v		c) structures the LCDST regulator scholar divided LCS of a prover, for whether each structure is non-internet internet and structure and structure of the structure internet and structure of the structure is non-internet internet and structure and stru				
	Font	Default Font						
	Italic							
	Bold							
	Mirrored							
	Visible							
	Horizontal Justification	Left						
	Vertical Justification	Тор						
	Color	2000		was not insided get in site	He 45. 433 and 41.5 mile were not free	uning LHC4013, which		
	Hyperlink				13 mgaleter akouli dimiyata 0.15 %. Yawa			
	Text Size	50 mils						



Common Improvements

Properties Panel in all editors Import from third party tools

	Project	Schematic	PCB	Symbols	Footprints
Altium Designer		•	•		•
Altium Circuit Maker			•		
Altium Circuit Studio		•	•		•
CADSTAR	•	•	•	•	
EAGLE	•	•	•		•
EasyEDA / JLCEDA Std	•	•	•	•	
EasyEDA / JLCEDA Pro	•		•		
Fabmaster	N/A	N/A	•	N/A	N/A
gEDA					•
LTspice	N/A	•	N/A		N/A
P-CAD			•		
Solidworks PCB		•	•		•
		Key: Suppo 	rted in KiCad 7.0	Support	ed in KiCad 8.0

+ Import vector graphics (DXF and SVG) to Schematic + Symbol editors

port Vector Graphics File	-		×
ement			
0000			
7.87402		mi	ls
Inches	~		
Cancel		ОК	
	00000 7.87402 Inches	ement mils Y: 0 10000 7.87402 Inches	ement mils V: 0 mi 100000 7.87402 mi Inches ~



kicad-cli pcb drc kicad-cli sch erc kicad-cli sch bom

Common Improvements

Properties Panel in all editors

Import from third party tools

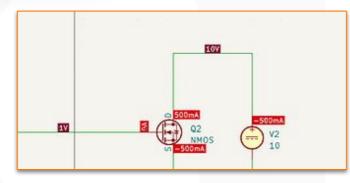
Command line drc, erc and native bom

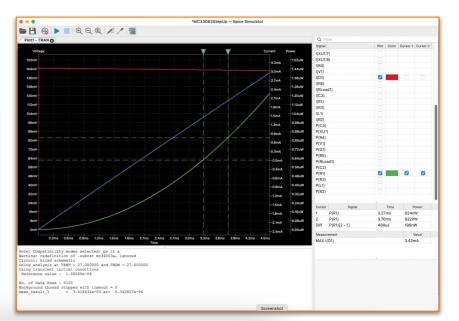


user@pc:\$ kicad-cli pcb drc myboard.kicad_pcb
Loading board
Running DRC
Found 497 violations
Found 200 unconnected items
Saved DRC Report to myboard.rpt
user@pc:\$ cat myboard.rpt
** Drc report for myboard.kicad pcb **
** Created on 2024-06-09T18:22:01+0200 **
** Found 497 DRC violations **
[diff_pair_gap_out_of_range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.6188
mm)
Rule: 100 ohm diff pair: error
@(161.8215 mm, 95.9016 mm): Track [/FPGAControler/SPI SCLK P] on L4 SIG, length 0.6443 mm
@(162.3504 mm, 96.4656 mm): Track [/FPGAControler/SPI SCLK N] on L4 SIG, length 1.2558 mm
[diff_pair_uncoupled_length_too_long]: Differential uncoupled length too long (100 ohm diff pair maximum uncoupled length
10.0000 mm; actual 10.8907 mm)
Rule: 100 ohm diff pair: error
@(161.3660 mm, 96.3572 mm): Track [/FPGAControler/SPI SCLK P] on F.Cu, length 0.7021 mm
@(161.3624 mm, 97.3536 mm): Track [/FPGAControler/SPI SCLK N] on F.Cu, length 0.7071 mm
[diff pair gap out of range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.6188
mm) Rule: 100 ohm diff pair; error
Q(161.8215 mm, 95.9016 mm): Track [/FPGAControler/SPI SCLK P] on L4 SIG, length 0.6443 mm
@(162.3504 mm, 96.4656 mm): Track [/FPGAControler/SPI_SCLK_N] on L4_SIG, length 1.2558 mm [diff pair gap out of range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.4769
Rule: 100 ohm diff pair; error
@(184.1112 mm, 94.3424 mm): Track [/FPGAControler/SPI_CS_P] on L4_SIG, length 5.0770 mm
Q(183.7836 mm, 94.9048 mm): Track [/FPGAControler/SPI_CS_N] on L4_SIG, length 5.0770 mm
[diff_pair_uncoupled_length_too_long]: Differential uncoupled length too long (100 ohm diff pair maximum uncoupled length
10.0000 mm; actual 12.6054 mm)

Schematic Editor Improvements

SPICE simulator improvements







Operating point (.op) Display Differential Cursors Power Plotting (e.g. Vin - Vout) New simulations: pole-zero, noise, S-parameter, and FFT



Schematic Editor Improvements

SPICE simulator improvements

Native BOM export tool

		Symbol Fields Table			•
Edit Export					
field delimeter:	1	Output file:			
String delimeter:	•	Preview:			-
leference delimiter:		"Reference","Value","Datasheet","Footprint","Qty" "Cl","luF 10V","","Capacitor SMD:1608 C",""			
ange delimiter:		*C2,C5,C6,C7,C8,C9,C10,C11,C12,C13","0.luF","","Capacitor_SMD: *C3,C4",*10uF 6.3V","","Capacitor SMD:1608 C",""	1608_C", ""		
C Keep tabs		<pre>"C14,C15,C16,C17,C18,C19,C20,C21","0.1uF 100V","","Capacitor_S "C22,C23,C24,C25,C26,C27,C29,C30,C31,C32,C33,C34,C35,C36,C37", "C28","15nF",","Capacitor_SMD:1608_C","" "D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D22,D23","TVS" "D15,D16,D17,D18,D19,D28,D21","USB","","LED SMD:Duo LED 1.6x0.</pre>	"22u+ 10V","","Capacitor_SMD:1608_C" ,"","Diode SMD:1006 C",""	· , · · -	
ormat presets:		D24,D25",5V","","Diode_SMD:1006_C","" "H1","Strap","","MountingHole:Plain Hole 3mm",""	o_Kingbright_APHBI000L20KSOKKC ;		
		<pre>"22", "USB1","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J3", "USB2","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J5", "USB3","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J5", "USB5","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J6", "USB5","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J7", "USB6","", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J7", "USB7",", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J8", "USB7",", "Connector JST:JST SH SM048-SRSS-TB 1x04-1MP P1 "J9", "EXTGND",", "SH Solder Pads:IP-I.5x1.5"," "JP1", "EXTPWR","", "Connector PinHeader 2.54mm:PinHeader 1x02 P "L0G01,L0G02,L0G03,L0G04", "L0g0",", "L0g0"," "R1", '10k","", "Resistor SMD:1608 C","" "R7,R8,R9,R10,R11,R12,R13","470",","Resistor SMD:1608 C","" "U1", "MALLincar XR22417'48",","Package DFN_QFN:TDFN-8_1.5x2mm F "Y1","12MHz 50ppm 16-20pF","","Crystal:Crystal_4-SMD_2.5x2mm","</pre>	.00mm_Horizontal","" .00mm_Horizontal","" .00mm_Horizontal","" .00mm_Horizontal"," .00mm_Horizontal"," .00mm_Horizontal","" 2.54mm_Vertical",""		



Schematic Editor Improvements

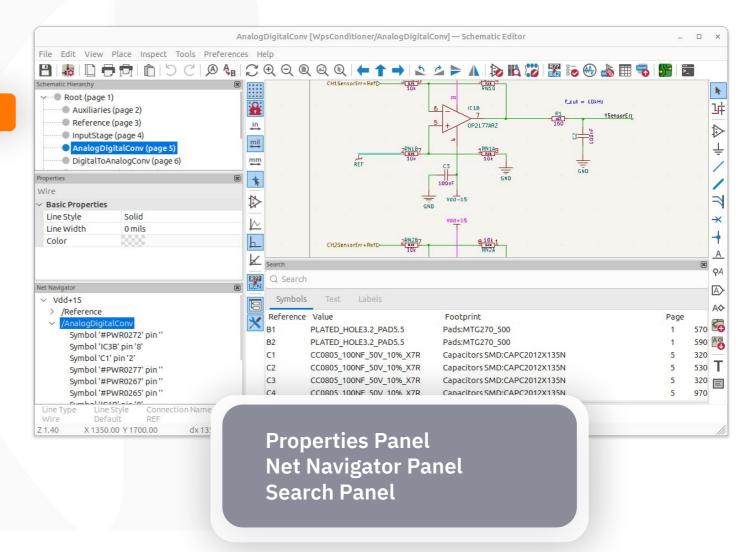
SPICE simulator improvements

Native BOM export tool

New UI panels

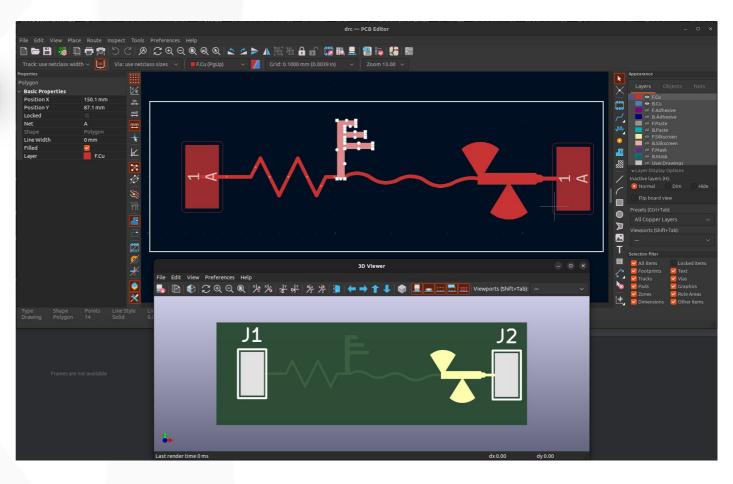
Cad





PCB Editor Improvements

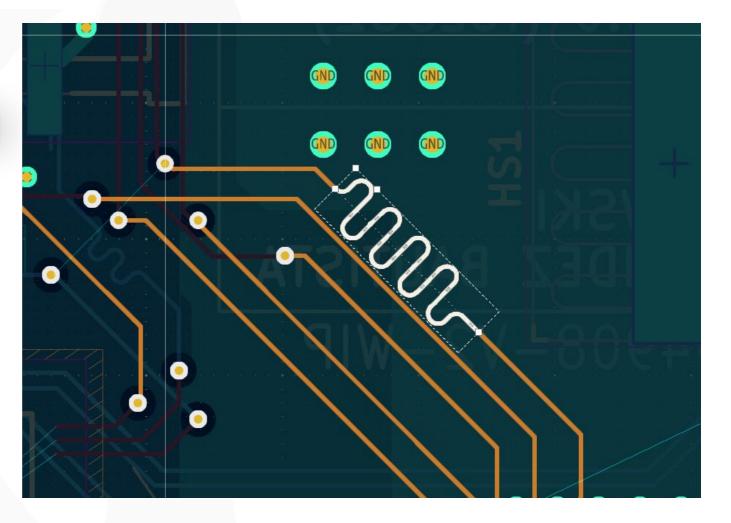
Assign nets to Graphic Shapes





PCB Editor Improvements

Assign nets to Graphic Shapes Interactive editable length tuner







PCB Editor Improvements

Assign nets to Graphic Shapes Interactive editable length tuner IPC-2581 output

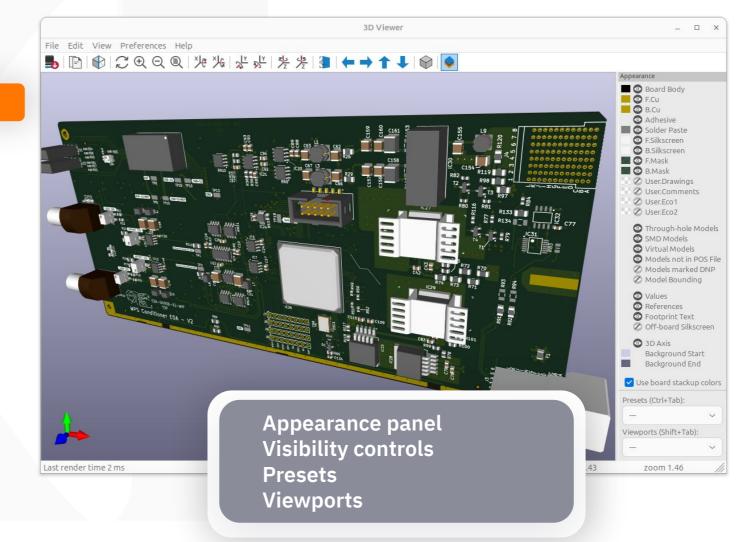


le: ipc2581.xml)
ile Format		BOM Columns	
Units:	Millimeters ~	Internal ID:	Generat <mark>e</mark> Unique ~
Precision:	3 - +	Manufacturer P/N:	Manufacturer ~
Version:	C ~	Manufacturer: Distributor P/N:	Manufacturer ~ Omit ~
Compress out	put	Distributor:	N/A

PCB Editor Improvements

Assign nets to Graphic Shapes Interactive editable length tuner IPC-2581 output

3D viewer





Completed Improvements

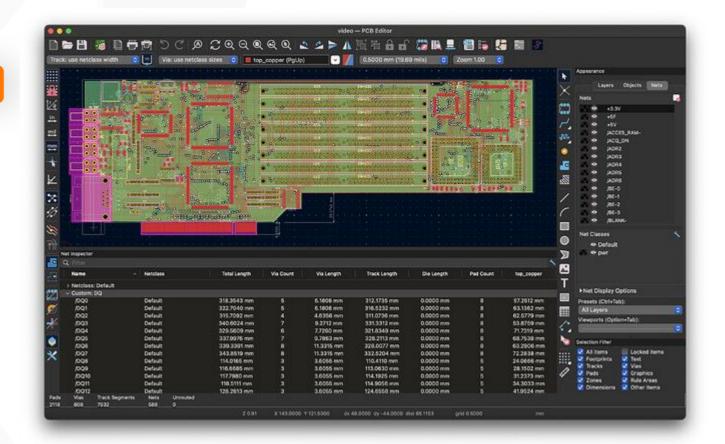
Zone Manager

			Zon	e Manager				×
Name Net Layers	layer Jayer m_layer m_layer Met Q search Electrical Properties Clearance: 0.3 mm Minimum width: 0.25 mm Hatched ∨ Hatched ∨ Hatch gap: 1.5 mm							
GND GND	layer							
+3.3V VDD_	layer							
GND Botto	om_layer							
↑↓ <mark>v</mark> Name Properties	<mark>☑ Net</mark> Q Search							
General			Electrical Properties			Fill		
Zone name:			Clearance:	0.3	mm	Fill type:	Solid fill 🛛 🗸	
Shape			Minimum width:	0.25	mm	Orientation:		
Locked			Dad connections:	Thormal collefe		Hatch width:		mm
Outline display:	Hatched 🗸 🗸		Pad connections:	Thermat reliers V		Hatch gap:	1.5	mm
	(Thermal relief gap:	0.381	mm			
Outline hatch pitch:	0.508	mm	Thermal spoke width:	0.381	mm	Smoothing effort:		
Corner smoothing:	None ~					Smoothing amount:	0.10 - +	
Fillet radius:		mm				Remove islands:	Always ~	
						Minimum island size:		
Repour						Apply	Cancel	<u>о</u> к

Completed Improvements

Zone Manager

Net Inspector docked panel

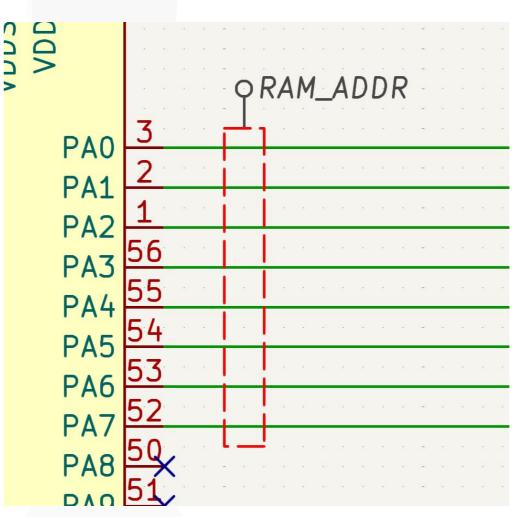


Completed Improvements

Zone Manager

Net Inspector docked panel

Schematic Rule Areas (Blankets)



Completed Improvements

Zone Manager

Net Inspector docked panel

Schematic Rule Areas (Blankets)

Native table support

Header 1	Header 2	Header 3	Header 4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4
			NE STATE AND A DESCRIPTION

-	er at at ba	ta da da tar	the de set the	an at be an at Straine and
	Header 1	Header 2 -	Header 3	Header 4
	cell1	cell2	cell3	cell4
	cell1	cell2	cell3	cell4
	cell1	cell2	cell3	cell4

Completed Improvements

Zone Manager

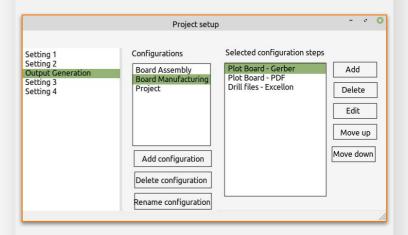
Net Inspector docked panel

Schematic Rule Areas (Blankets)

Native table support

Embedded files (e.g. 3D models)

Planned features



GUI Output Jobs

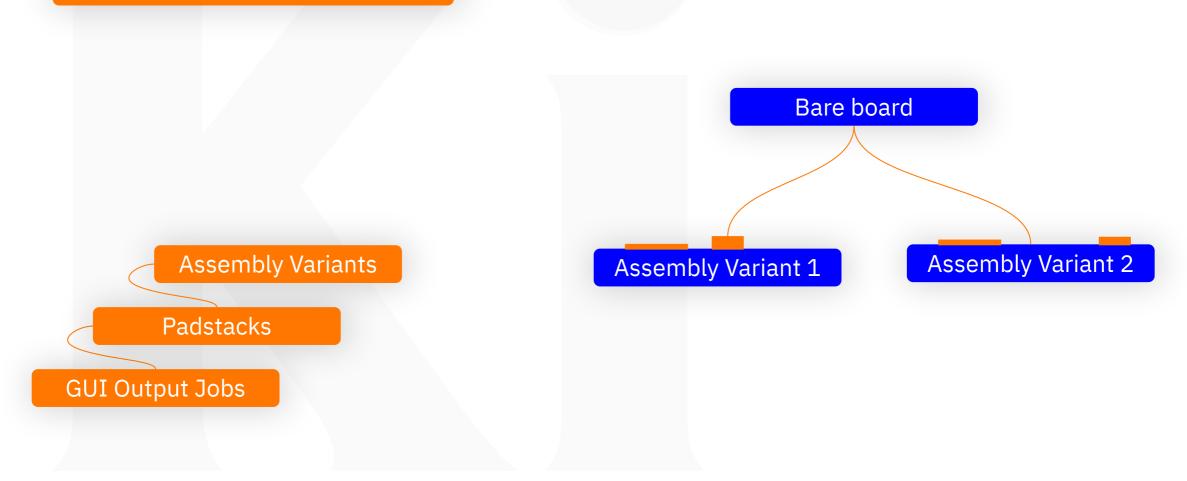
Planned features

Padstacks

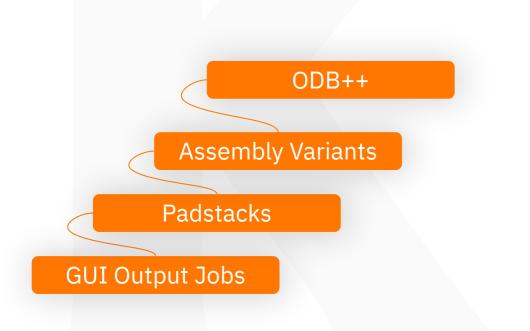
GUI Output Jobs

Tented/Untented Vias V Import from other tools

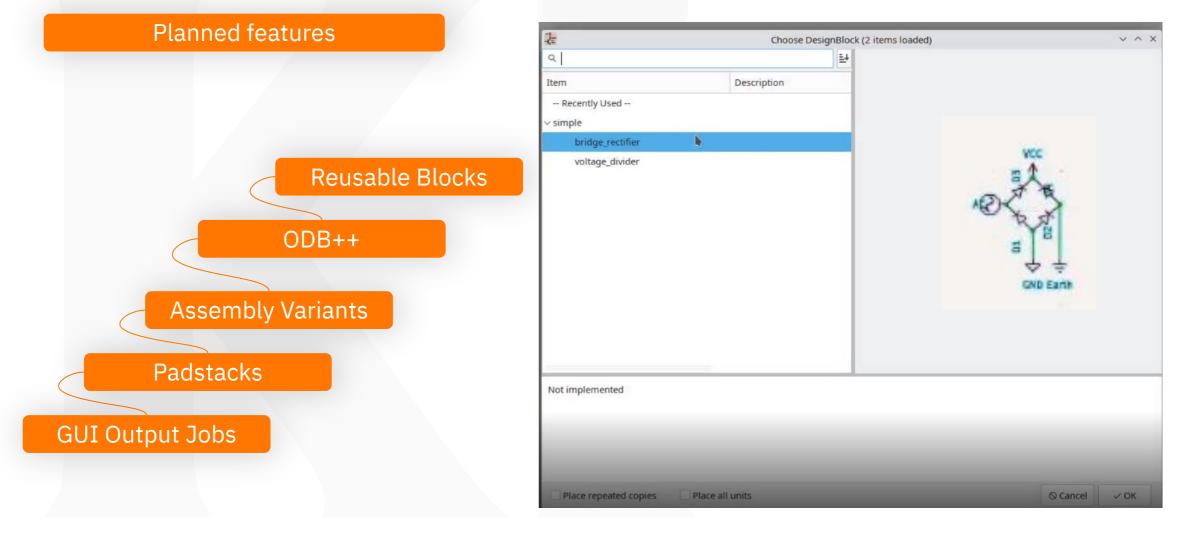
Planned features



Planned features







Want to know more?

KiCad v8 release blog post:

https://www.kicad.org/blog/2024/02/Version-8.0.0-Released/

Upcoming KiCad v9 features forum post:

https://forum.kicad.info/t/post-v8-new-features-and-development-news/48614



Questions?