



# KiCad Status 2024

## Version 8 and beyond



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14/06/2024

## CERN electronics forum



# Version 8

## Common Improvements

Properties Panel in all editors

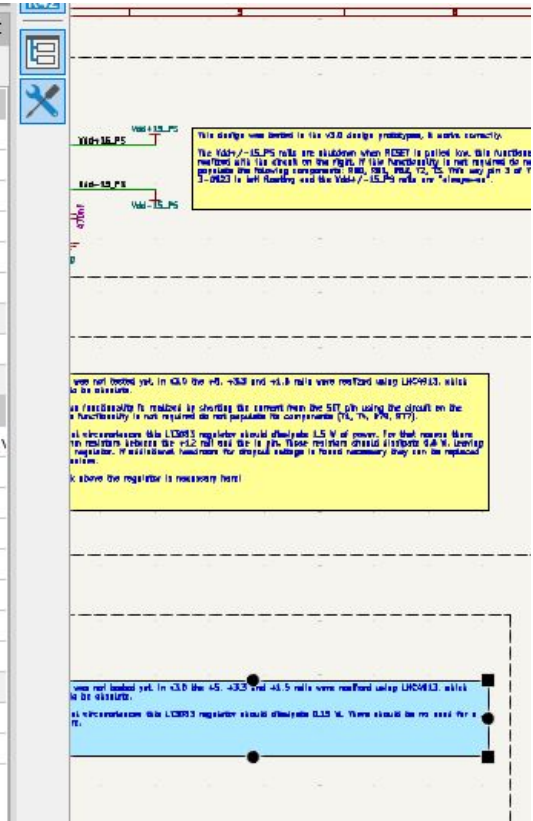


Properties Panel for a Text Box:

Basic Properties	
Start X	7250 mils
Start Y	6543 mils
End X	11550 mils
End Y	7243 mils
Line Width	0 mils
Line Style	Solid
Line Color	Black
Filled	<input checked="" type="checkbox"/>
Fill Color	Yellow

Text Properties	
Text	This design was not tested yet. In v...
Font	Default Font
Italic	<input type="checkbox"/>
Bold	<input type="checkbox"/>
Mirrored	<input type="checkbox"/>
Visible	<input checked="" type="checkbox"/>
Horizontal Justification	Left
Vertical Justification	Top
Color	Checkerboard
Hyperlink	
Text Size	50 mils



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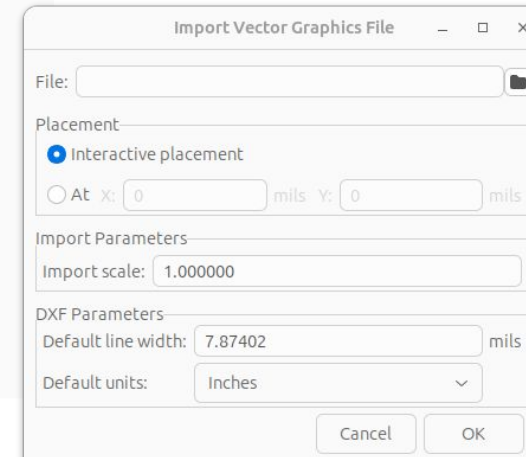
Import from third party tools



	Project	Schematic	PCB	Symbols	Footprints
Altium Designer		●	●	●	●
Altium Circuit Maker		●	●	●	●
Altium Circuit Studio		●	●	●	●
CADSTAR	●	●	●	●	●
EAGLE	●	●	●	●	●
EasyEDA / JLCEDA Std	●	●	●	●	●
EasyEDA / JLCEDA Pro	●	●	●	●	●
Fabmaster	N/A	N/A	●	N/A	N/A
gEDA					●
LTspice	N/A	●	N/A		N/A
P-CAD			●		
Solidworks PCB		●	●	●	●

Key: ● Supported in KiCad 7.0 ● Supported in KiCad 8.0

+ Import vector graphics (**DXF and SVG**) to Schematic + Symbol editors



# Version 8

```
kicad-cli pcb drc  
kicad-cli sch erc  
kicad-cli sch bom
```

## Common Improvements

Properties Panel in all editors

Import from third party tools

Command line drc, erc and native bom

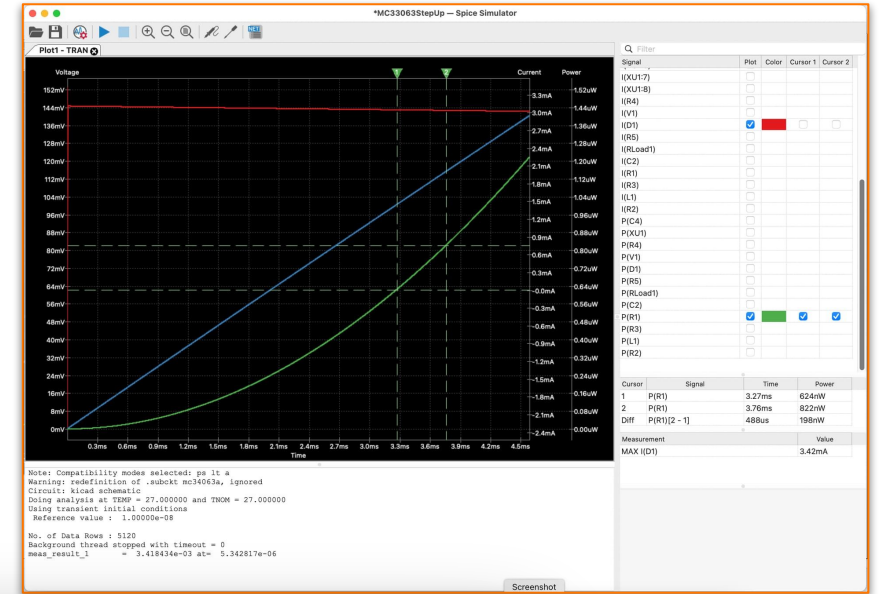
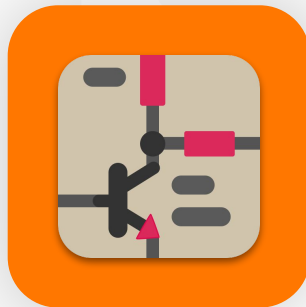
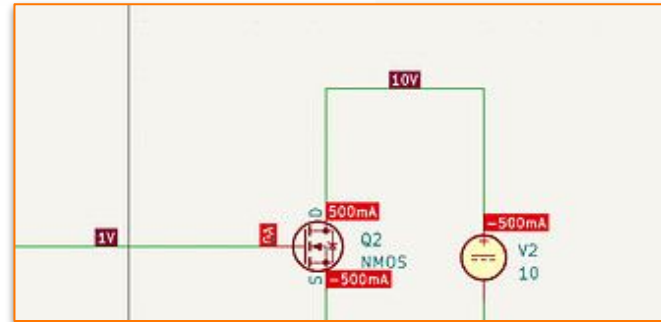


```
user@pc:~$ kicad-cli pcb drc myboard.kicad_pcb  
Loading board  
Running DRC...  
Found 497 violations  
Found 200 unconnected items  
Saved DRC Report to myboard.rpt  
user@pc:~$ cat myboard.rpt  
** Drc report for myboard.kicad_pcb **  
** Created on 2024-06-09T18:22:01+0200 **  
  
** Found 497 DRC violations **  
[diff_pair_gap_out_of_range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.6188 mm)  
Rule: 100 ohm diff pair; error  
@(161.8215 mm, 95.9016 mm): Track [/FPGAControler/SPI_SCLK_P] on L4_SIG, length 0.6443 mm  
@(162.3504 mm, 96.4656 mm): Track [/FPGAControler/SPI_SCLK_N] on L4_SIG, length 1.2558 mm  
[diff_pair_uncoupled_length_too_long]: Differential uncoupled length too long (100 ohm diff pair maximum uncoupled length 10.0000 mm; actual 10.8907 mm)  
Rule: 100 ohm diff pair; error  
@(161.3660 mm, 96.3572 mm): Track [/FPGAControler/SPI_SCLK_P] on F.Cu, length 0.7021 mm  
@(161.3624 mm, 97.3536 mm): Track [/FPGAControler/SPI_SCLK_N] on F.Cu, length 0.7071 mm  
[diff_pair_gap_out_of_range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.6188 mm)  
Rule: 100 ohm diff pair; error  
@(161.8215 mm, 95.9016 mm): Track [/FPGAControler/SPI_SCLK_P] on L4_SIG, length 0.6443 mm  
@(162.3504 mm, 96.4656 mm): Track [/FPGAControler/SPI_SCLK_N] on L4_SIG, length 1.2558 mm  
[diff_pair_gap_out_of_range]: Differential pair gap out of range (100 ohm diff pair maximum gap 0.4500 mm; actual 0.4769 mm)  
Rule: 100 ohm diff pair; error  
@(184.1112 mm, 94.3424 mm): Track [/FPGAControler/SPI_CS_P] on L4_SIG, length 5.0770 mm  
@(183.7836 mm, 94.9048 mm): Track [/FPGAControler/SPI_CS_N] on L4_SIG, length 5.0770 mm  
[diff_pair_uncoupled_length_too_long]: Differential uncoupled length too long (100 ohm diff pair maximum uncoupled length 10.0000 mm; actual 12.6054 mm)
```

# Version 8

## Schematic Editor Improvements

SPICE simulator improvements



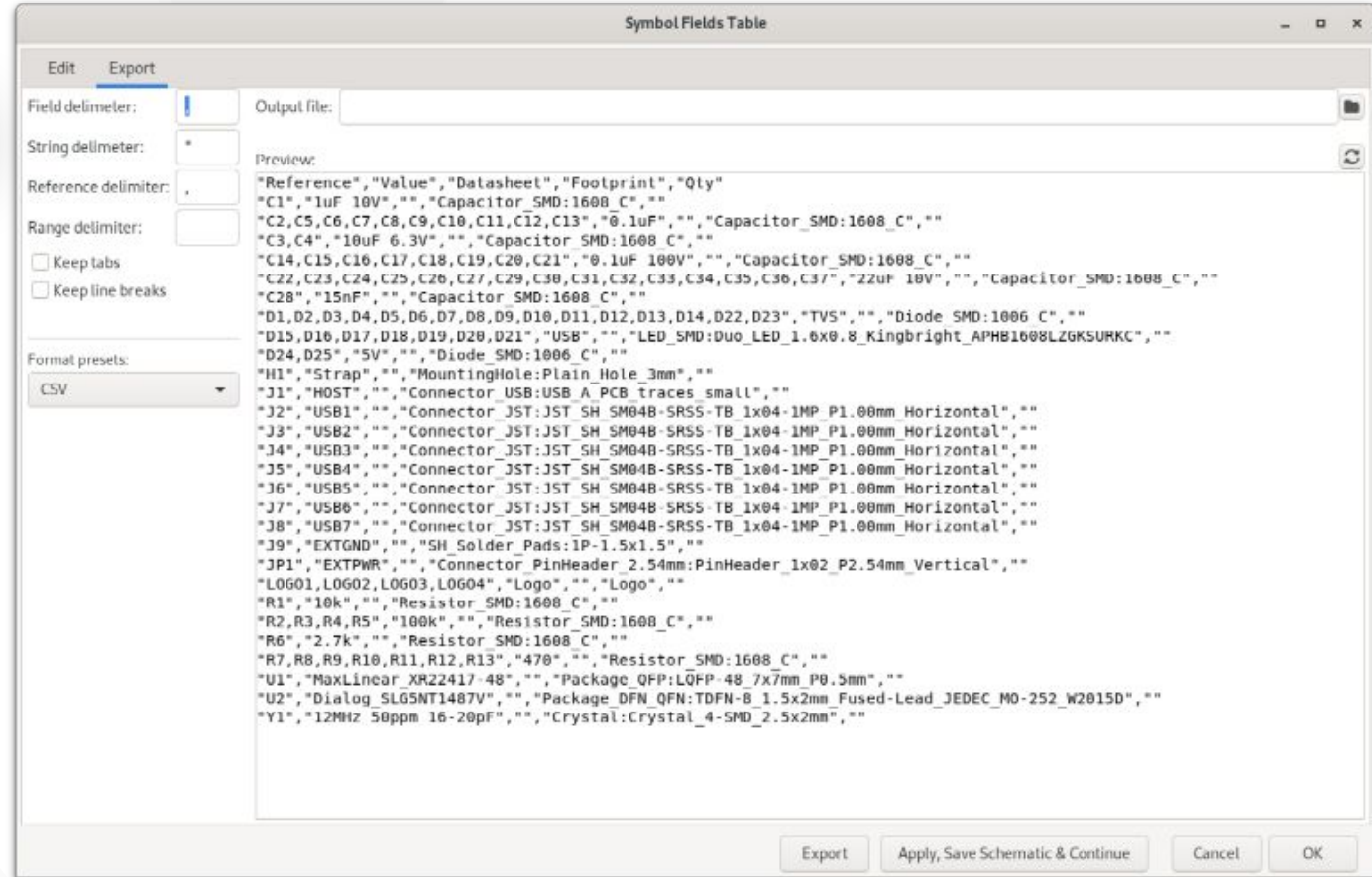
Operating point (.op) Display  
Differential Cursors  
Power Plotting (e.g.  $V_{in} - V_{out}$ )  
New simulations: pole-zero,  
noise, S-parameter, and FFT

# Version 8

## Schematic Editor Improvements

SPICE simulator improvements

Native BOM export tool





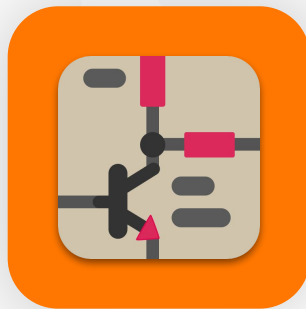
# Version 8

## Schematic Editor Improvements

SPICE simulator improvements

Native BOM export tool

New UI panels



The screenshot displays the KiCad Schematic Editor interface for a project named 'AnalogDigitalConv'. The main workspace shows a circuit diagram with an operational amplifier (OP2177ARZ) and various passive components like resistors and capacitors. The interface includes several panels:

- Schematic Hierarchy:** A tree view showing the project structure with 'AnalogDigitalConv (page 5)' selected.
- Properties:** A panel showing wire properties such as Line Style (Solid), Line Width (0 mils), and Color.
- Net Navigator:** A tree view showing the project's netlist structure, with 'AnalogDigitalConv' selected under the 'Vdd+15' net.
- Search:** A panel with a search bar and a table of search results.

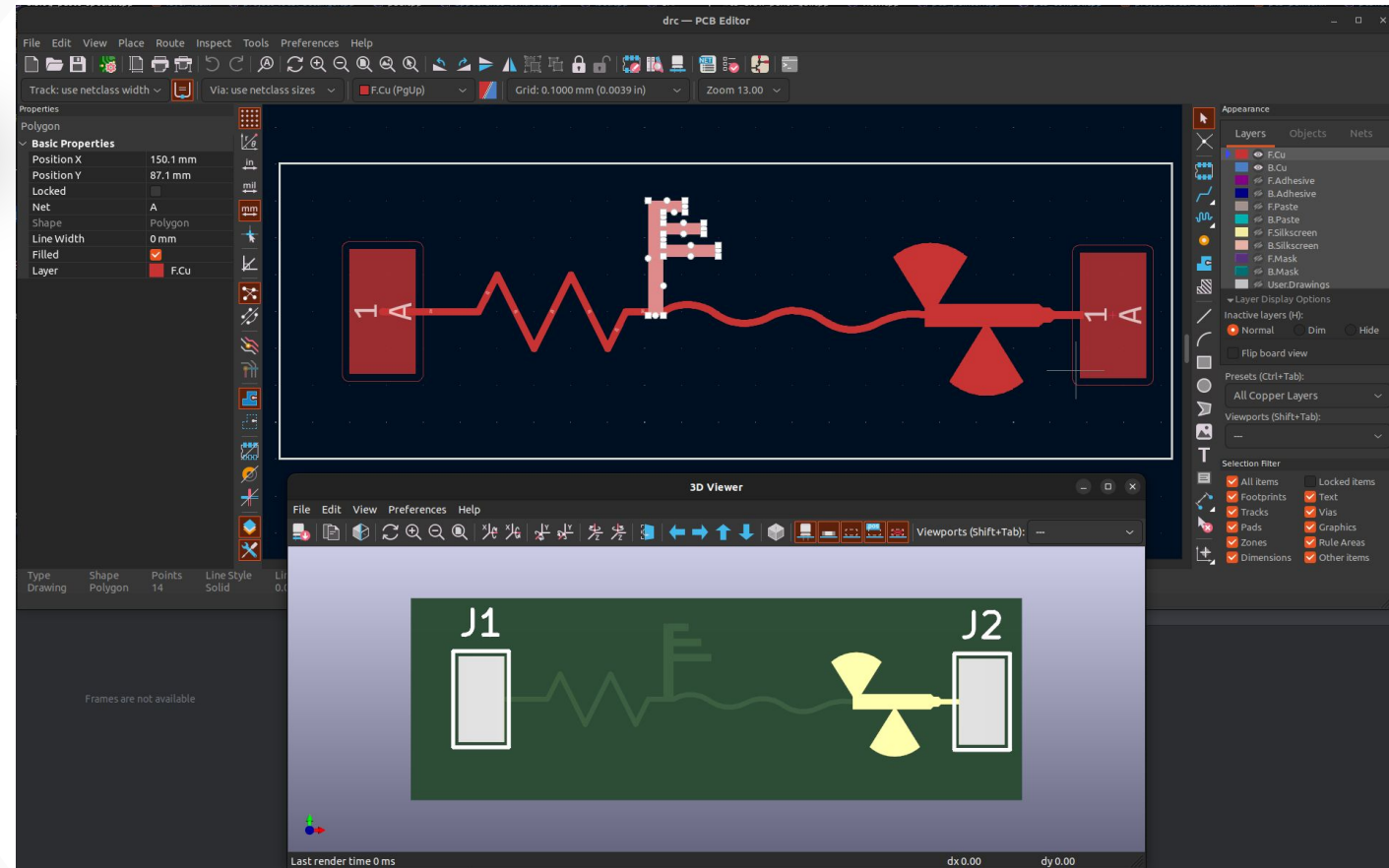
Reference	Value	Footprint	Page
B1	PLATED_HOLE3.2_PAD5.5	Pads:MTG270_500	1 570
B2	PLATED_HOLE3.2_PAD5.5	Pads:MTG270_500	1 590
C1	CC0805_100NF_50V_10%_X7R	Capacitors SMD:CAPC2012X135N	5 320
C2	CC0805_100NF_50V_10%_X7R	Capacitors SMD:CAPC2012X135N	5 530
C3	CC0805_100NF_50V_10%_X7R	Capacitors SMD:CAPC2012X135N	5 320
C4	CC0805_100NF_50V_10%_X7R	Capacitors SMD:CAPC2012X135N	5 970

Properties Panel  
Net Navigator Panel  
Search Panel

# Version 8

## PCB Editor Improvements

Assign nets to Graphic Shapes



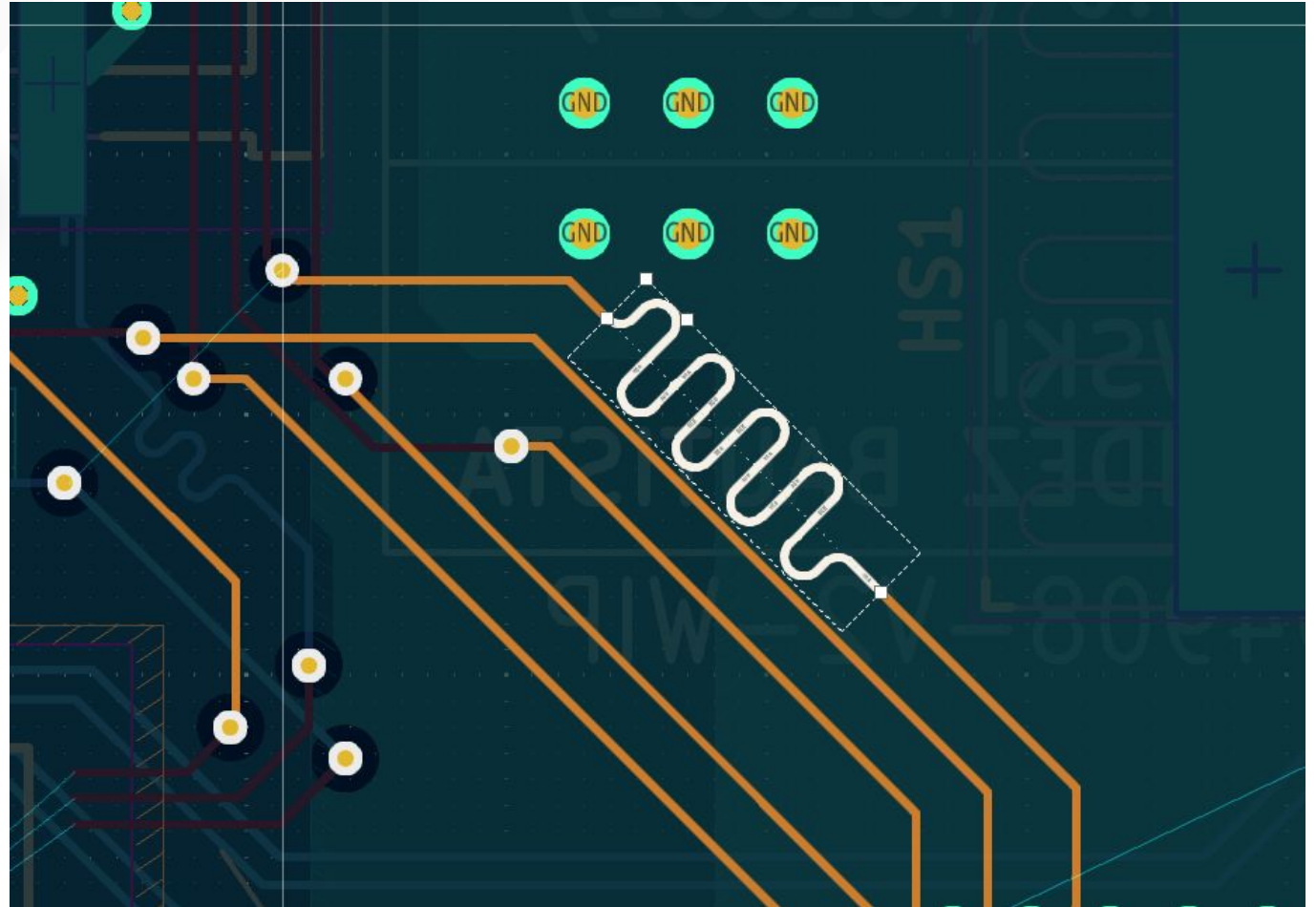
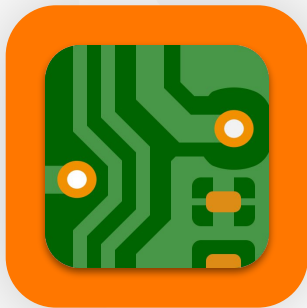


# Version 8

## PCB Editor Improvements

Assign nets to Graphic Shapes

Interactive editable length tuner



# Version 8

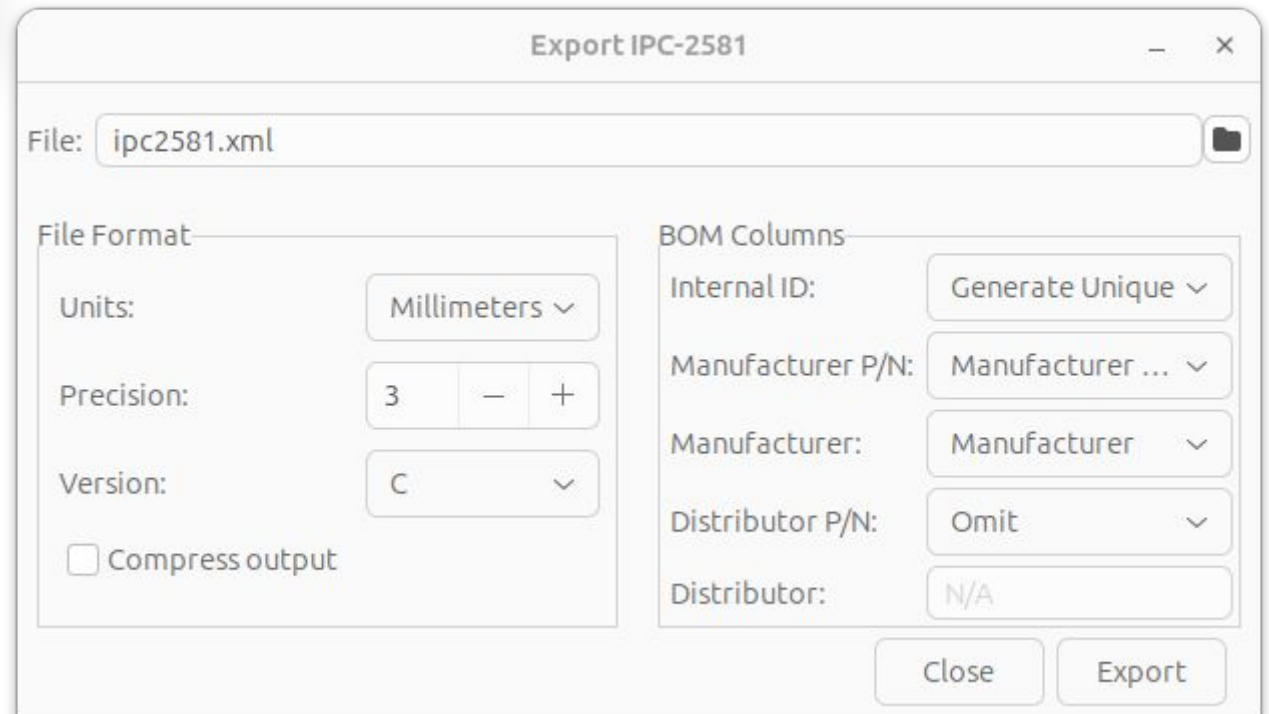


## PCB Editor Improvements

Assign nets to Graphic Shapes

Interactive editable length tuner

IPC-2581 output



# Version 8

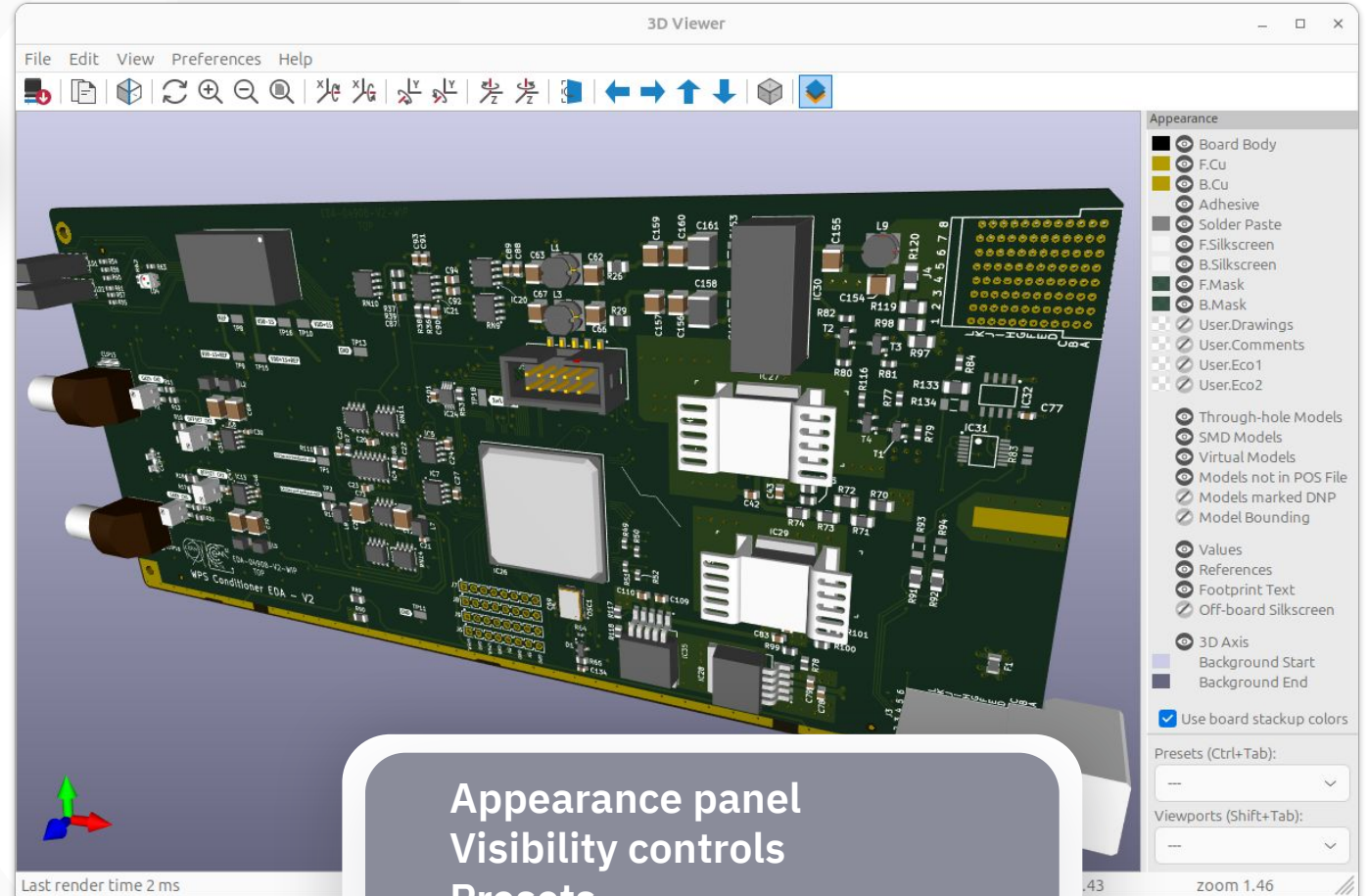
## PCB Editor Improvements

Assign nets to Graphic Shapes

Interactive editable length tuner

IPC-2581 output

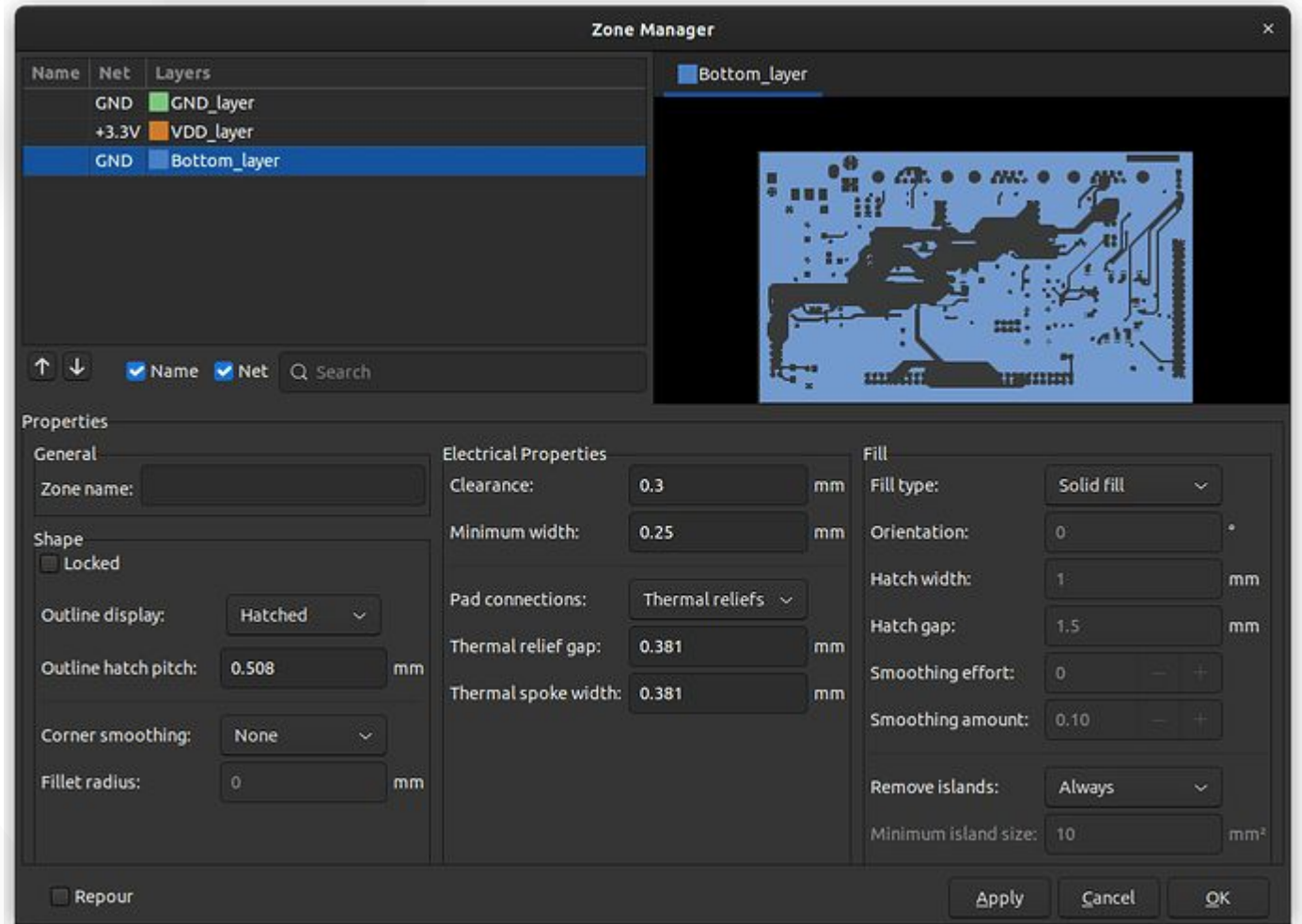
3D viewer



# Upcoming Version 9 (Jan 2025)

## Completed Improvements

Zone Manager



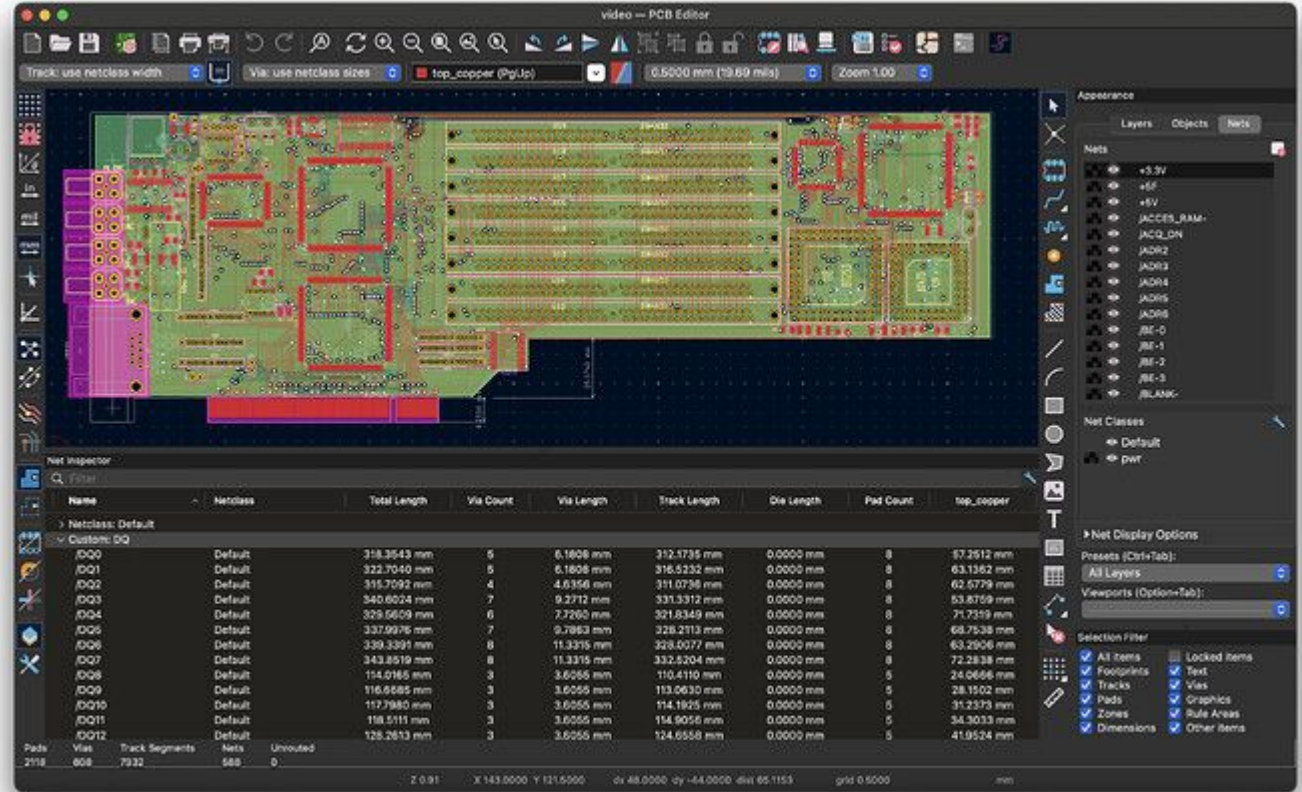


# Upcoming Version 9 (Jan 2025)

## Completed Improvements

Zone Manager

Net Inspector docked panel



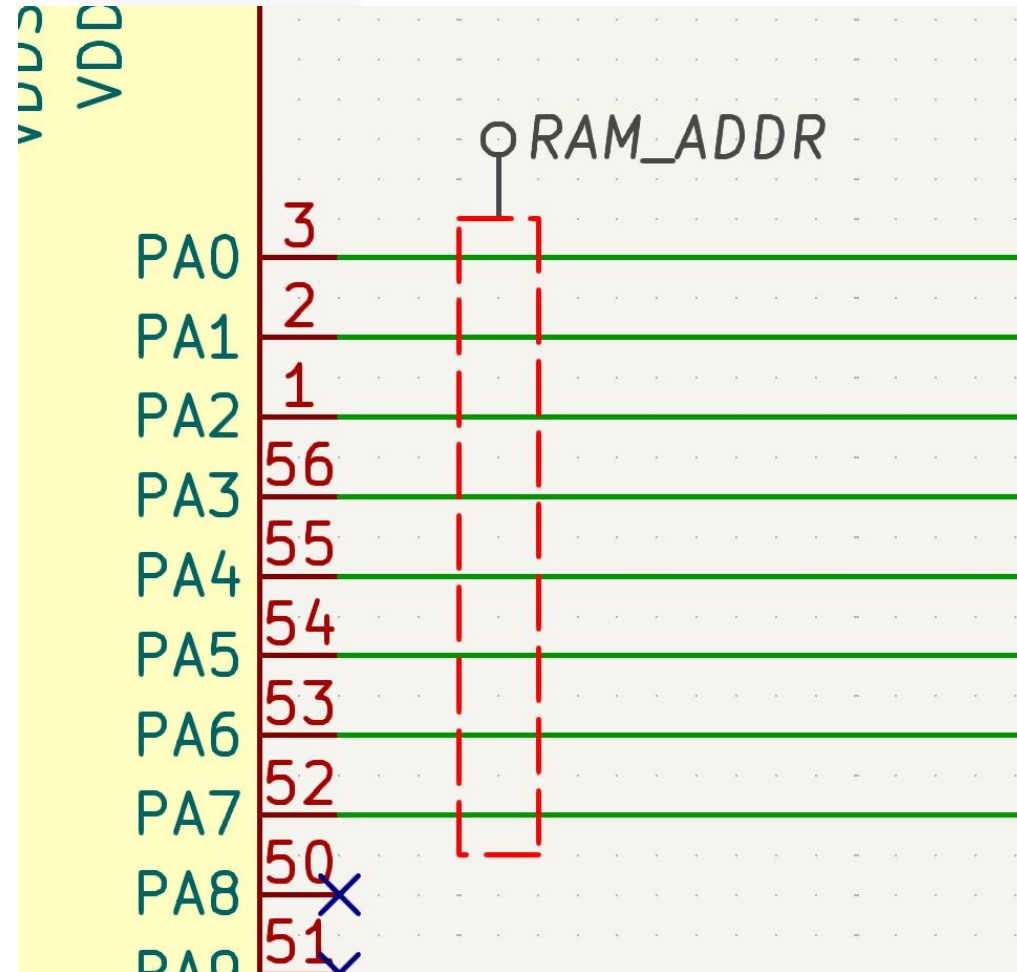
# Upcoming Version 9 (Jan 2025)

## Completed Improvements

Zone Manager

Net Inspector docked panel

Schematic Rule Areas (Blankets)





# Upcoming Version 9 (Jan 2025)

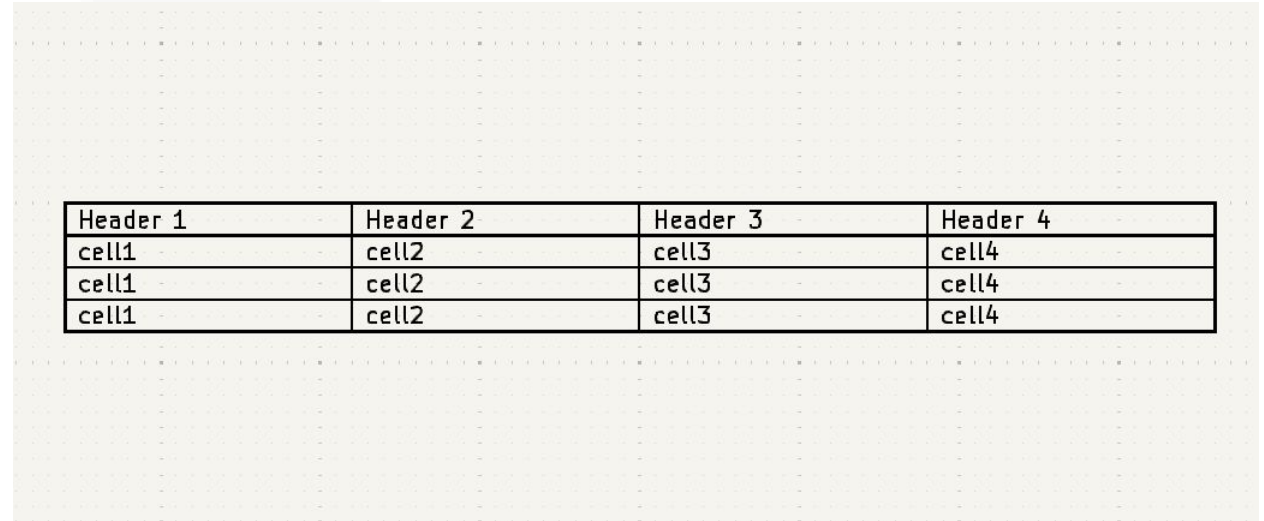
## Completed Improvements

Zone Manager

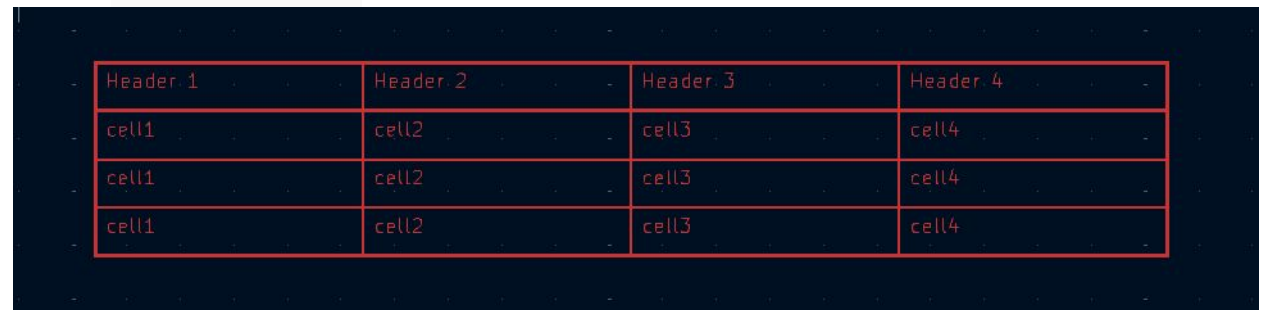
Net Inspector docked panel

Schematic Rule Areas (Blankets)

Native table support



Header 1	Header 2	Header 3	Header 4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4



Header 1	Header 2	Header 3	Header 4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4
cell1	cell2	cell3	cell4

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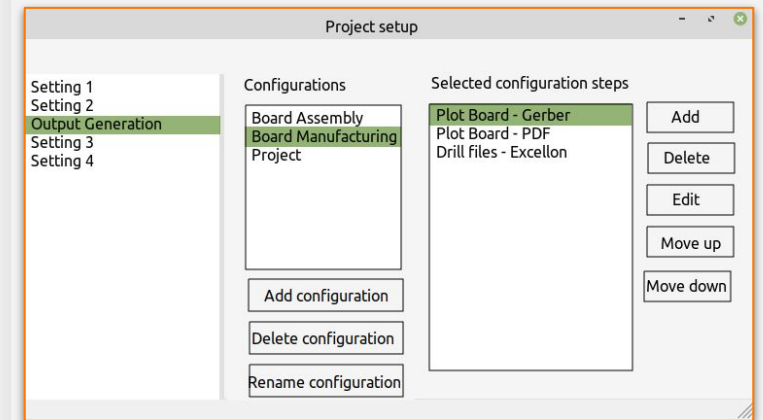
Native table support

Embedded files (e.g. 3D models)

# Upcoming Version 9 (Jan 2025)

Planned features

GUI Output Jobs

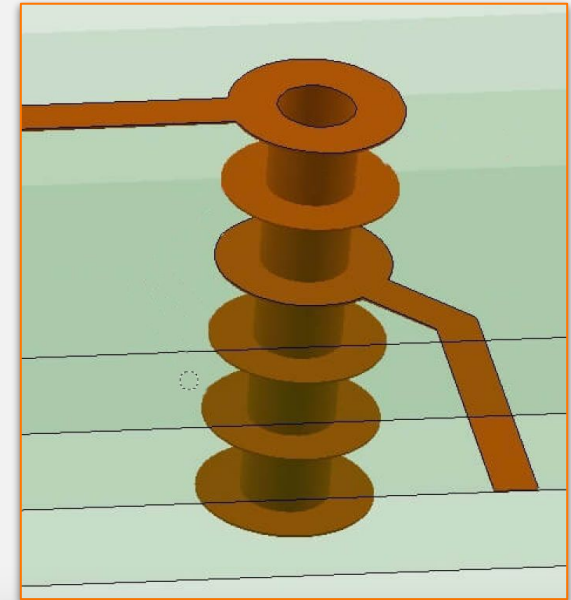


# Upcoming Version 9 (Jan 2025)

Planned features

Padstacks

GUI Output Jobs



Tented/Untented Vias   
Import from other tools

# Upcoming Version 9 (Jan 2025)

Planned features

Assembly Variants

Padstacks

GUI Output Jobs

Bare board

Assembly Variant 1

Assembly Variant 2

# Upcoming Version 9 (Jan 2025)

Planned features

ODB++

Assembly Variants

Padstacks

GUI Output Jobs





# Upcoming Version 9 (Jan 2025)

## Planned features

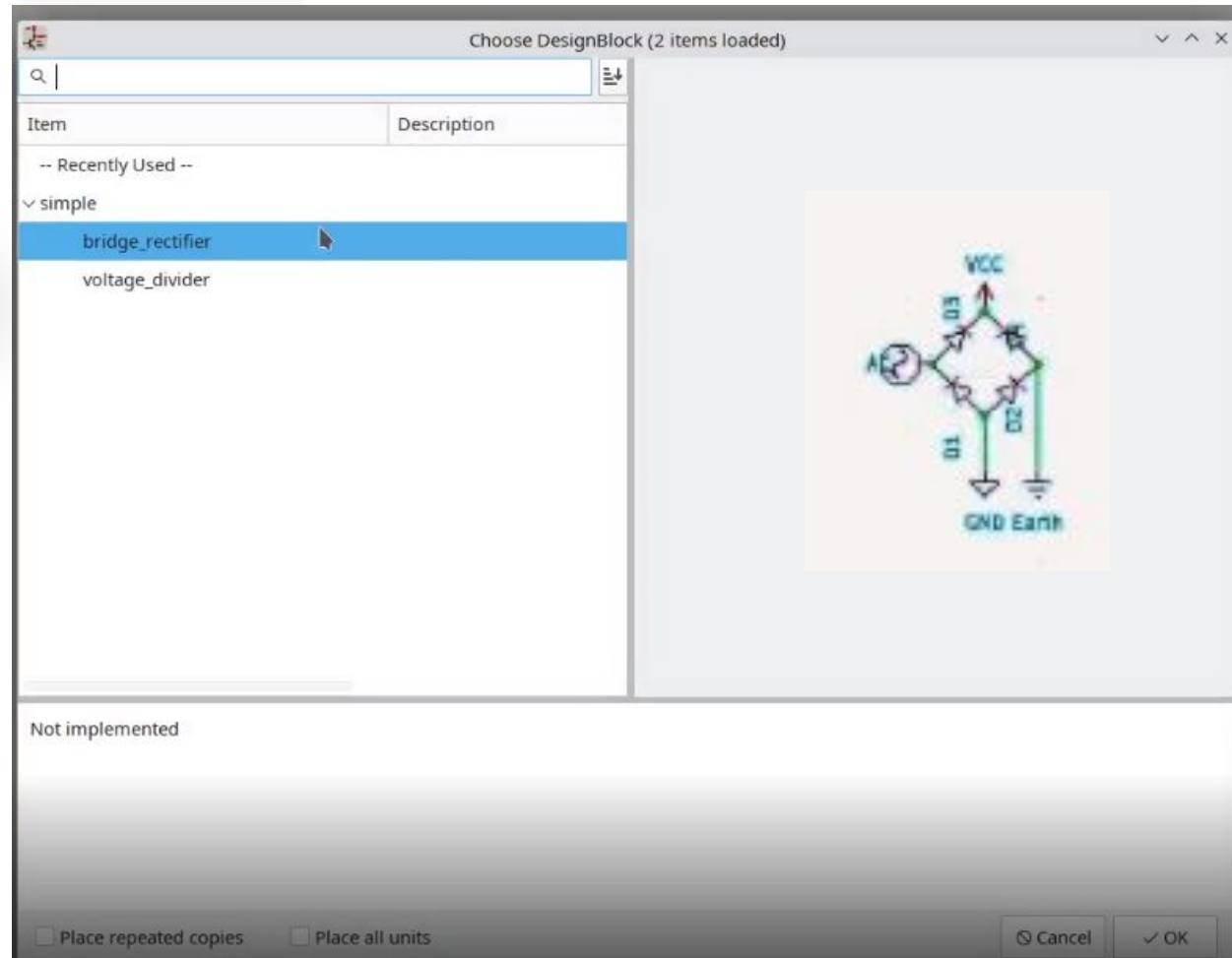
Reusable Blocks

ODB++

Assembly Variants

Padstacks

GUI Output Jobs



# Want to know more?

KiCad v8 release blog post:

<https://www.kicad.org/blog/2024/02/Version-8.0.0-Released/>

Upcoming KiCad v9 features forum post:

<https://forum.kicad.info/t/post-v8-new-features-and-development-news/48614>

# Questions?

