

Status overview of Korean group activities for MTD ETL



Dong Ho Moon

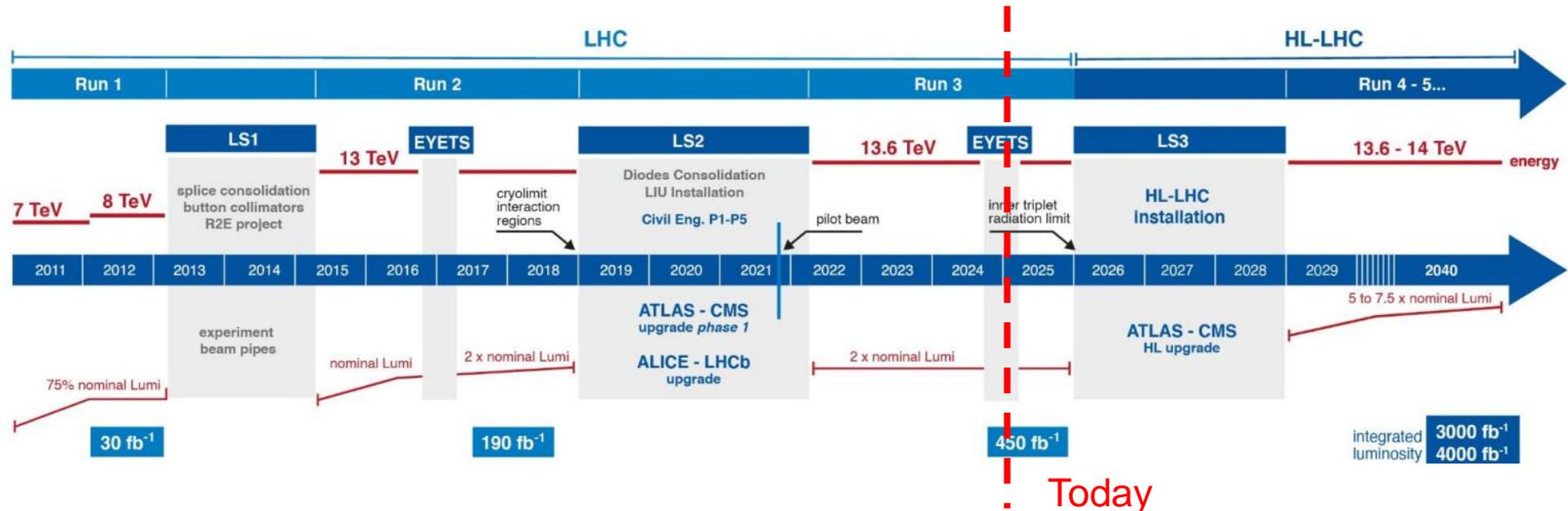
On behalf of CMS collaboration

Chonnam National University

2025/01/15 ATHIC 2025 @ Odisha, India

High Luminosity LHC Era is coming

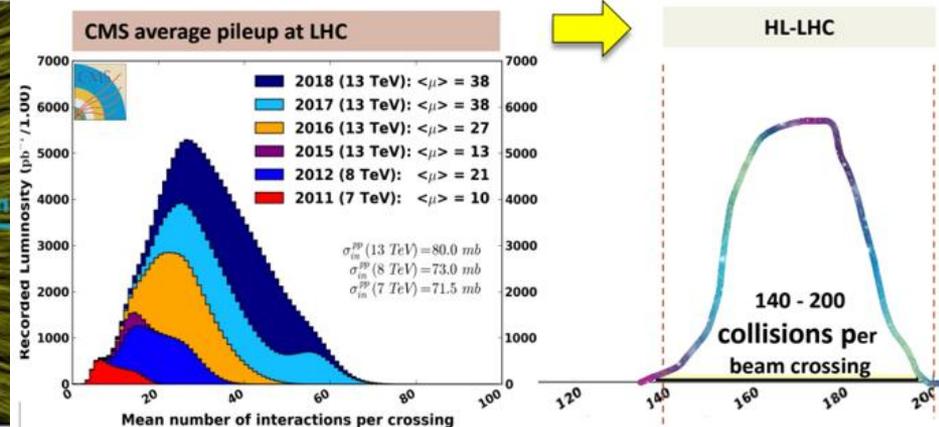
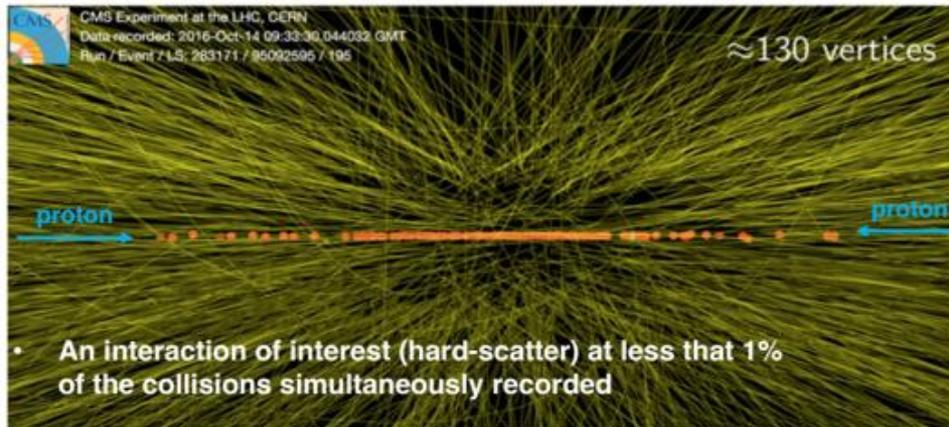
- LHC beam optics and injectors are upgrade to increase the intensity
 - Purpose to increase the LHC performance to maximize the potential for new discoveries after 2029
 - The luminosity will increase from $1.7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ up to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
 - Current collected data (2009-2025) : $\sim 400 \text{ fb}^{-1}$
 - Target luminosity (2029-2042) : $> 3000 \text{ fb}^{-1}$ (1 year data equivalent to ~ 10 years of collected data)



High Luminosity LHC Era is coming

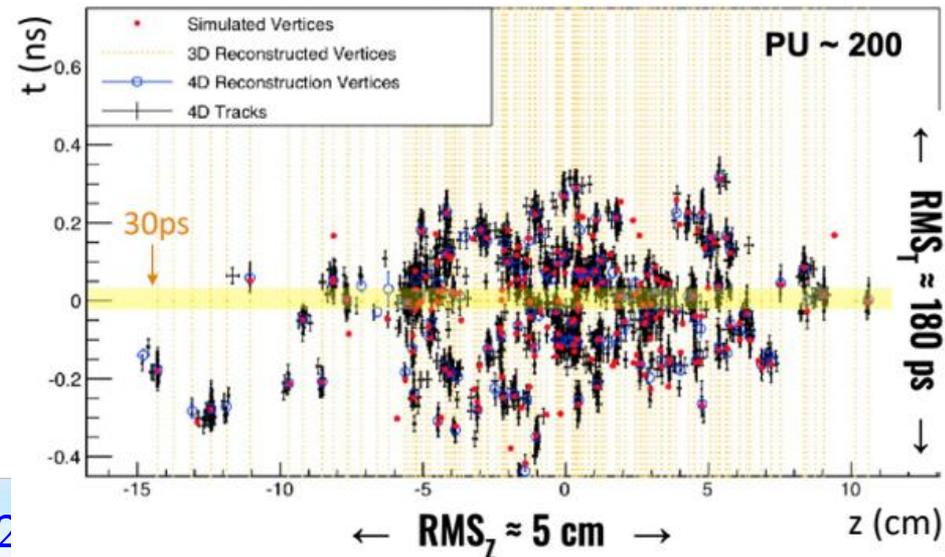
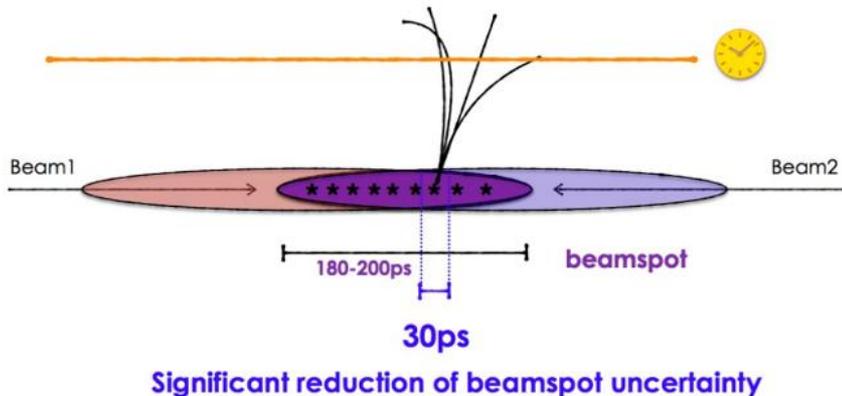
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- About 400 collisions/beam crossing (expect a lot of pileup events)
 - ~ 130 vertices in one bunch collisions
 - Need to weed out the experimental observables in pileup events

Real life event at the LHC emulating HL-LHC conditions



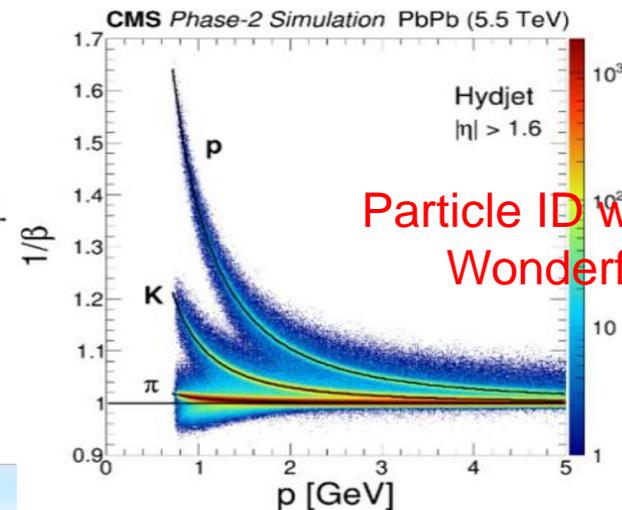
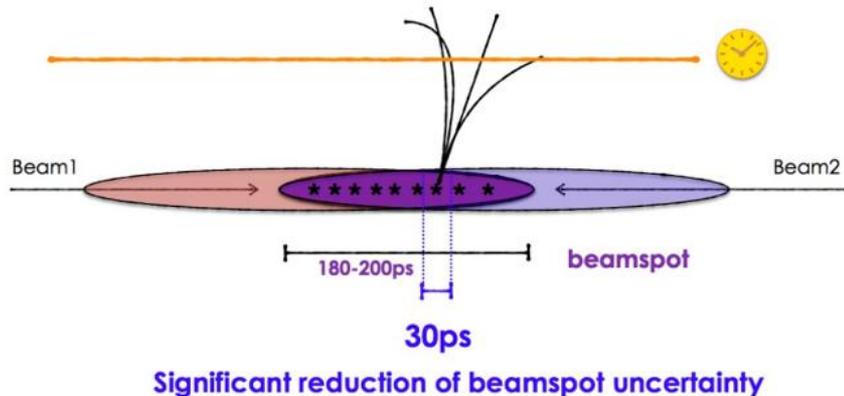
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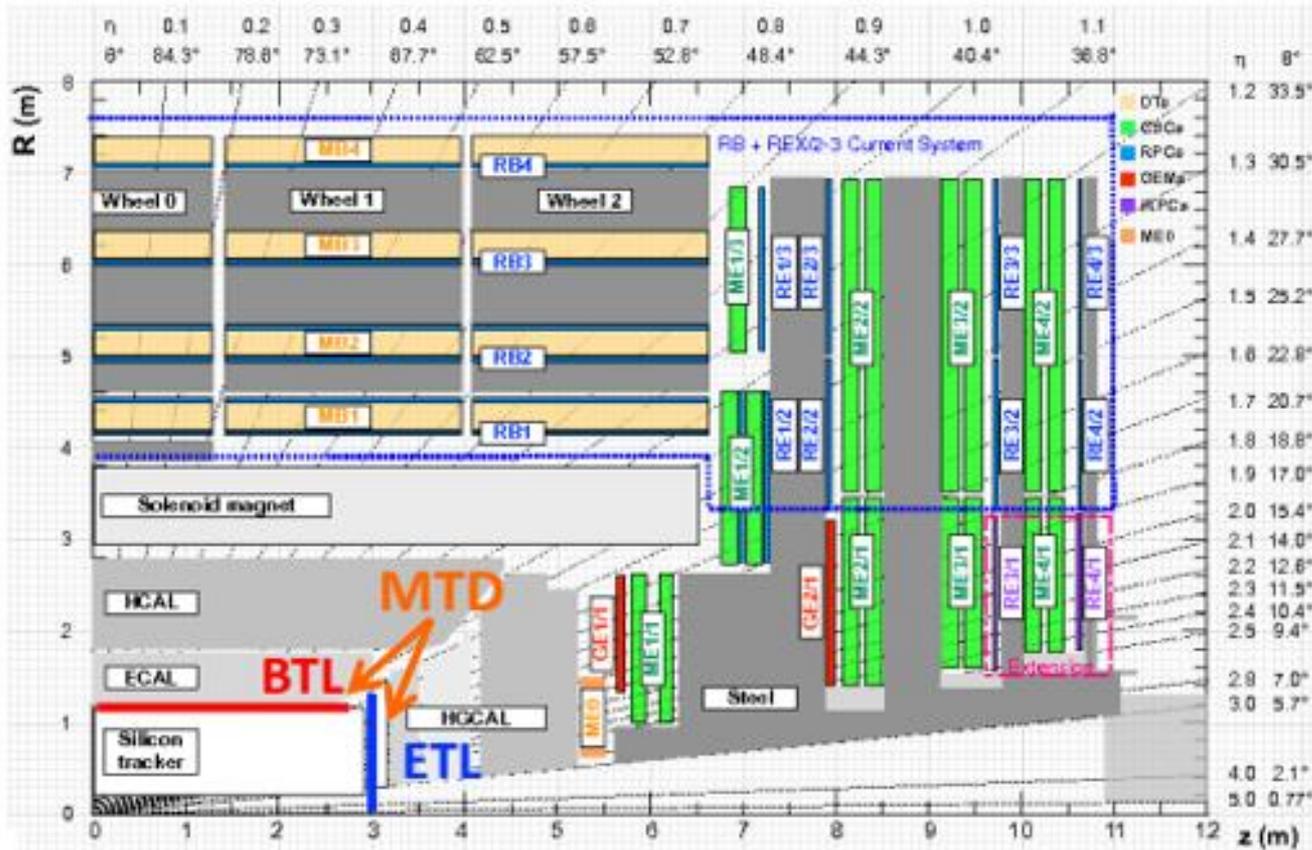
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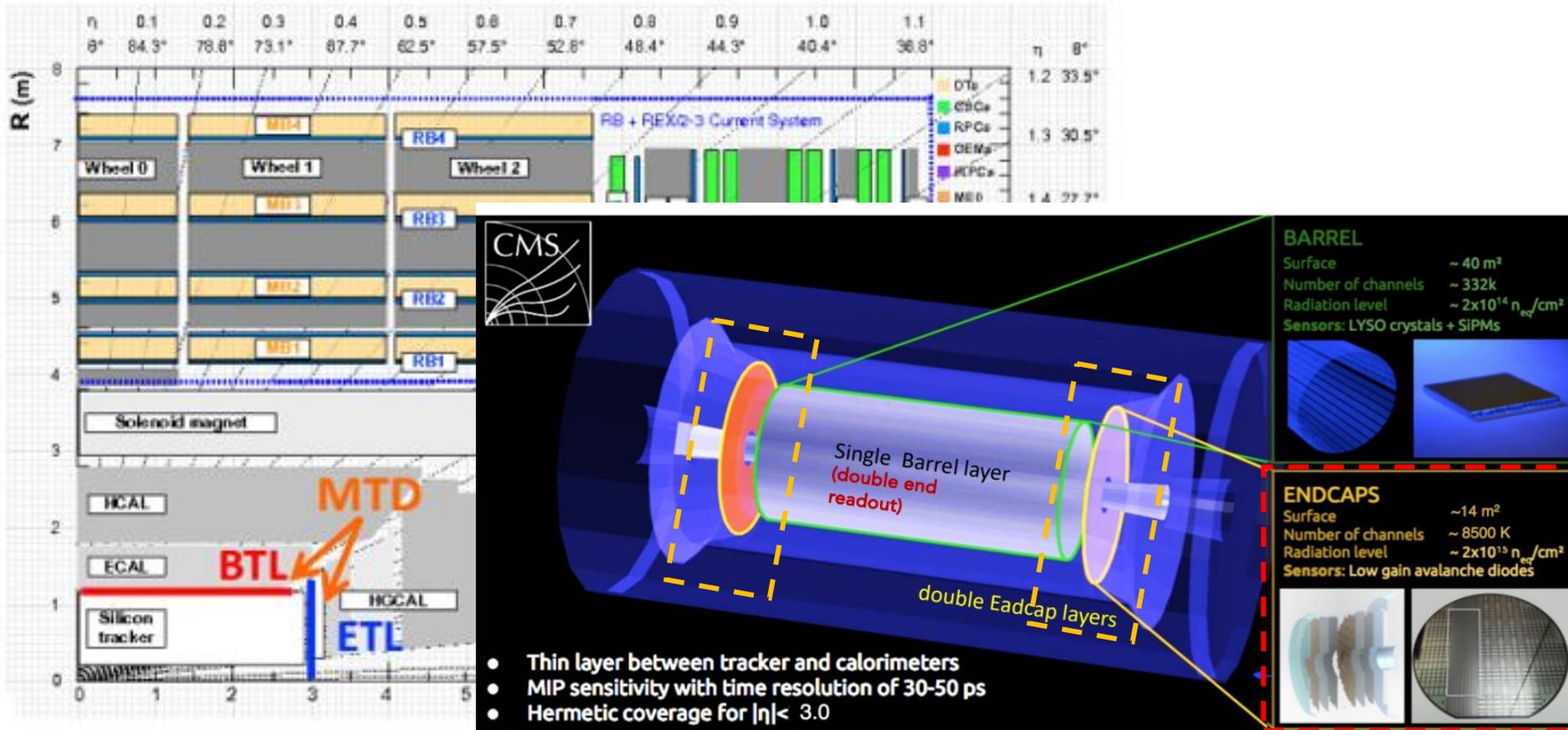
Particle ID will be possible !!!
Wonderful advantage for
Heavy ion crew

Mip Timing Detector (MTD)



- MTD will be installed at the space between tracker and calorimeter.
- Barrel Timing Layer (BTL) : LYSO crystal + SiPM
- Endcap Timing Layer (ETL) : LGAD sensor + ASIC (ETROC)

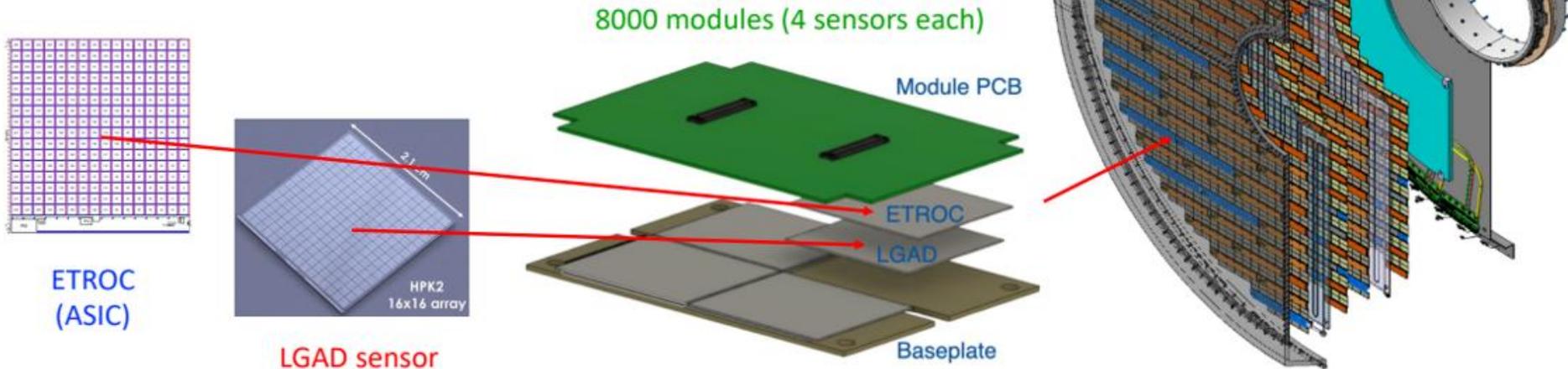
Mip Timing Detector (MTD)



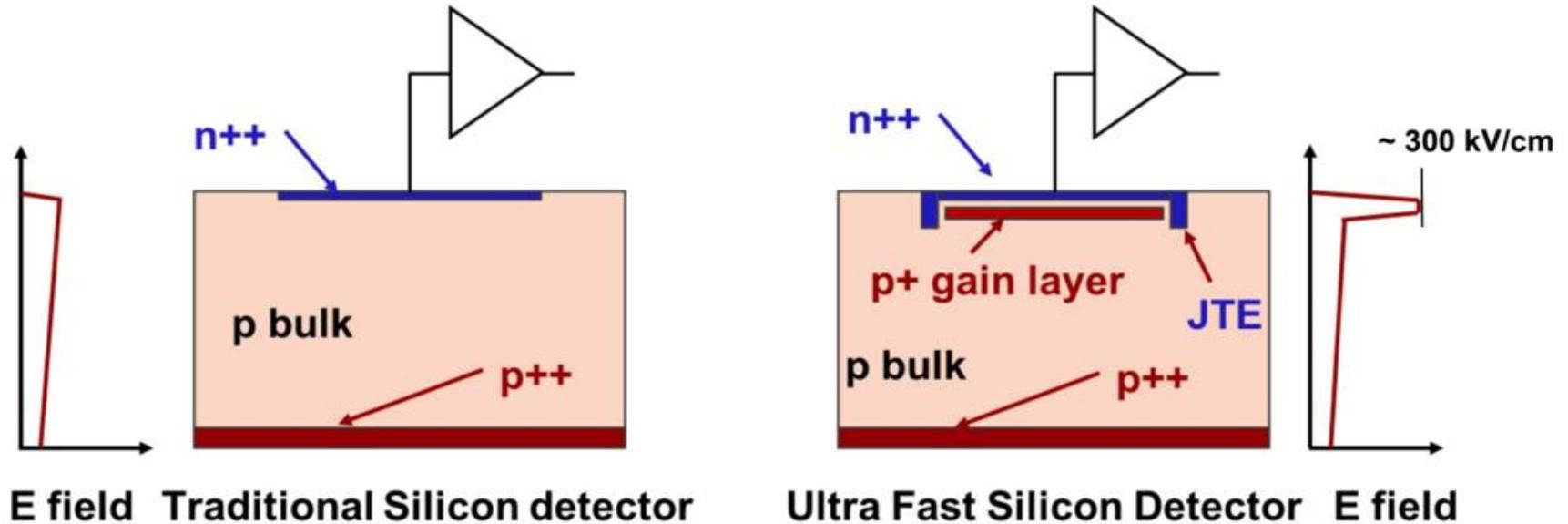
- MTD will be installed at the space between tracker and calorimeter.
- Barrel Timing Layer (BTL) : LYSO crystal + SiPM
- Endcap Timing Layer (ETL) : LGAD sensor + ASIC (ETROC)
- Korean CMS group is responsible for 25 % of MTD Endcap Timing Layer (ETL) production.

Design of MTD ETL

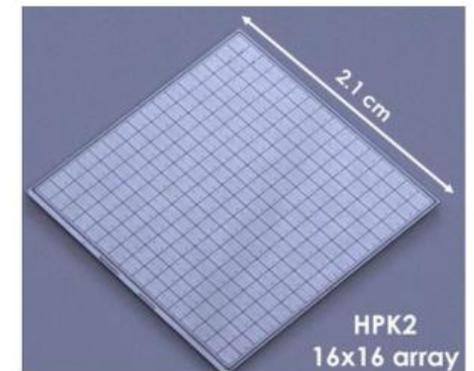
- Two **double-sided disks** for each side
 - Maximize geometrical acceptance (85%/disk)
 - Widened coverage : $1.6 < |\eta| < 3.0$
 - Average of 1.8 hits per track
 - **Time resolution per track < 35 ps**
- Low-Gain Avalanche Diode (**LGAD**) sensor bump bonded readout ASIC (**ETROC**)



Low Gain Avalanche Diode (LGAD) sensor



- LGAD characteristics
 - 16x16 pixel matrix, 1.3x1.3 mm² pixel size
 - Highly improved radiation tolerance
 - Very low gain factor (10-30) : excellent S/N ratio
 - Thin implanted gain layer (35-50 μm)
 - Gain uniformity (>8 fC of charge)
- Additional gain layer : highly boron-doped thin layer
 - Able to generate the high E field enough charge multiplication



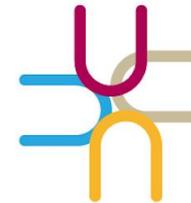
Korean CMS MTD Group



경북대학교
KYUNGPOOK NATIONAL UNIVERSITY



고려대학교
KOREA UNIVERSITY



강릉원주대학교
GANGNEUNG-WONJU NATIONAL UNIVERSITY



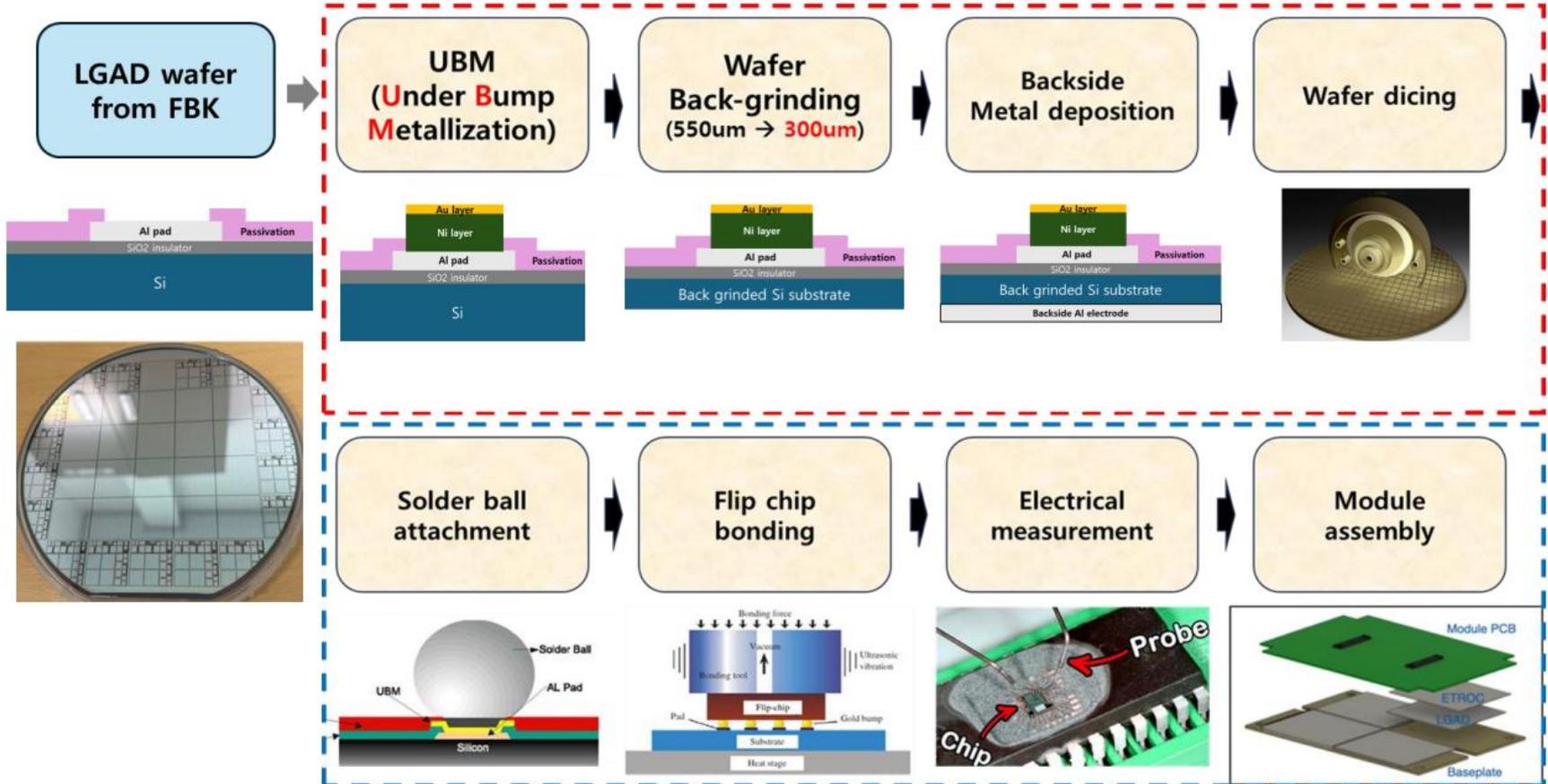
전남대학교
CHONNAM NATIONAL UNIVERSITY

- Held 1st intensive MTD workshop in Gangneung, Korea
- 4 institutions and ~ 20 members

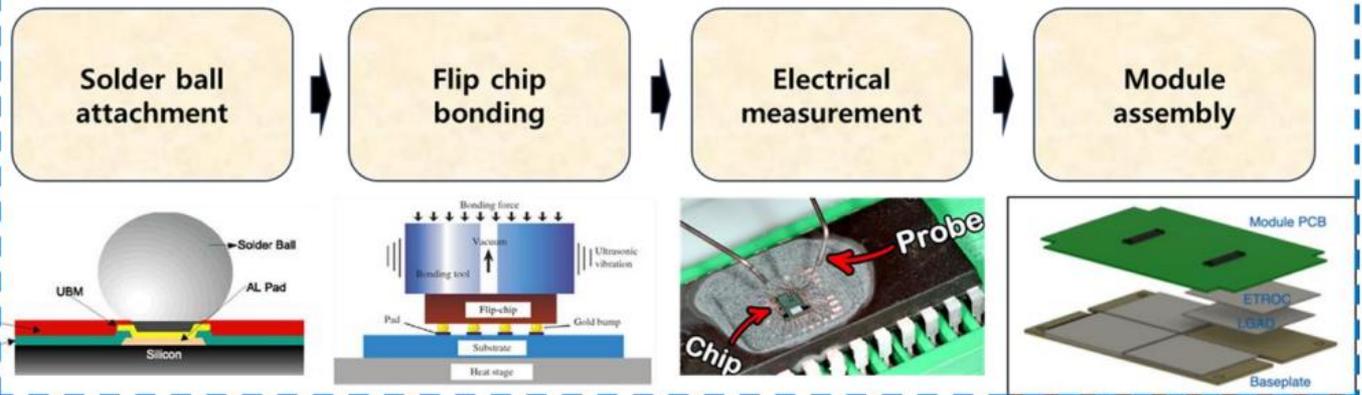
Korean CMS MTD Group Contributions

- Participated wafer market survey
- LGAD post-processing, bump bonding and module assembly

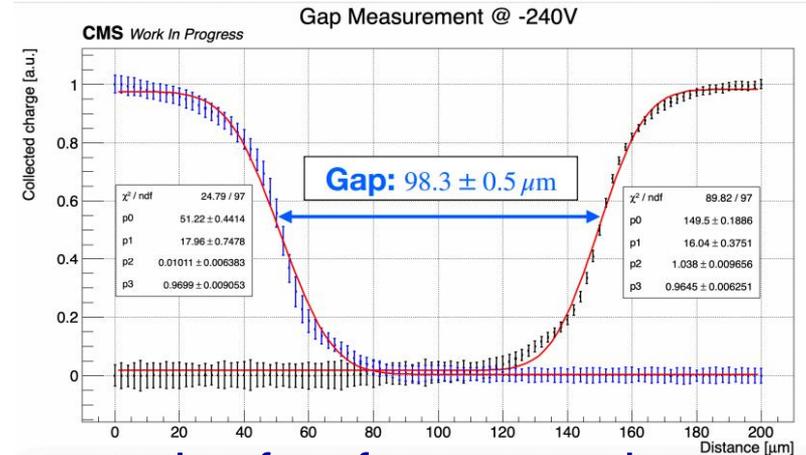
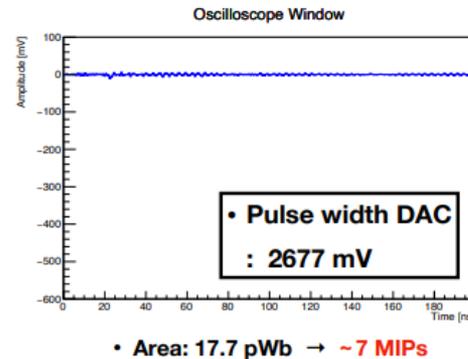
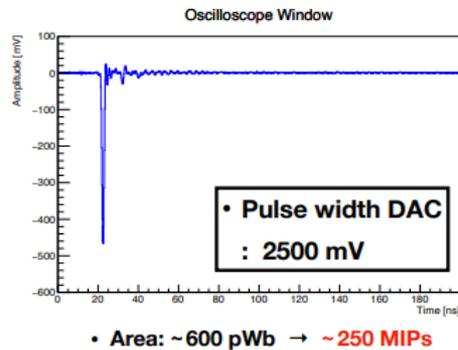
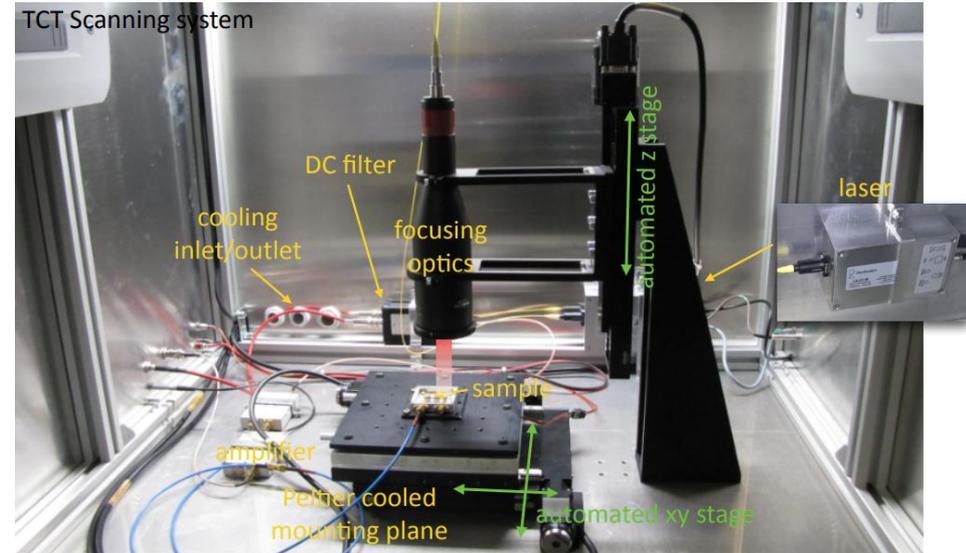
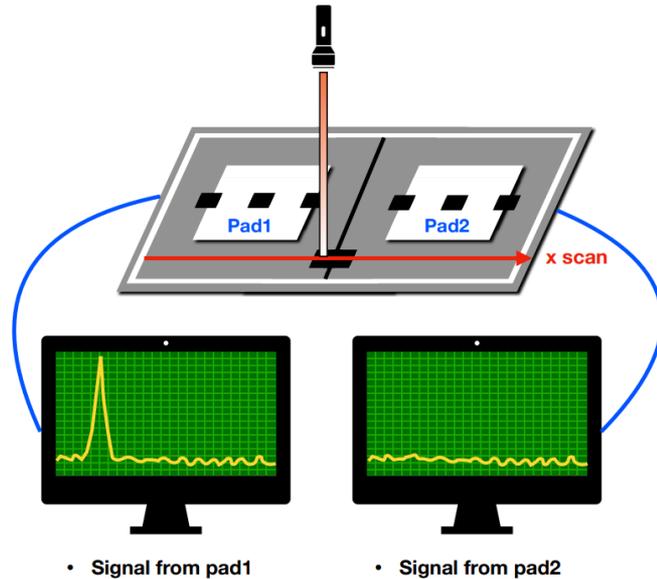
1) LGAD wafer post-processing



2) Bump bonding and module assembly

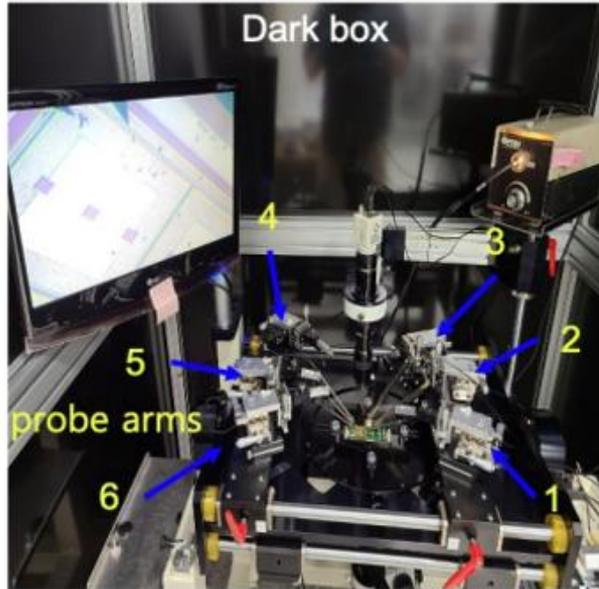


Market Survey for wafer companies

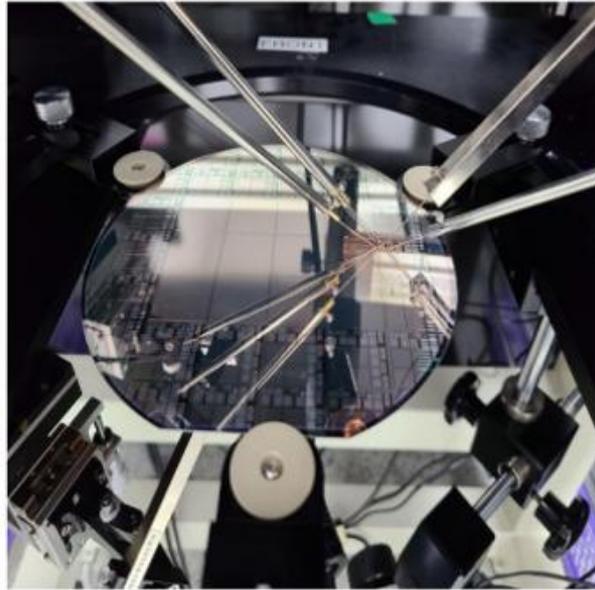


- Contributed to market survey : comparison study of wafer companies.

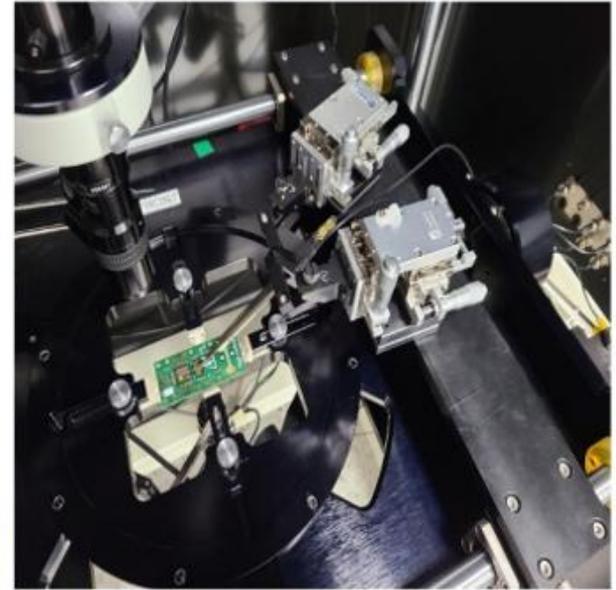
Test setup for wafer and sensor level



● Overview

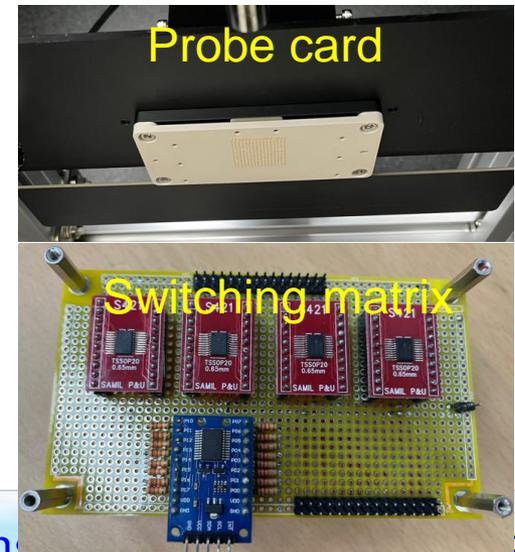


● wafer tray

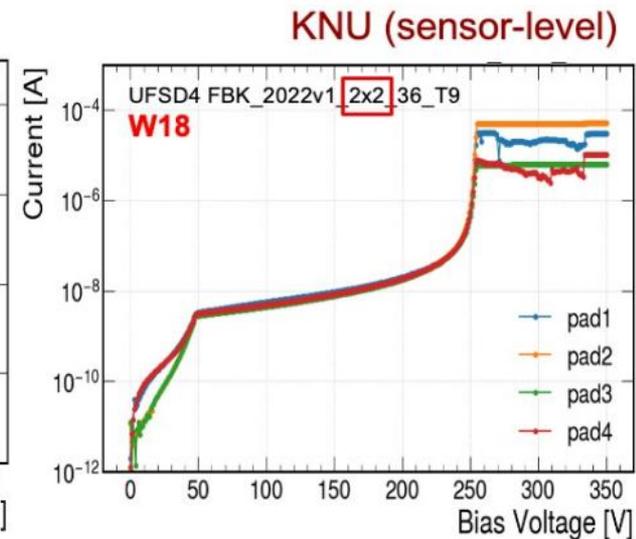
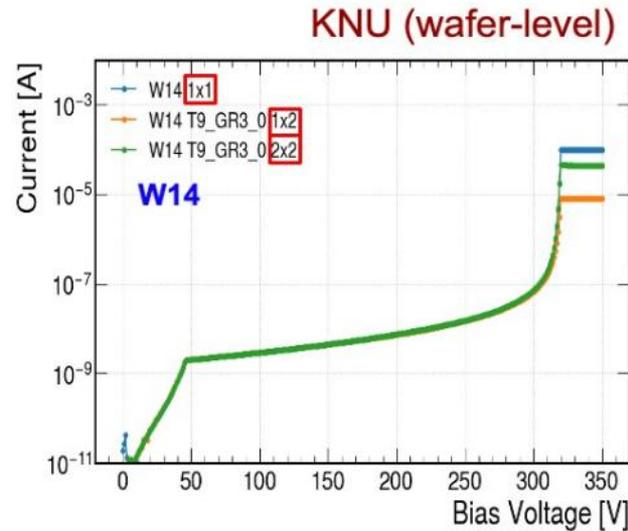
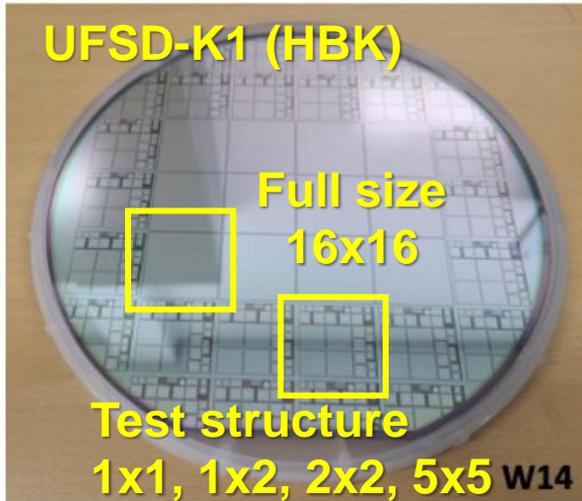


● sensor tray

- Six probe arms that use magnets to connect with the station
 - Signal read-out, bias voltages supplying, and 4 for grounding
- Two types of tray available for wafer-level and sensor-level tests
- **KCMS will prepare a probe card and switching matrix for 16x16 sensors**

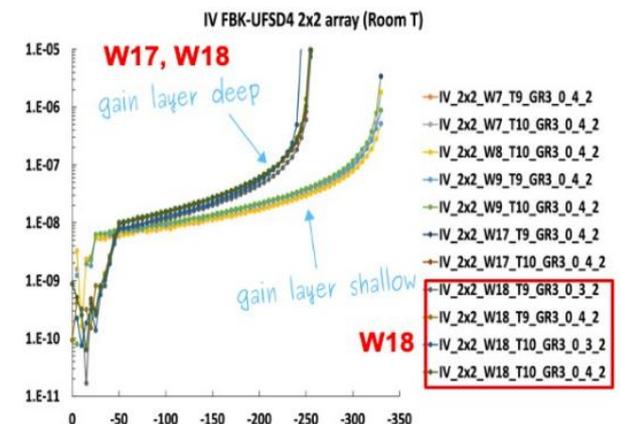


Test results for wafer and sensor level

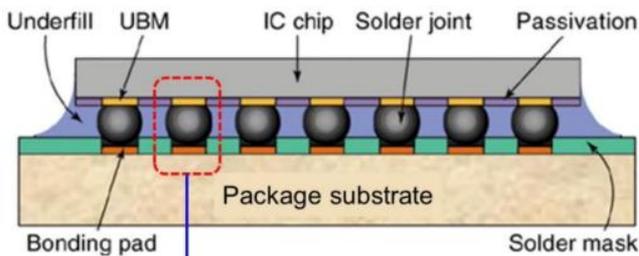
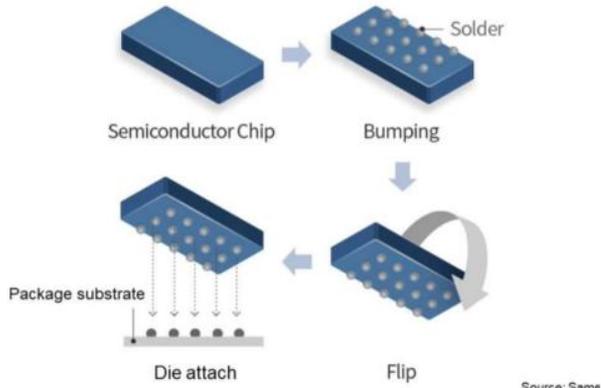


- Bias voltage applied from 0 V to -350 V
- Tested in room temperature
- Breakdown voltage
 - $V_{BD} \sim 320$ V in W14 and $V_{BD} \sim 250$ V in W18
 - Not depending on the sensor structures in the W14
- Comparable with Torino group results

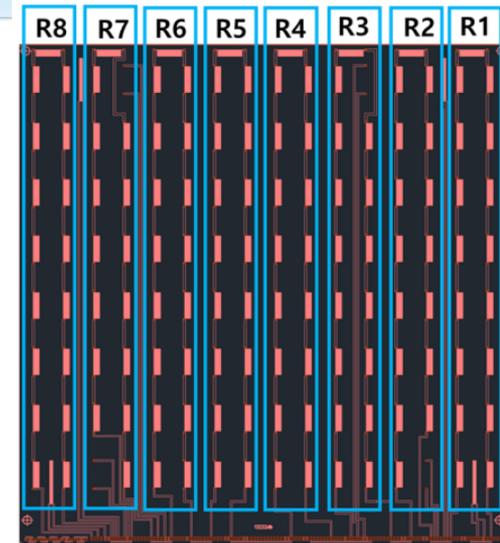
Torino



Bumping and flip chip bonding



Bumps on die should be located at exact location of bond pad of package substrate



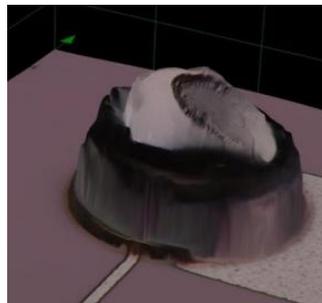
ROIC dummy device

Unit : Ohm

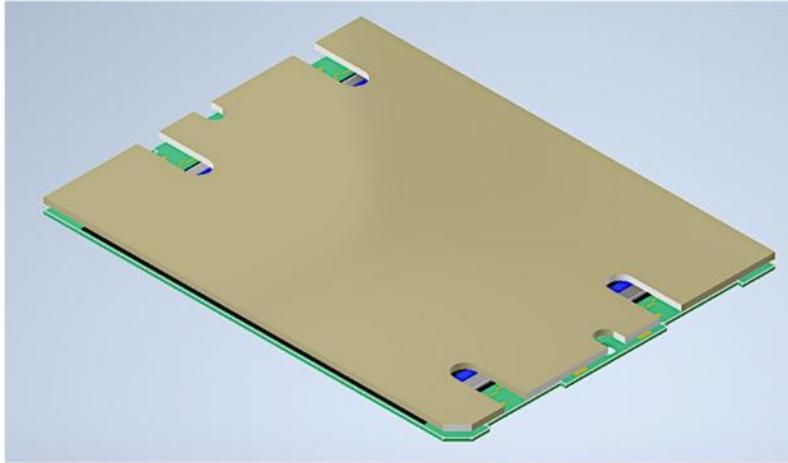
Sample	R1	R2	R3	R4	R5	R6	R7	R8
S1	808	276	253	185	20	21	215	516
S2	291	33	37	202	57	27	240	440

Resistance test

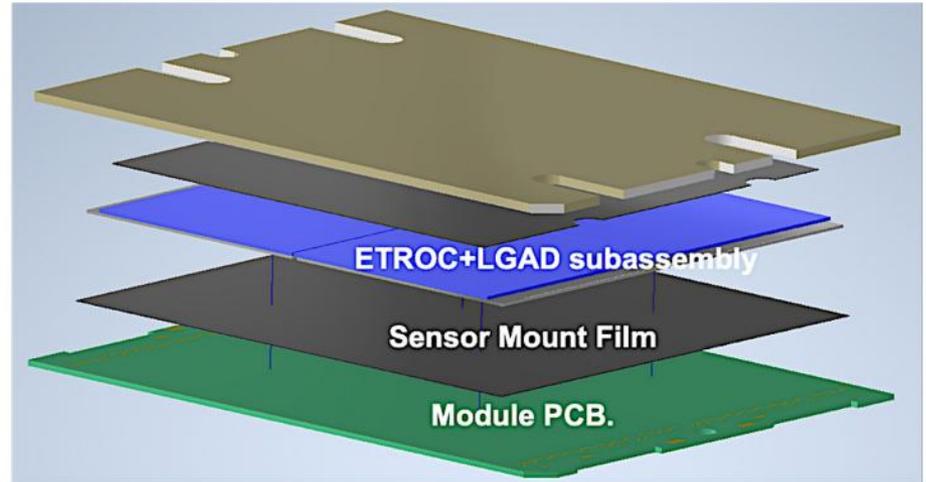
- Bump bonding test with dummy wafers
 - Searching for appropriate vendors
- Resistance test, 3D imaging inspection



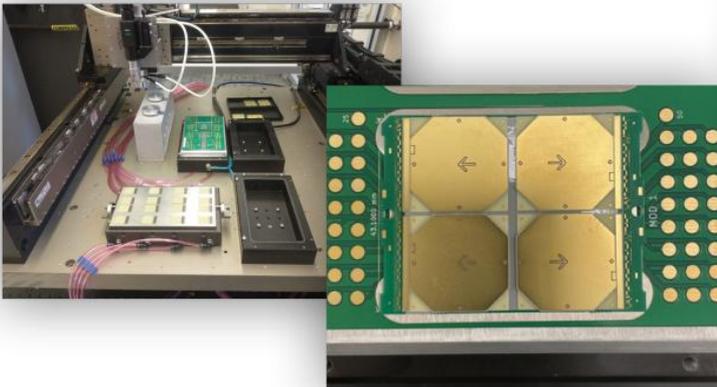
Module assembly



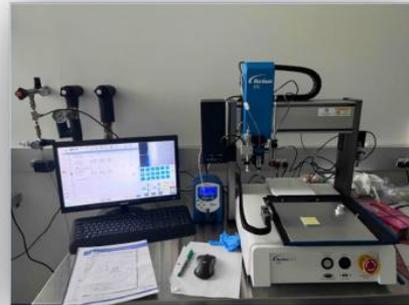
PCB + subassembly



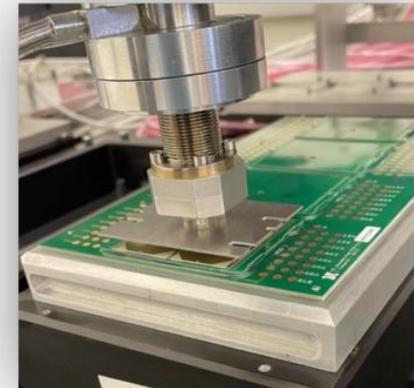
Basic scheme of a module



Pick & place sensor +
PCB

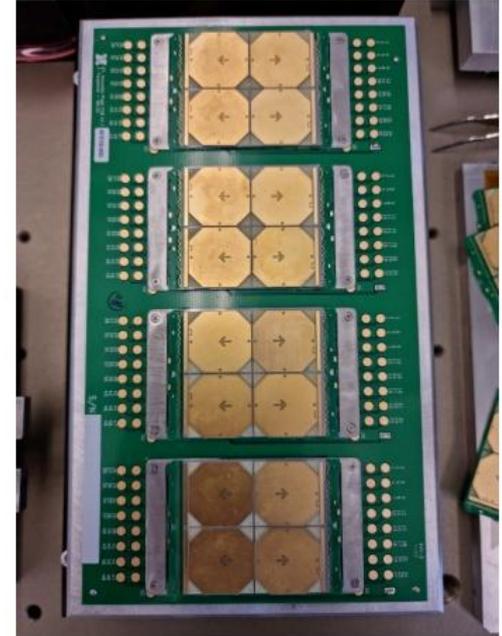
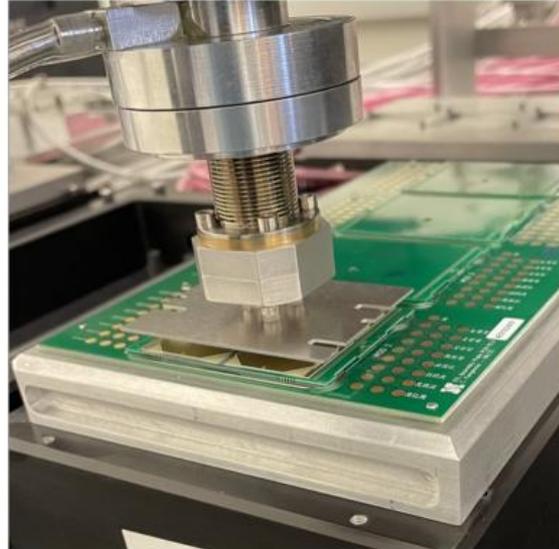
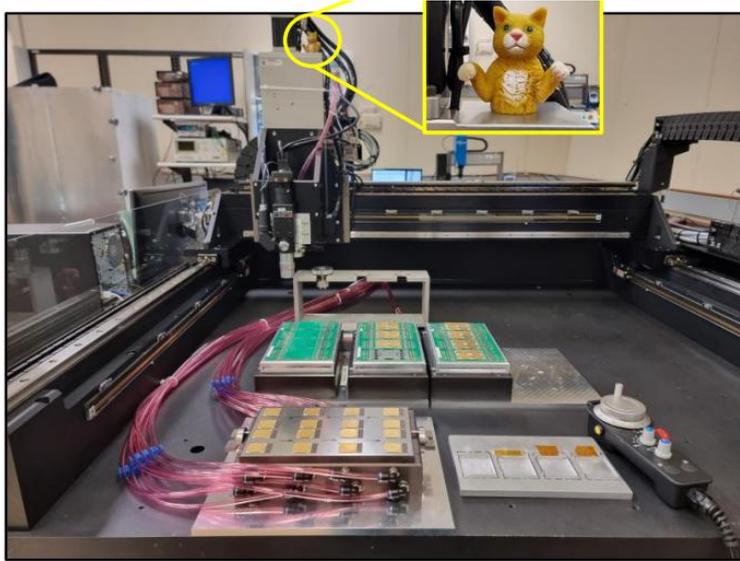


Wirebond and
encapsulating

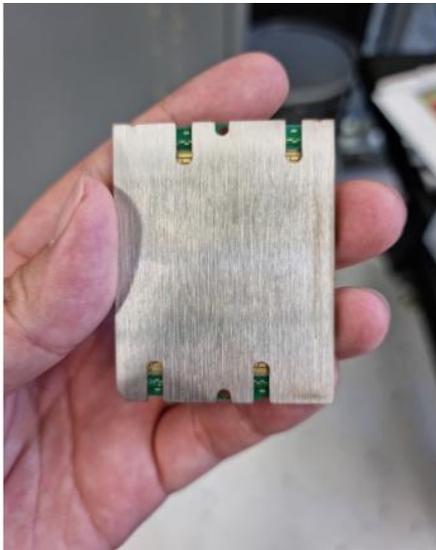


Apply film to baseplate, pick and
place, and cure film

Module assembly



Robotic gantry (SiDet, FNAL)

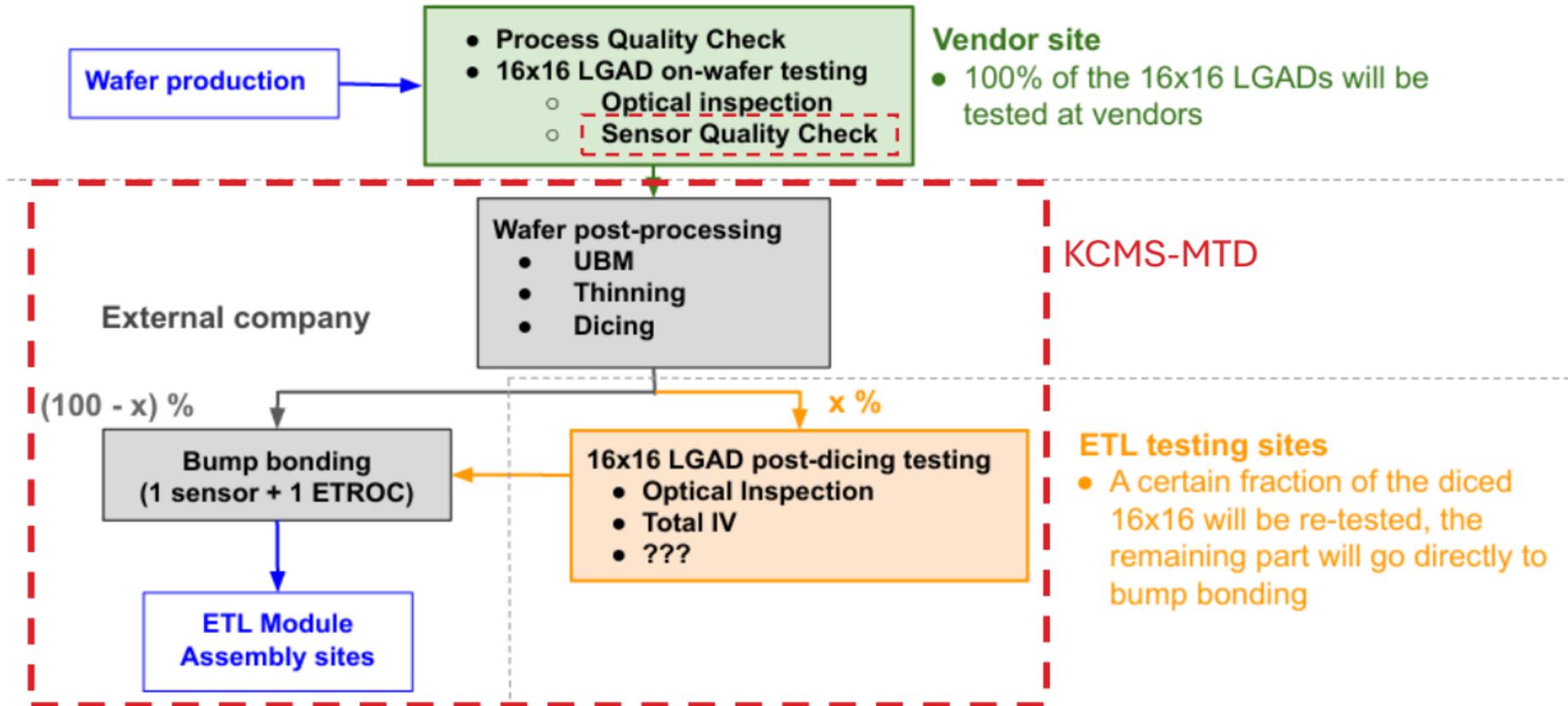


- Visiting Fermi Lab. to participate assembly process
- Preparation of the full assembly process is completed and ready to go.
- 50% throughput demonstration with mockup components ongoing at assembly sites.
- Robotic gantry shows good subassembly alignment below the 100 μm limit.

QA/QC preparation at Korea site

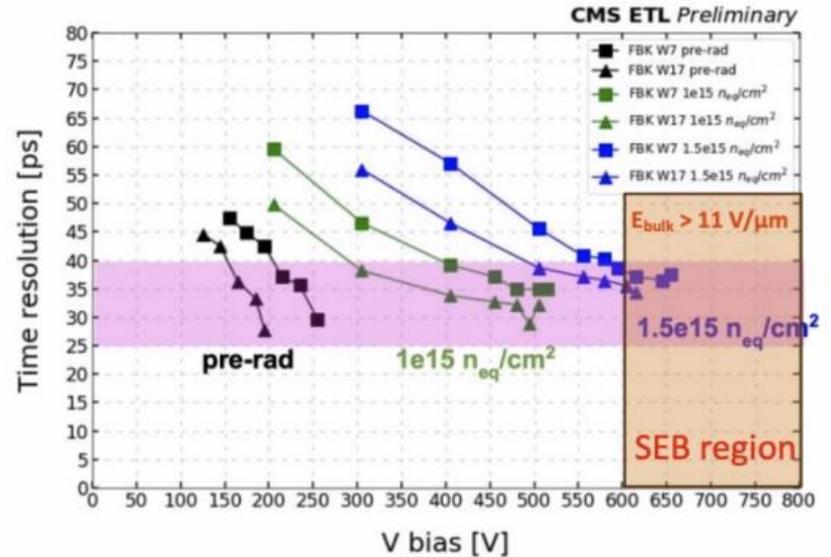
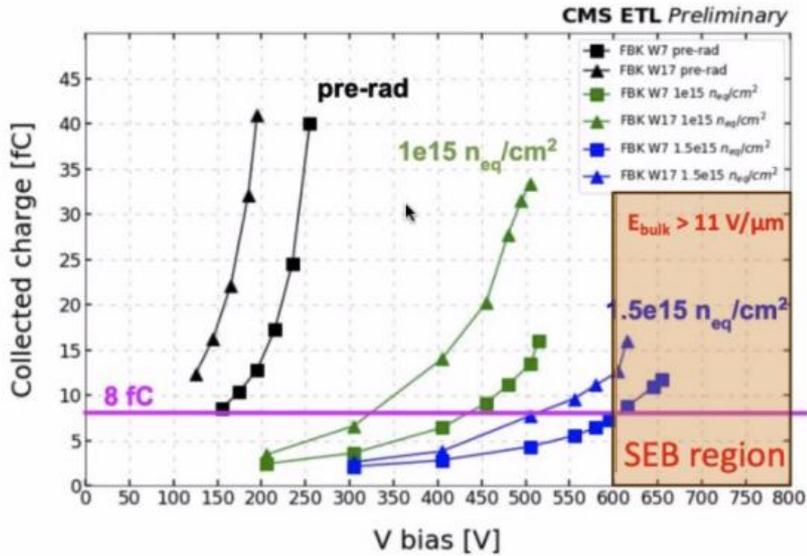


ETL QA/QC plans



- Building Quality Assurance (QA)/Quality Control (QC) facility in Korea
 - Leakage current, breakdown voltage, V_{GL} uniformity etc.

Irradiation test in KOMAC



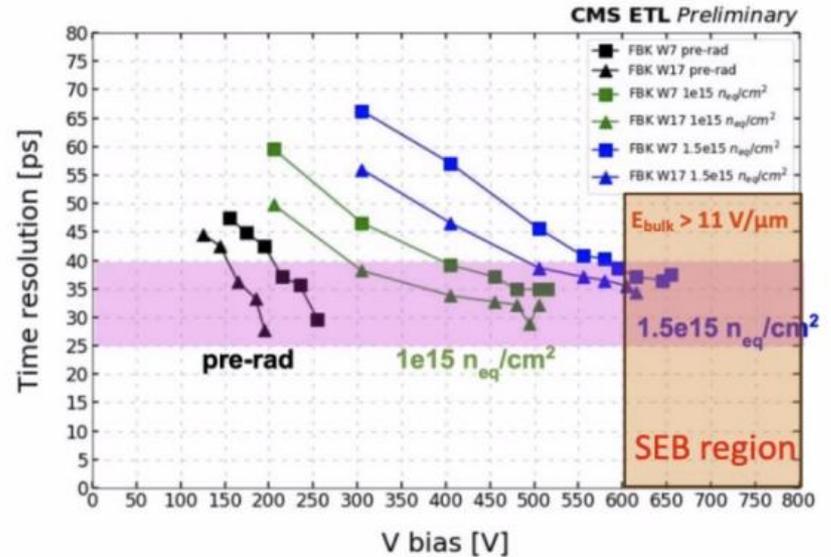
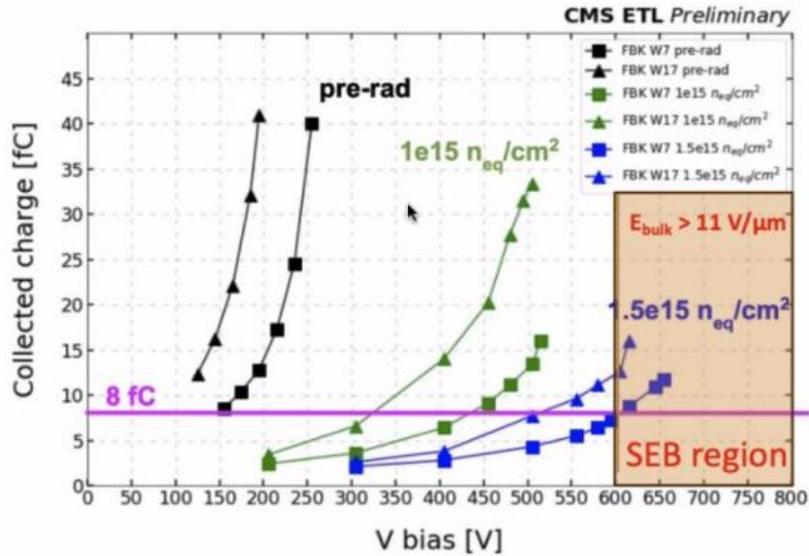
- Irradiation damage has been tested with beta source (^{90}Sr) at FBK
- Single event burn-out (SEB) observed at high radiation environment
- Follow up irradiation test has been carried out at KOMAC facility in Korea (100 eV proton beam)

KOMAC accelerator

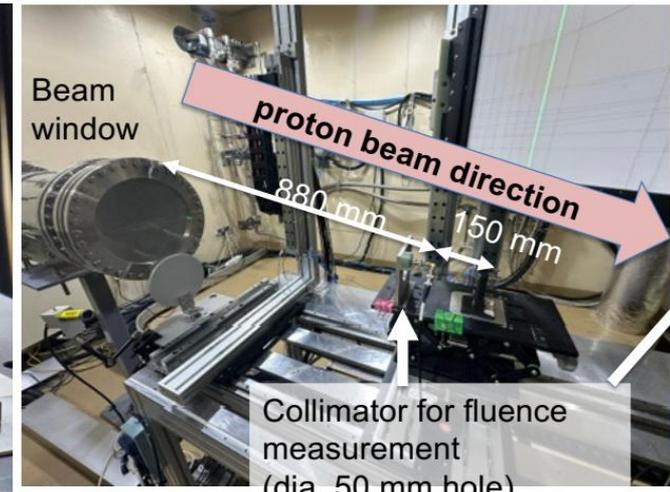
- Beam size : 30 mm
- Beam flux : $10^{10} \sim 10^{11}$ /pulse
- Beam energy : 20 MeV, 100 MeV



Irradiation test in KOMAC



- Follow up irradiation test has been carried out at KOMAC facility in Korea (100 MeV proton beam)
 - 2 LGAD itself
 - 2 Bump-bonded dummy wafer + chip
 - UFSD-K1 (after post process)
- Analysis is ongoing.



Summary and plan

- CERN-Korea CMS sign up MoU in 2022

Memorandum of Understanding (MoU) for Korea-CMS contribution towards the MIP timing detector (MTD) for the Phase-2 CMS Upgrade

between

The CMS Collaboration at CERN, hereafter referred to as CMS, on the one hand
and

The CMS Korea Institutes, hereinafter referred to as KCMS, on the other hand and
hereinafter collectively referred to as Parties



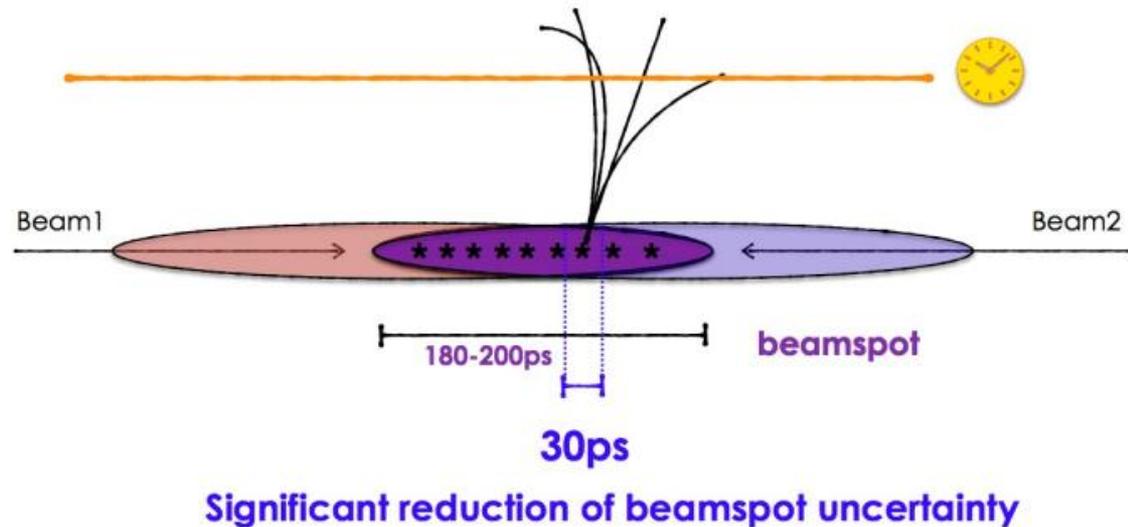
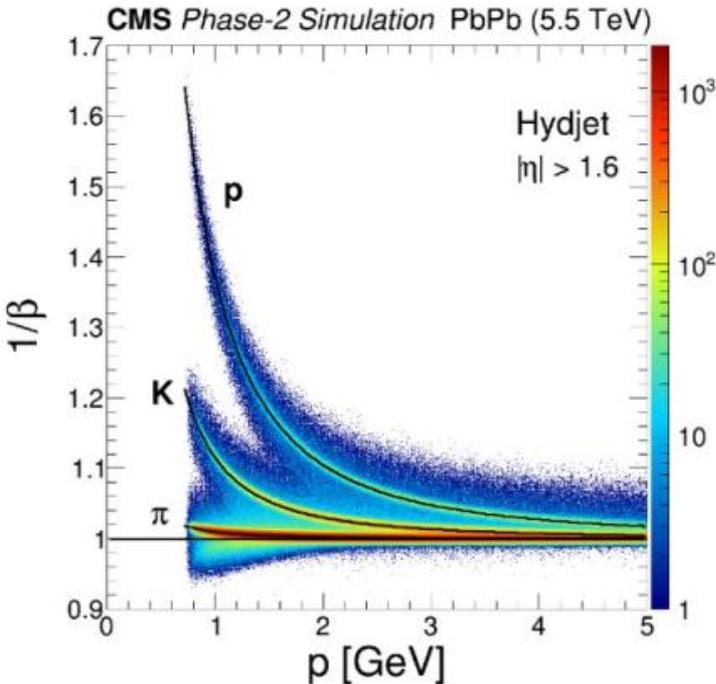
- Korea CMS is responsible for 25 % of LGAD sensor, post-process, module assembly of MTD ETL production.
 - 2.2 MCHF budge approved by National Research Foundation (NRF)
- First Korea-Italy LGAD sensors (UFSD-K1,K2) were produced, and evaluation is ongoing in Korea.
- QC/QC facility is ongoing to build.
- Irradiation test results are ongoing to analyze.

A large, abstract watercolor splash in shades of purple, blue, green, and yellow, centered on a white background. The splash has a soft, textured appearance with various colors blending into each other.

Backup

Advantage for heavy ion crew

MTD Physics motivation: particle ID

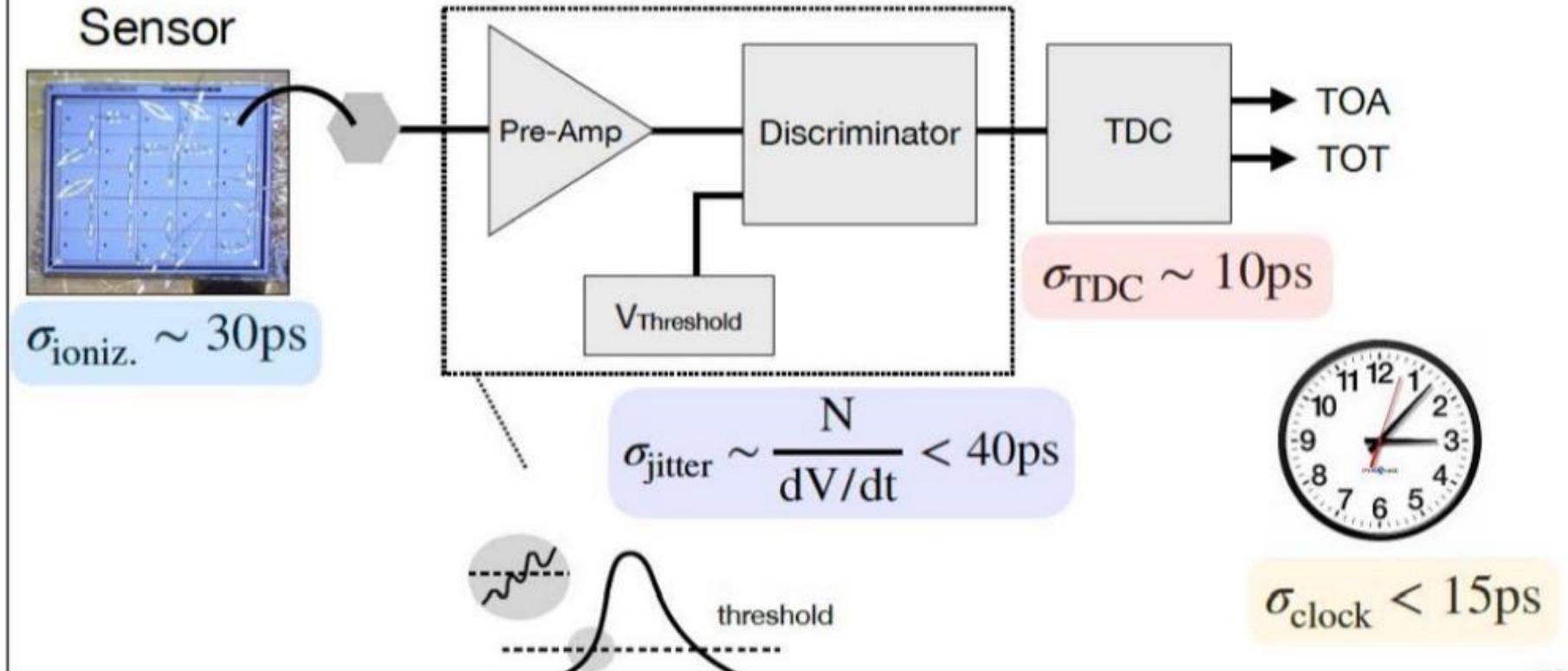


- ❑ MTD can provide significant improvement for particle ID
 - Heavy ion charm tag
- ❑ Significant gains for searches for long-lived new particles

Timing Resolution

ETL - Timing Resolution

$$\sigma_t^2 = \sigma_{\text{ionization}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{clock}}^2$$



MTD BTL

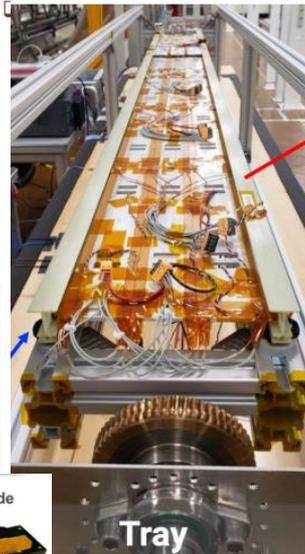
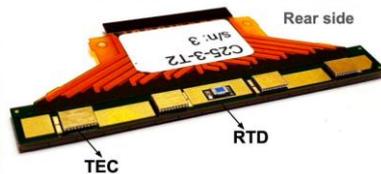
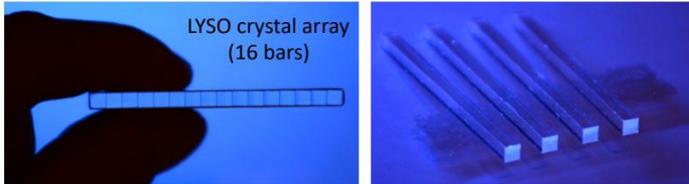
MTD : Barrel Timing Layer (BTL)

3.8 cm thin cylindrical detector

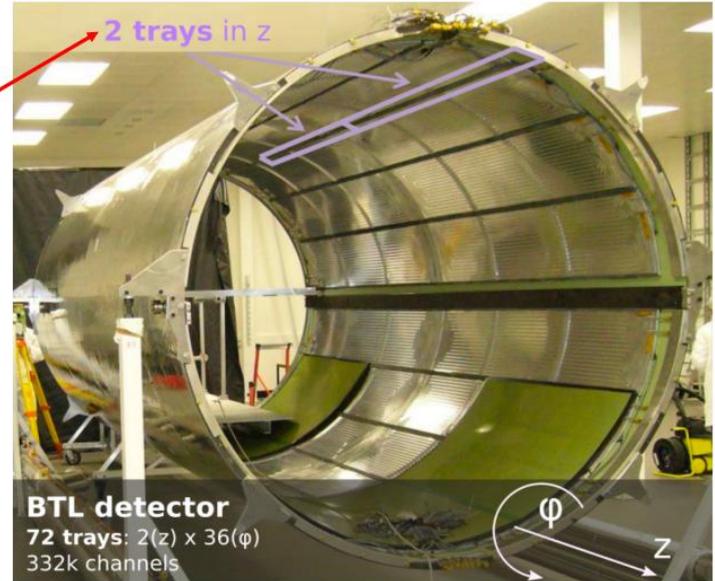
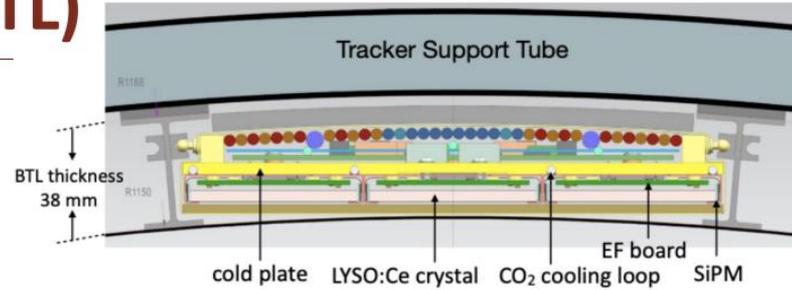
- located inside the tracker support tube, $|\eta| < 1.45$
- ~ 5 m long, 38 m^2 surface

LYSO crystal bars (166k)

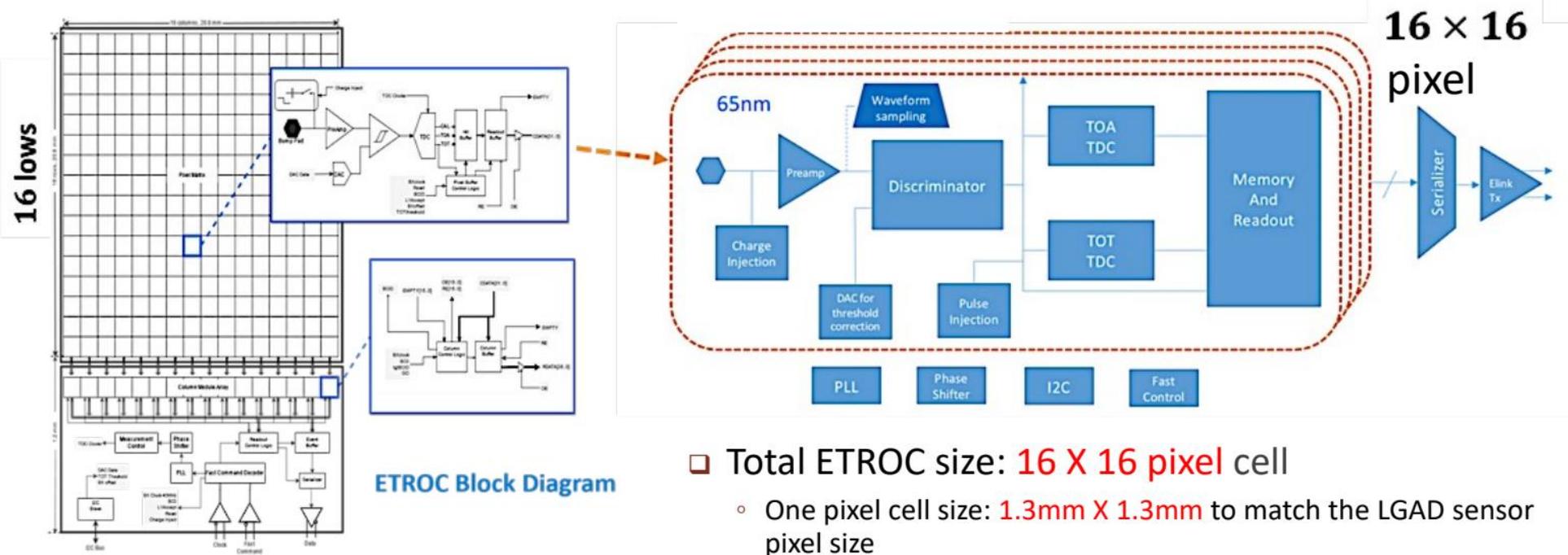
- Cerium-doped lutetium yttrium orthosilicate (LYSO:Ce) scintillation medium
- Well established in PET applications and vendors widely available
- High radiation tolerance
- $\tau_{\text{rise}} : \sim 100 \text{ ps}$, $\tau_{\text{decay}} : \sim 40 \text{ ns}$
- High Light Yield : $40000 \text{ } \gamma/\text{MeV}$



24!



Endcap Timing Layer ReadOut Chip (ETROC)

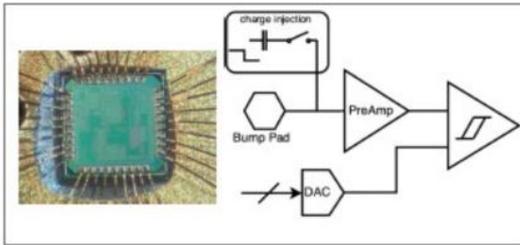


- ❑ Total ETROC size: **16 X 16 pixel** cell
 - One pixel cell size: **1.3mm X 1.3mm** to match the LGAD sensor pixel size
- ❑ Targeting signal charge (1MIP): **6 - 20 fC**
- ❑ TDC (time-to-digital converter) range
 - ~5 ns TOA (time of arrival)
 - ~10 ns TOT (time over threshold)

ETROC Development Plan

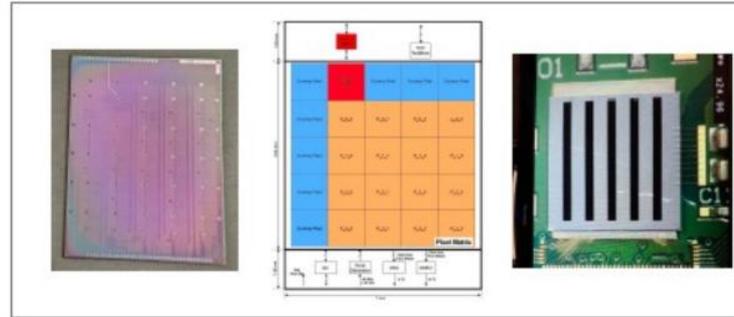
2018

ETROC0 (1x1)



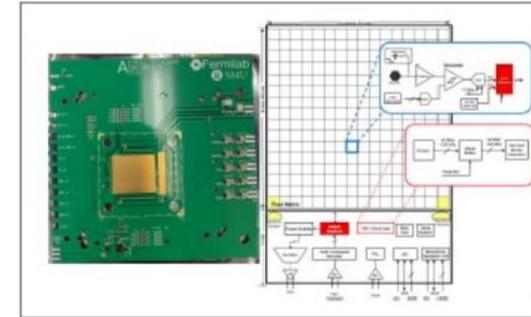
2020

ETROC1 (4x4)



2023

ETROC2 (16x16)



- Analog front-end only
- Wire-bonded with LGAD sensor reached ~ 33 ps time resolution per hit with preamp. waveforms
- Passed 100 Mrad TID

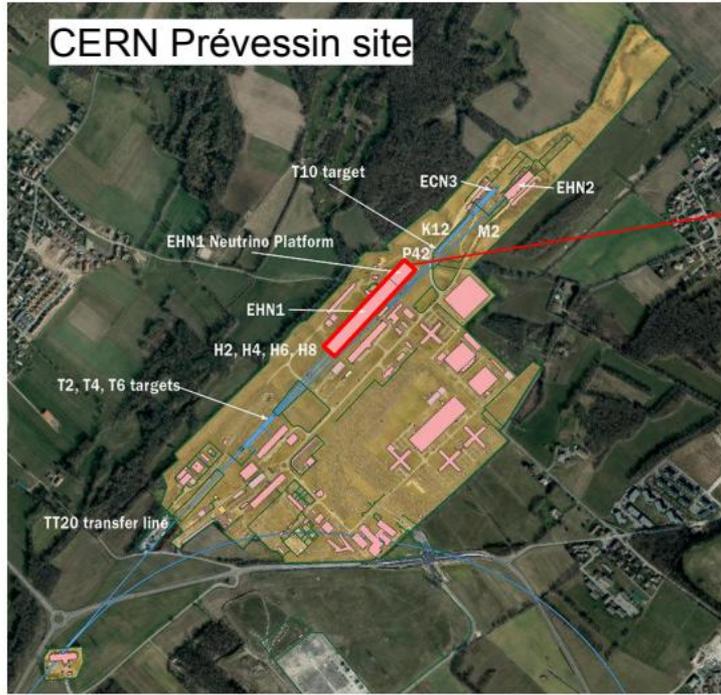
- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~ 42 ps time resolution per hit with TDC data

- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

□ ETROC3 : Final chip

- The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
- Submission scheduled for 2024

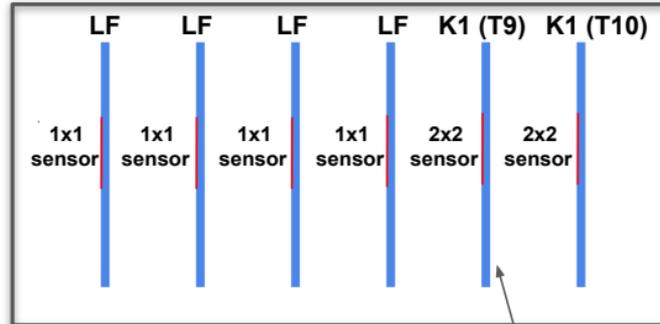
ETROC test in Fermi Lab.



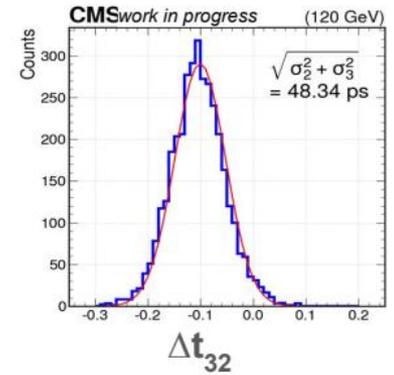
120 GeV Pion beam from SPS used for measurement of timing resolution of LGAD sensors

Only single channel is connected to the signal readout for UFSD-K1 (T9), UFSD-K1 (T10) sensors

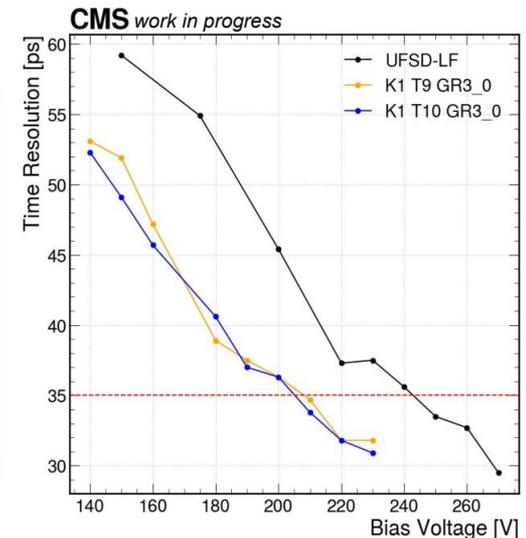
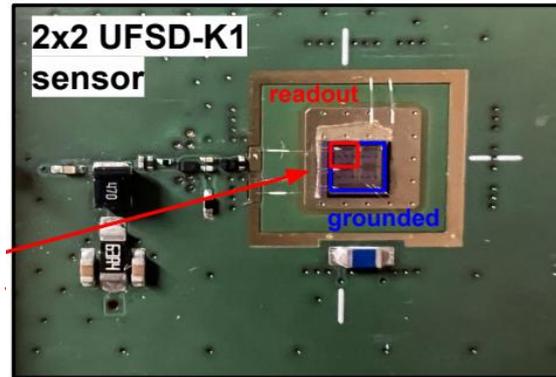
Test module (6 slots)



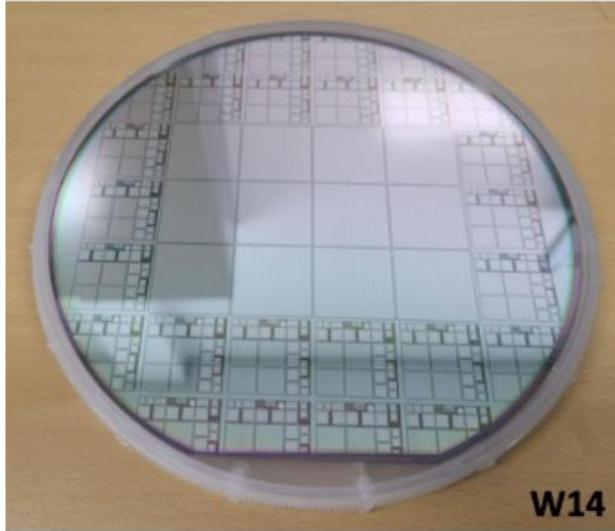
Santa-Cruz board



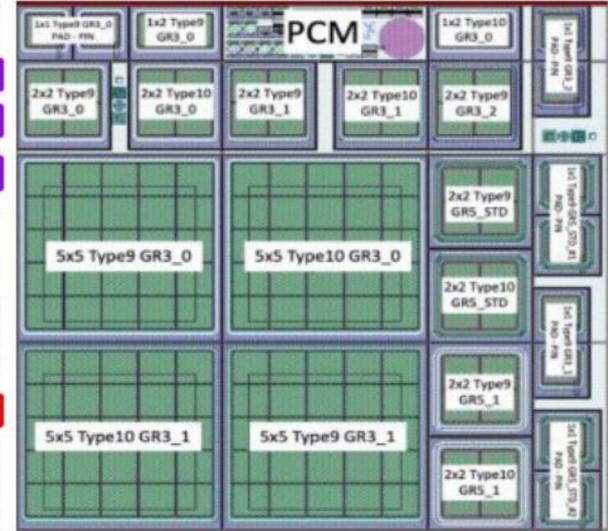
Wire bonded to Santa-Cruz Board



UFSD4 (FBK, Italy) wafers test in Korea

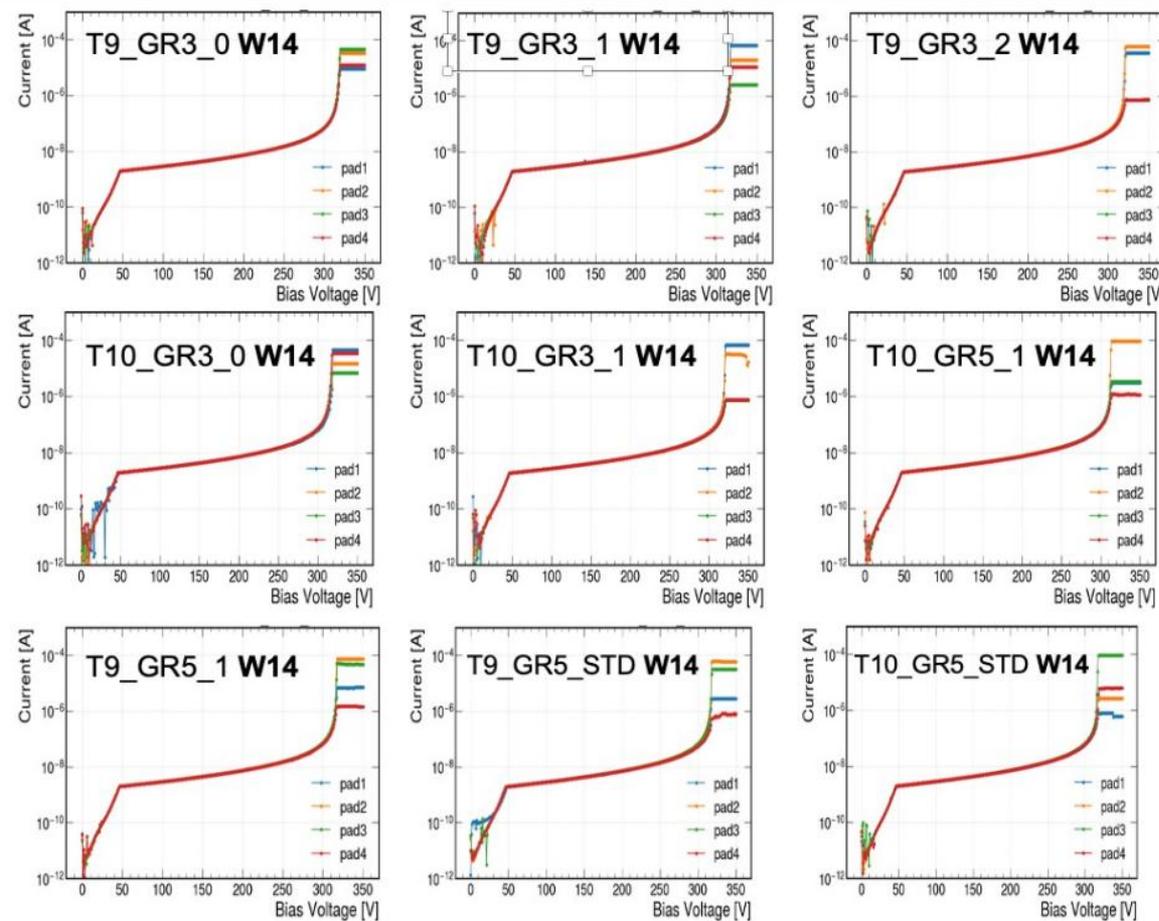


Wafer Group	Wafer #	DI	Gain Layer		Diffusion
			Dose	Carbon	
1	1	Shallow	0.96	0.8	CH-BL
2	2	Shallow	1.00	1	CH-BL
3	3	Shallow	0.98	1	CH-BL
3	4	Shallow	0.98	1	CH-BL
4	5	Shallow	0.98	0.8	CH-BL
4	6	Shallow	0.98	0.8	CH-BL
4	7	Shallow	0.98	0.8	CH-BL
4	8	Shallow	0.98	0.8	CH-BL
4	9	Shallow	0.98	0.8	CH-BL
5	10	Shallow	0.98	0.8 + CS0.6	CH-BL
5	11	Shallow	0.98	0.8 + CS0.6	CH-BL
6	12	Deep	0.75	0.6	CL-BL
7	13	Deep	0.77	0.6	CL-BL
8	14	Deep	0.77	0.6	CL-BL
8	15	Deep	0.77	0.6	CL-BL
9	16	Deep	0.79	0.6	CL-BL
9	17	Deep	0.79	0.6	CL-BL
9	18	Deep	0.79	0.6	CL-BL

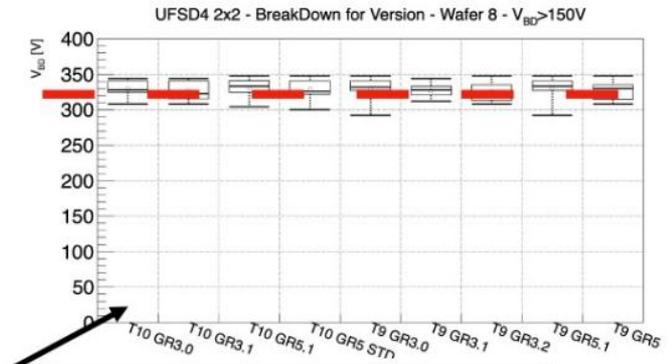


- ❑ The **Red box** represents the UFSD4 wafer #14 (W14), which has undergone wafer-level testing at KNU
- ❑ The **Purple box** represents three wafers which are shipped to CERN today for ETROC2 testing
- ❑ New 16 wafers (UFSD-K1), will be available for testing in a few weeks

I-V measurement of 2x2 sensors in wafer level (UFSD4 W14) at KNU

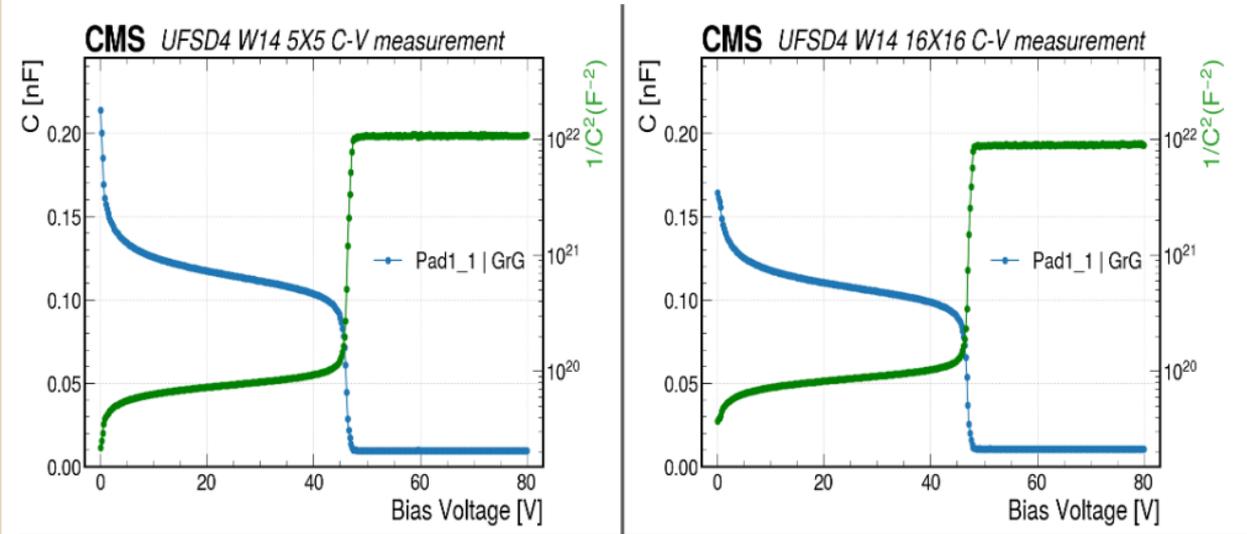
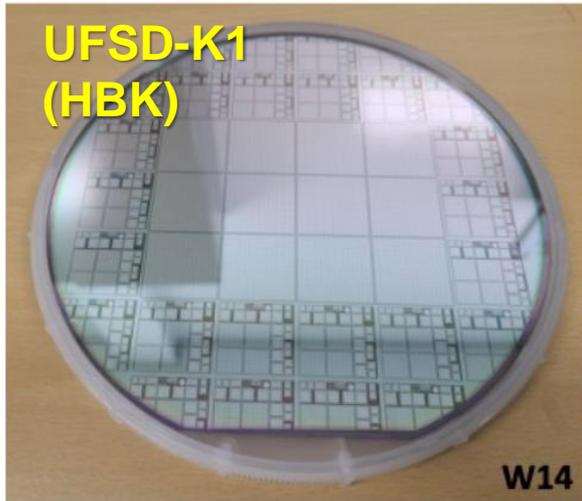


- Bias Voltage applied from 0 V to -350 V ($\Delta V = 1$ V)
- Room temperature
- Breakdown Voltage
 - $V_{BD} \sim 320$ V
 - The breakdown voltages are consistent in 2x2 sensors

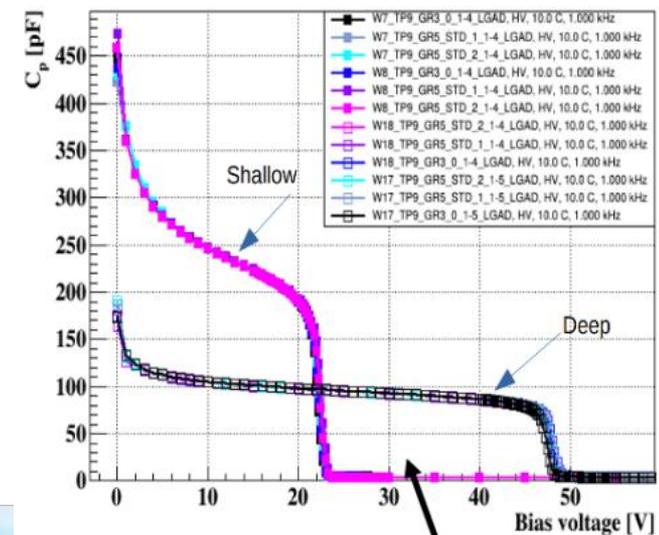


From Marta Tornago's talk,
<https://indico.cern.ch/event/1141394/>

Test results for wafer and sensor level



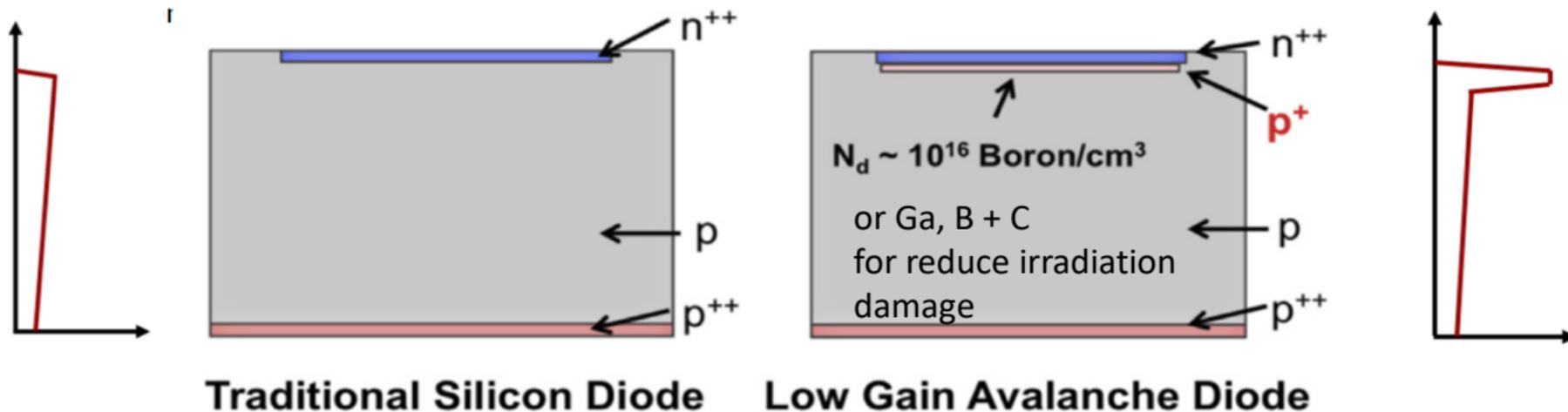
- ❑ Bias Voltage applied from 0 V to -80 V ($\Delta V = 0.2$ V)
- ❑ AC frequency (10 kHz)
- ❑ Room temperature
- ❑ **Depletion Voltage**
 - Gain layer depletion Voltage ~ 44 V
 - Full depletion Voltage ~ 47 V



Low Gain Avalanche Diode (LGAD) Sensors

LGAD sensor design

- ❑ LGAD sensor on endcap timing layer
 - Provides timing information for next-generation detectors
- ❑ Thin implanted gain layer of overall thickness of 35–50 μm
 - Fast timing can be achieved in silicon diodes with a thin depletion region to have short drift times & fast rise time.
 - 50 μm thick depletion region gives < 500 ps rise time.
- ❑ E field amplification from internal p^+ doping layer of silicon diode sensor
- ❑ Achieve a low-jitter, low noise with large signal
- ❑ Implement the internal gain of the sensor at 10-30 while providing 30-50 ps time resolution.



PN Junction Diode

