# Status of TileCal Cesium Phase II electronics

Alexander Solodkov
on behalf of the
ATLAS TileCal Cesium team

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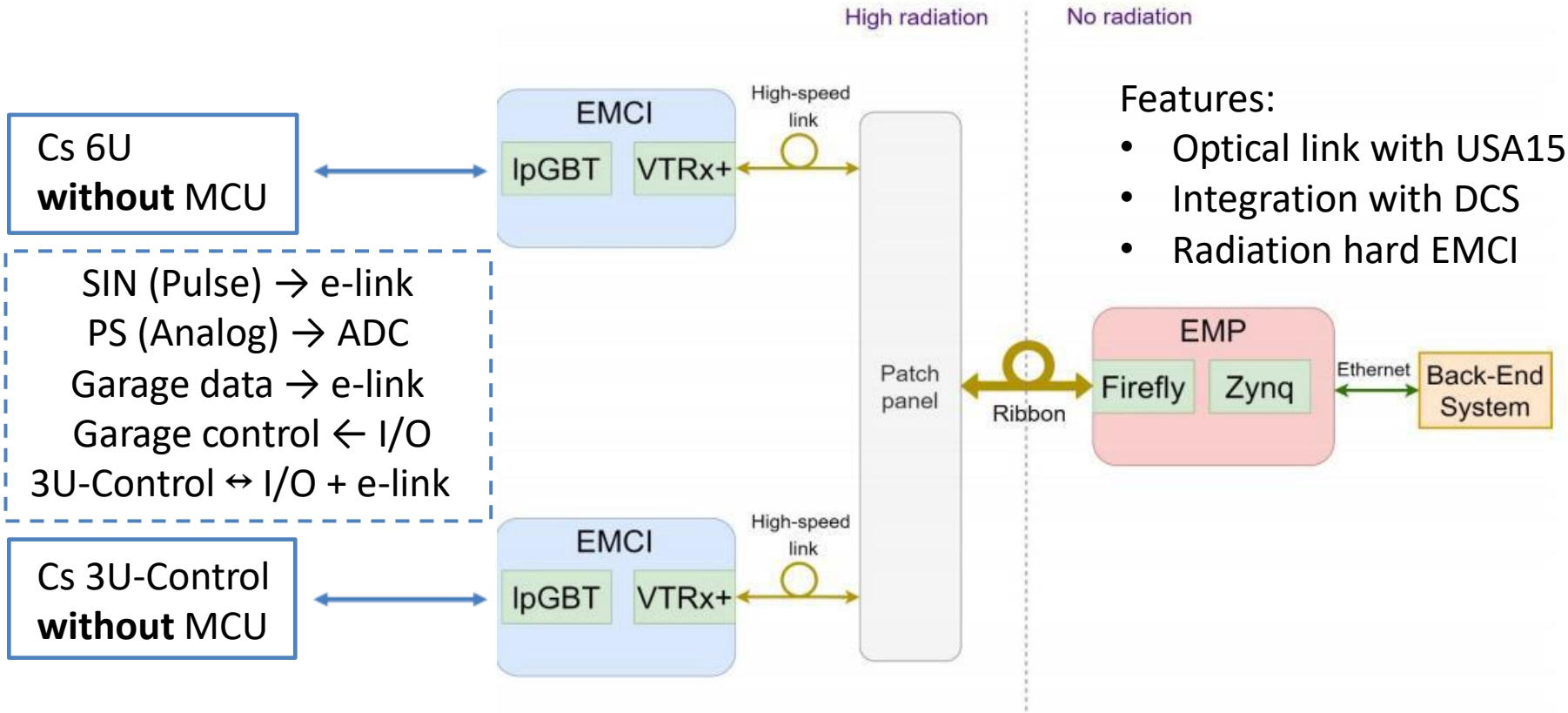
# Design of Phase II Cesium electronics




- New design for Cs electronics has been proposed after first PDR
- It is based on new modules developed for Phase II upgrade – EMCI and EMP
- Cs electronics becomes significantly simpler (no MCU, no multiplexers)
- Processing of all the signals will be done inside EMP

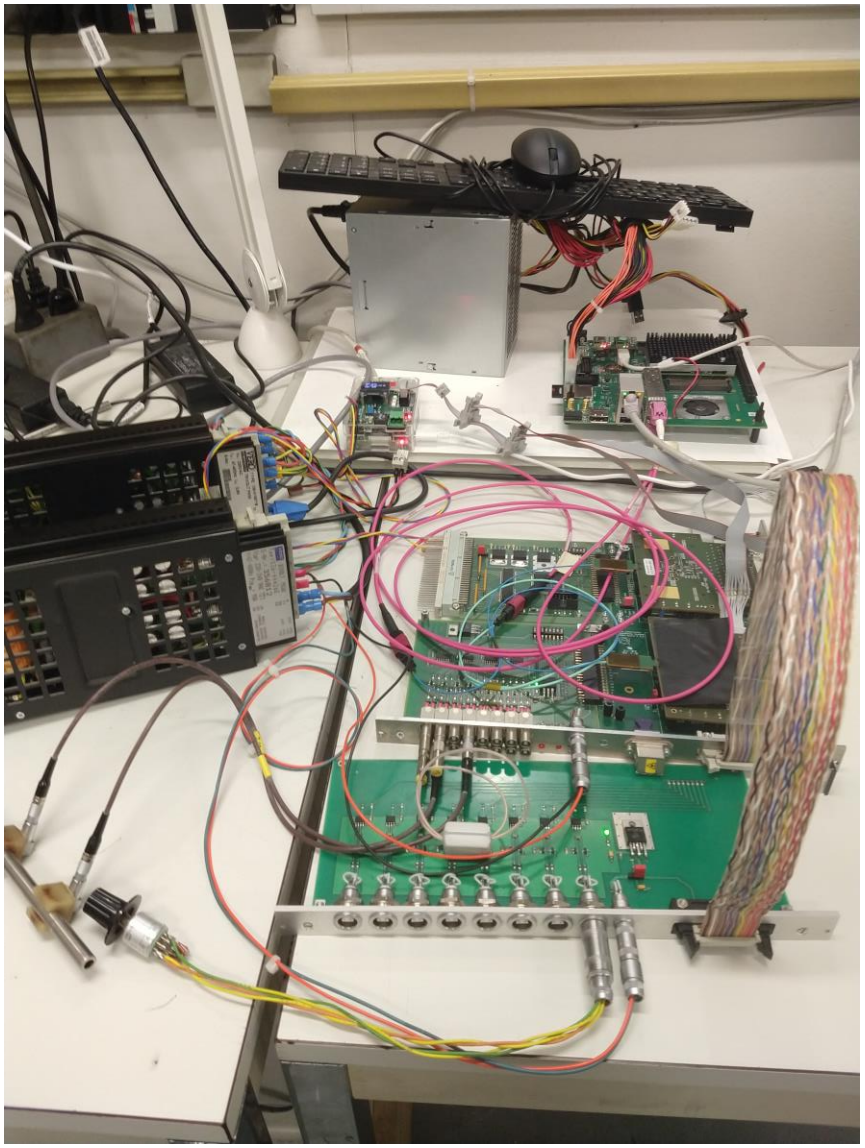
# Second Test stand

The second test stand was setup in November 2023, immediately after previous meeting
It is very similar to first test stand but with Trenz TEBF0808 development Board with two SFP+ ports and Trenz TE0807-0-S014 SoM

In addition to all the boards tested before – 6U-ADC board was connected to another board via 20pin connector on the front panel

Latest Trenz emp_assembly firmware (November 2023) prepared by EMP team was used without modifications for tests of ADC and GPIO readout

This new firmware contained few updates in LpGBT IP which are required for correct communication with LpGBT V1 chip



# Tests with Trenz board

- Alma9 OS was running on Trenz SoM
- emp_fw_v0.11 was loaded as an overlay
- Slightly modified versions of lpGbtAdc, lpGbtGpio, lpGbtRegister and lpGbtConfiguration programs from LpGbtSw repository were used for tests

- We were able to read successfully all ADC values, all GPIO values, set GPIO values (two registers for 8 “high” and 8 “low” GPIO channels)
  - GPIO signals were used to switch on HV for Geiger counter and to switch various LEDs
- We were even able to reset EMCI and to load full configuration from EMP to EMCI, i.e. in principle, piGBT is not needed anymore

- Unfortunately, communication over EC/IC channel was possible only with one EMCI (first production but with resoldered LpGBT V1)
- Newer EMCI (second production) had correct signals from 6U-SIN in eLinks, but didn’t provide good ADC/GPIO data at all

# GPIO and ADC tests

```
Reset EMCI

Write: Register Address: 0x000 Value: 0x01 = 00000001 = 001 completed successfully.
Write: Register Address: 0x0F8 Value: 0x04 = 00000100 = 004 completed successfully.

Load firmware

[15338.715799] fpga_manager fpga0: writing emp_fw_v0.11.bit.bin to Xilinx ZynqMP FPGA Manager

Configure EMCI

Read:  Register Address: 0x000 Value: 0x00 = 00000000 = 000
Read:  Register Address: 0x0F8 Value: 0x00 = 00000000 = 000
Read:  Register Address: 0x150 Value: 0xB2 = 10110010 = 178

2023-12-09 22:16:15.220542 [RegisterClerkFactory.cpp:27, INF] getClerk for lpgbt-uio://emp_lpgbt_10
2023-12-09 22:16:15.387391 [LpGbtUioBackend.cpp:21, INF] Initializing uio device 'emp_lpgbt_10'
2023-12-09 22:16:15.387635 [LpGbtUioBackend.cpp:24, INF] The magic number for this uio device is: 656d7049
--------------------------------------------------------------------------------------------------------------
2023-12-09 22:16:15.387817 [lpGbtConfiguration.cpp:129, INF] Starting LpGbt configuration using: 'lpgbt_config_ALL.conf'
76%
2023-12-09 22:16:15.401258 [lpGbtConfiguration.cpp:170, INF] End of file reached after line 256

2023-12-09 22:16:15.401426 [lpGbtConfiguration.cpp:178, INF] LpGbt Configuration Done!

Write: Register Address: 0x055 Value: 0x3C = 00111100 = 060 completed successfully.
Read:  Register Address: 0x1AF Value: 0xBE = 10111110 = 190
Read:  Register Address: 0x1B0 Value: 0x05 = 00000101 = 005

2023-12-09 22:16:15.766482 [RegisterClerkFactory.cpp:27, INF] getClerk for lpgbt-uio://emp_lpgbt_10
2023-12-09 22:16:15.935052 [LpGbtUioBackend.cpp:21, INF] Initializing uio device 'emp_lpgbt_10'
2023-12-09 22:16:15.935294 [LpGbtUioBackend.cpp:24, INF] The magic number for this uio device is: 656d7049
2023-12-09 22:16:15.946156 [lpGbtAdc.cpp:104, INF] For channel 0 got ADC value: 39
2023-12-09 22:16:15.946584 [lpGbtAdc.cpp:104, INF] For channel 1 got ADC value: 38
2023-12-09 22:16:15.946999 [lpGbtAdc.cpp:104, INF] For channel 2 got ADC value: 39
2023-12-09 22:16:15.947399 [lpGbtAdc.cpp:104, INF] For channel 3 got ADC value: 38
2023-12-09 22:16:15.947805 [lpGbtAdc.cpp:104, INF] For channel 4 got ADC value: 38
2023-12-09 22:16:15.948208 [lpGbtAdc.cpp:104, INF] For channel 5 got ADC value: 38
2023-12-09 22:16:15.948614 [lpGbtAdc.cpp:104, INF] For channel 6 got ADC value: 39
2023-12-09 22:16:15.949017 [lpGbtAdc.cpp:104, INF] For channel 7 got ADC value: 154

Write: Register Address: 0x055 Value: 0x00 = 00000000 = 000 completed successfully.
Read:  Register Address: 0x1AF Value: 0x82 = 10000010 = 130
Read:  Register Address: 0x1B0 Value: 0x05 = 00000101 = 005
```

Change one bit and ask to check CRC which forces EMCI restart

Load firmware as an overlay

Verify that EMCI restarted and has correct TX/RX/10Gbit/FEC5

Load config to EMCI

Write to GPIO register
Read two GPIO registers

Read 8 ADC values
first 7 – pedestals
last – with sensor

Write to GPIO register
Read two GPIO registers

First version of EMCI has 10 in GPIO bits 15-14

256 values in config file = 256 fuses

enable up/down eLinks and configure GPIO

GPIO configuration:
0-9 – input
10-13 – output
14-15 – input

# Production and tests of new boards

- In 2024 we started preparation for final production of all the boards
- Instead of production at IHEP, Protvino new PCBs were ordered from AMSET company in Bratislava (Slovakia)
- First set of the new boards will arrive at CERN ~next week and we are going to test them immediately
- It would be nice to test them with latest version of EMP firmware and possibly with different EMCIs
  - We need to understand better why one of two EMCI didn't work for us

# THANK YOU