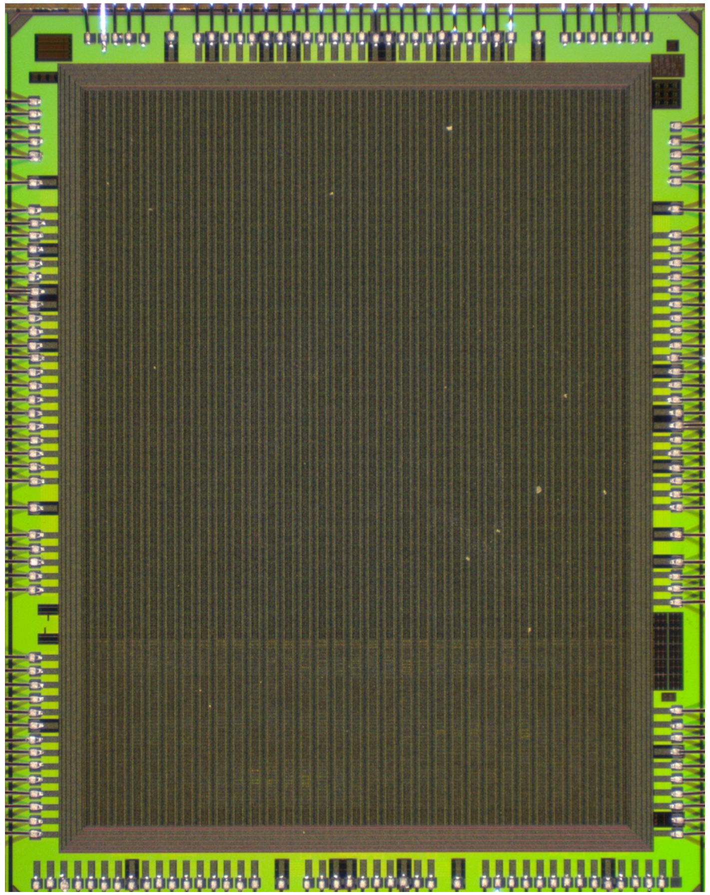
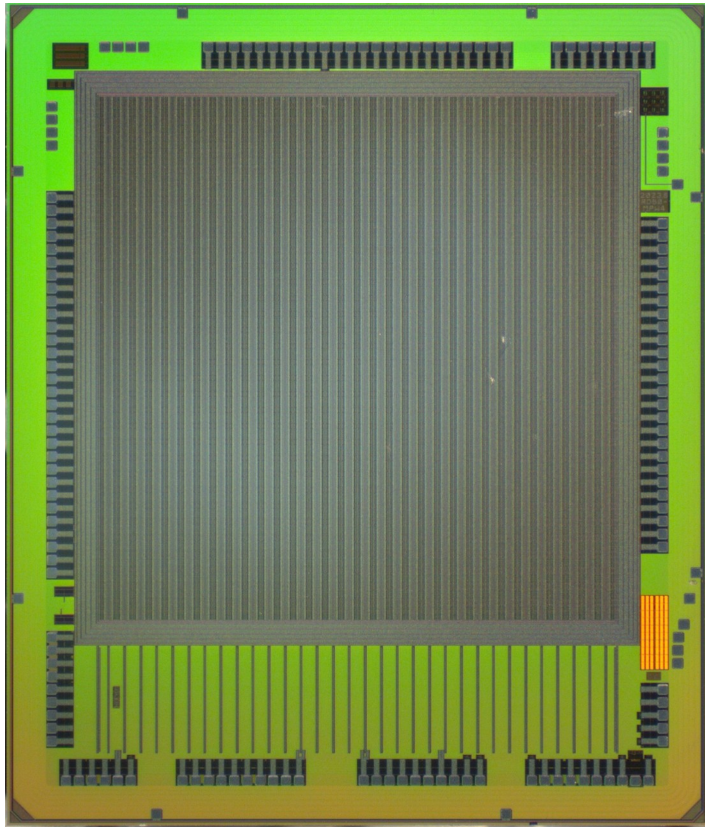
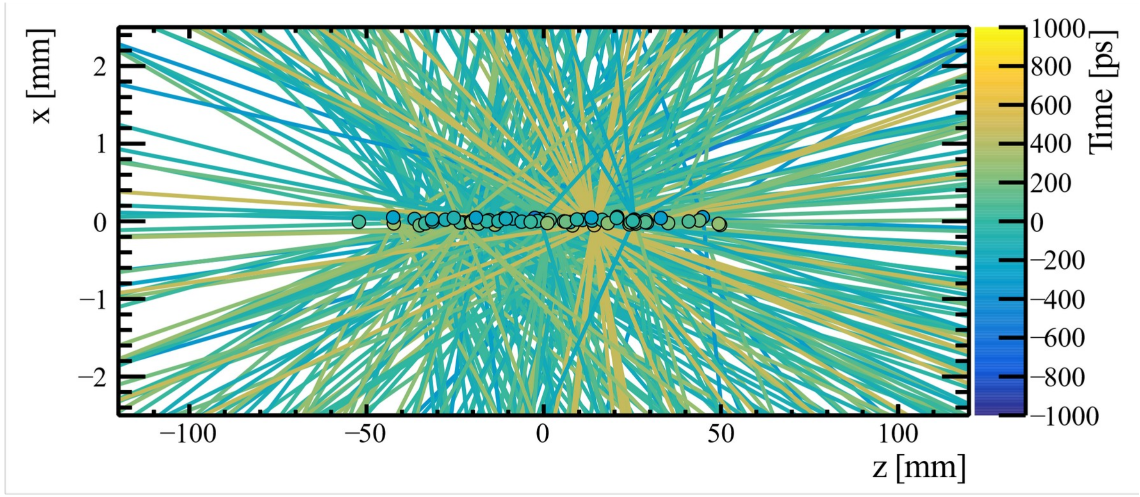
Timing performance of the RD50-MPW4





A short, why timing?

- Next future accelerator is the High-Luminosity upgrade of the LHC
  - More collisions per interaction window
  - Higher track densities
  - Higher amounts of radiation
- Track time resolution ~30 ps can resolve many of these issues → 4D Tracking



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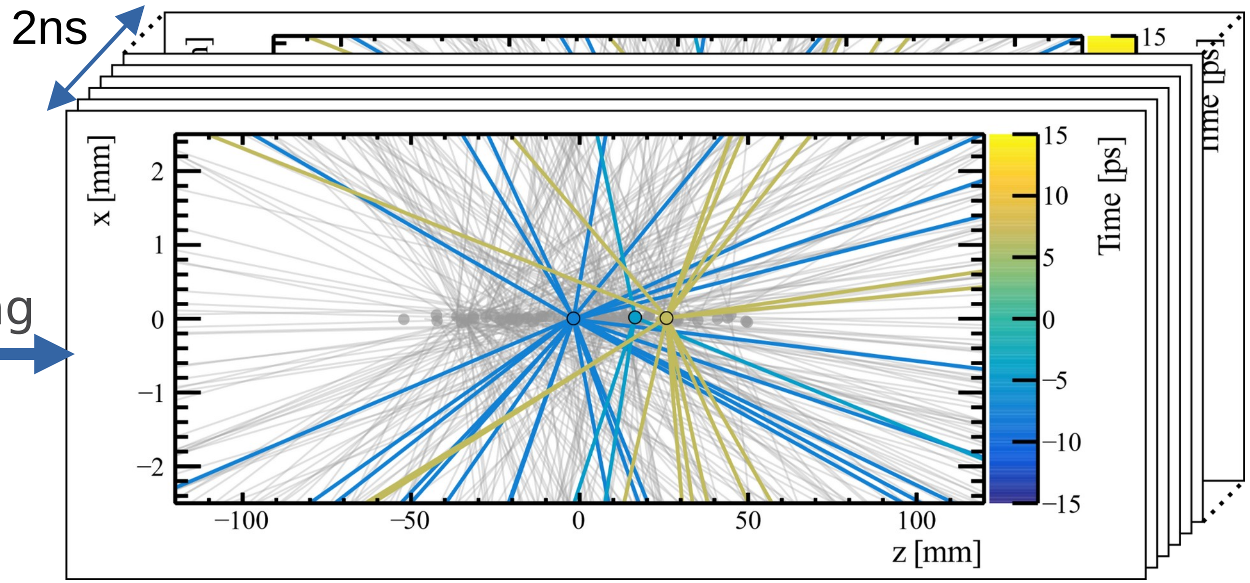
Timing



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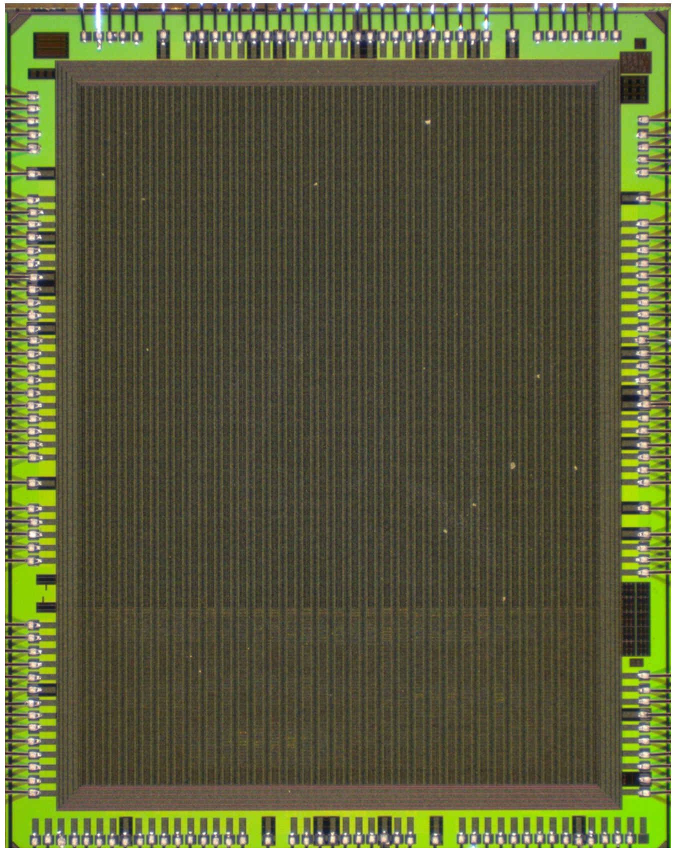
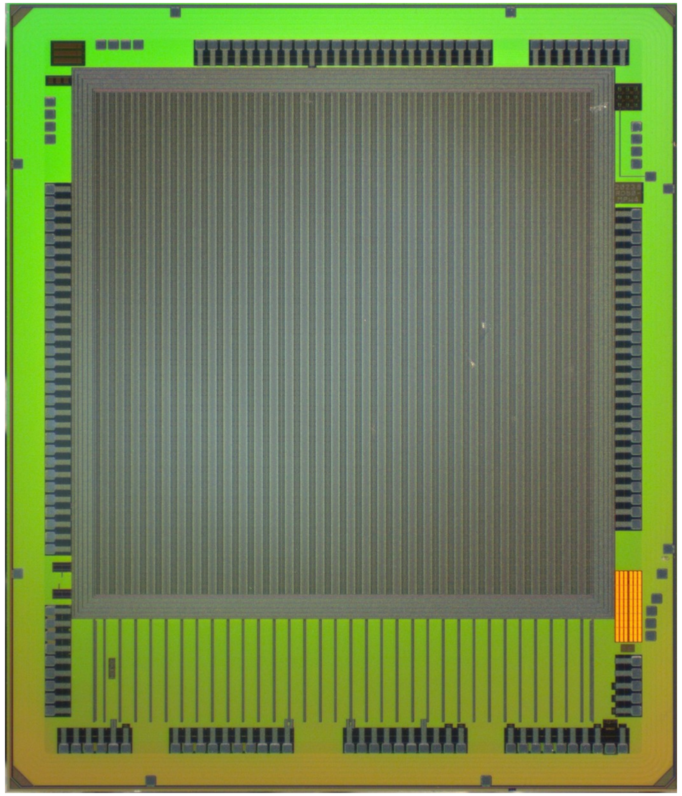
MPW3 and MPW4

- Investigated both MPW3 and MPW4
  - MWP4 not available when Thijs started
  - Wished to investigate differences between the two
- Select MPW3 results are in backup as they are not as relevant for this talk
- All MPW4 results are based on the topside biasable version
- Time with MPW4 was limited for Thijs.

MPW3
(Sep.2023-Jan.2024)



MPW4
(Jan.2024-Mar.2024)



MPW3 (@13000e-)

- Strong difference between clock on and off
  - Larger variance in ToT
    - Worse charge calibration
  - Larger variance in ToA
    - Worse time resolution

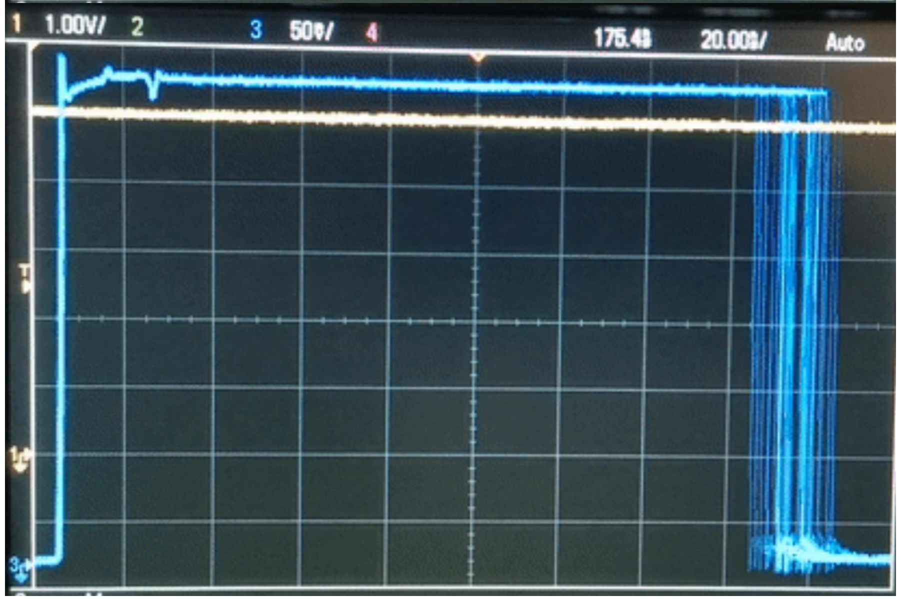
$$\sigma_t = \sqrt{\mathrm{var(ToA)}}$$

    - Clock on = ~2 ns
    - Clock off = ~293 ps

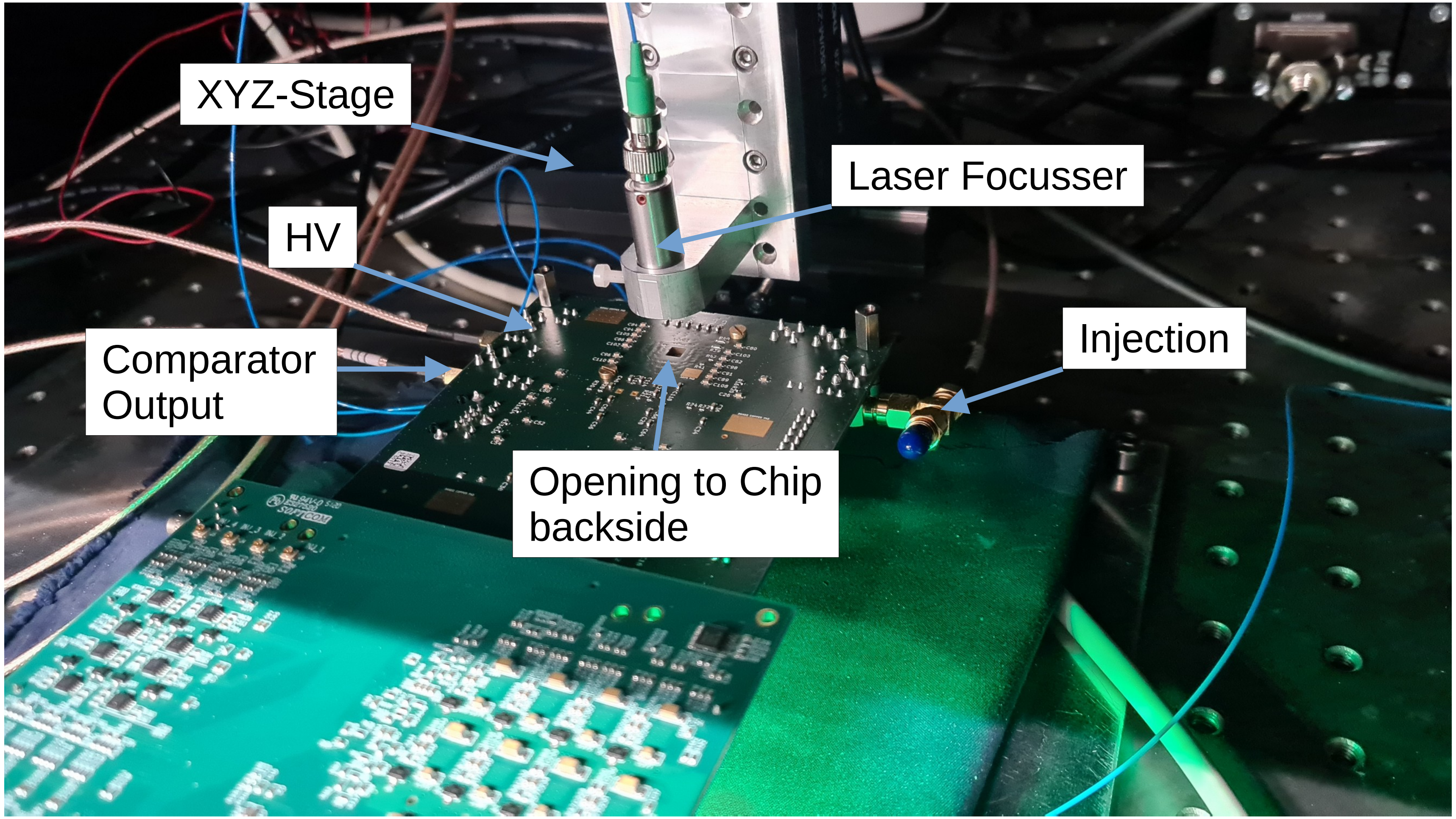
- Investigated whether issue is present still in MPW4

Clock On

Clock Off

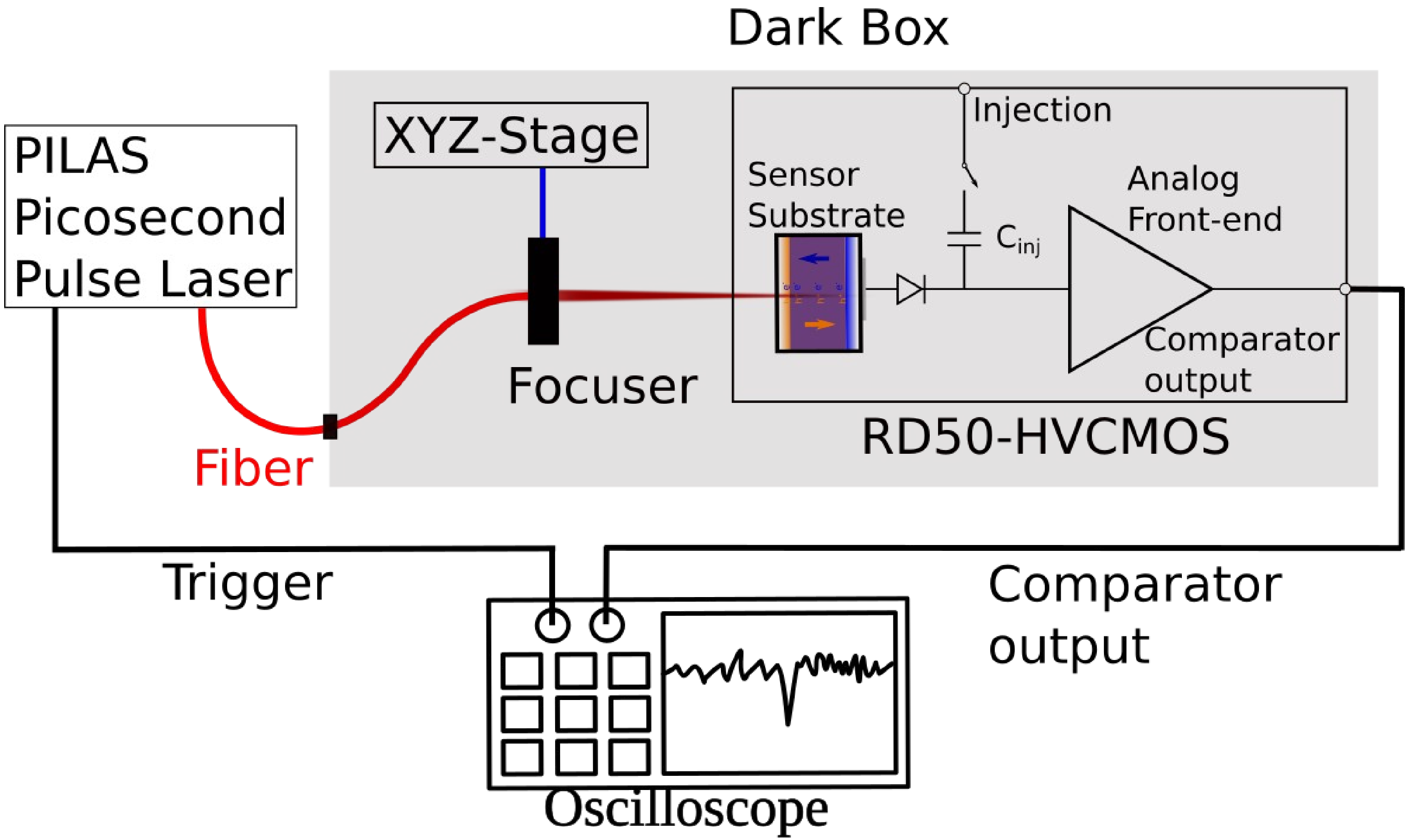


Measurement Setup at Nikhef



Measurement Setup at Nikhef

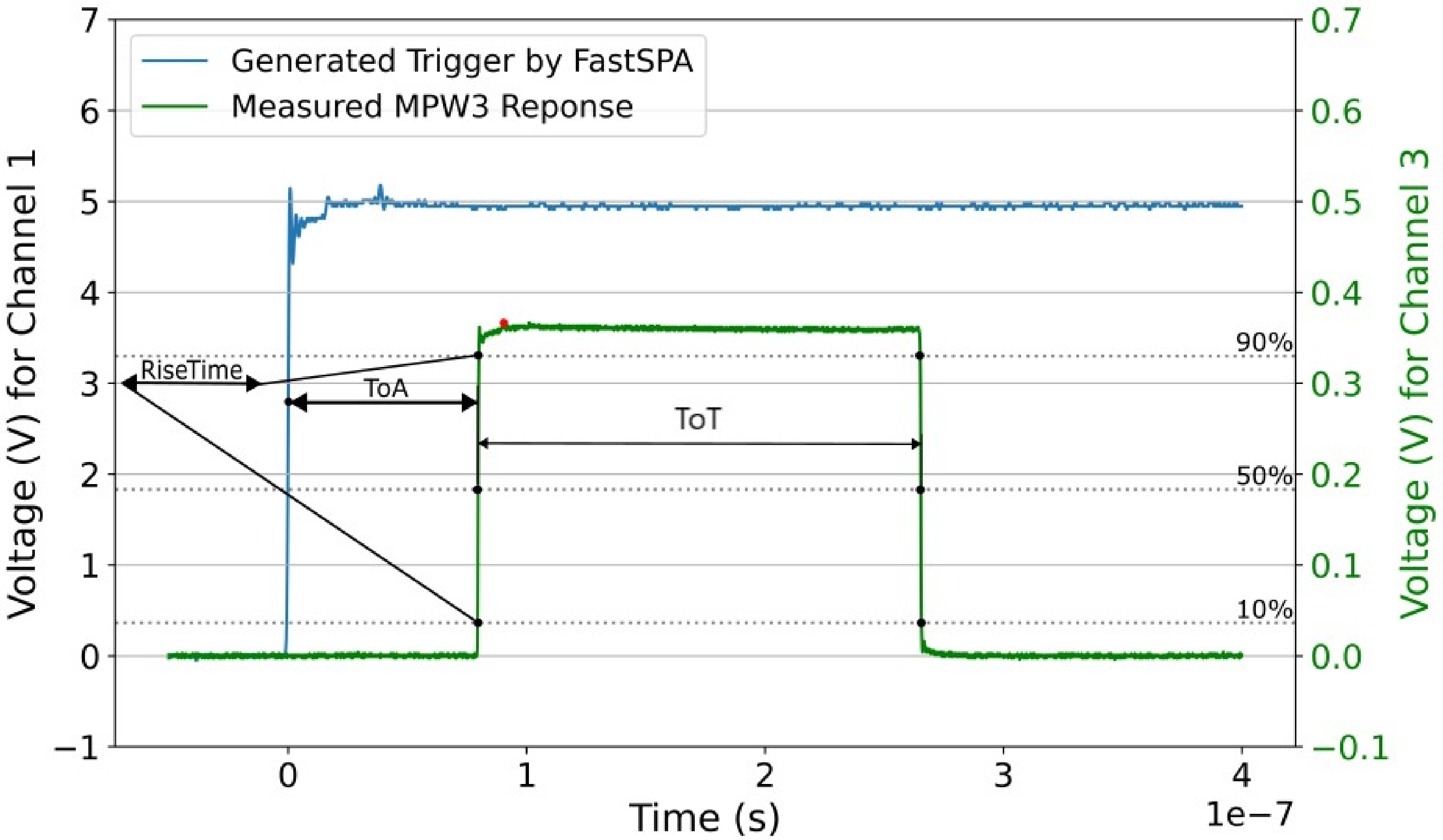
- CHECK THESE VALUES AGAIN
- PILAS picosecond pulse Laser (FastSPA)
  - 940 nm
  - t_{jitter} = ~1.9 ps
  - t_{rise} = ~35 ps
  - t_{pulse} = ~46 ps
  - E_{pulse} = ~5 pJ
  - f_{pulse} = 40 MHz



What we measure

- Mainly interested in timing performance of HV-CMOS technology
  - Analog only
  - Read out using Scope Ifiniium MXR604A
    6 GHz, 16 Gsa/s, 10 bit
- $t_{rise} = t_{rise\text{-}MPW\text{-}90\%} - t_{rise\text{-}MPW\text{-}10\%}$
- $ToT = t_{fall\text{-}MPW\text{-}50\%} - t_{rise\text{-}MPW\text{-}50\%}$
- $ToA = t_{rise\text{-}MPW\text{-}50\%} - t_{rise\text{-}trig\text{-}50\%}$

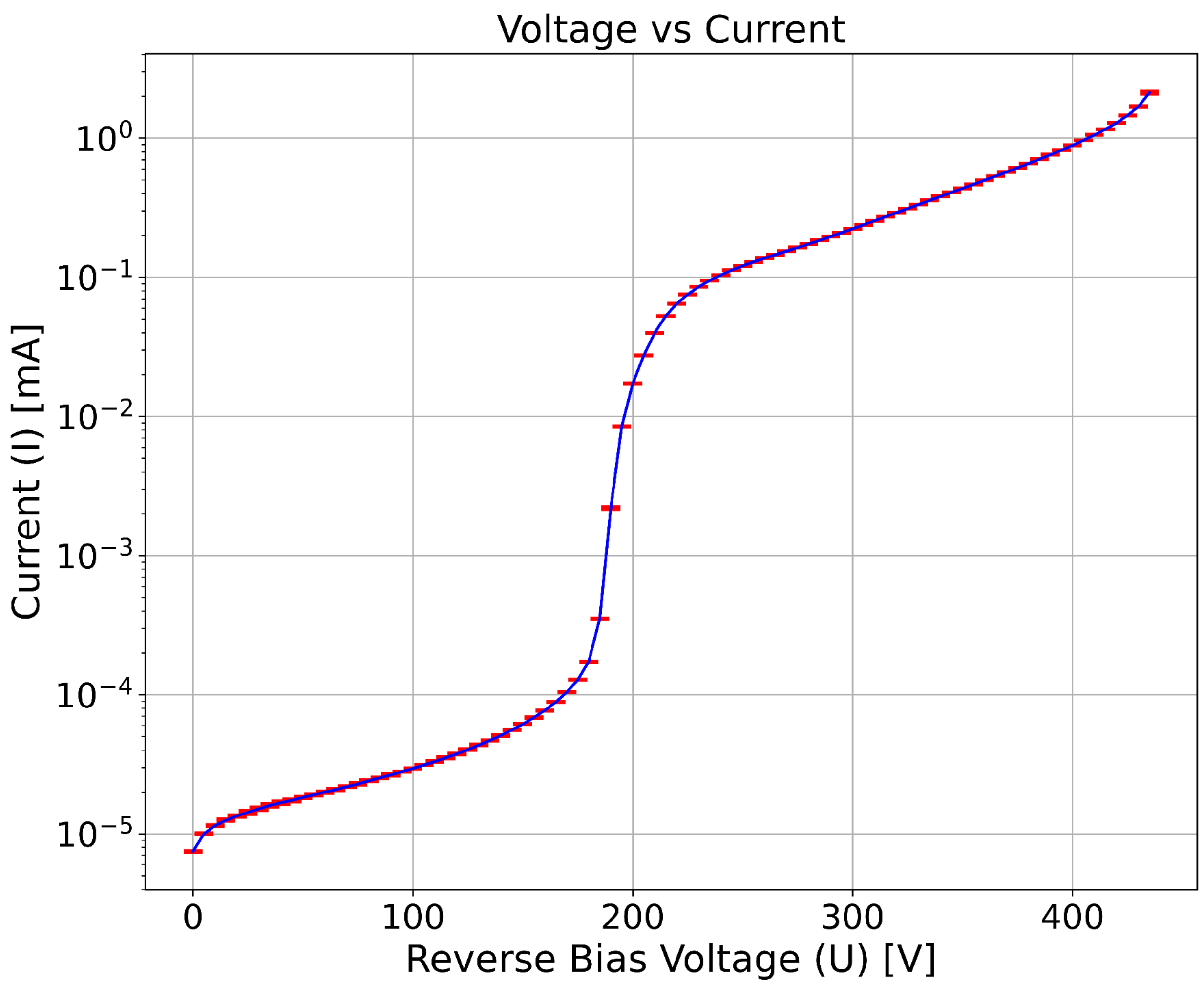
$$\sigma_t = \sqrt{\mathrm{var}(\mathrm{ToA})}$$



- Limited by unavailability of direct source follower output. (Need to test if Abuffout works as I hope)

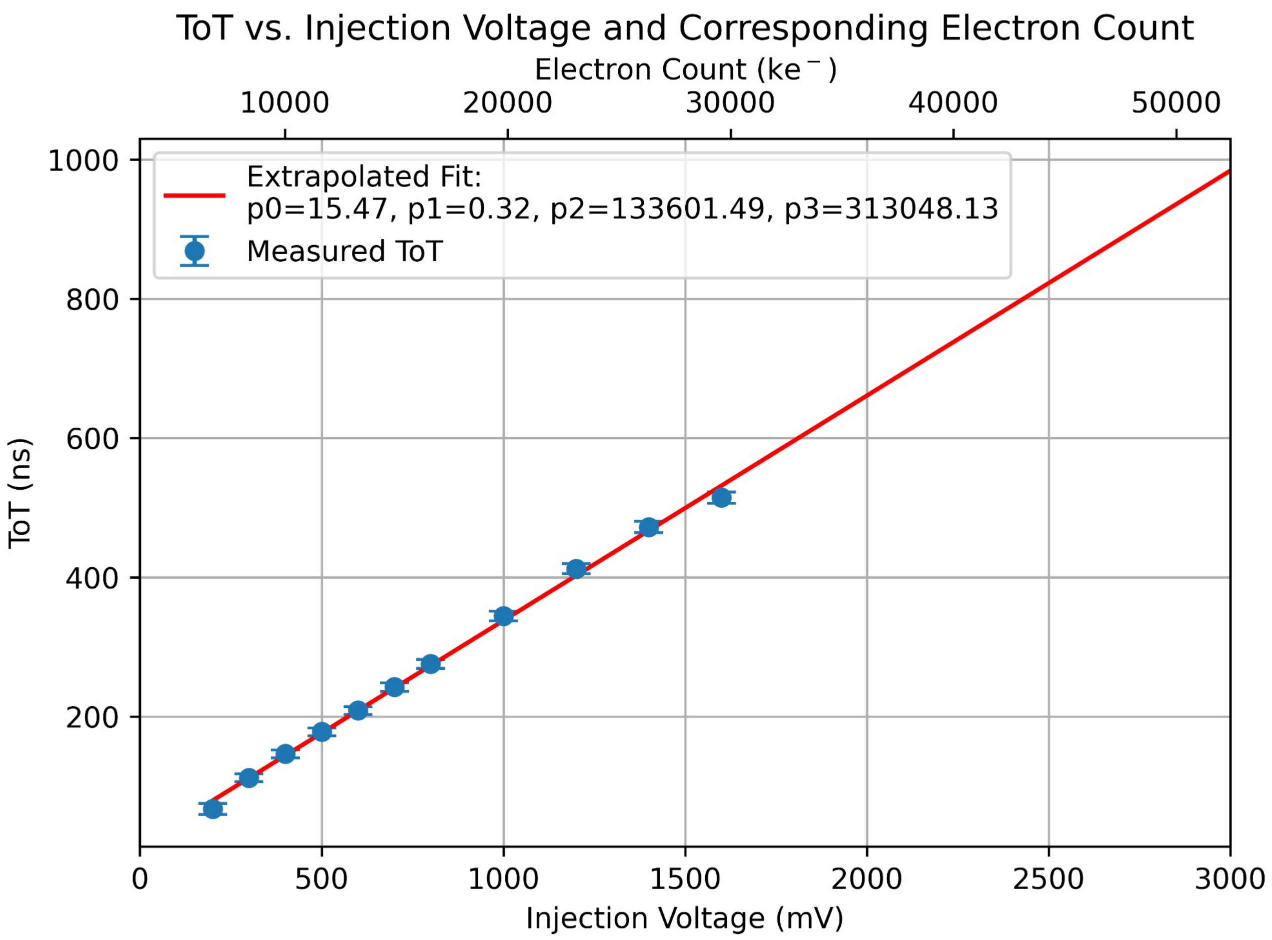
IV curve of MPW4 (topside, full chip)

- Biased MPW4 up to 500V
- Large increase in current at 200V could be due to reach of backside + backside defects
- True breakdown begins at around 500V



ToT to Charge Calibration (single pixel)

- Performed standard charge calibration using injection voltages
- Original plan was to perform this for all pixels, and scan in pixel effects.
- Limited time meant focus was shifted to comparison with MPW3 results concerning periphery noise with clock and and off

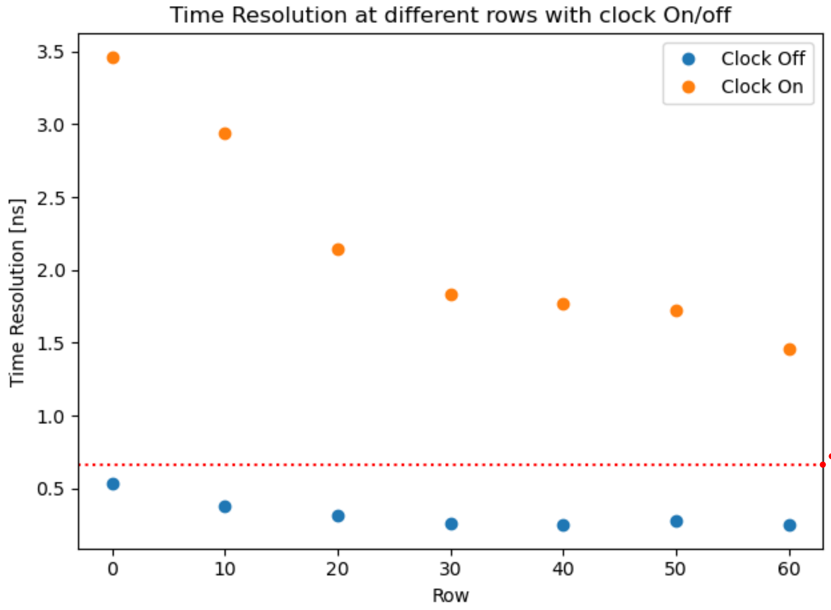


Time resolution MPW3 vs MPW4

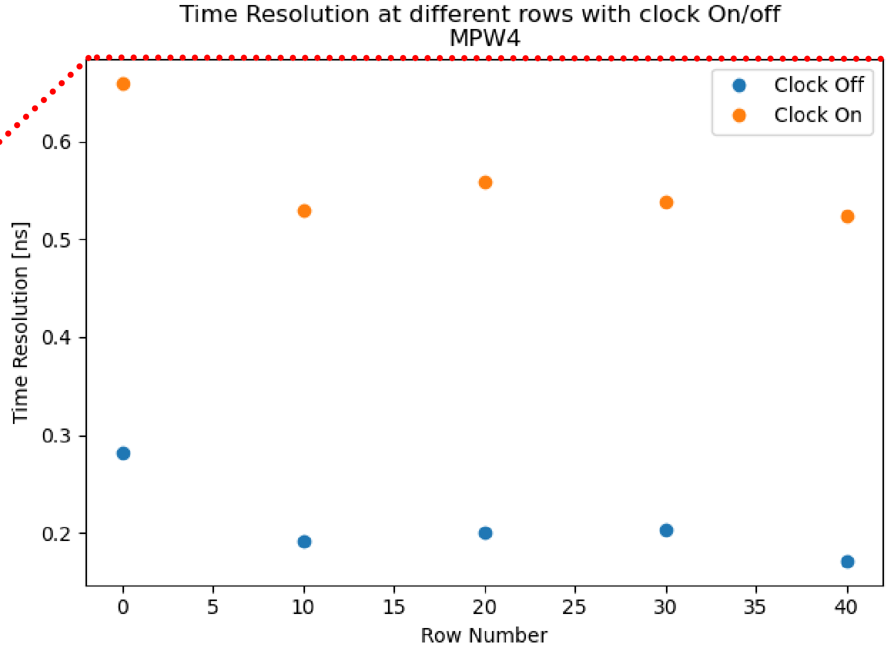
- Results are more qualitative (injected charge via laser differs)
- Overall time resolution for MPW4 is far better due to reduced noise in the periphery
- Clock effects are still present in the performance
- Some effect of closeness to periphery persists

$$\sigma_t \propto \frac{dV/dt}{\sqrt{S/N}}$$

MPW3



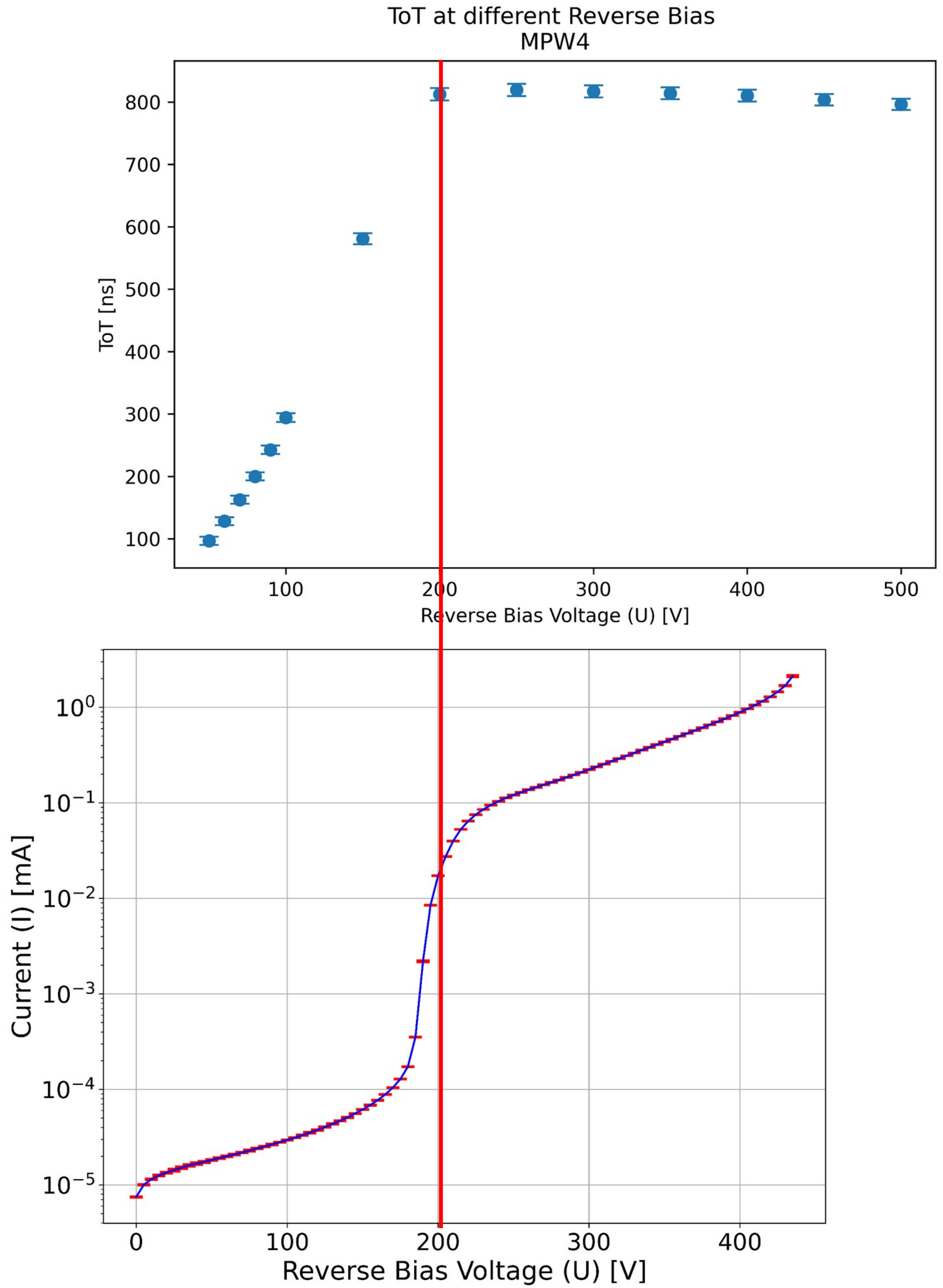
MPW4



Improving the Time Resolution

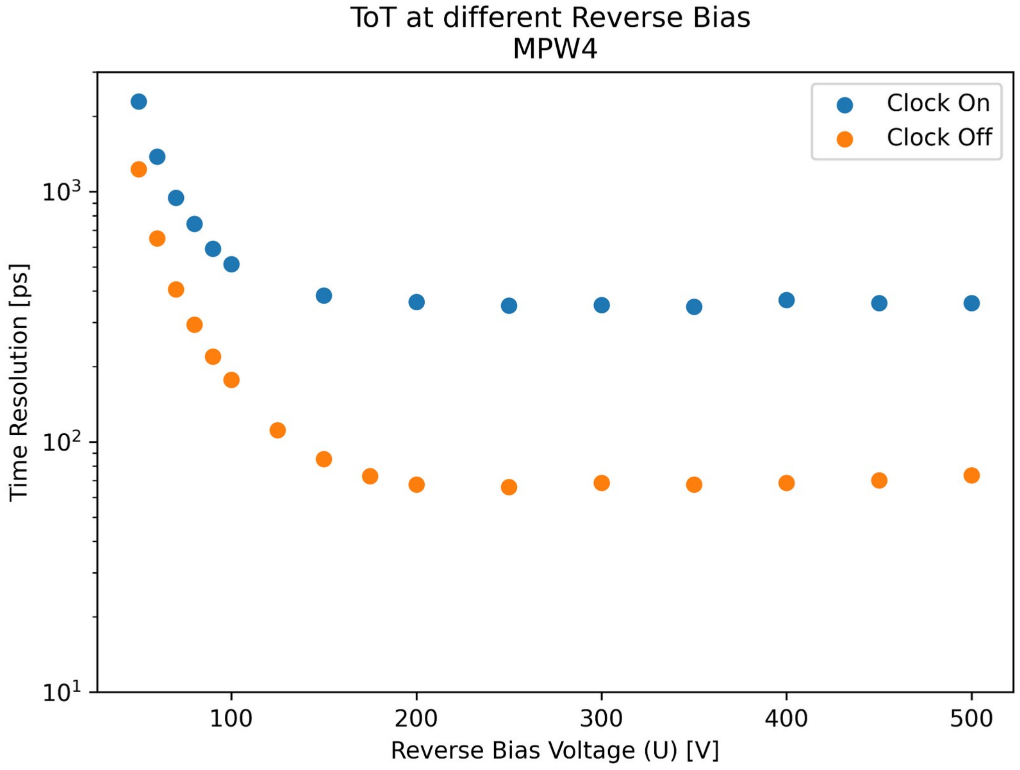
- Overdepletion increases electric field strength
  - → Faster charge collection
  - → Higher dV/dt
  - → Improves time resolution

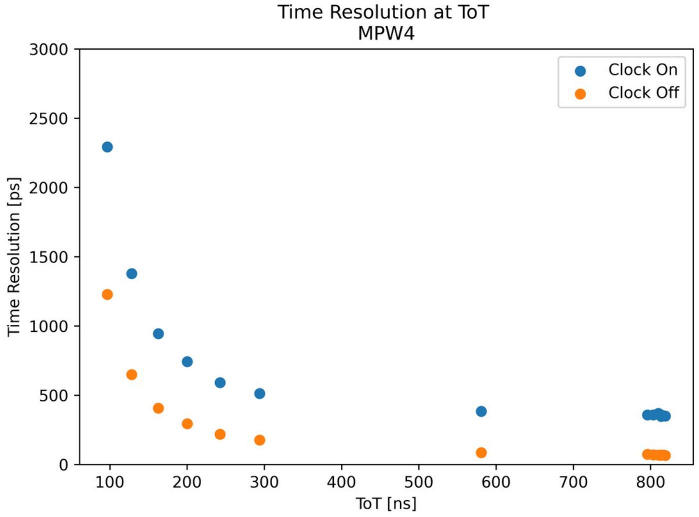
- ToT increase stops around 200V
- Similar to the the large increase of current
  - Further indicates reach of full depletion
  - → Any voltage above 200V should improve time resolution



Improving the Time Resolution

- Unfortunately charge injected was far beyond expected MIP (44000e-)
  - No time to repeat
- Mostly looking at trends
- Time resolution improves up until 200V
  - Same as increase in measured charge
    → Result most likely just based on Timewalk
- No effect of overdepletion visible in the behavior





Conclusion

- The MPW4 is far better than its predecessor in terms of noise and time resolution
- Current iteration of chip can reach O(500/200 ps) analog time resolution (clock on/off)
- Still not insignificant noise present in the system when clock is active

Outlook

- Possible that improvement of time resolution with higher bias was not visible due to limitation from the Amplifier (low Bandwidth?)
- Amplifier current DAC was already set to one of the highest values as far as I remember.

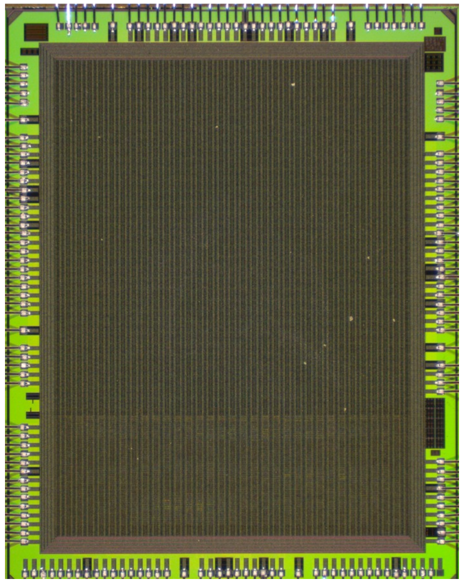
- Do not expect to see any differences in in-pixel relative to MPW2 outside of the matrix border.
- Interested to investigate differences in measured charge, noise and time resolution both over the row and in-pixel for irradiated vs non-irradiated sensors. (requires a new student)

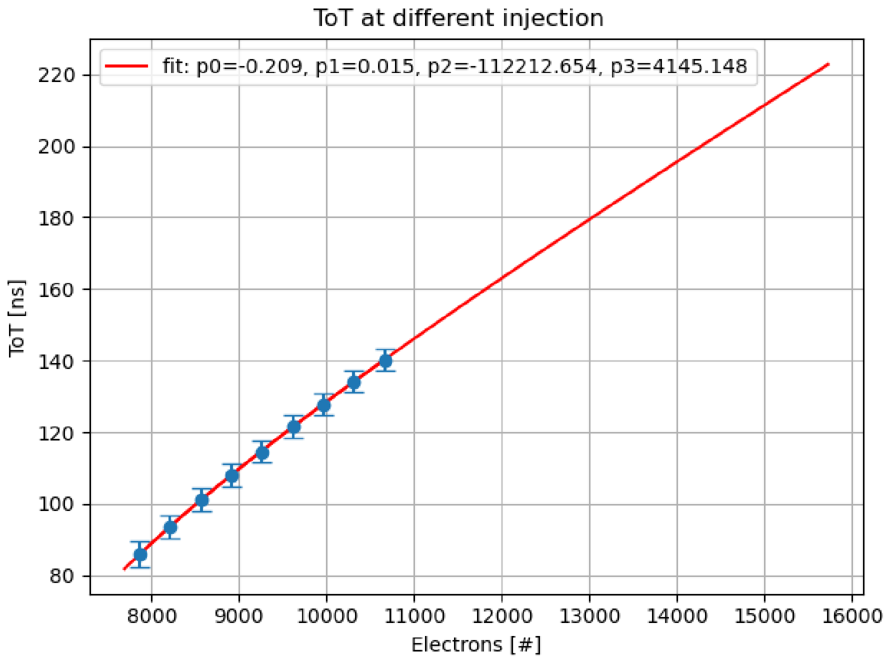
- For more detailed investigation into advantages of HV-CMOS relative to HR-CMOS in terms of 4D-tracking, access to analog signals, timing optimized front-end (larger amplifier current range) and possible investigations into variations of the well layouting would be of interest.

BACKUP
(MPW3+ Super Simple Timing)

MPW3 results

- MPW3 was measured at
  - 100V bias
  - Standard DAC values
  - Clock on and clock off
- What was measured
  - Analog only
  - Charge calibration of pixels using charge injection via pulse generator
  - Time resolution
  - Row dependence of results



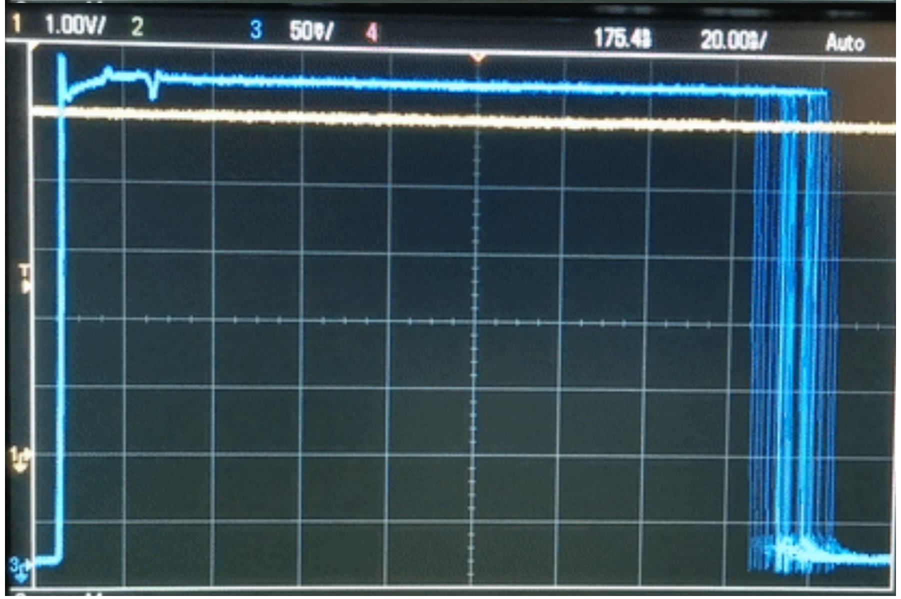


MPW3 (@13000e-)

- Strong difference between clock on and off

Clock On

Clock Off

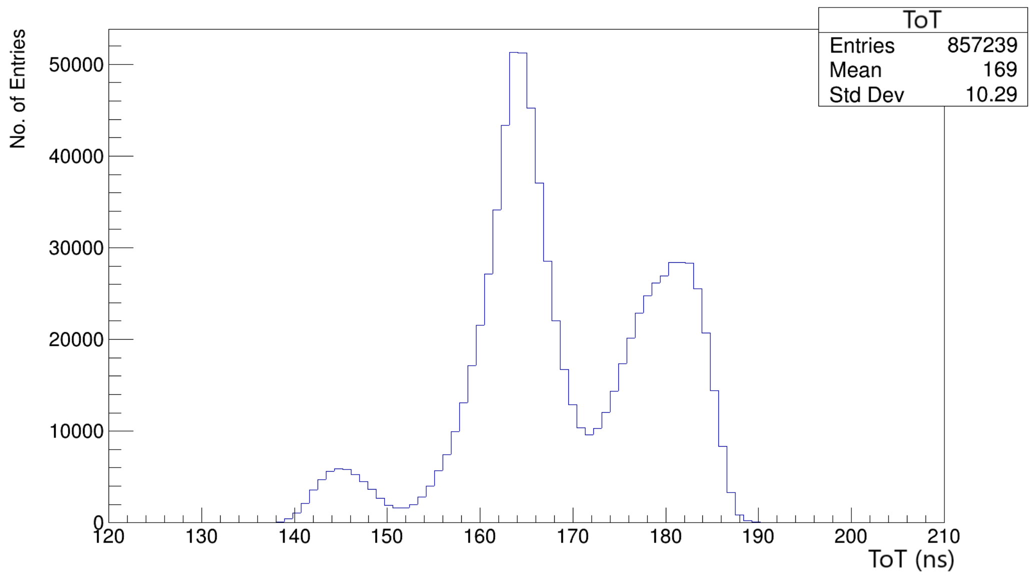


MPW3 (@13000e-)

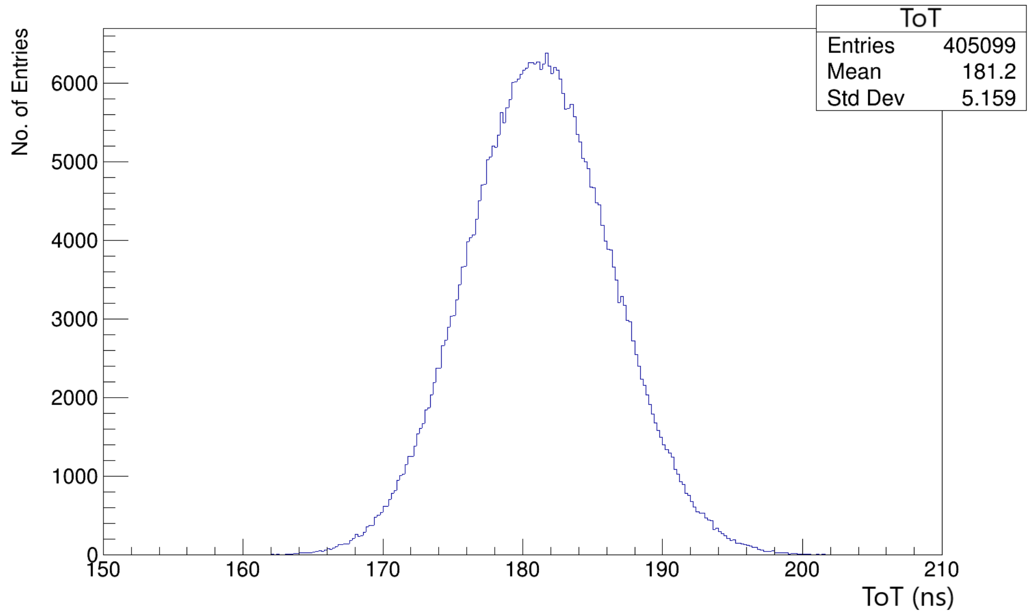
- Strong difference between clock on and off
  - Larger variance in ToT
    - Worse charge calibration

ToT

Clock On



Clock Off

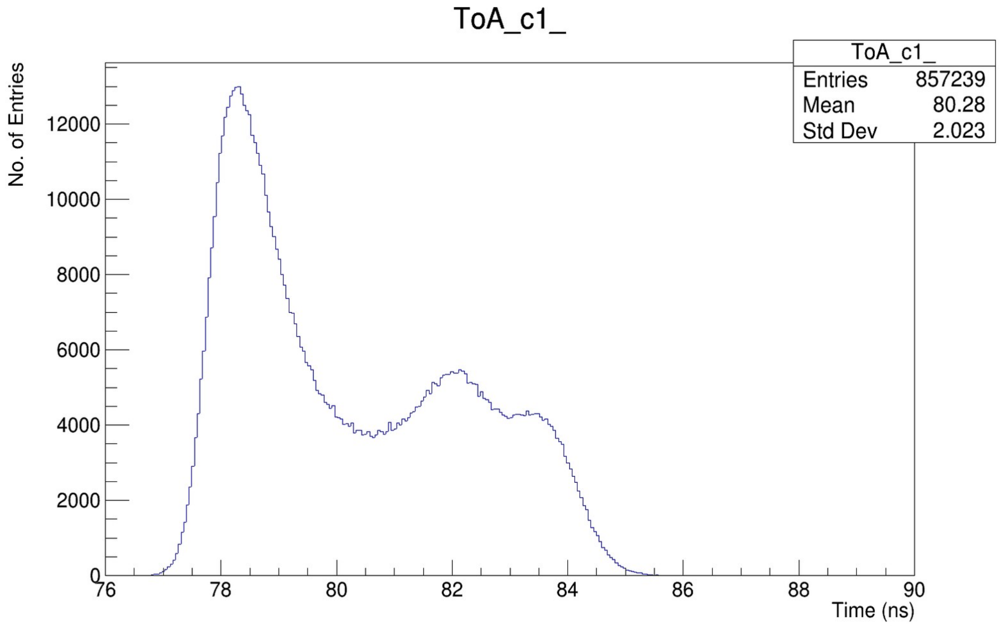


MPW3 (@13000e-)

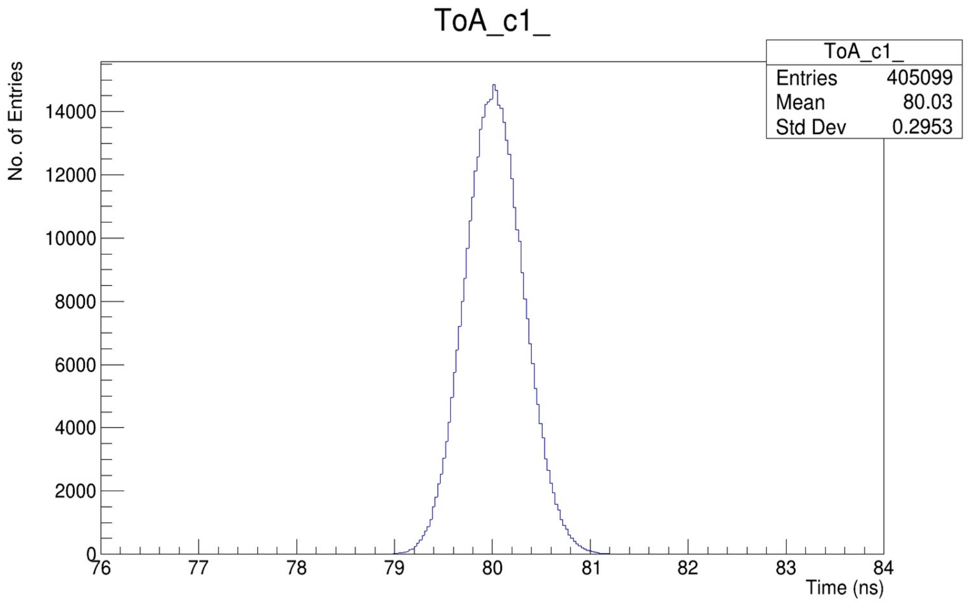
- Strong difference between clock on and off
  - Larger variance in ToT
    - Worse charge calibration
  - Larger variance in ToA
    - Worse time resolution

$$\sigma_t = \sqrt{\mathrm{var}(\mathrm{ToA})}$$

Clock On



Clock Off



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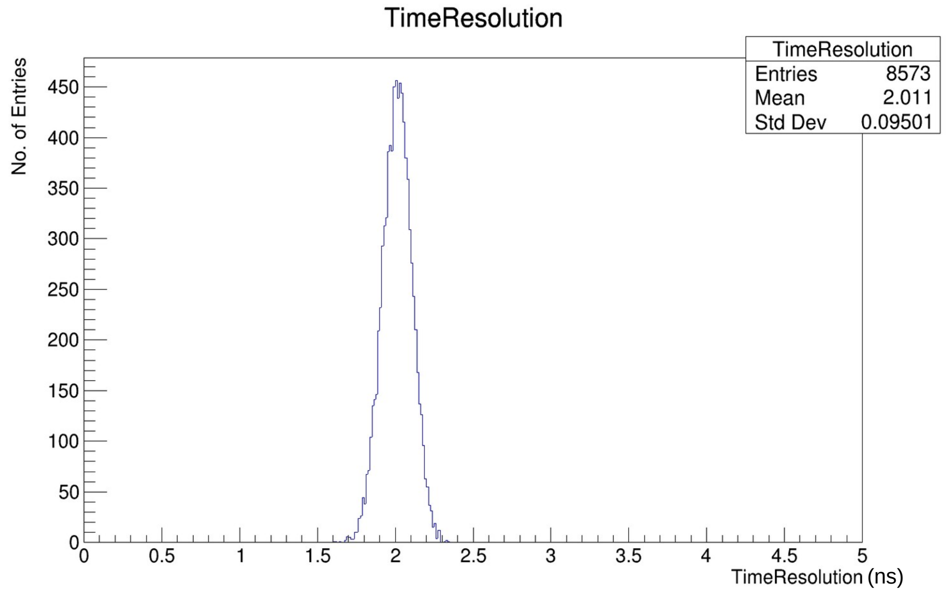
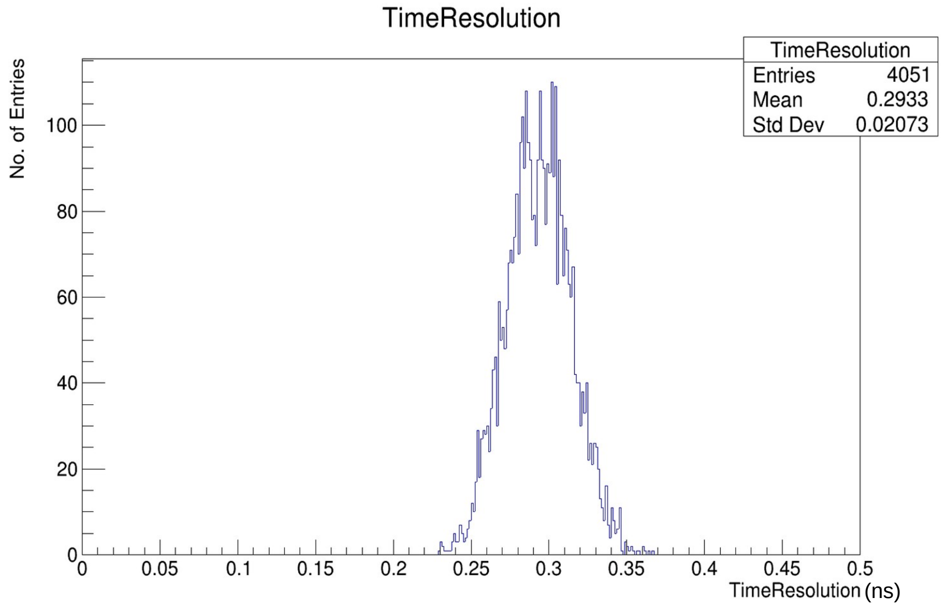
$$\sigma_t = \sqrt{\mathrm{var}(\mathrm{ToA})}$$

    - Clock on = ~2 ns
    - Clock off = ~293 ps

Clock On

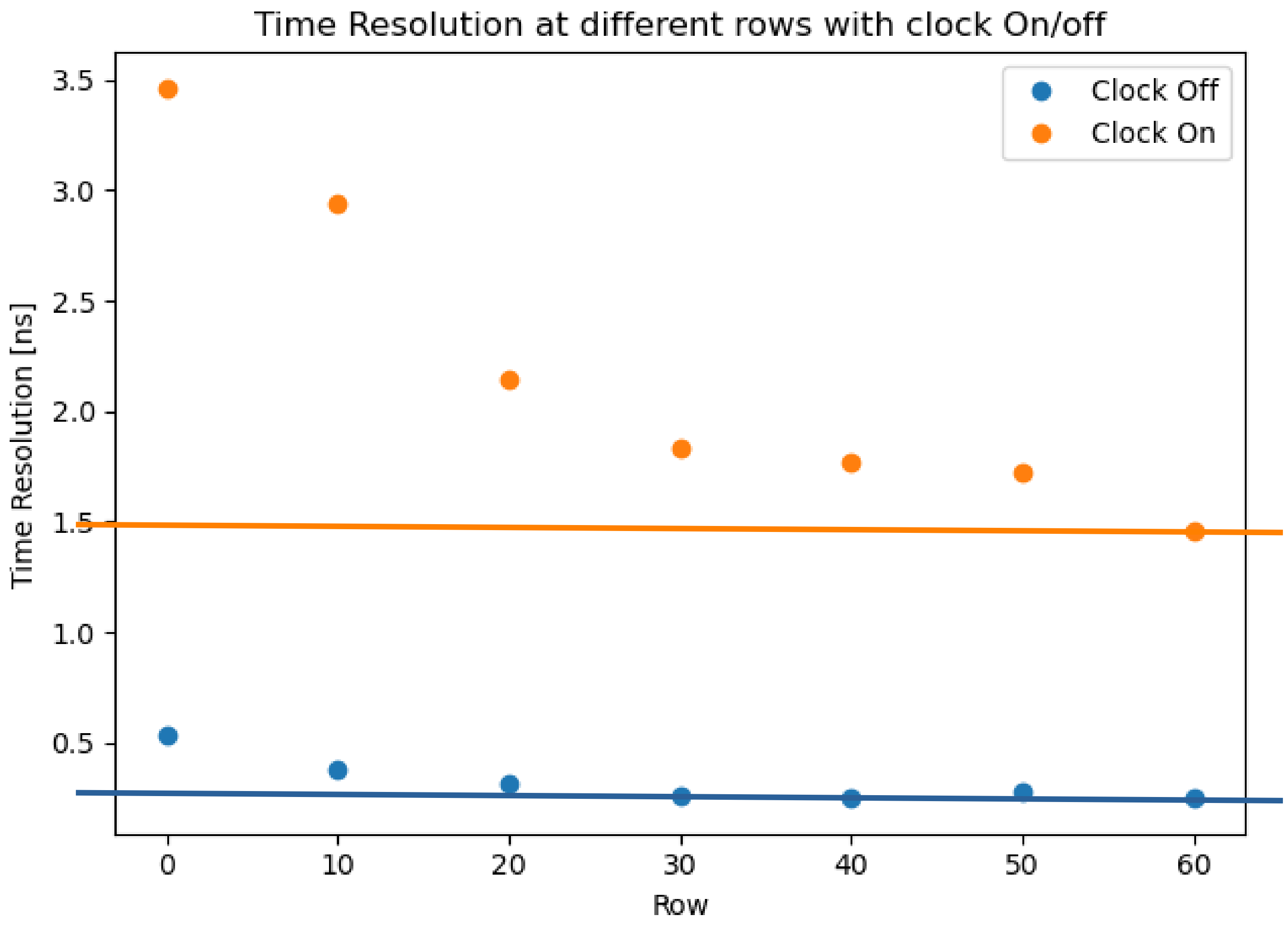


Clock Off



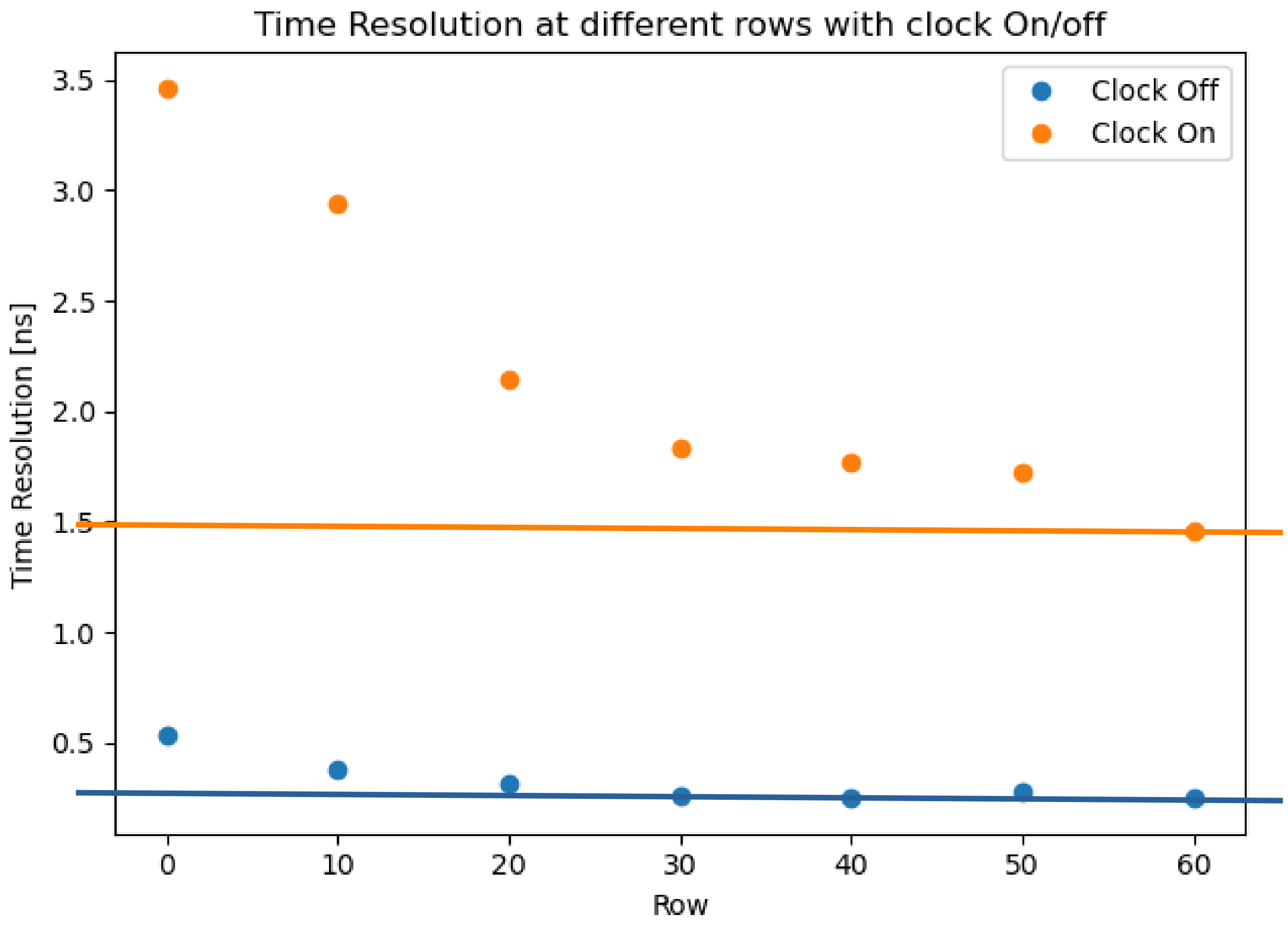
MPW3 for different row values

- Investigated row dependence due to closeness to periphery
- Closer to periphery = Worse time resolution
  - Present in both with and without clock
  - Far stronger with clock on



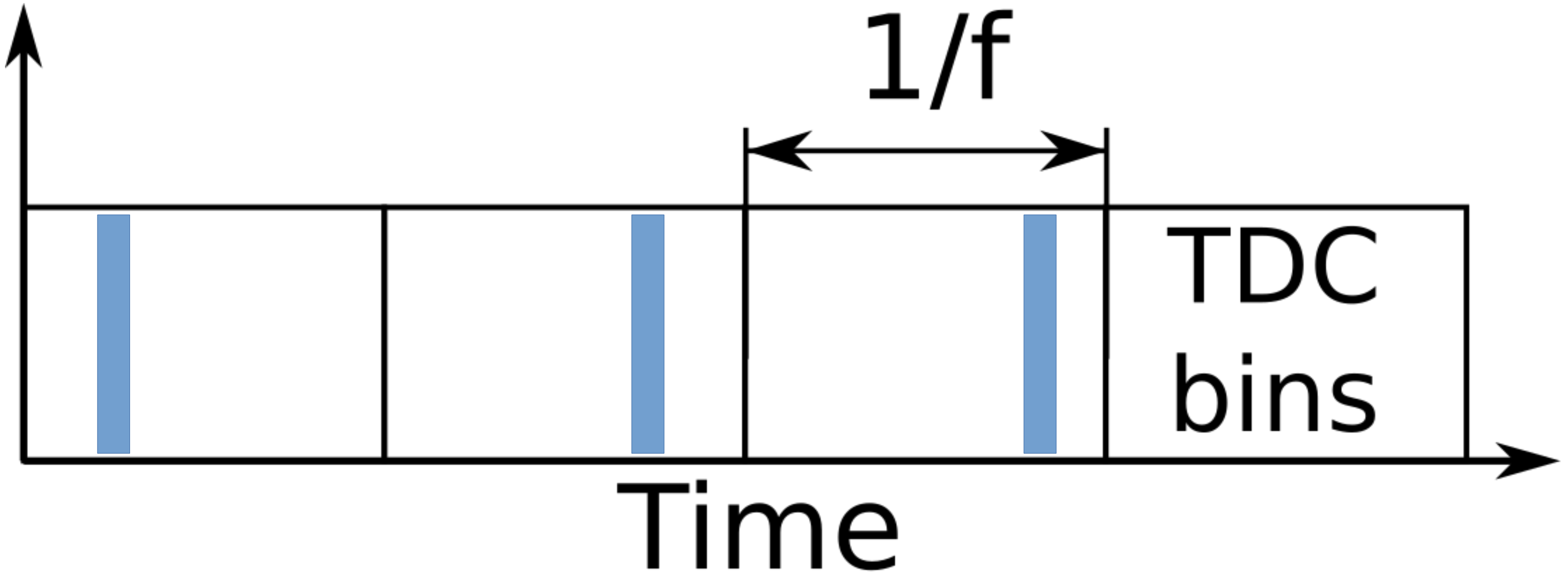
MPW4 for different row values

- Investigated row dependence due to closeness to periphery
- Closer to periphery = Worse time resolution
  - Present in both with and without clock
  - Far stronger with clock on



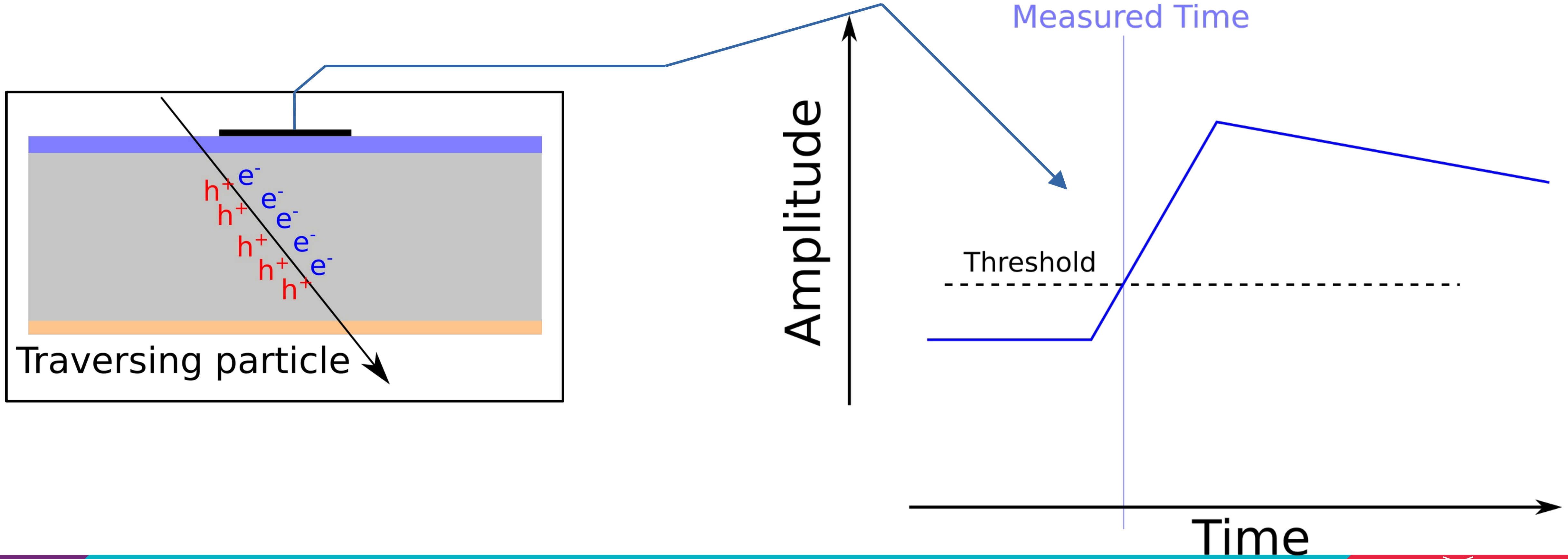
Contributions to time resolution

$$\sigma_t^2 = \sigma_{\text{clock-global}}^2 + \sigma_{\text{clock-on-chip}}^2 + \sigma_{TDC}^2 + \ldots$$



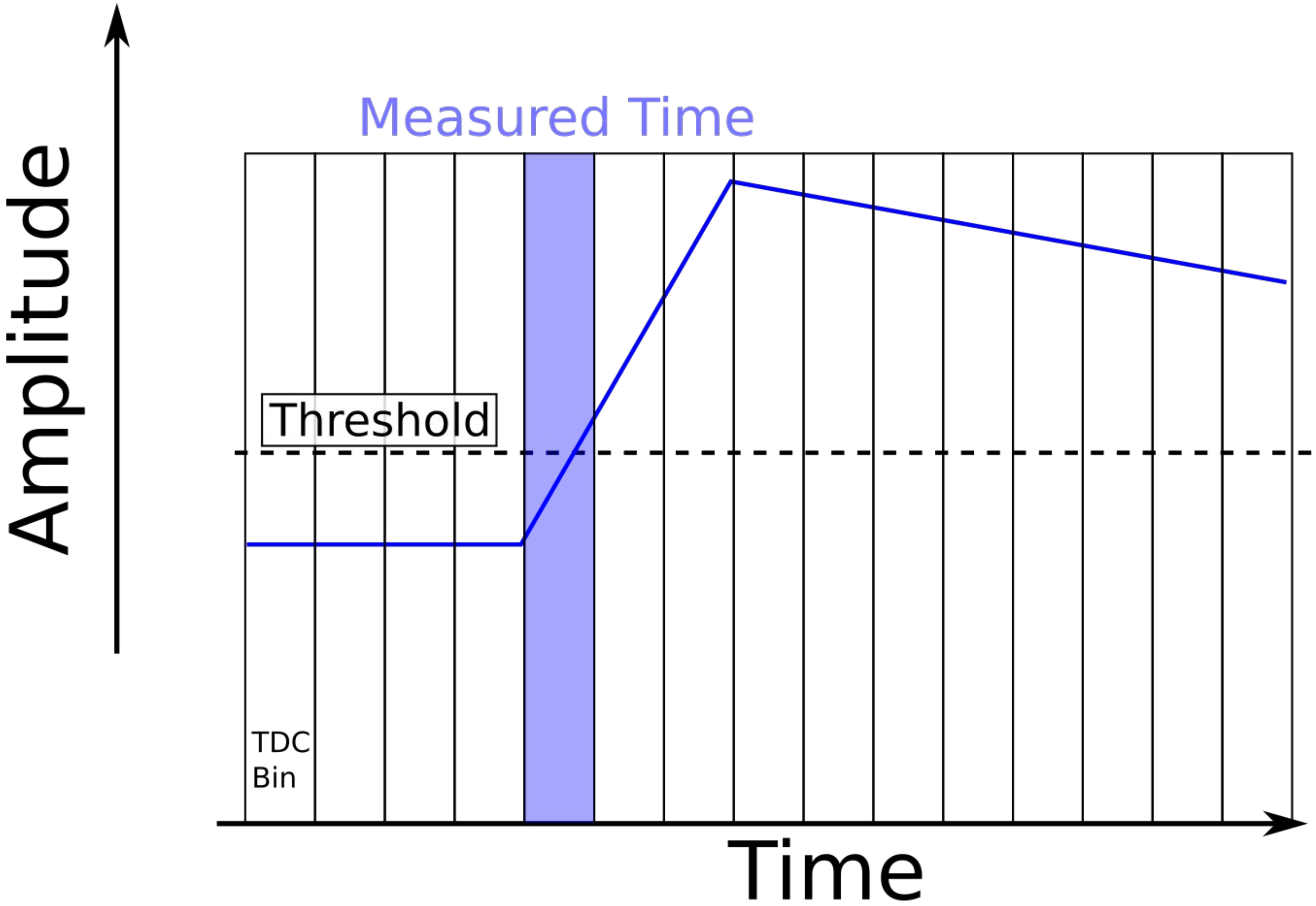
What is actually measured

- Measured is the time when a gathered charge signal crosses a threshold



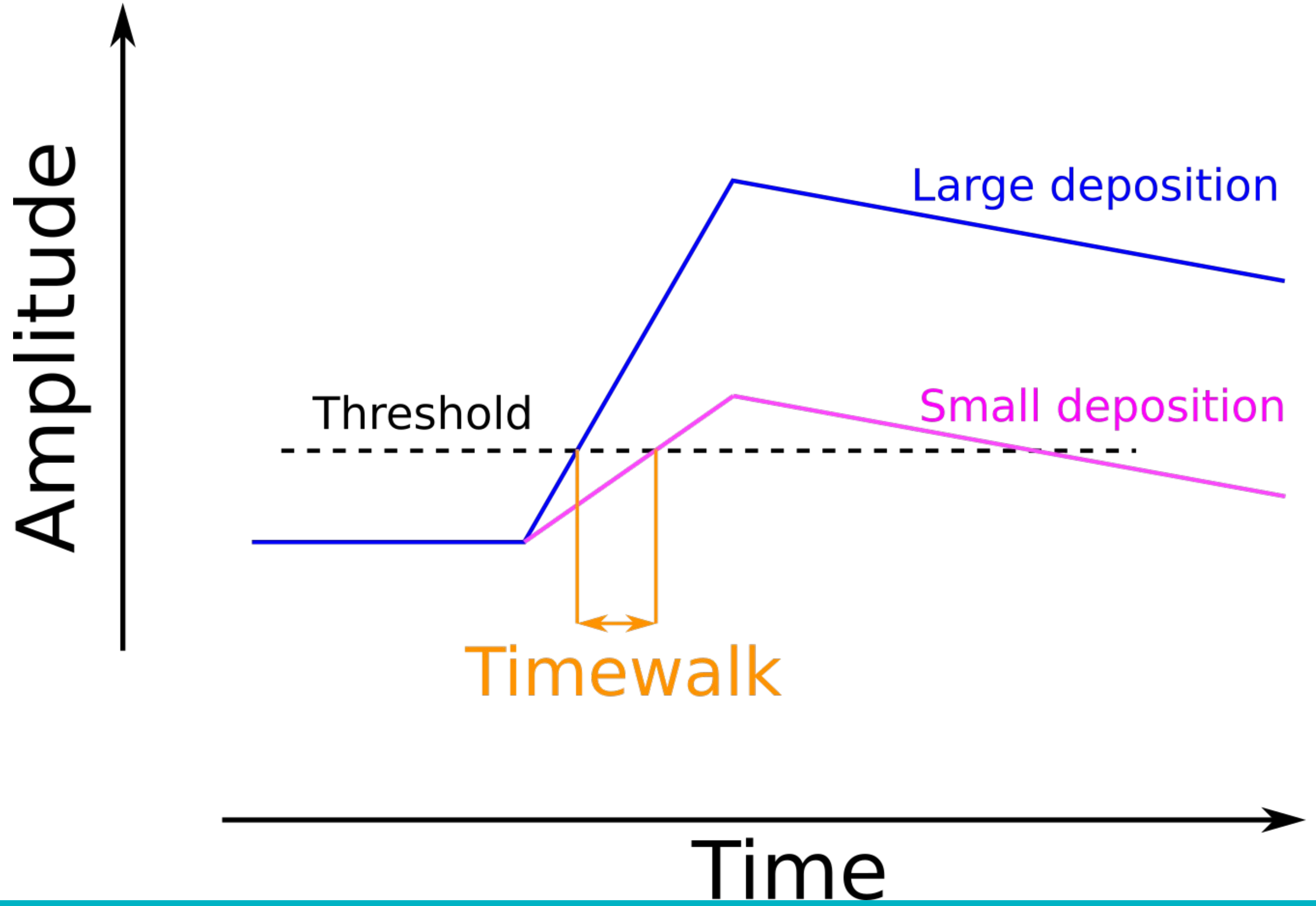
Contributions to time resolution

$$\sigma_t^2 = \sigma_{clock\text{-}global}^2 + \sigma_{clock\text{-}on\text{-}chip}^2 + \sigma_{TDC}^2 + \ldots$$



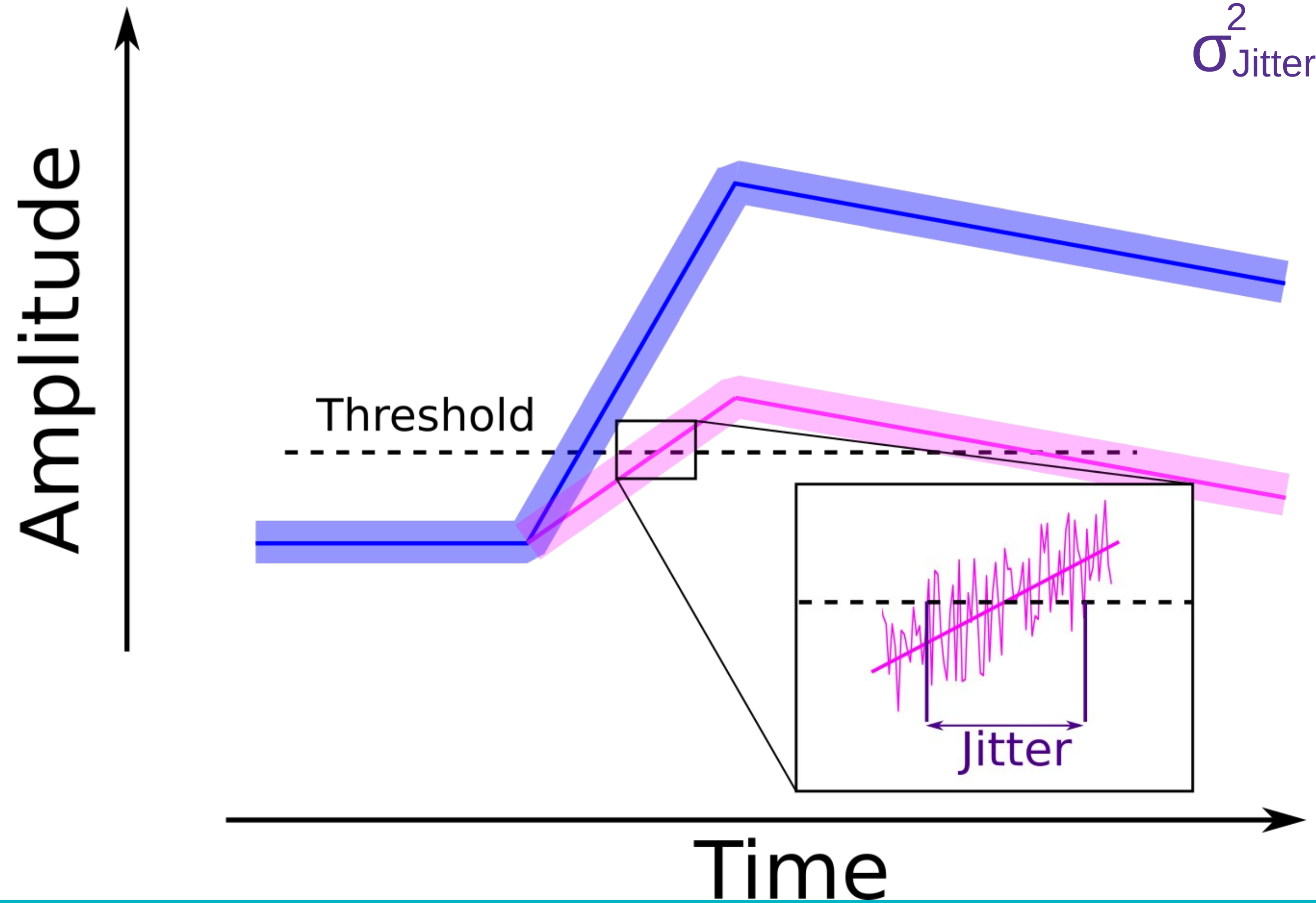
Contributions to time resolution

$$\sigma_t^2 = \sigma_{clock\text{-}global}^2 + \sigma_{clock\text{-}on\text{-}chip}^2 + \sigma_{TDC}^2 + \sigma_{Timewalk}^2 + \ldots$$



Contributions to time resolution

$$\sigma_t^2 = \sigma_{clock\text{-}global}^2 + \sigma_{clock\text{-}on\text{-}chip}^2 + \sigma_{TDC}^2 + \sigma_{Timewalk}^2 + \underbrace{\sigma_{Landau}^2 + \sigma_{Front\text{-}end}^2}_{\sigma_{Jitter}^2}$$



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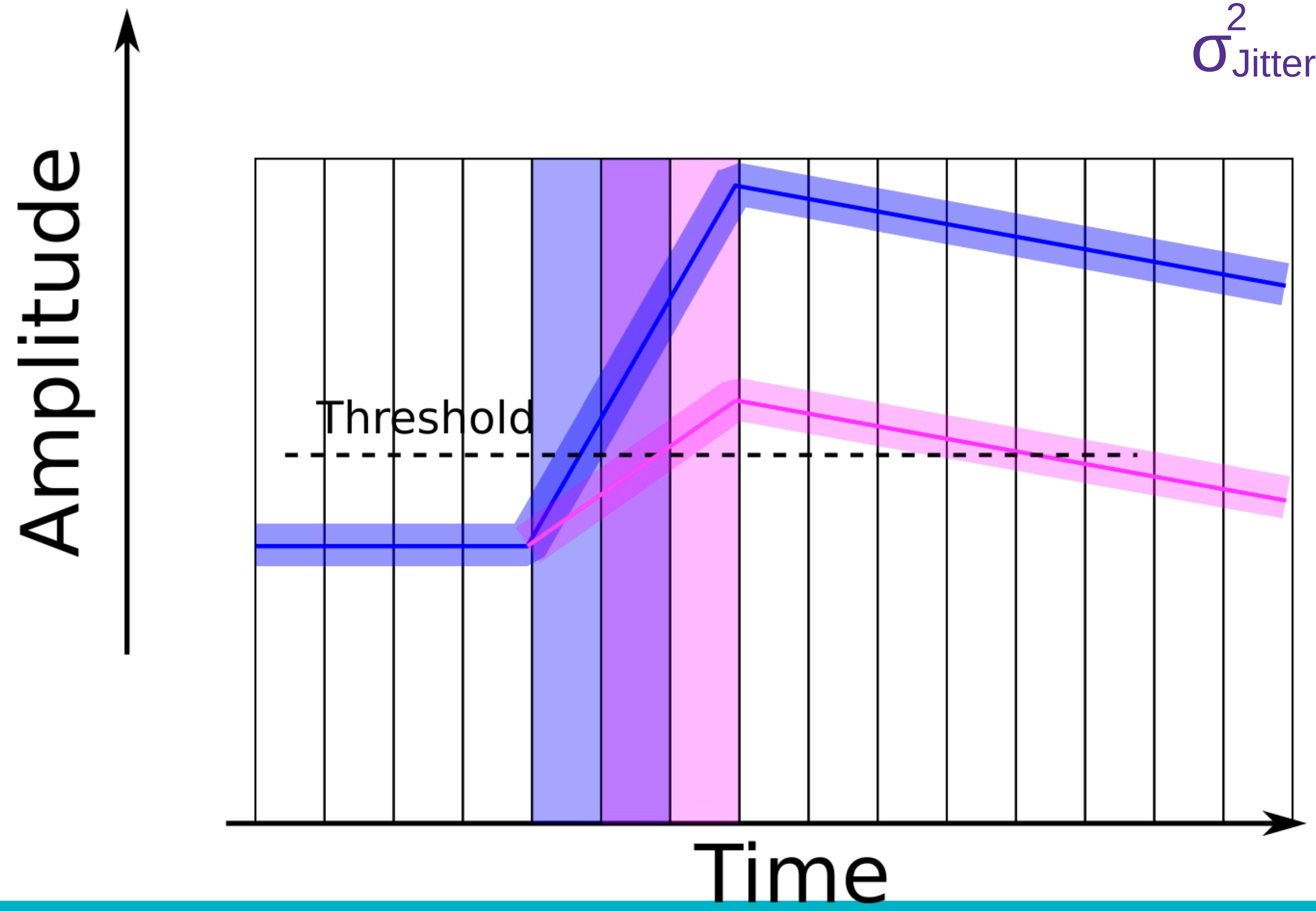
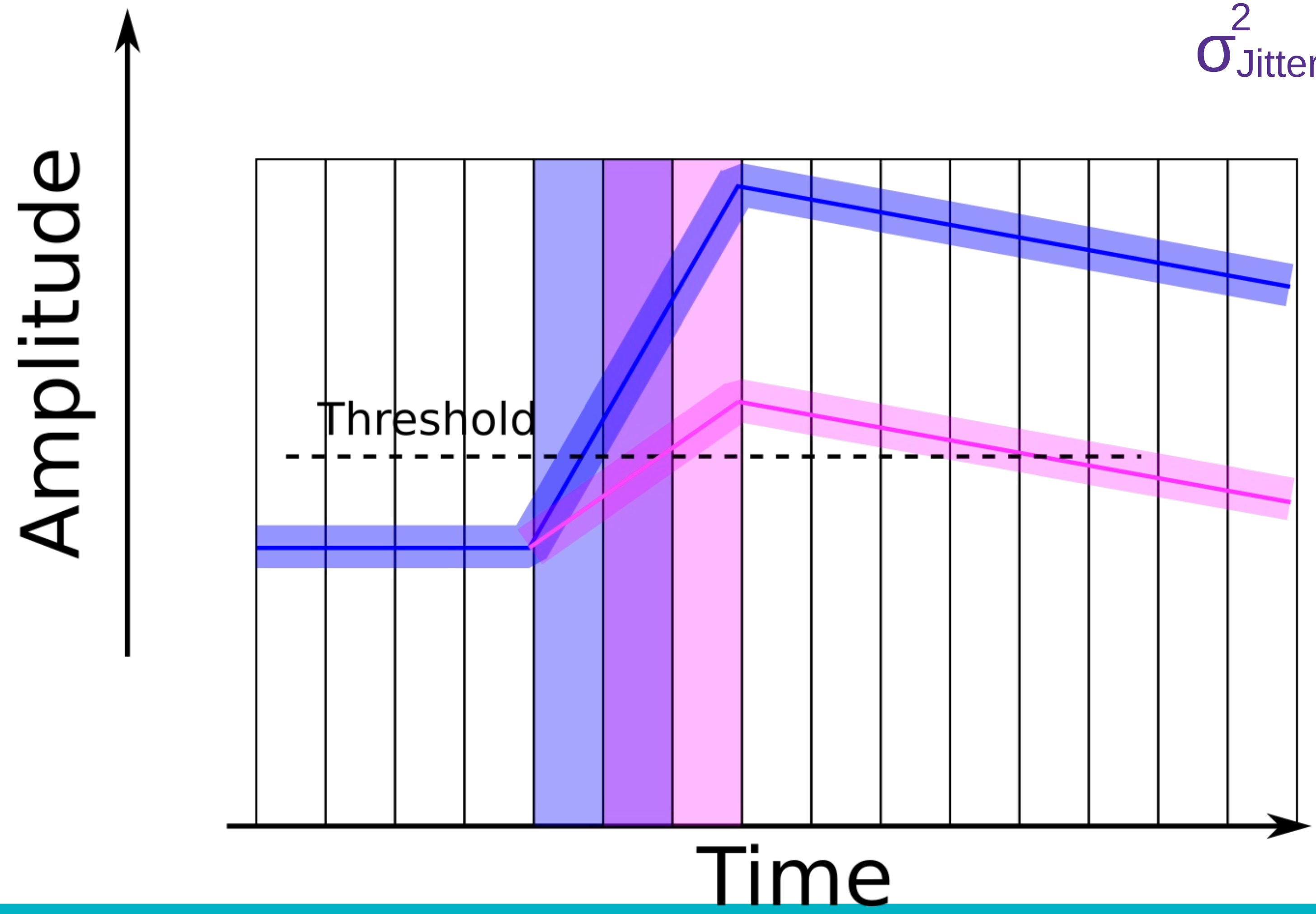


Contributions to time resolution

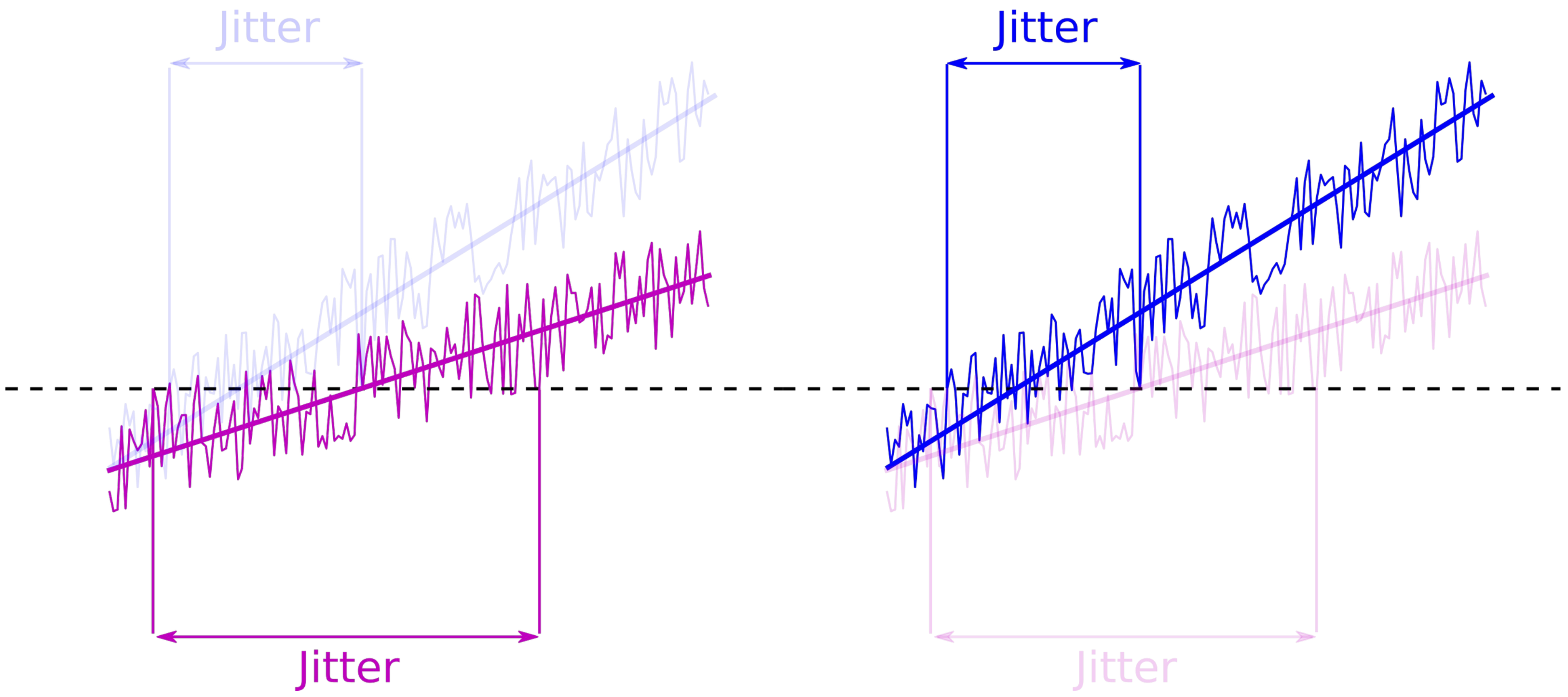
$$\sigma_t^2 = \sigma_{clock\text{-}global}^2 + \sigma_{clock\text{-}on\text{-}chip}^2 + \sigma_{TDC}^2 + \sigma_{Timewalk}^2 + \underbrace{\sigma_{Landau}^2 + \sigma_{Front\text{-}end}^2}_{\sigma_{Jitter}^2} (+ \sigma_{Pixel\text{-}to\text{-}Pixel}^2)$$

Removed through calibration, requires high statistics



Signal rise time

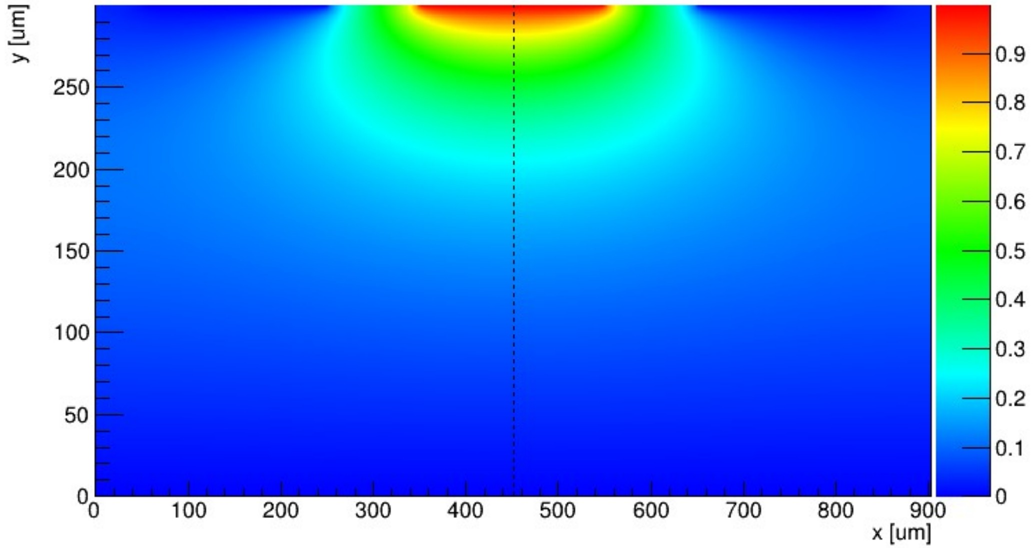
- Jitter depends on front-end noise and therefore capacitance
- For the same amount of noise a fast rising signal is impacted less for its time resolution



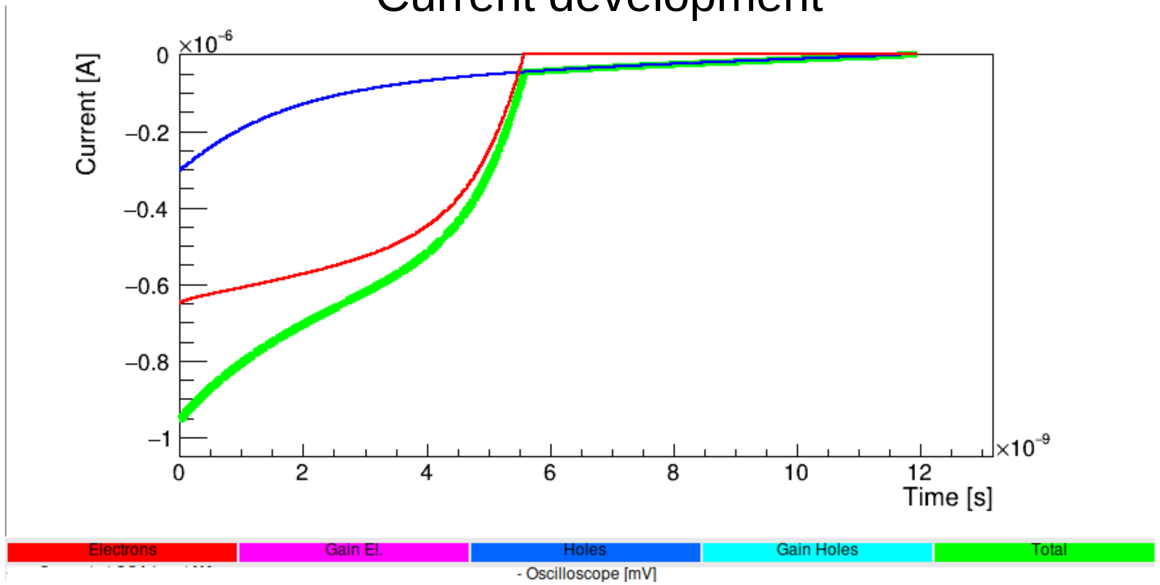
Signal rise time

- Geometry of electrodes plays a huge role in timing
- Affects the weighting potential
  → Affects the shape of the rising signal flank

Weighting Potential
(300 micron pitch 200 micron electrode)



Current development



Signal rise time

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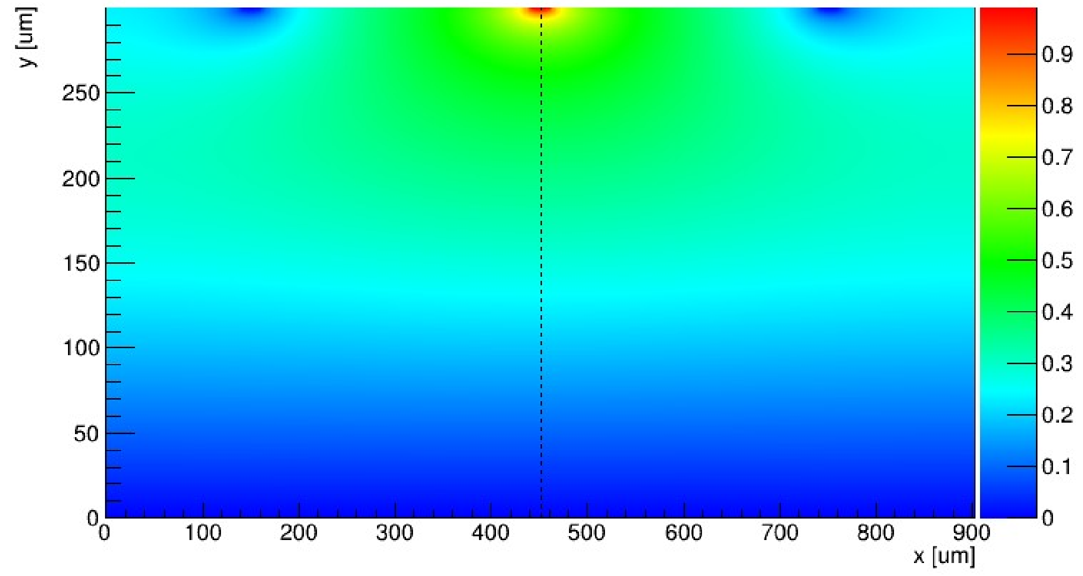
Weighting Potential
(300 micron pitch 20 micron electrode)



Current development