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# 28nm front end ASIC and 12” LGADs for 3D integration

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On behalf of the 3D Integrated Sensing Solutions (3DIntSenS) Collaboration



U.S. DEPARTMENT  
of ENERGY

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# 3D Integrated Sensing Solutions: Project Overview

- 2-year R&D project funded under the DOE “Accelerate Innovations in Emerging Technologies” call
- Joint effort by SLAC, Fermilab and LLNL teams
- Highly granular precision timing detectors, essential for achieving scientific breakthroughs across HEP, NP, BES, and FES applications, require 3D-integration between high performance sensors and readout ASICs that has been cost-prohibitive for the majority of scientific community
- **Objective:** Develop technology to enable cost-effective large-scale particle detectors with 3D-integrated ASIC designs to simultaneously achieve 10  $\mu\text{m}$  position resolution and 10 ps precision timing, with low-power consumption and high throughput rates.

## Technical approach:

- ❑ Design and manufacture **LGADs on 12” 65nm CMOS foundry node** for 3D integration with advanced ASIC technology
- ❑ Develop **ASICs in 12” 28nm CMOS** node to meet aggressive power and timing requirements for HEP, BES, FES applications
- ❑ Develop 3D integration capability  
12” LGAD and 12” 28nm ASIC wafer-to-wafer bonding (*next phase*)

# LGAD: Low Gain Avalanche Diode detectors

Thin silicon sensors with gain layer for high-field region and charge multiplication  
Moderate internal gain (~10:20), to improve SNR.

Applications in:

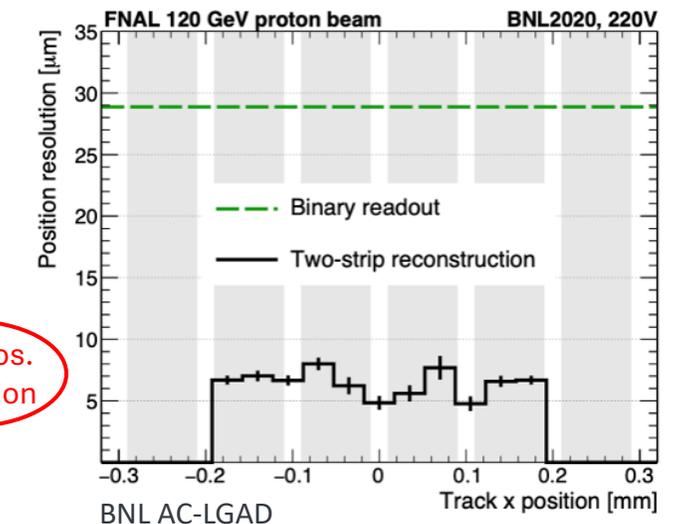
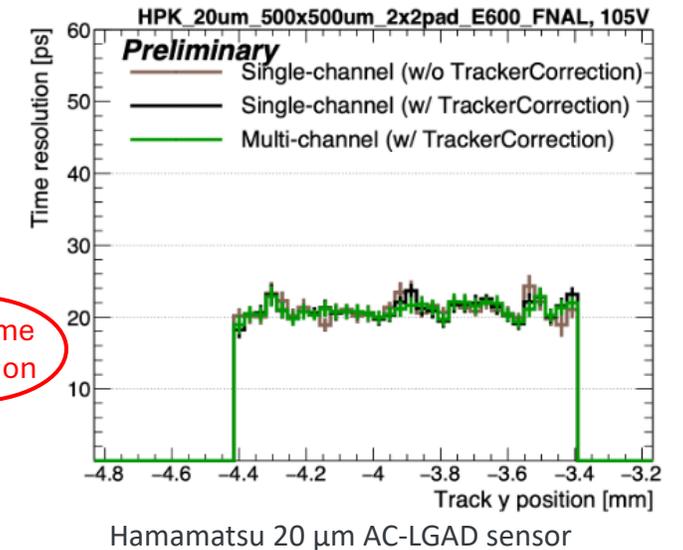
**High Energy Physics:** 4D particle tracking: provide excellent timing (<30ns) and position resolution.

- CMS and ATLAS are building first-generation detectors (1mm pixel pitch, ~30ps resolution).
- Beam demonstration of ~5  $\mu\text{m}$ , ~30 ps resolutions with AC-LGADs beam.
- Particle ID with Time of Flight

**Fusion Energy Science:** Inertial Confinement Fusion (ICF) experiments measure peak plasma burn durations below 100 ps: need to sample with precision ~10 ps.

**Basic Energy Science:** Development of large area camera systems for deployment at DOE Photon sources

- Synchrotron radiation facilities
- Time-resolved X-ray imaging
- Soft X-ray imaging: gain improves signal-to-noise for soft x-rays



# 3D integration: motivation

## Demonstration at Fermilab (2009-2014)

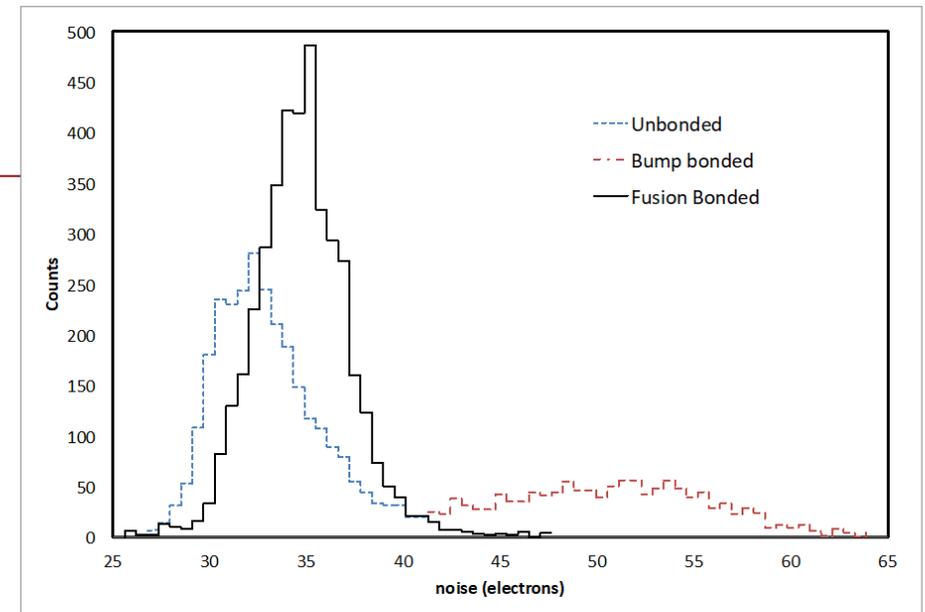
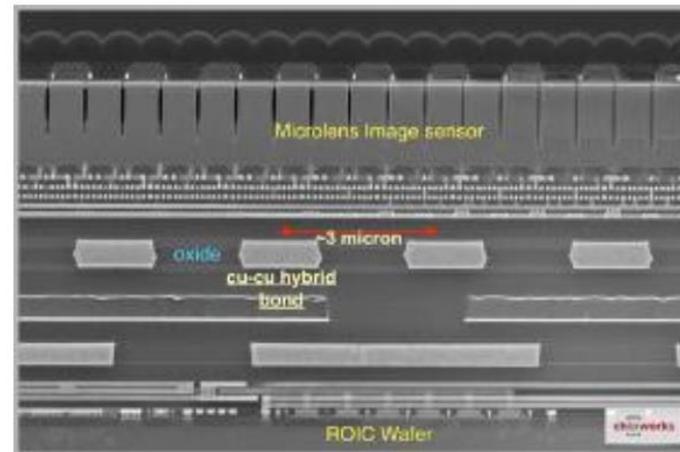
Reducing input and interconnect capacitance reduces noise and improves SNR and jitter

- VIPIC 1 (64 x 64 pixels)
- Lower input capacitance in the fusion-bonded version

ENC on fusion bonded device is close to that measured for floating inputs

ENC=40e C<20fF

ENC=70e C>80fF



VIPIC1 with DBI bonded sensor Sn-Pb bump-bonded on PCB

# LGAD Development

- Development in partnership with Tower Semiconductor
- Full wafer run on 12" process 65nm process (first LGAD process on 12" wafers)

## Reach Through (RT) LGADs:

- Proven design with planned deployment for the CMS and ATLAS upgrades
- Limited fill factor due to junction termination extension (JTE), used to compare to existing devices

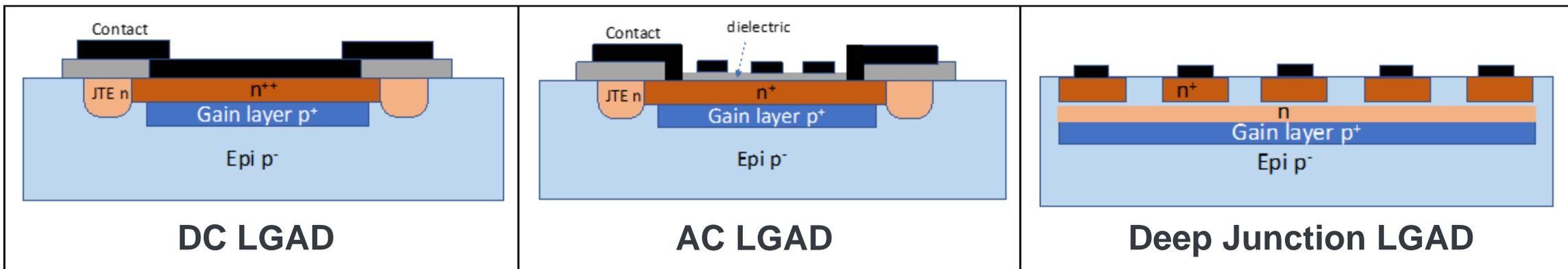
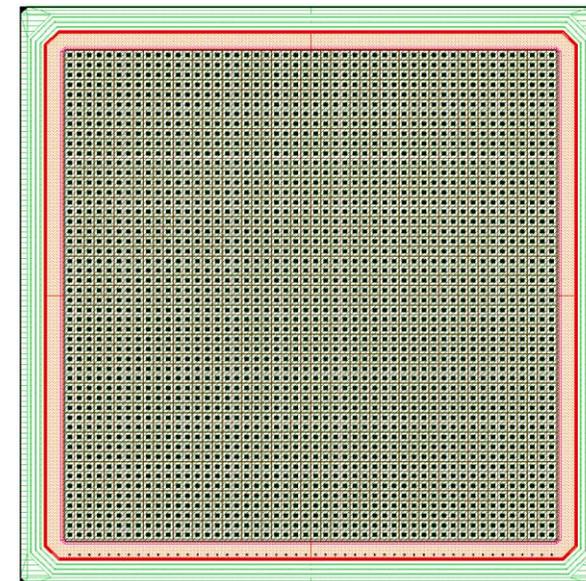
## AC LGADs:

- Solve the fill factor problem
- Bipolar signals, resistive cathode, complex response.

## Deep Junction (DJ) LGADs:

- Also provide 100% fill factor but require high energy implants or engineered substrates.
- New variety of LGAD, loss of gain between pixels

100 $\mu$ m pitch AC coupled LGAD  
50x50 prototype array layout:



# LGAD Development

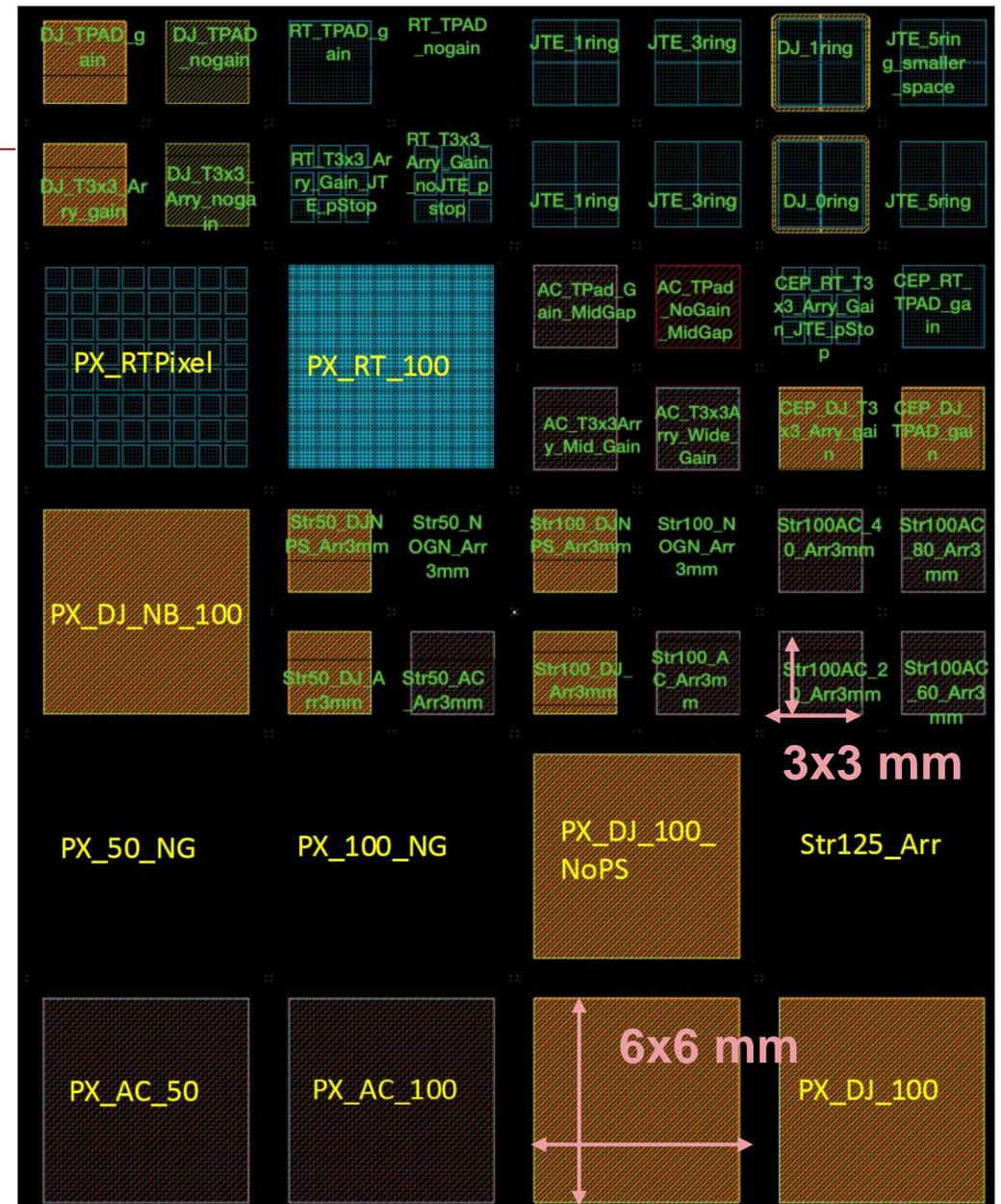
~50 separate sensor structures:

- 11 6x6mm pixels arrays (50, 100  $\mu\text{m}$  pitch) for BB
- 12 3x3mm strip arrays (20, 40, 60, 80, 100  $\mu\text{m}$  pitch) for WB
- 16 device test structures (Foundry PCMs + 3x3 macro pixels + pad diodes)
- 8 guard ring test structure

Sensor study to optimize doses, energies and edge termination strategies. Production splits.

Standard CMOS model forces special considerations for detector design: define active regions to exclude STI, metal density and spacing, angles restricted to 45° and 90°, vias size and location, oxide thickness, etc.

3000 mm



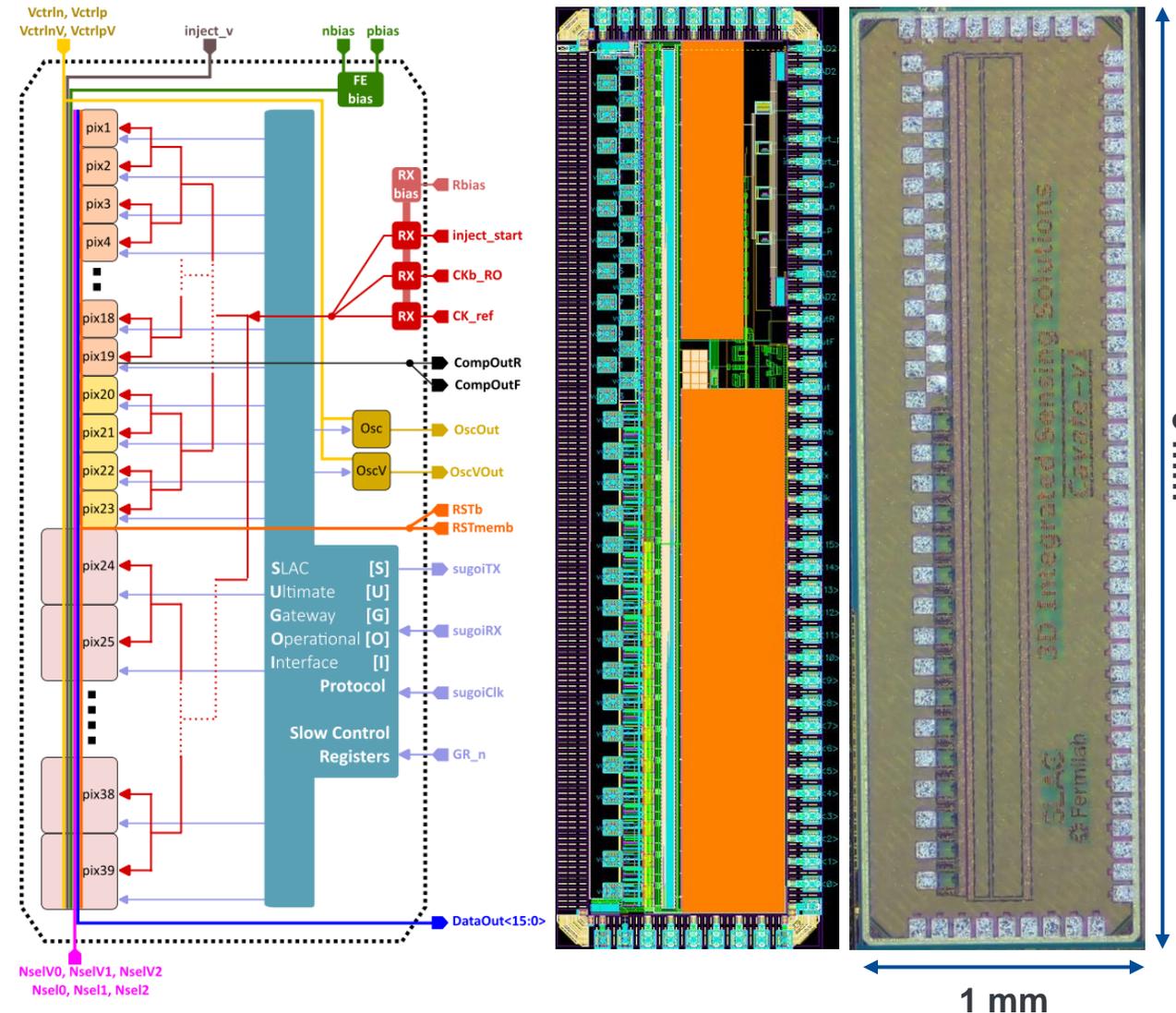
2400 mm

# Readout ASIC: 1<sup>st</sup> prototype

[see Bojan Markovic's TWEPP 2024 presentation](#)

- The first 28nm LGAD readout ASIC prototype (1x3mm<sup>2</sup>) was submitted for fabrication in August 2024:
  - Linear pixel array (39 pixels) of different flavors: 2 variants of 50μm and 1 variant of 100μm size pixels;
  - Timing critical signals (clock, test injection signal) distributed via balanced distribution three; *low-jitter receives courtesy of Carl Grace (LBNL)*;
  - Sparsified readout (pixel address, TOA and TOT data are sent out for pixels that receive events over the threshold);
  - SLAC's SUGOI protocol for ASIC slow-control configuration;

First readout ASIC prototype: block schematic, layout, and die



3 mm

1 mm

# Pixel

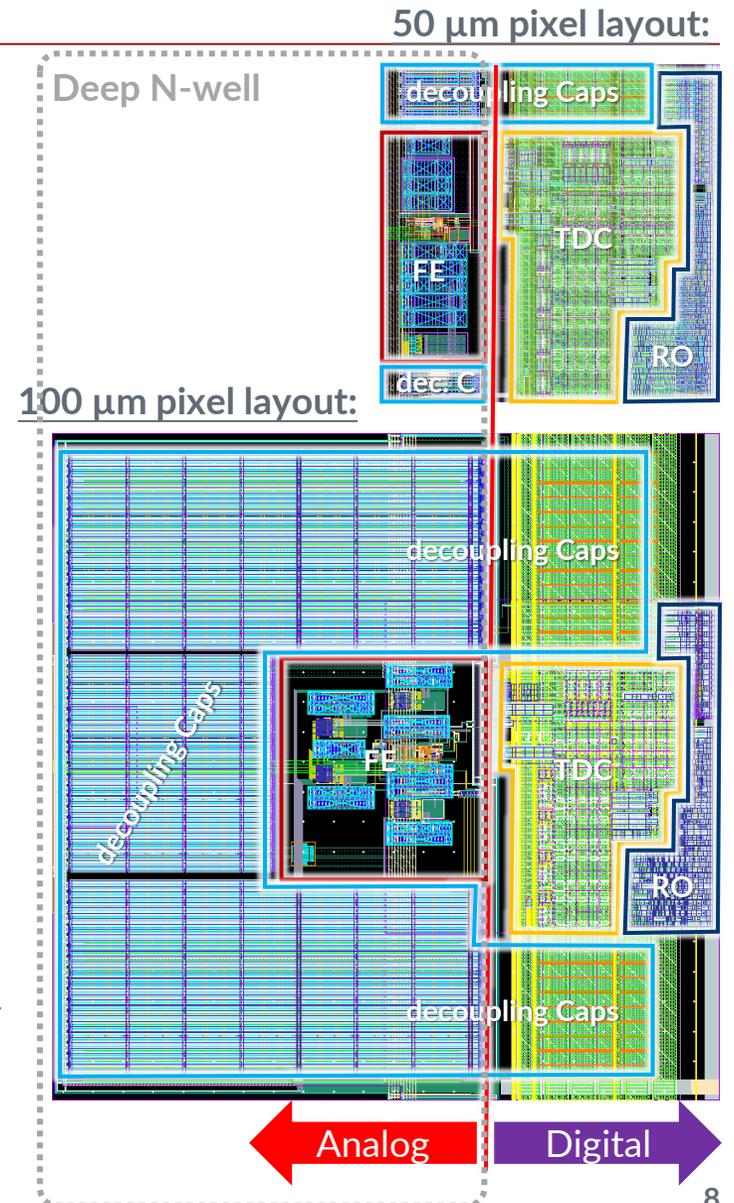
- ❑ Analog frontend in deep n-well shared between column pixels
  - Analog section uses about 40 % of the 50  $\mu\text{m}$  pixel area
- ❑ Digital section includes:
  - TDC performing both TOA and TOT measurements, based on silicon demonstrated design (see [Julia Mendez TWEPP talk](#))
  - Readout logic
- ❑ Decoupling caps (plenty in the 100  $\mu\text{m}$  pixel version)

Frontend Specification	Value
Total Power Density	$1\text{ W/cm}^2$
Power $50 \times 50\ \mu\text{m}^2$	$25\ \mu\text{W}$
Time of Arrival (ToA) Jitter	$10\ \text{ps}_{rms}$
Min Signal for ToA Jitter	$1.3\ \text{fC}$
Max Signal	$13\ \text{fC}$
Dynamic Range	10 – 20
Recovery Rate	100 kHz
LGAD Input Cap. Approx.	$11.52\ \text{aF}/\mu\text{m}^2$
Amplitude Accuracy	10 %

*Jitter specification is paramount*

[1] J. Mendez et al. "Design update and characterization of sub-10ps TDC ASIC in 28nm for future 4D trackers", TWEPP 2024.

[2] L. Ruckman et al. "Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers", TWEPP 2023.



# Analog Front-End: Architecture

@Troy England (FNAL, tengland@fnal.gov)

❑ 50  $\mu\text{m}$   $e^-$  and  $h^+$  readout, 100  $\mu\text{m}$   $e^-$  readout

❑ The signal path consists of:

## 1. Preamplifier

- The circuit is based on [1]
- Open loop voltage gain at frequencies of interest, active feedback for DC biasing and recovery.
- Time over threshold used to access amplitude information

## 2. additional gain

- abundant gain used in place of a specialized comparator

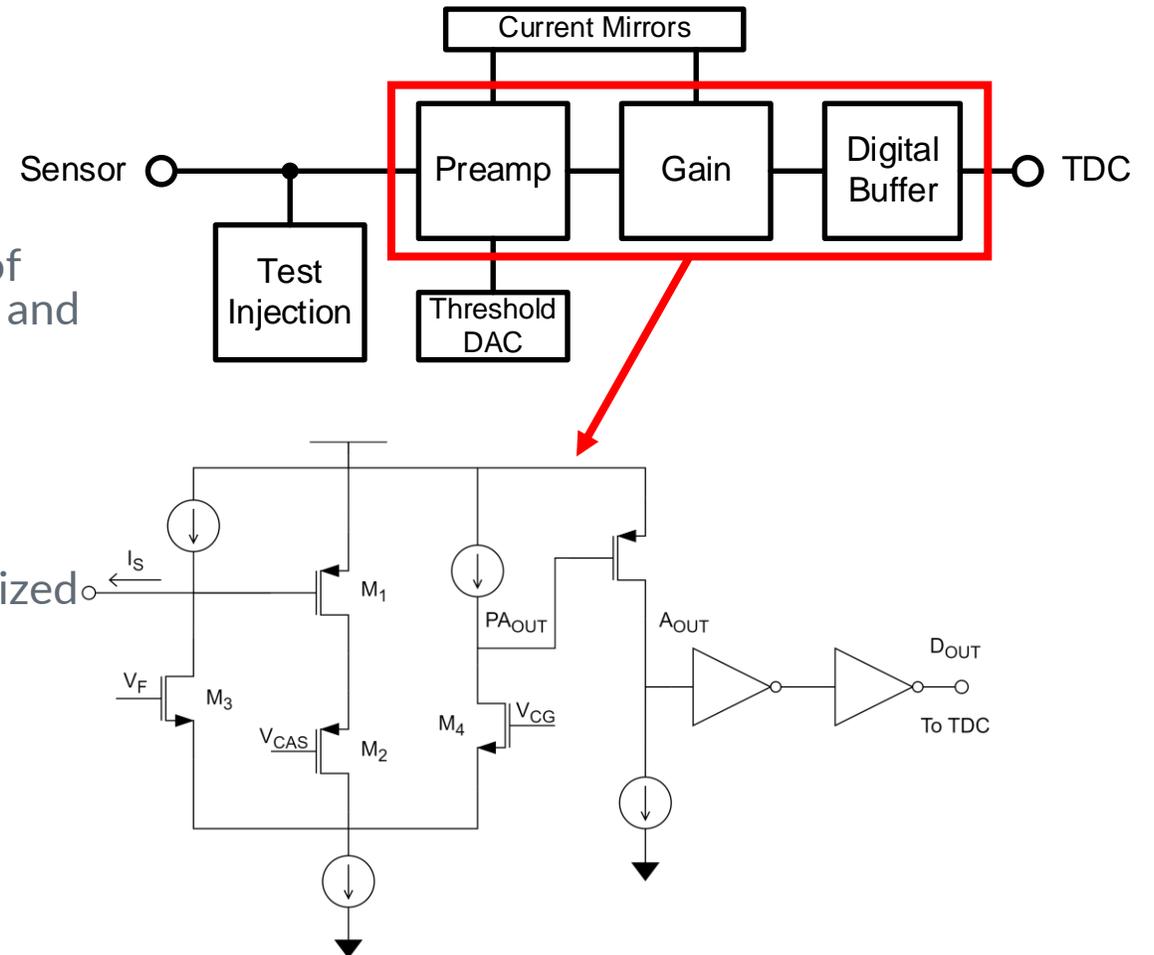
## 3. digital buffer

❑ Support circuitry includes:

## 4. current mirrors

## 5. DAC for setting the threshold ( $V_{CG}$ , 5bit)

## 6. charge injection for testing



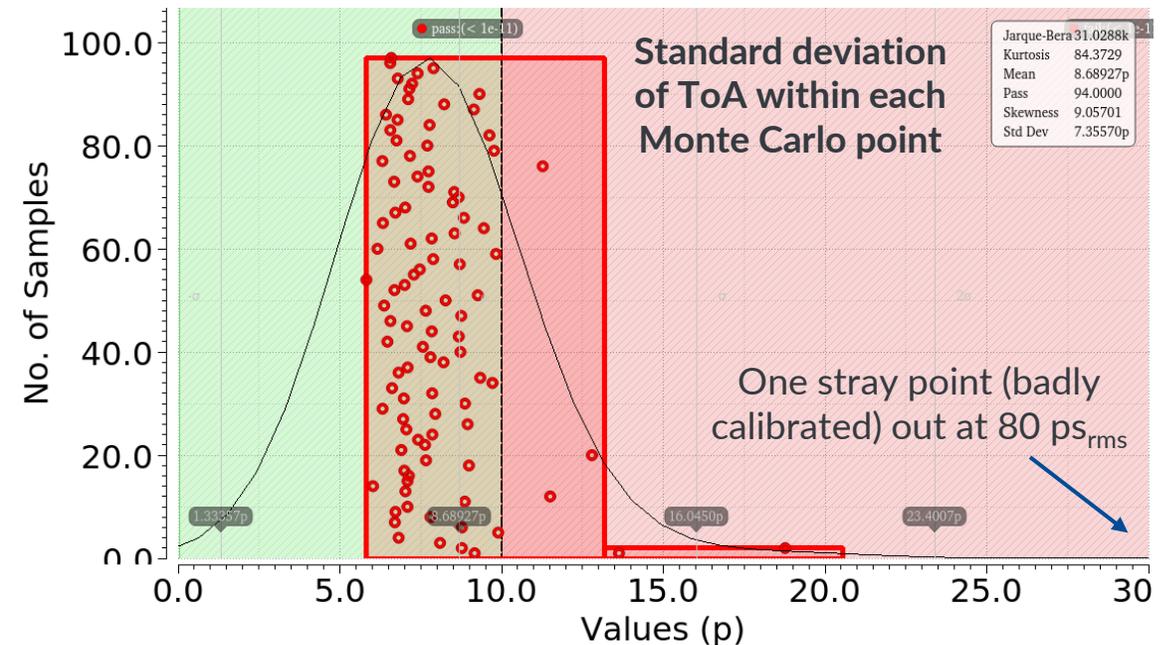
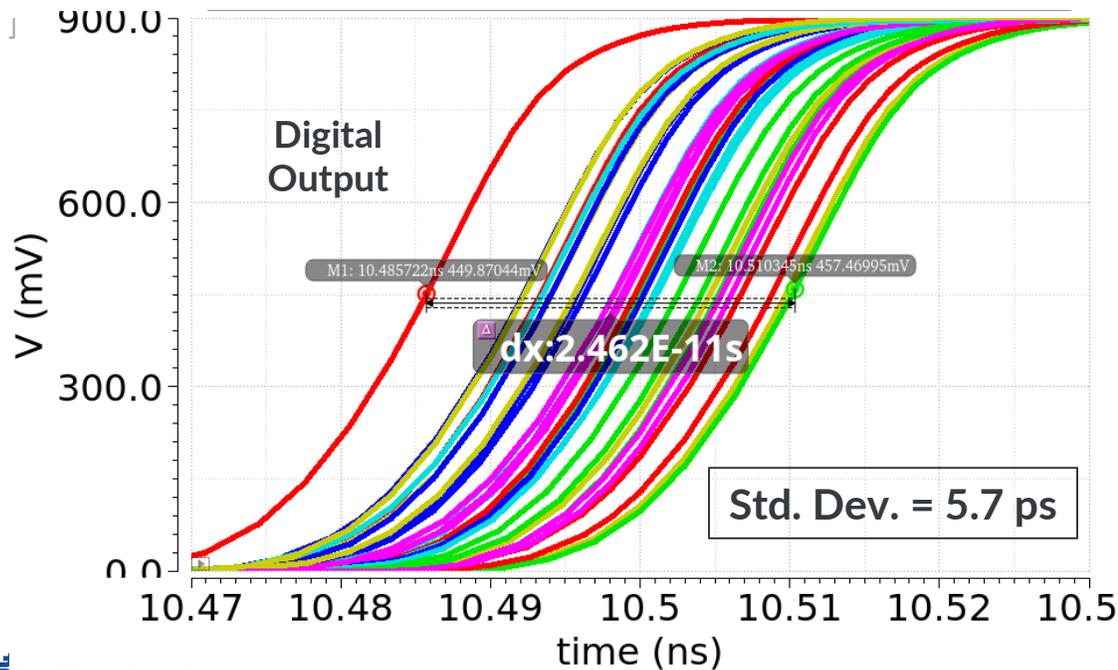
[1] "A transimpedance amplifier using a novel current mode feedback loop"  
<https://www.sciencedirect.com/science/article/pii/S0168900295014543>

# Analog Front-End: TOA Jitter Simulation

@Troy England (FNAL,  
tengland@fnal.gov)

- ❑ Filled RCC PEX simulation:
  - Nominal PVT, conservative accuracy, 30 runs
  - Minimum input charge: 1.3 fC
  - Noise to 30 GHz
    - Includes 10 nV/rtHz supply noise
    - Includes LGAD capacitance
    - No noise from LGAD (landau fluctuations)

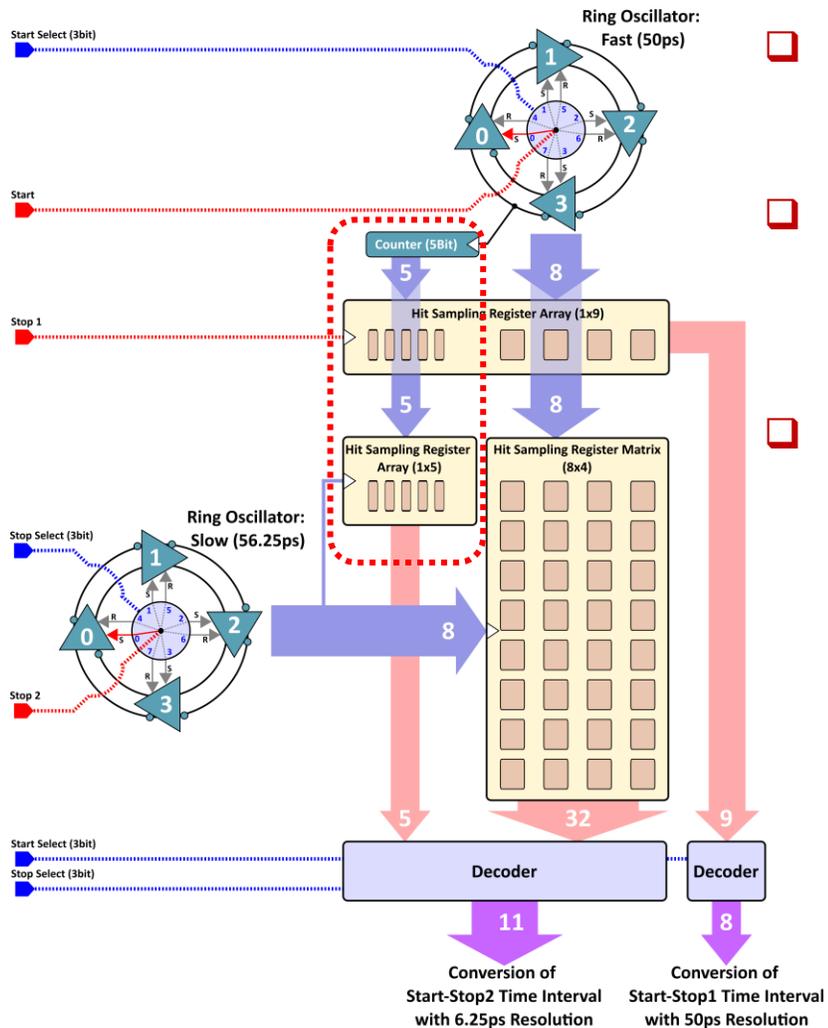
- ❑ 100 Monte Carlo runs with both Global and Local variation:
  - The DAC provides enough range and resolution to deal with the variation
  - 30 transient noise runs at each MC point with conservative accuracy and 30 GHz max frequency
  - 1.3 fC input charge



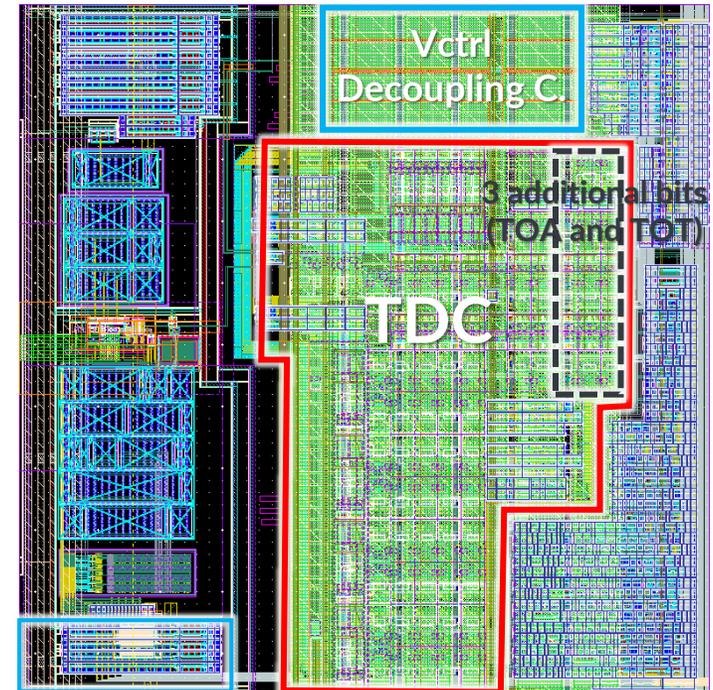


# TDC improvements

@Bojan Markovic (SLAC, markovic@slac.stanford.edu)



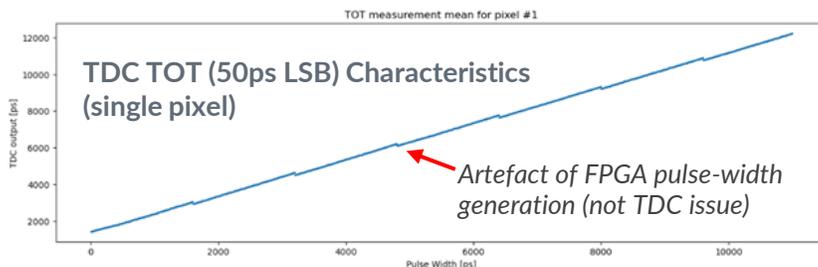
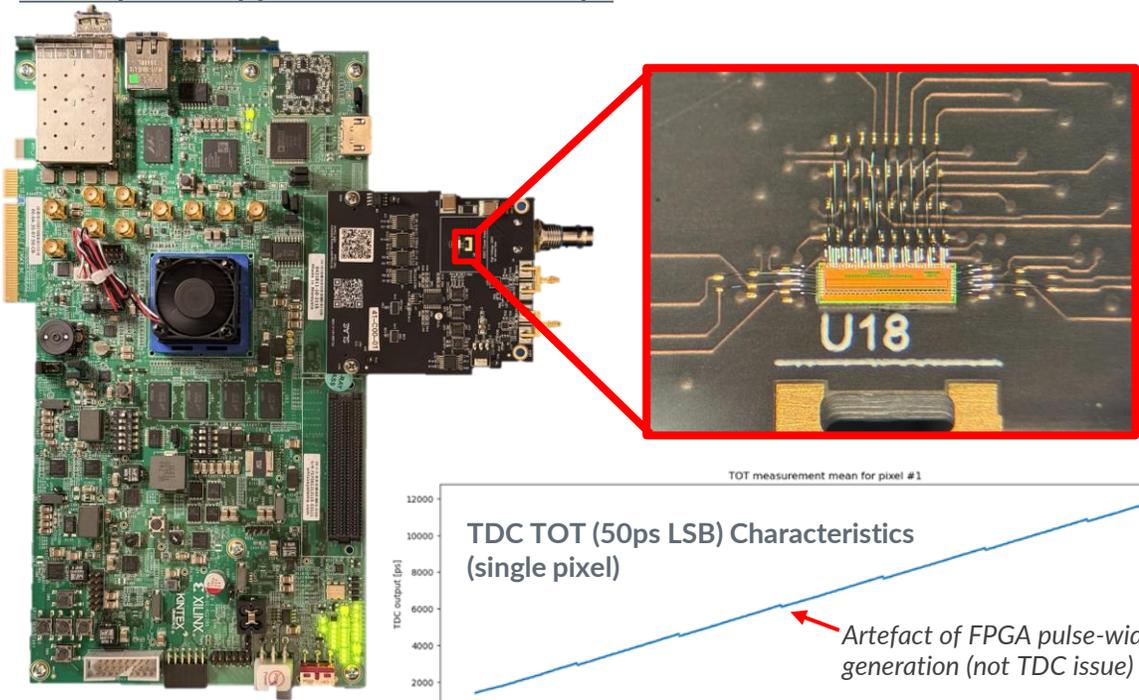
- ❑ Added 3 bit to TOA and TOT to extend the range from 1.6ns to 12.8ns
- ❑ Added decoupling caps on TDC control lines (Vctrl) to limit the disturbances causing characteristic curvature and jitter increase
- ❑ Fixed top level parasitic that caused race condition in counter sampling, resulting in “glitches” in conversion characteristic



	TDC metrics
<b>Technology</b>	28nm
<b>Timing resolution</b>	6.25ps (TOA) / 50ps (TOT)
<b>Time depth</b>	1.6ns (8bit / 5bit) 12.8ns (11bit / 8bit) easily extendable by simple addition of bits to the counter
<b>TDC area</b>	26μm x 40.5μm (1.7μm x 13.3μm per additional bit)
<b>Power consumption</b>	(average, 25ns conversion cycle / bunch crossing)
10% occupancy	16μW 51.1μW
1% occupancy	2.5μW 6.2μW

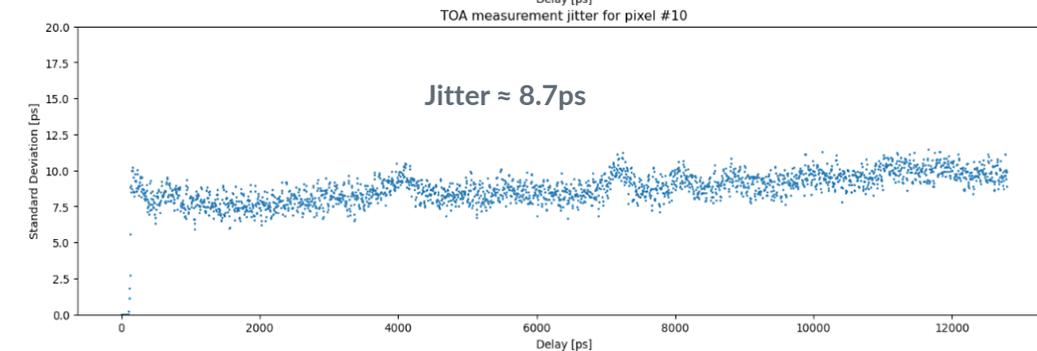
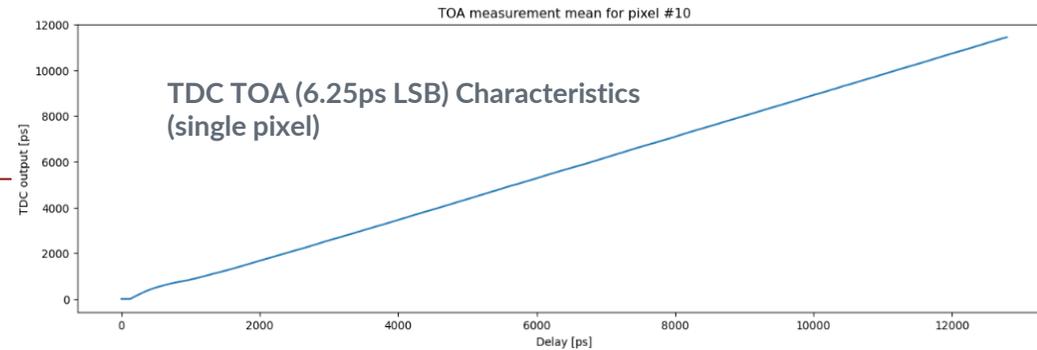
# TDC characterization

TDC prototype ASIC test setup:

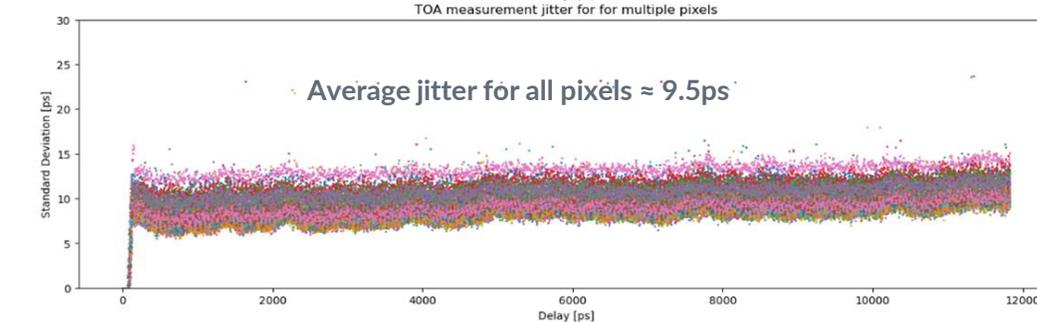
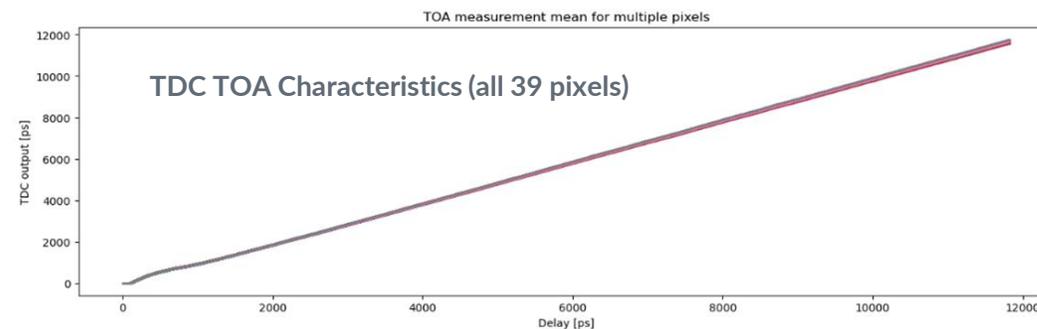


## Summary:

- ❑ Overall good performance
- ❑ Few issues that are well understood and fixed for MPW2
- ❑ Full system jitter is around  $10 \text{ ps}_{\text{rms}}$
- ❑ Confidence in achieving sub-10ps system jitter in MPW2

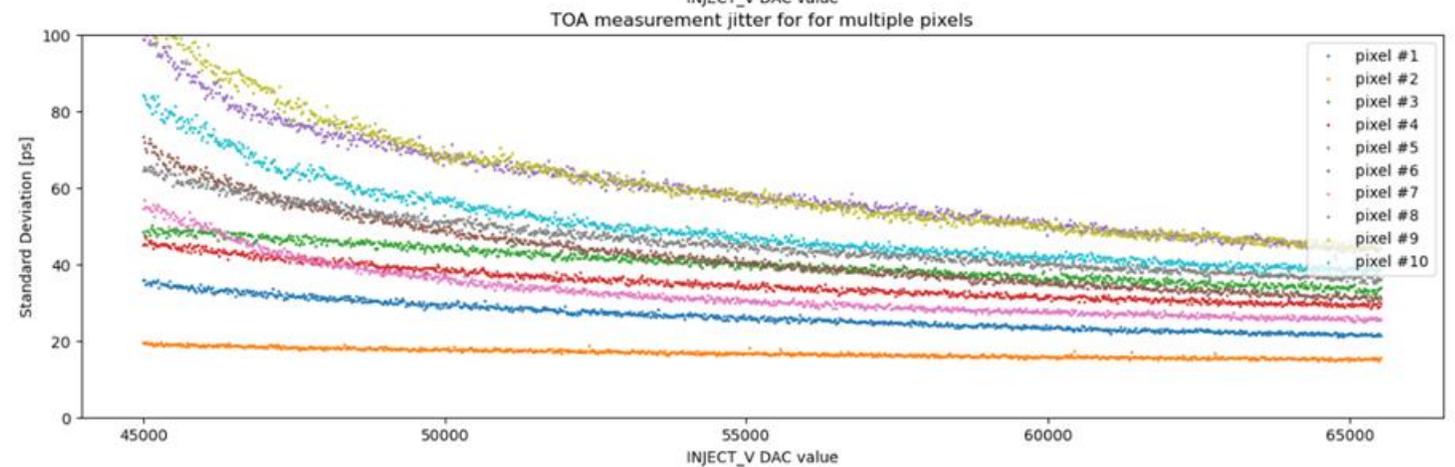
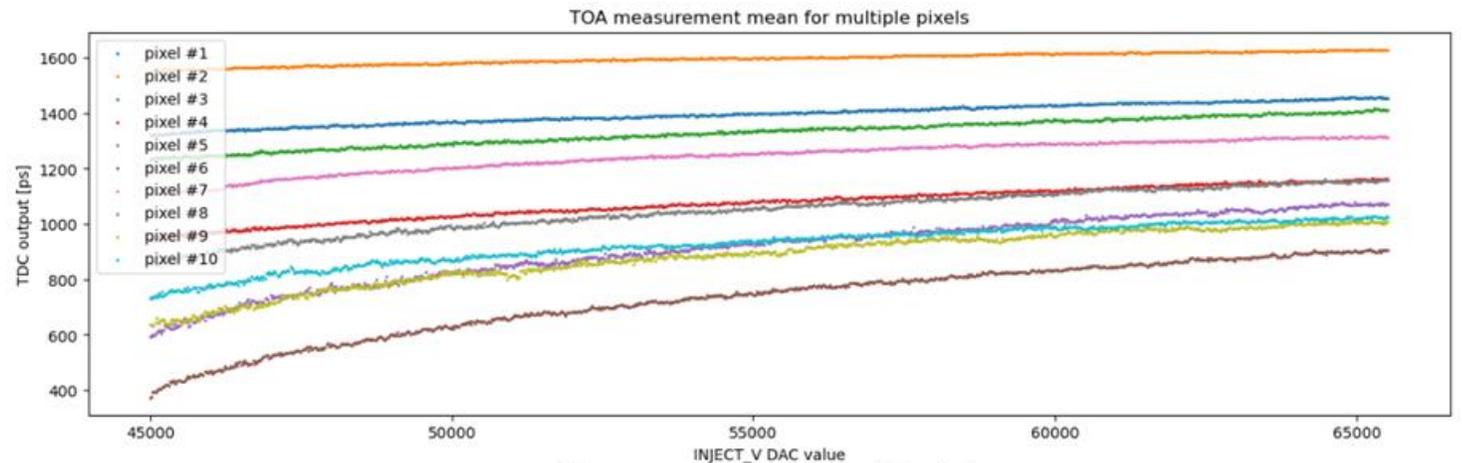
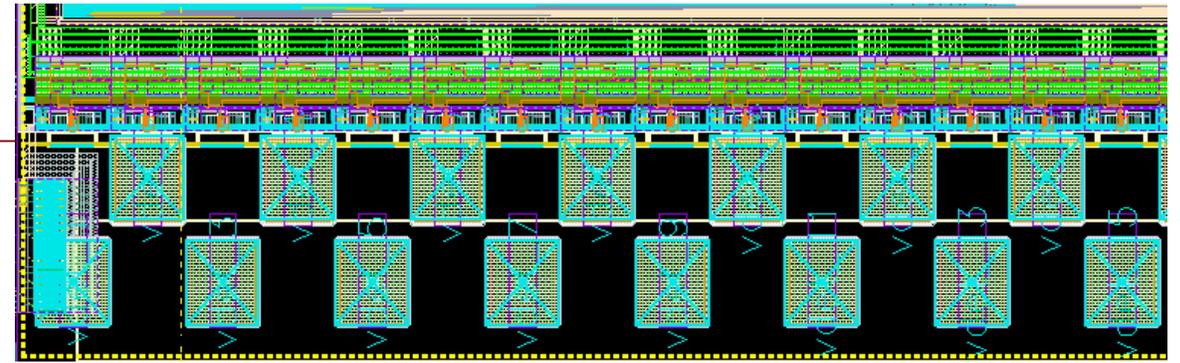


Average Standard Deviation for pixel #10: 8.722719760893227ps



# Front-end characterization

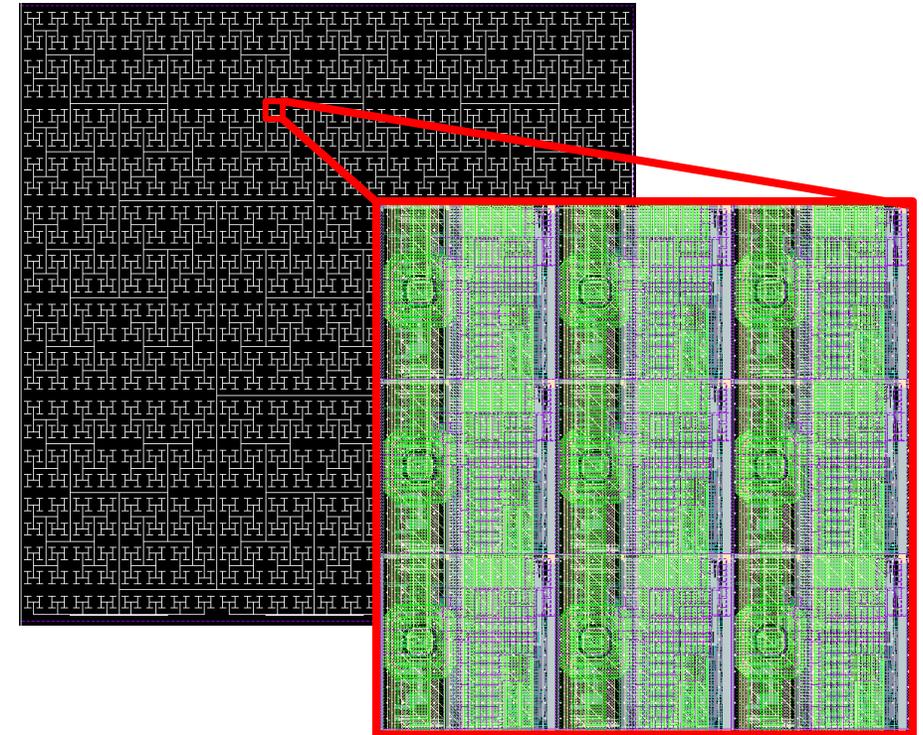
- Issue with charge injection circuit pulses on test boards limits the test range
- Issue with power supply distribution means that pixel rows sees increasing supply impedance (worse for large pixels)
- Dominates jitter except for first few pixels
- Even pixels achieve better pixels than odds because of reduce connection capacitance to the pad. Channel #2 achieves 20ps
- → fixed in the next iteration



# Readout ASIC: 2<sup>nd</sup> prototype



- 2<sup>nd</sup> prototype in 28nm to be taped out in September 2025
- **THRIGLAV: THRee-d InteGrated LgAd driVer**
- (5x6mm<sup>2</sup>) with 100x100 50μm pitch pixel array, incorporating learning from the 1<sup>st</sup> run.
- 100x100 pixel matrix with clock distribution tree completed
- Optimization of pixel blocks based on feedback from MPW1 in progress
- Digital control and readout logic design, fast IO driver.
- At the end of 2<sup>nd</sup> year, we anticipate first demonstration of 28nm readout chip bump-bonded to the prototype LGAD array with high-precision timing performance.
- For the next project phase, we would proceed to wafer-to-wafer bonding of 12" LGAD and 12" 28nm ASIC wafers.



Layout of the pixel matrix highlighting the clock distribution tree with zoom on 3x3 pixel region

# Summary and Next Steps

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- ❑ LGAD and ASIC development proceeding in parallel
- ✓ The first 28nm LGAD readout ASIC prototype was submitted for fabrication
- ✓ LGAD fabrication run at Tower Semiconductor imminent
- ❑ Characterization of first prototype revealed issue with power distribution, but combination of pixel front end and TDC demonstrated sub 20ps jitter
- ❑ Second readout ASIC to be submitted in September, incorporating lessons from the 1<sup>st</sup> run
- ❑ Towards 3D: bump bonded ASIC + sensor characterization and beam test to follow
- ❑ Next project phase: wafer-to-wafer bonding of 12" LGAD and 12" 28nm ASIC wafers

# Acknowledgements

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- **SLAC:** Julie Segal (PI), Bojan Markovic, Lorenzo Rota, Angela Kok, Chris Kenney, Ariel Shwartzman, Aseem Gupta, Julian Mendez, Larry Ruckman, Christos Bakalis
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- **LLNL:** Arthur Carpenter, Ann Garafalo, Clemet Trosseille

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