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28nm front end ASIC and 12"LGADs for 3D integration

The 3DIntSenS Collaboration—a joint effort between SLAC, Fermilab, and LLNL—is developing enabling technologies for next-generation radiation imaging detectors that combine ultra-fine spatial resolution (˜10 µm) with precision timing (<20 ps), while maintaining low power <1W/cm2 and high data throughput. The approach leverages 3D integration between advanced CMOS readout ASICs and finely pixelated LGAD sensors to achieve the performance and scalability required for large-area, high-rate applications.
High-granularity, precision-timing detectors are essential for scientific advances in HEP, NP, BES, and FES, but widespread adoption is limited by the cost and complexity of 3D integration. To close this gap, the collaboration is developing LGAD sensors compatible with 12-inch commercial CMOS processes, enabling cost-effective integration with high-performance ASICs under development.
We present the design and results from a 28 nm CMOS ASIC prototype, including a low-jitter front end, and in-pixel TDC demonstrating sub-10 ps timing resolution. We also report on the co-design and characterization of reticle-scale LGAD sensors with 50 µm and 100 µm pixels, and introduce the next 10k-pixel ASIC designed for full 3D integration. These advances represent a critical step toward scalable, high-resolution radiation imaging systems for future scientific instrumentation.
Summary:
Highly granular precision timing detectors are essential for advancing scientific discovery across High Energy Physics (HEP), Nuclear Physics (NP), Basic Energy Sciences (BES), and Fusion Energy Sciences (FES). Their critical importance has been emphasized in multiple strategic planning efforts, including the DOE Basic Research Needs (BRN) Report, the European Strategy for Particle Physics, and Snowmass. A key enabling technology for these detectors is 3D integration of finely segmented sensors with advanced CMOS readout ASICs. However, current 3D integration approaches remain cost-prohibitive for large-scale scientific applications.
Addressing this challenge is the focus of the 3D Integrated Sensing Solutions (3DIntSenS) collaboration between SLAC, Fermilab, and LLNL, supported by the DOE Accelerated Innovation in Emerging Technologies program. In partnership with a leading commercial semiconductor foundry, the collaboration is developing LGAD sensors compatible with 12-inch CMOS wafer processes, optimized for cost-effective 3D integration with high-performance readout ASICs. A co-design approach ensures simultaneous optimization of both sensor and ASIC technologies.
The first prototype ASIC features a linear array of 50 µm and 100 µm pixels, matched to LGAD cell variants. Each pixel integrates a low-jitter front-end, fast comparator, and a high-resolution in-pixel Time-to-Digital Converter (TDC). The system targets timing resolution below 20 ps with power consumption under 1 W/cm². Initial testing confirms sub-10 ps jitter for the in-pixel TDC.
The TDC employs a 2D Vernier ring oscillator architecture with an embedded sliding-scale technique, enabling simultaneous measurement of Time-of-Arrival (TOA) and Time-over-Threshold (TOT) with resolutions of 6.25 ps (8-bit) and 50 ps (5-bit), respectively. Power consumption scales with occupancy, averaging 18.4 µW at 10% and 2.9 µW at 1% occupancy per TDC.
The prototype has been characterized using on-chip charge injection and will be wire-bonded to LGAD sensors, including designs from the reticle-scale 12-inch wafers. Finally, we will present the design of the second-generation 10k-pixel ASIC in final design stages and scheduled for fabrication by the end of the year, to be bump bonded testing and system validation, and eventually for 3D integration.

Workshop topics

Front-end electronics and readout

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