



ALICE



6-10 July 2025, Bratislava, Slovakia
iWoRiD

ITS3: A truly cylindrical tracker for ALICE

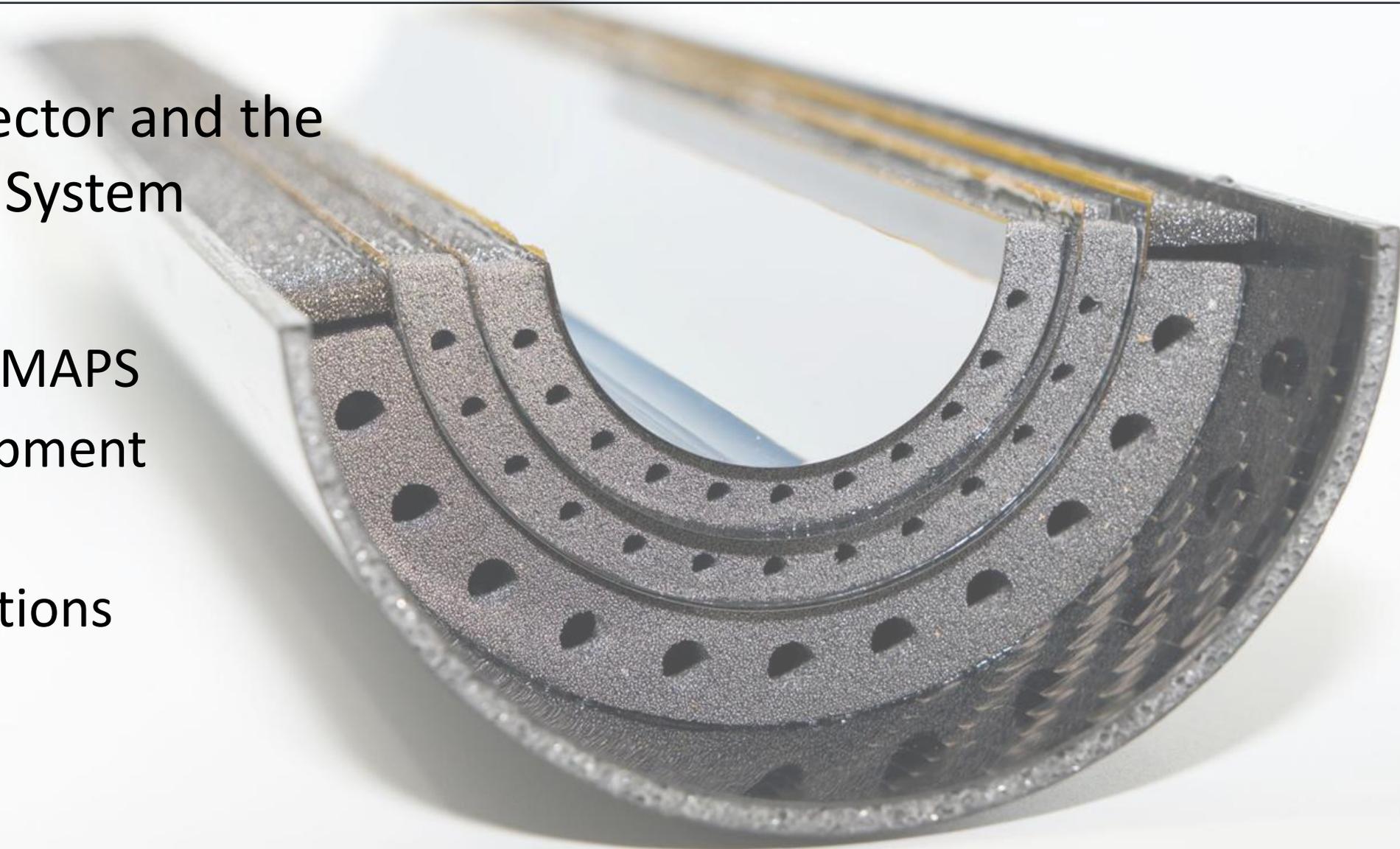
Anna Villani
on behalf of the ALICE collaboration

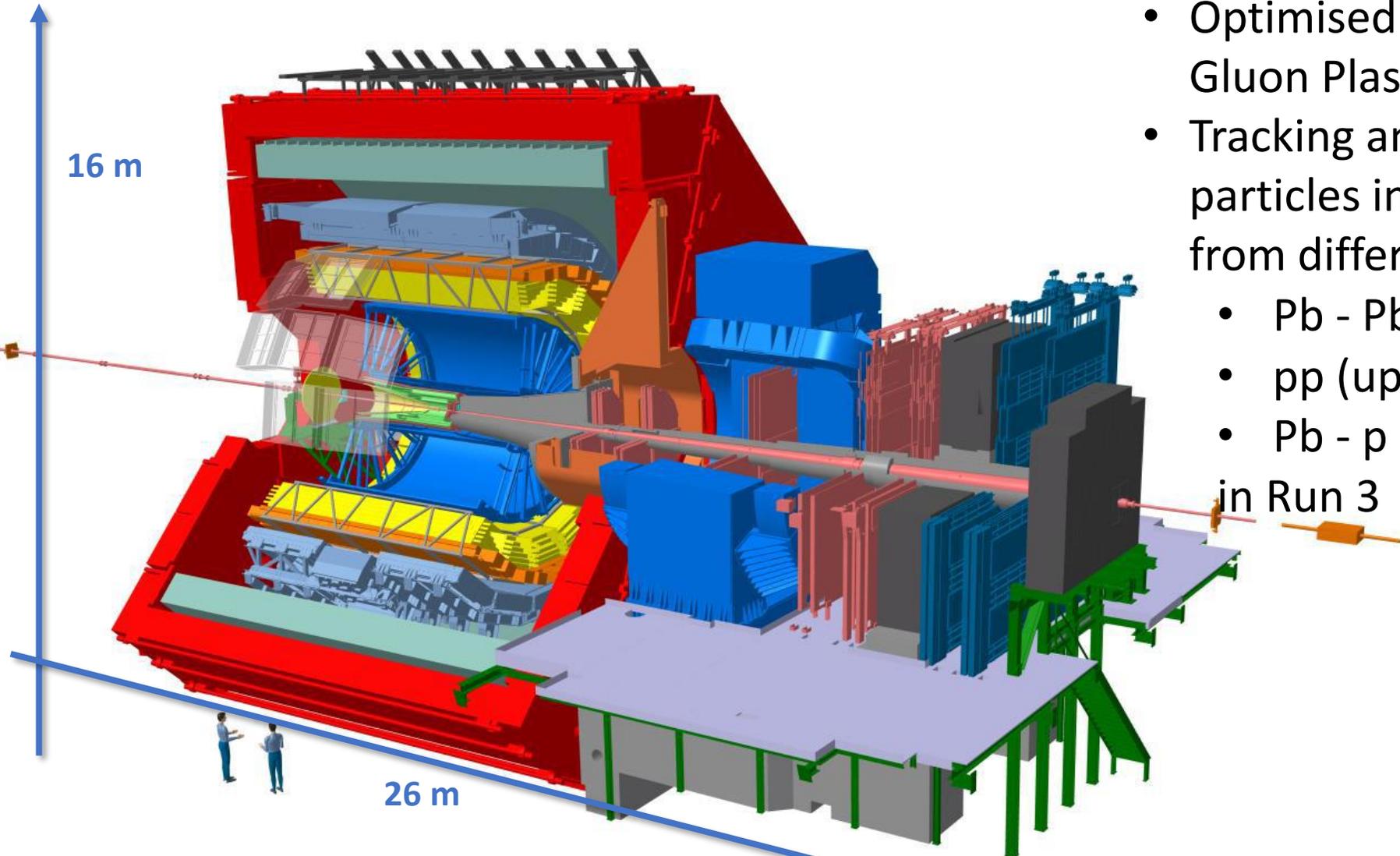


**UNIVERSITÀ
DEGLI STUDI
DI TRIESTE**

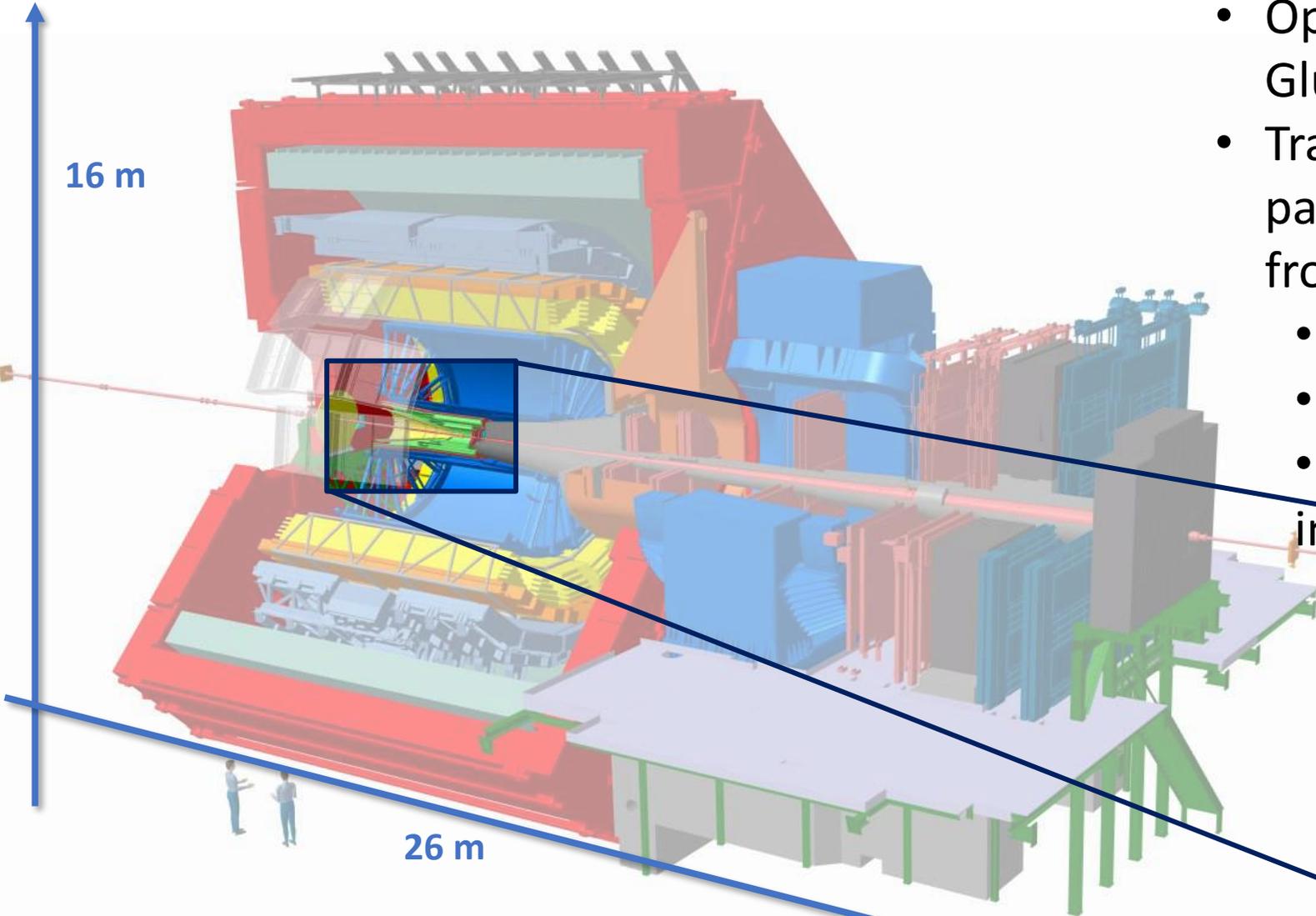


- The ALICE detector and the Inner Tracking System
- ITS3 R&D
 - Bent silicon MAPS
 - Chip development
 - Mechanics
 - Interconnections
 - Air cooling

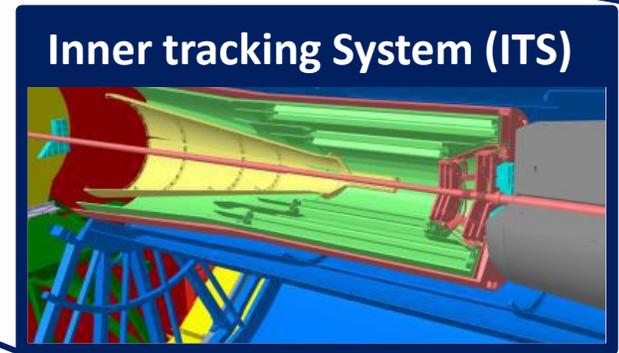


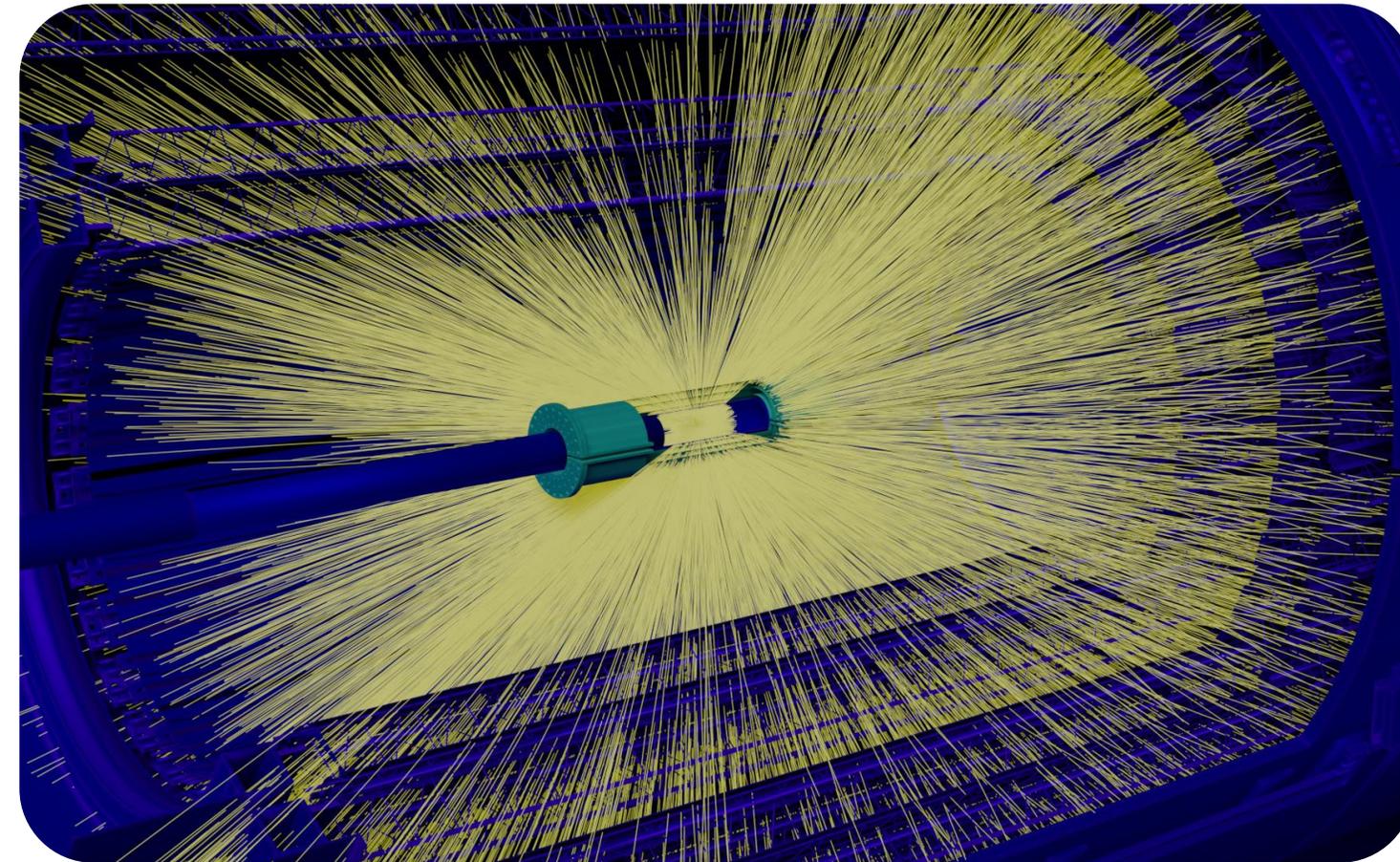


- Optimised for the study of the Quark Gluon Plasma (QGP)
 - Tracking and identification of particles in high multiplicity events from different collision systems:
 - Pb - Pb (up to $\sqrt{s_{NN}}=5.36$ TeV)
 - pp (up to $\sqrt{s}=13.6$ TeV)
 - Pb - p (up to $\sqrt{s_{NN}}=8.0$ TeV)
- in Run 3

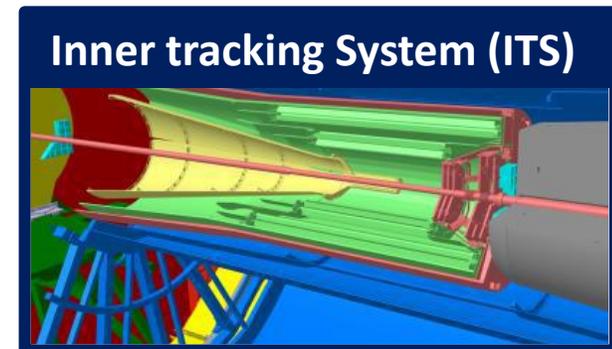


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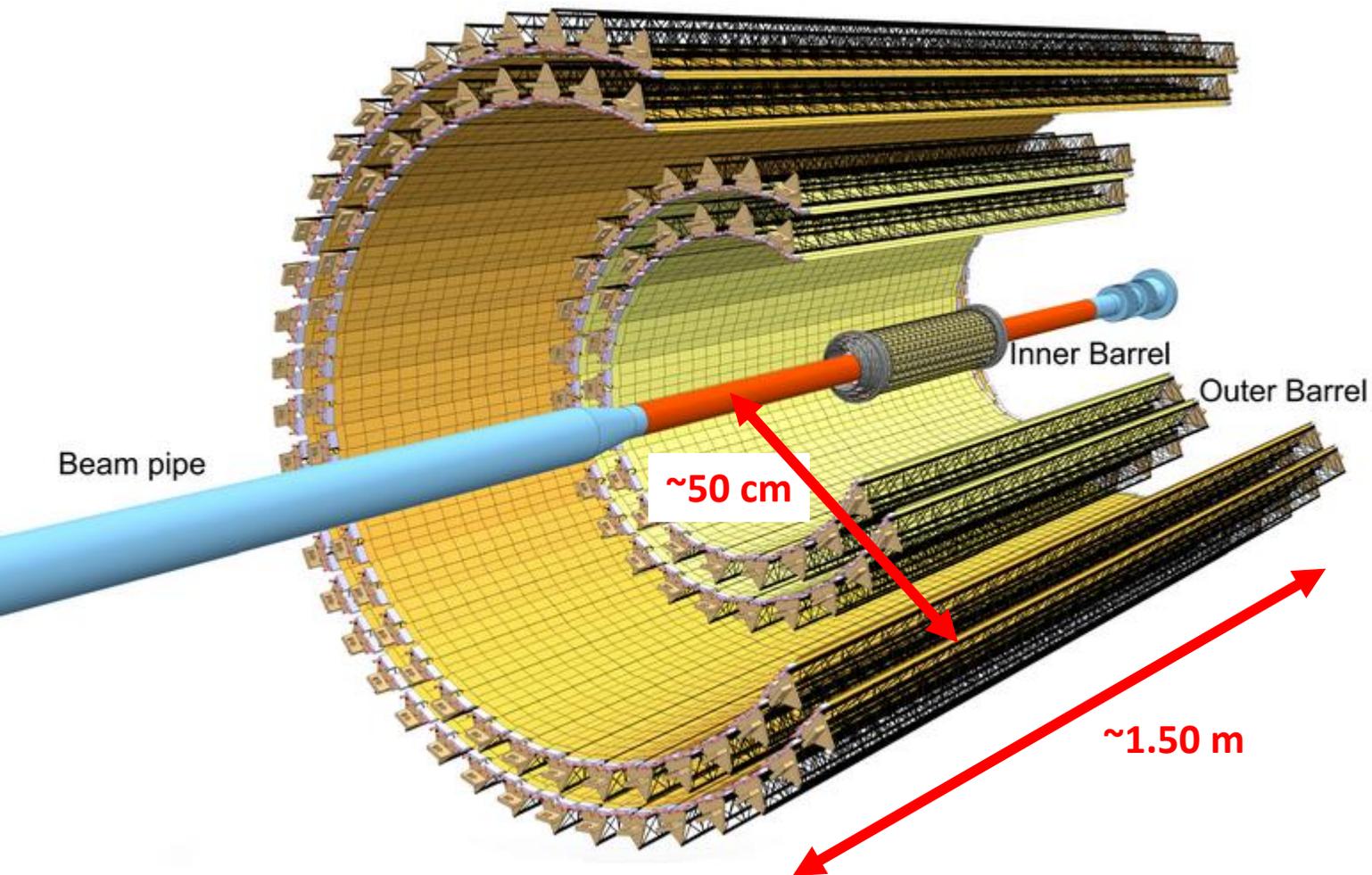




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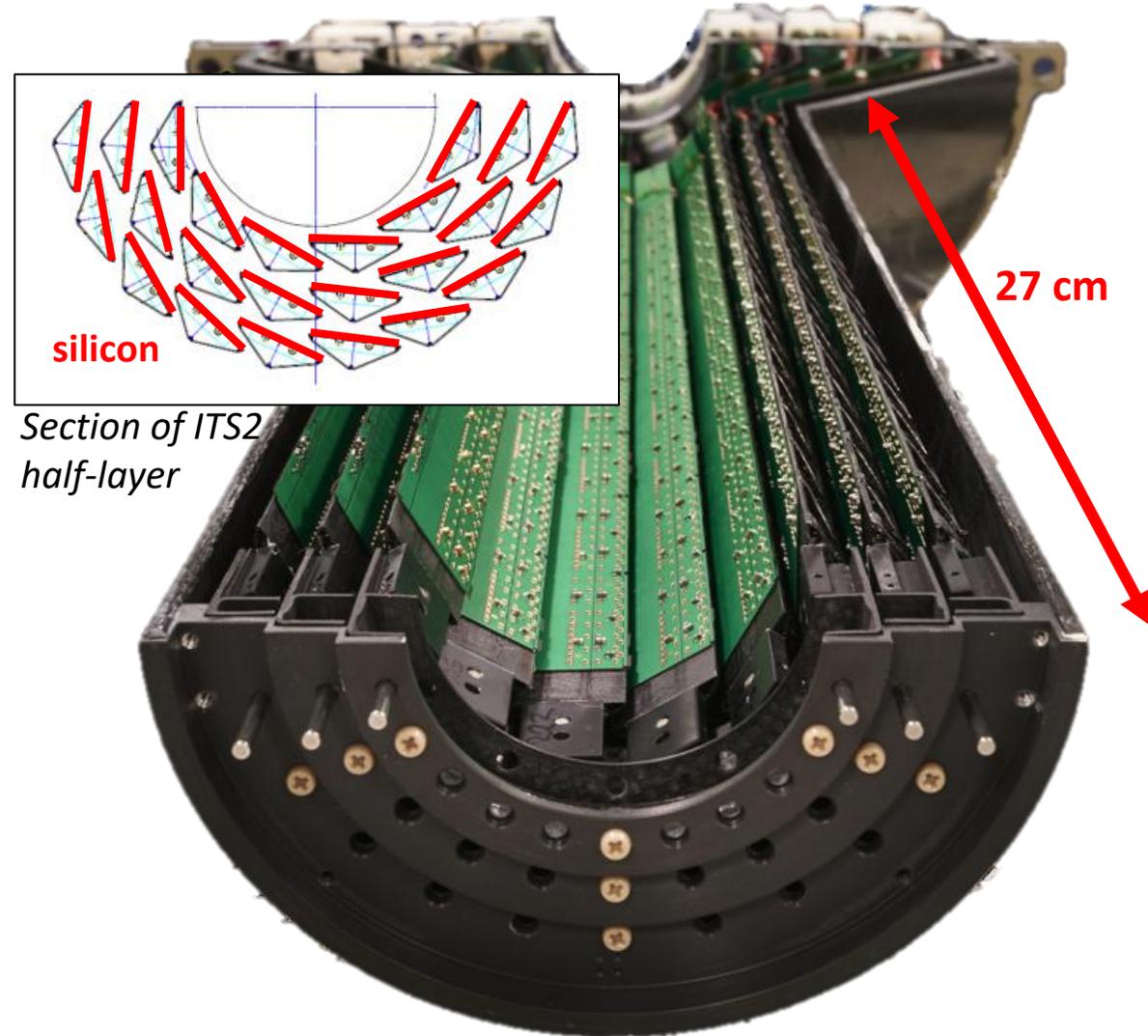
The Inner Tracking System



ITS2:

- Installed in 2021
- 7 layers
- Monolithic Active Pixel silicon Sensors (MAPS) technology

ITS2 innermost 3 half-layers

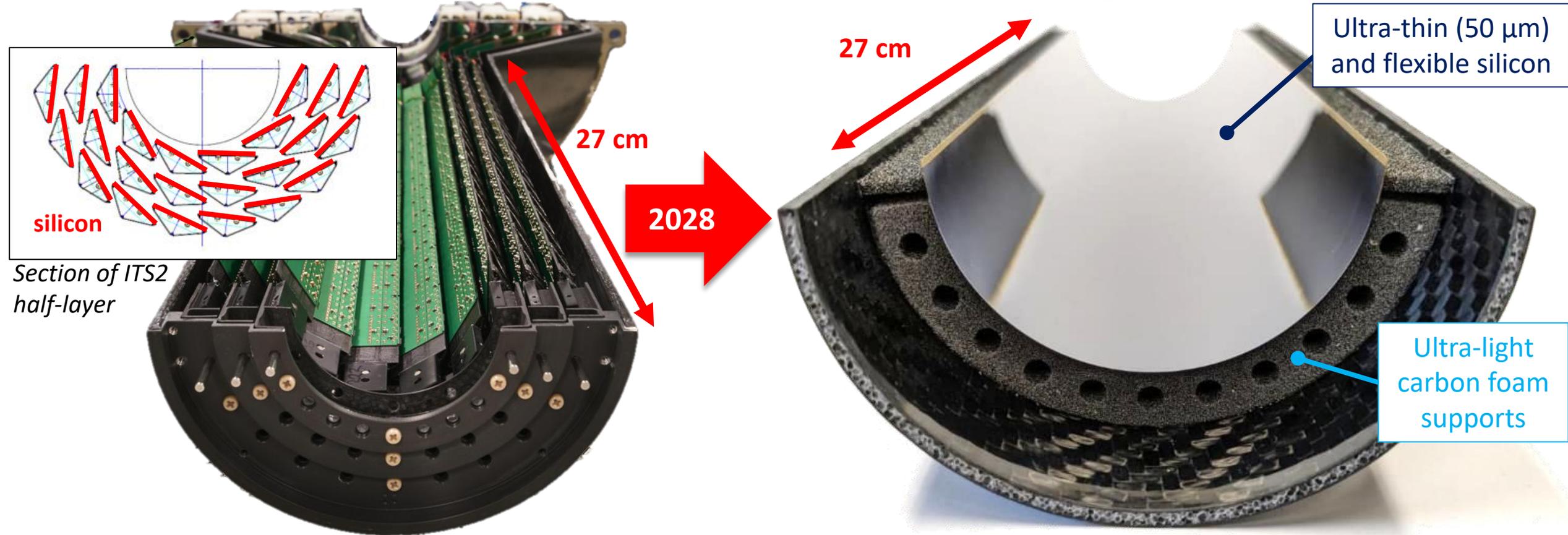


- Installed in 2021
- Monolithic Active Pixel silicon Sensors (MAPS)
- Material budget of 0.36% X_0 per layer
- 50 μm thick sensor = 0.05% X_0
- Radius 1st layer = 24 mm

The Inner Tracking System

ITS2 innermost 3 half-layers

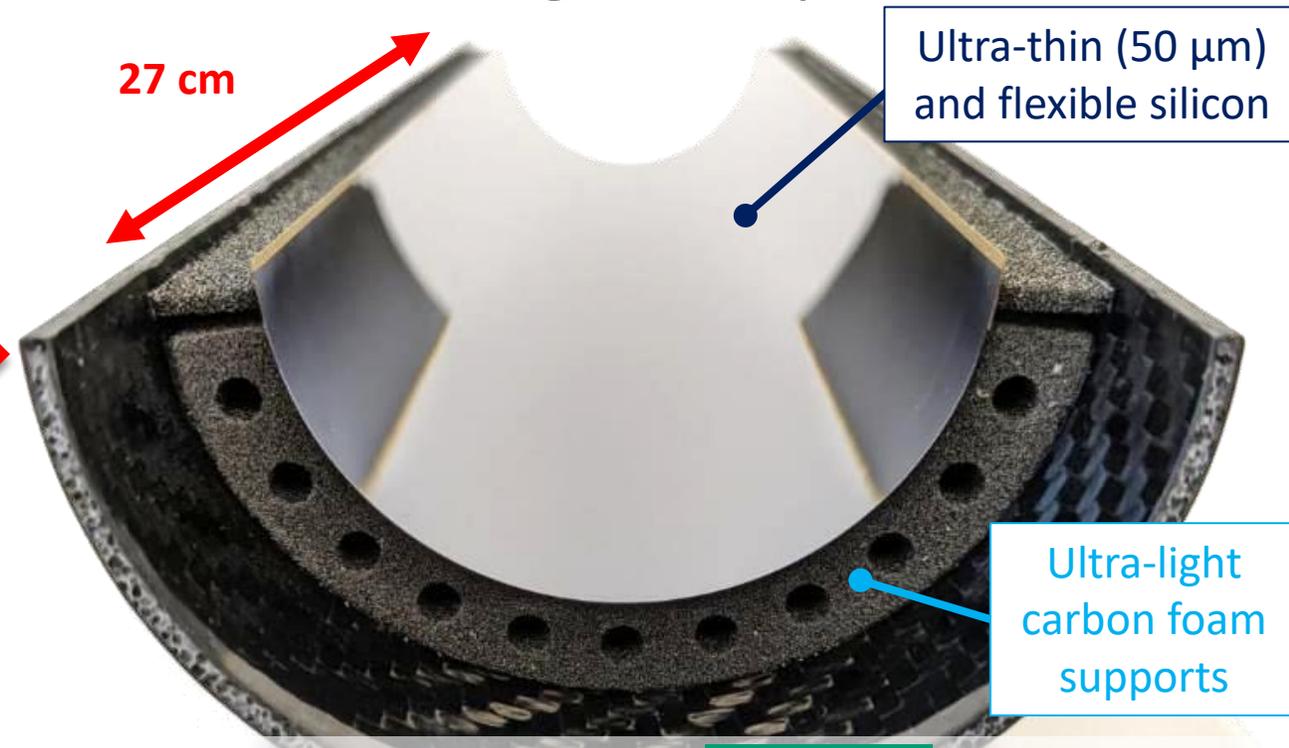
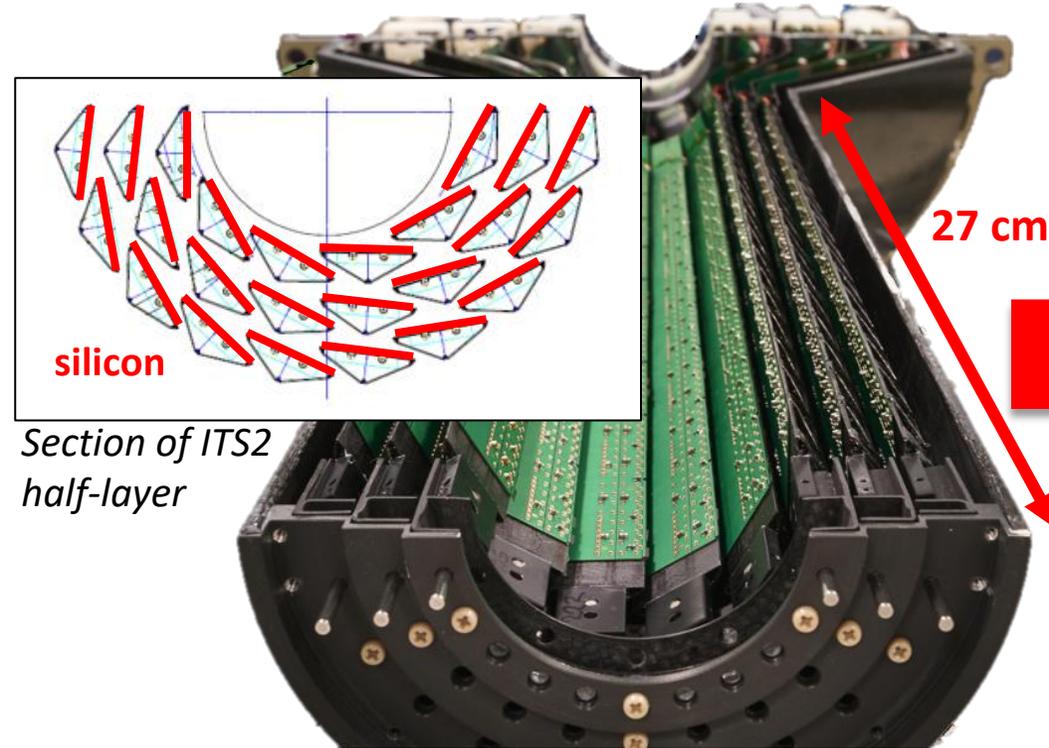
ITS3 single half-layer model



Technical Design Report approved in 2024: [link](#)

ITS2 innermost 3 half-layers

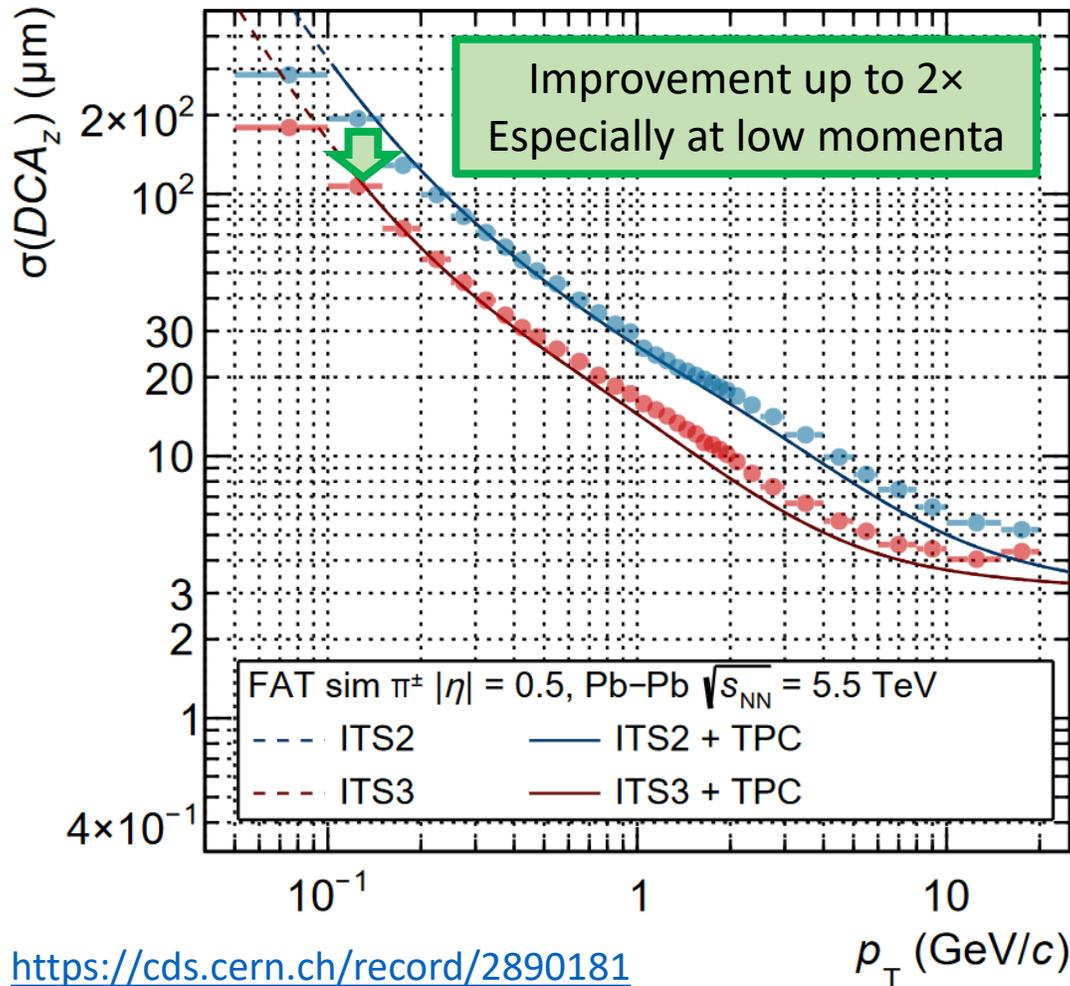
ITS3 single half-layer model



- Material budget of **0.36% X_0** per layer
- 50 μm thick sensor = 0.05% X_0
- Radius 1st layer = **24 mm**
- Beam pipe **700 μm** thick, radius **18 mm**

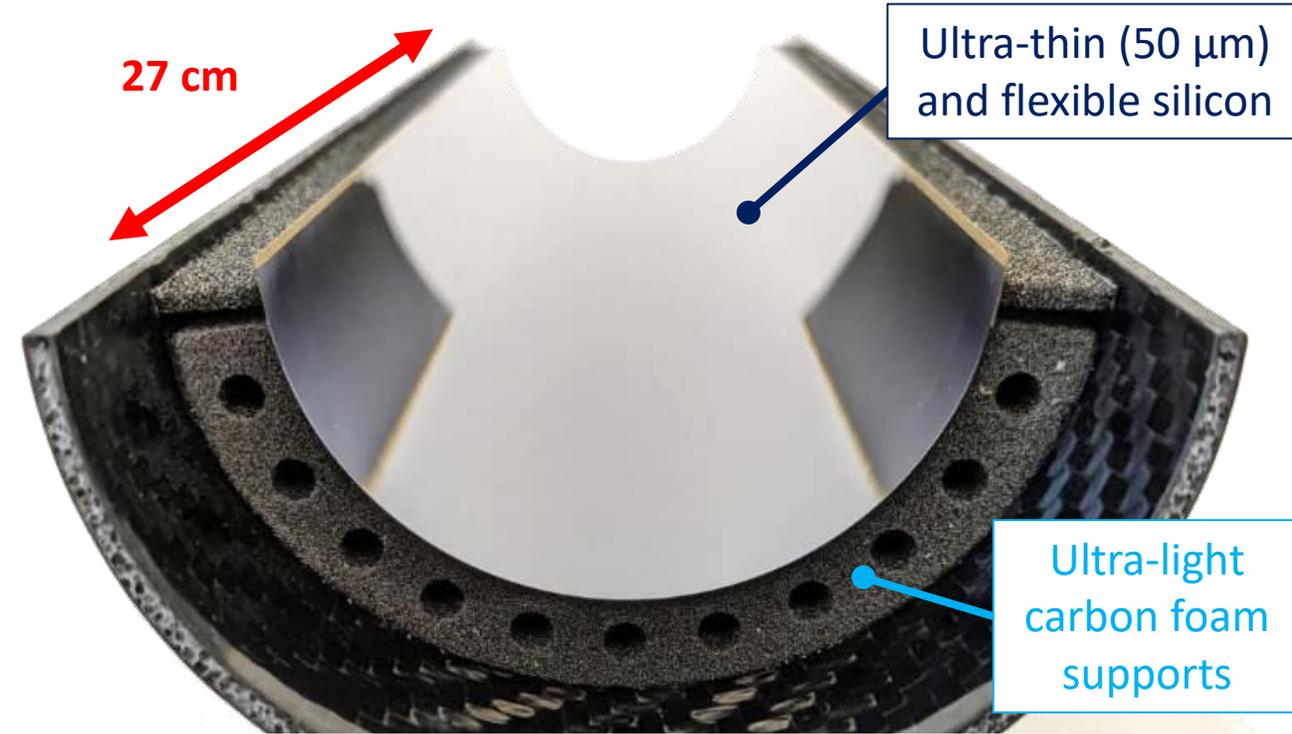
- Material budget of **0.09% X_0** per layer
- 50 μm thick sensor
- Radius 1st layer = **19 mm**
- Beam pipe **500 μm** thick, radius **16 mm**

Pointing resolution



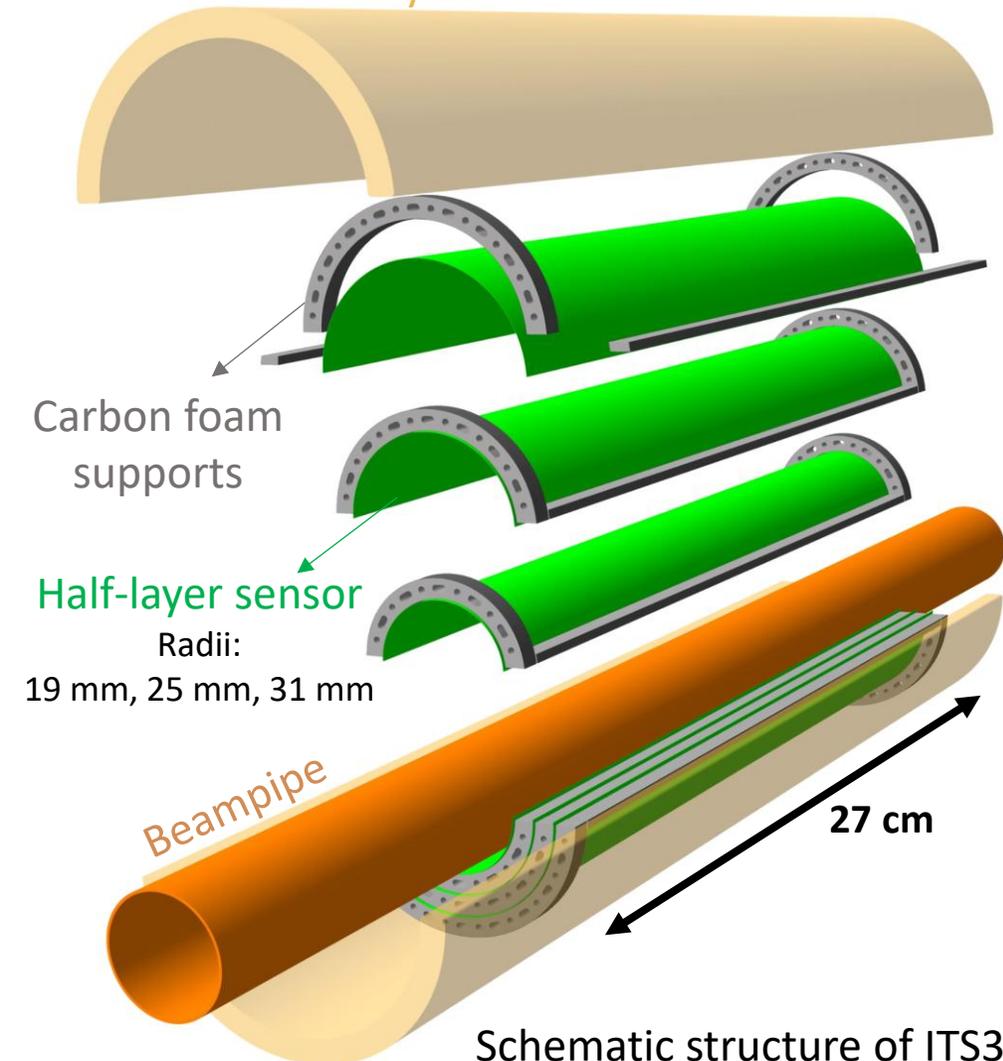
<https://cds.cern.ch/record/2890181>

ITS3 single half-layer model



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Cylindrical Structural Shell

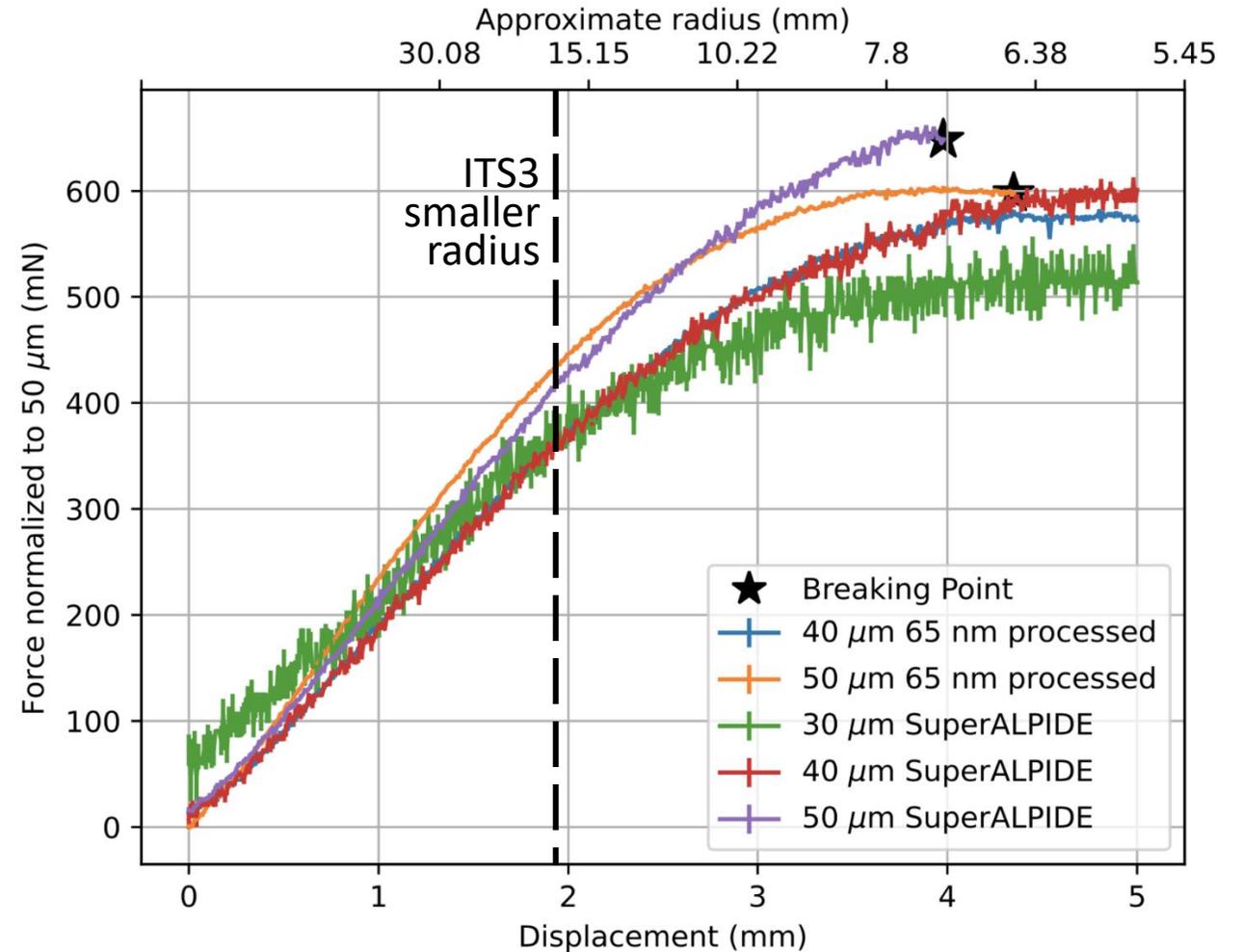
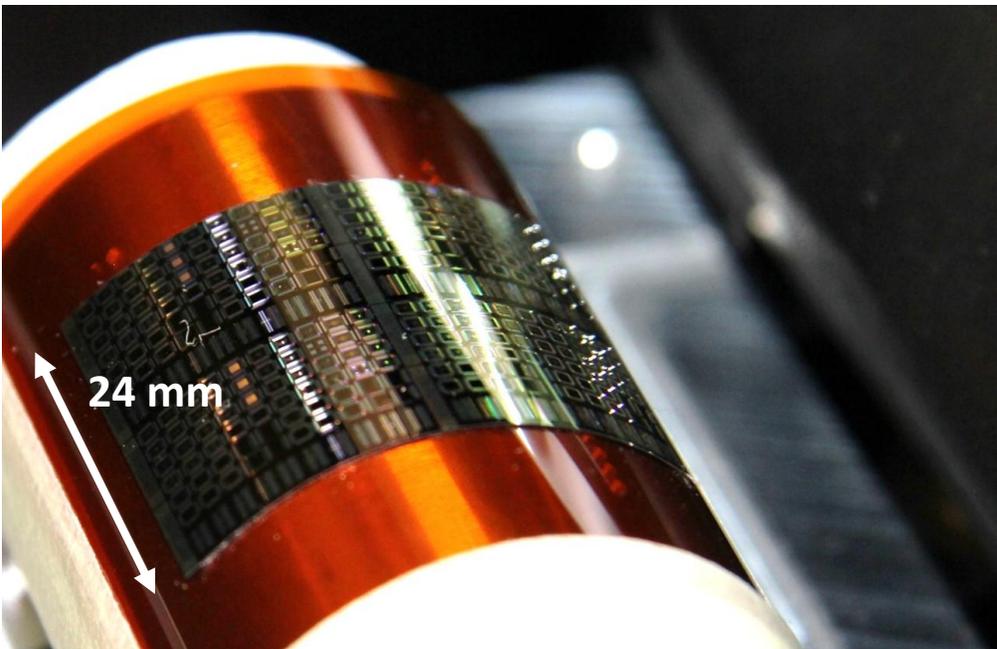


ITS3 key elements:

1. 3 truly cylindrical **self-supporting** layers
2. Each layer made by **2 flexible MAPS** sensors which:
 1. have a **large-area**, up to $O(10 \times 27 \text{ cm}^2)$
 2. are **ultra-thin** ($50 \mu\text{m}$)
3. Ultra-light carbon foam structures keep the sensor in position
Air cooled ($T_{\text{air}} \sim 20 \text{ }^\circ\text{C}$)

Bent MAPS

- 50 μm MAPS can be bent to the ITS3 target

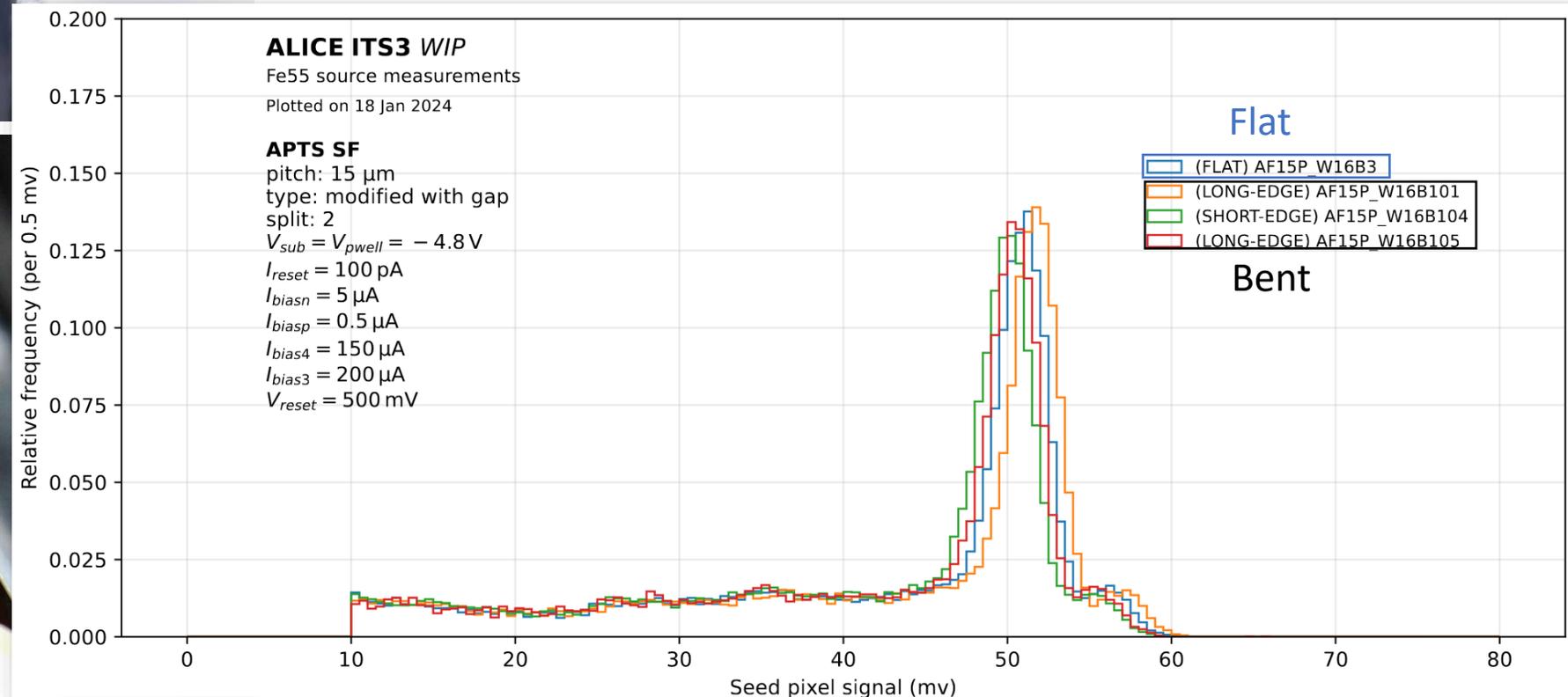
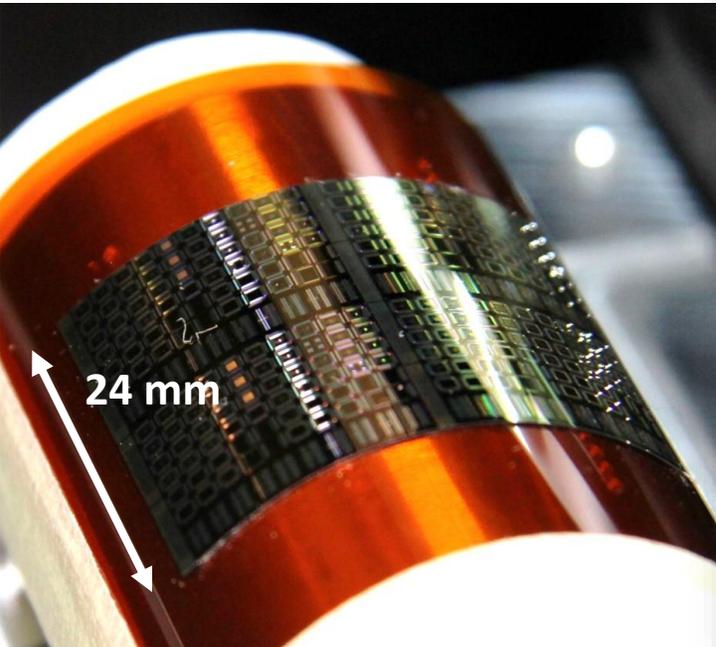


Silicon sensor bending



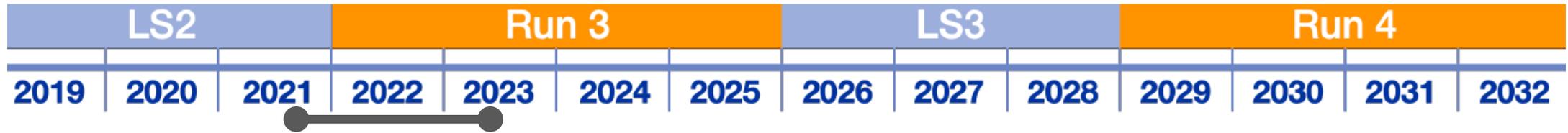
- 50 μm MAPS can be bent to the ITS3 target
- Bent ALPIDE \rightarrow performance is unaffected
- Confirmed using analog test structures in the 65 nm CMOS process

• doi.org/10.1016/j.nima.2021.166280
 • <https://arxiv.org/abs/2502.04941>



Chip development

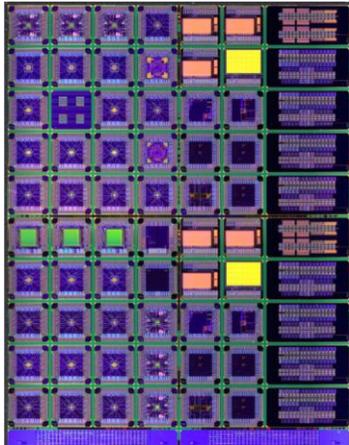
Chip development roadmap



Past: received in Sept 2021

MLR1 – First MAPS in CMOS 65 nm

- Small-scale prototypes
- Technology qualified
- Performance explored beyond ITS3 requirements



DPTS: 1. <https://doi.org/10.1016/j.nima.2023.168589>

2. <https://arxiv.org/abs/2505.05867>

APTS-SF: <https://doi.org/10.1016/j.nima.2024.169896>

APTS-OA: <https://doi.org/10.1016/j.nima.2024.170034>

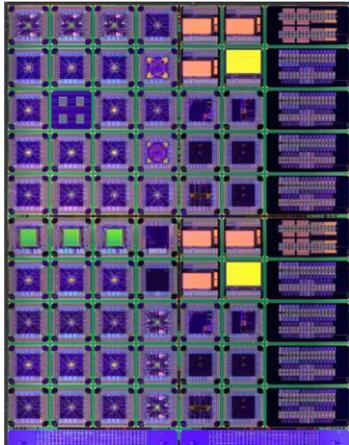
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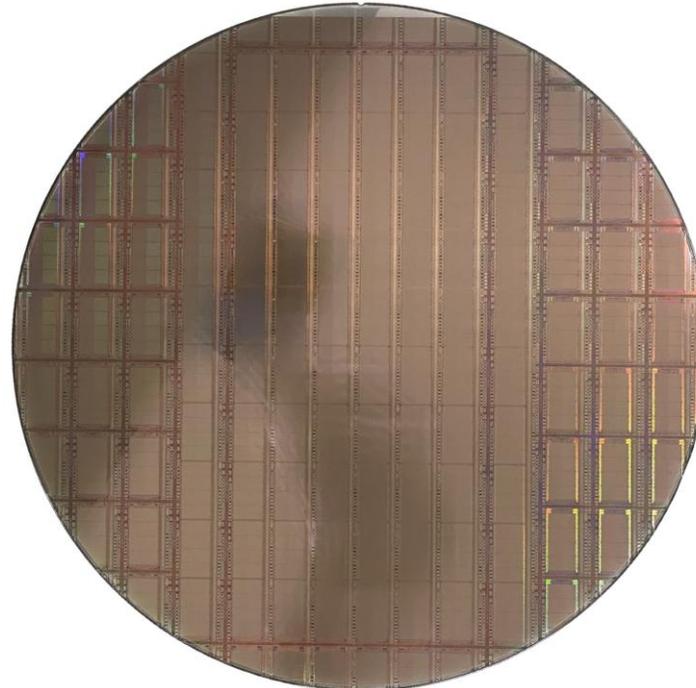
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Present: received in May 2023

ER1 – First stitched MAPS

- First large-area prototypes
- Stitching validation

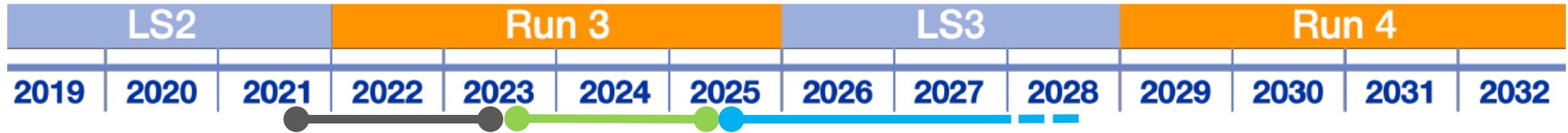


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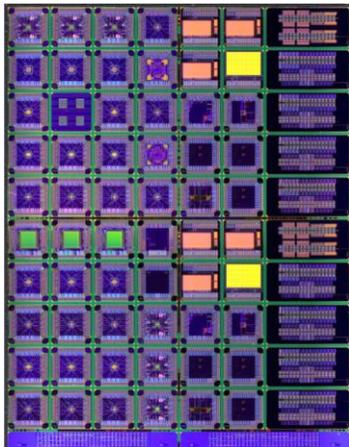
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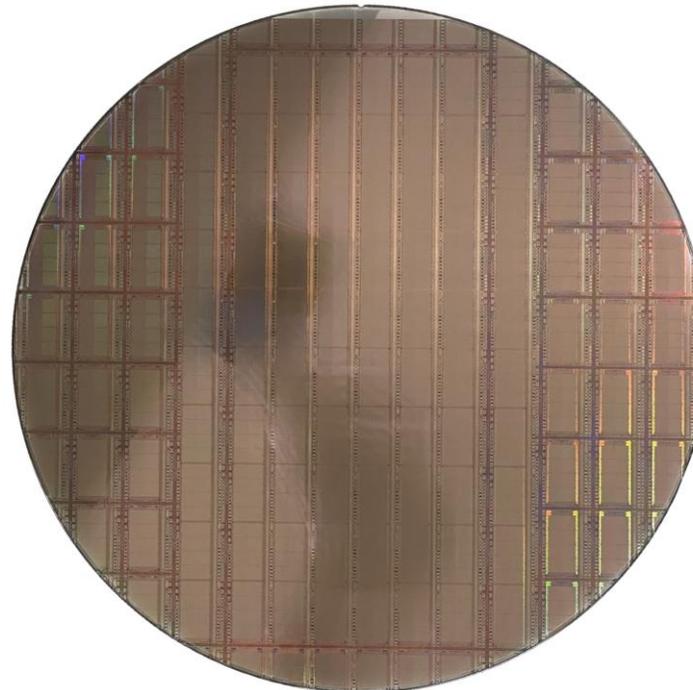
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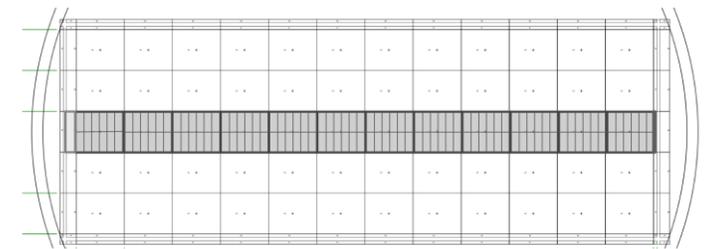
- First large-area prototypes
- Stitching validation



Future: exp. ER2 in Nov 2025, ER3 2027

ER2 – Full-scale prototype

ER3 – Final sensor production



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Large-area MAPS: stitching

Lithographic mask



Stitched sensors:

- Repeated identical but functionally independent units
- In-silicon interconnections and peripheral structures along the outer edges of the resulting large-area chip

Ø = 300 mm (12") silicon wafer

Lithographic mask



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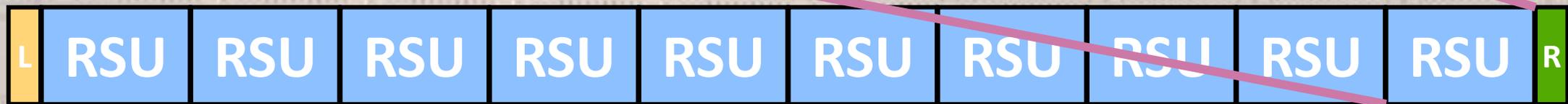
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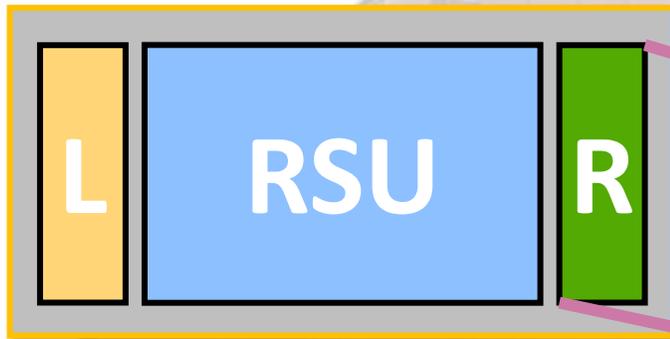
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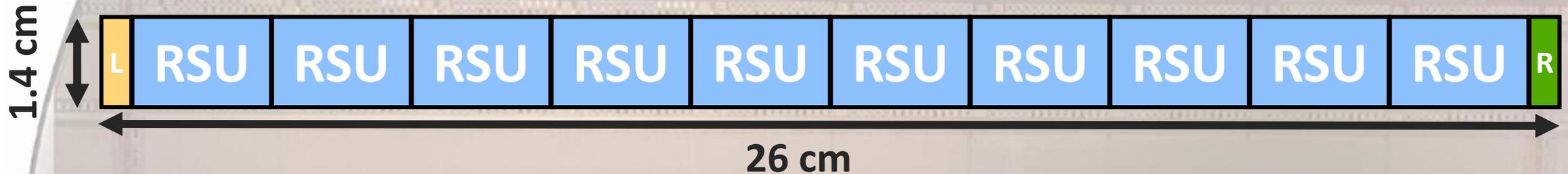
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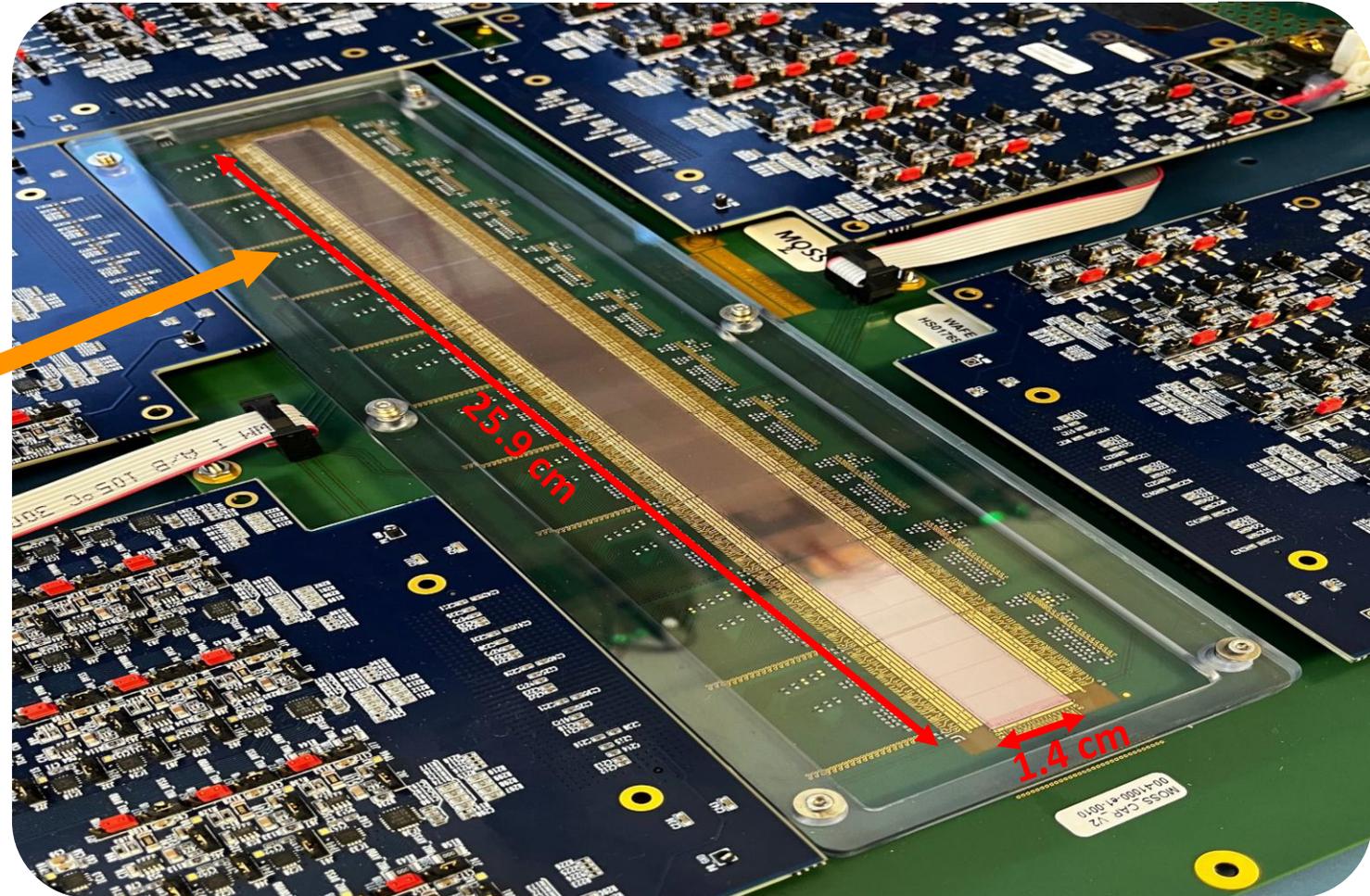
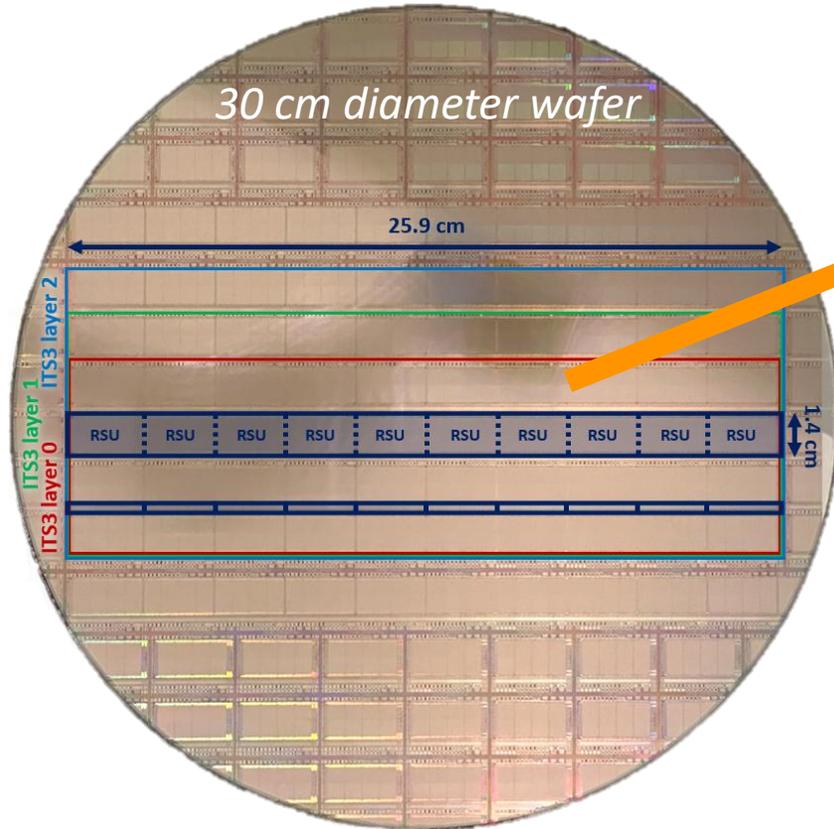
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First stitched prototype



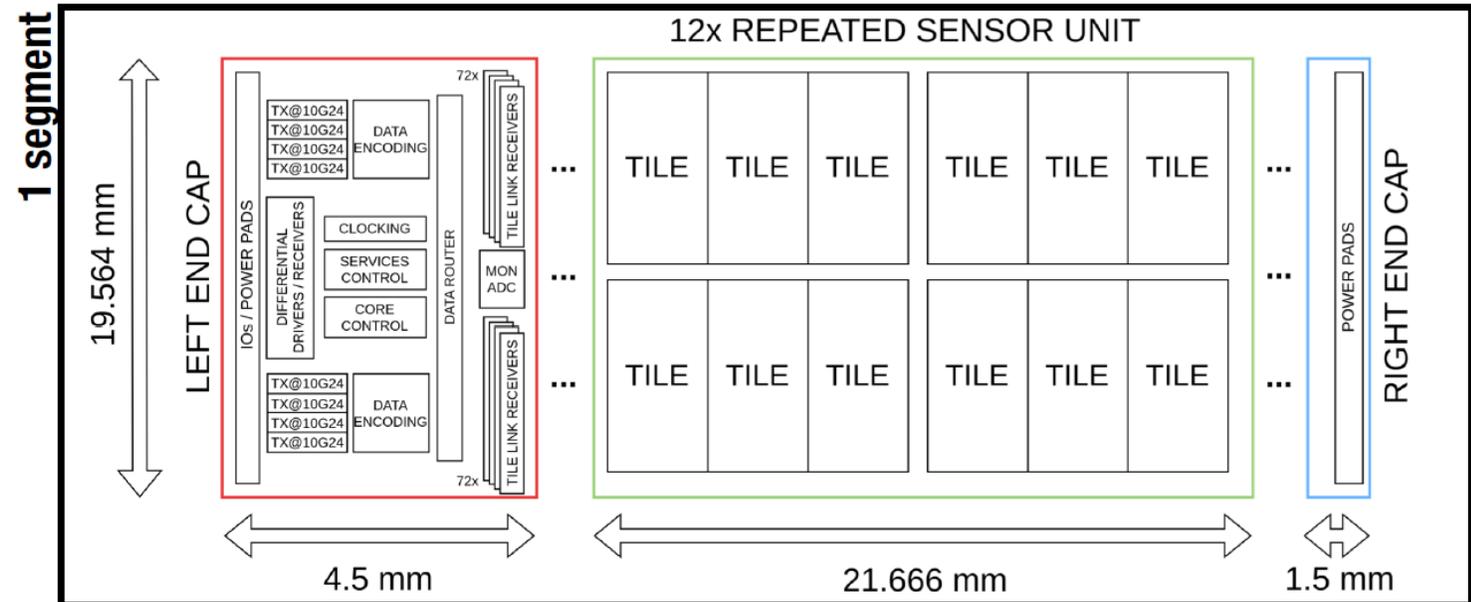
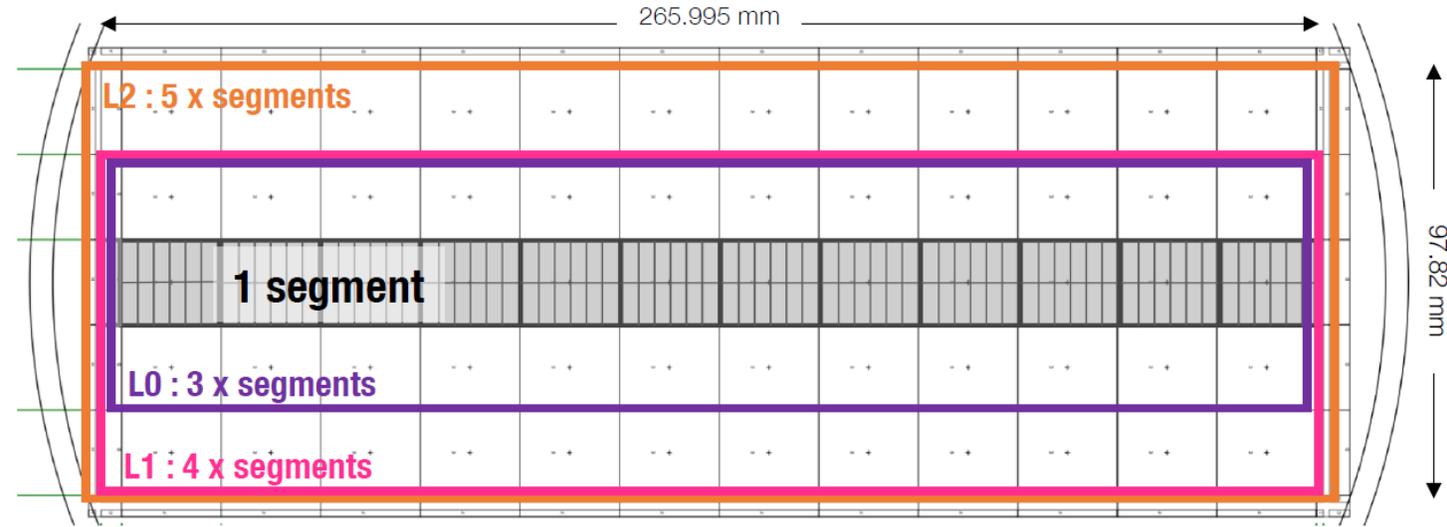
ER1: **MO**nolithic **Stitched** Sensor, MOSS:

- $25.9 \times 1.4 \text{ cm}^2$

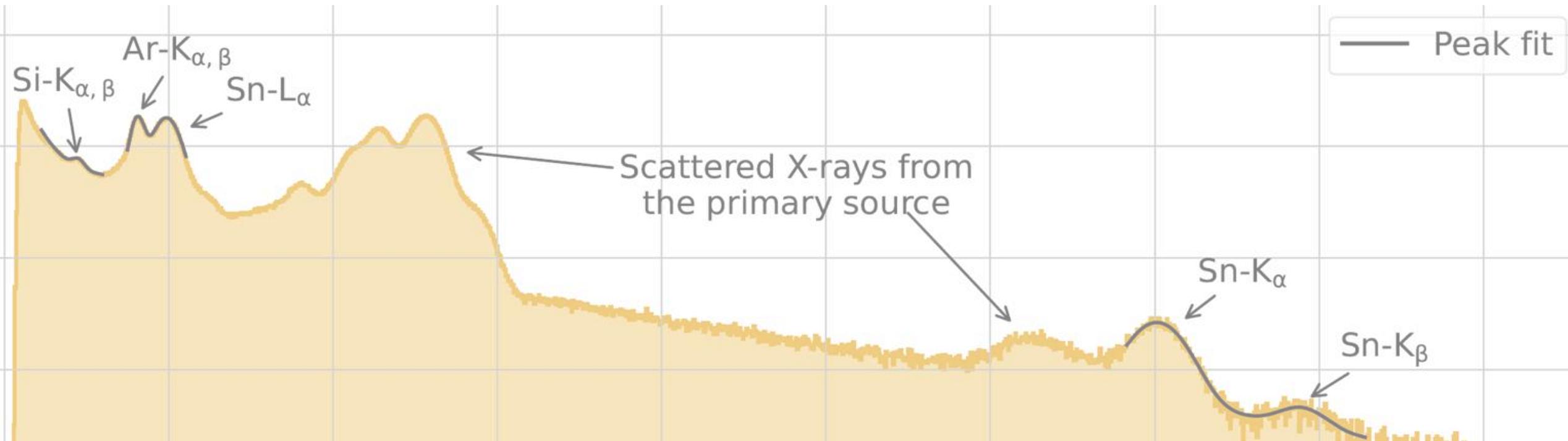


MOSAIX:

- Divided in segments
 - Pixel pitch: $20.8 \times 22.8 \mu\text{m}$
 - 12 RSU per segment
 - 12 tiles per RSU
 - Different pixel variants for operational margins
-
- Design in-depth verification ongoing
 - ER2 implementation procedure and scripts identical for ER3
 - Final ER2 submission → June 2025

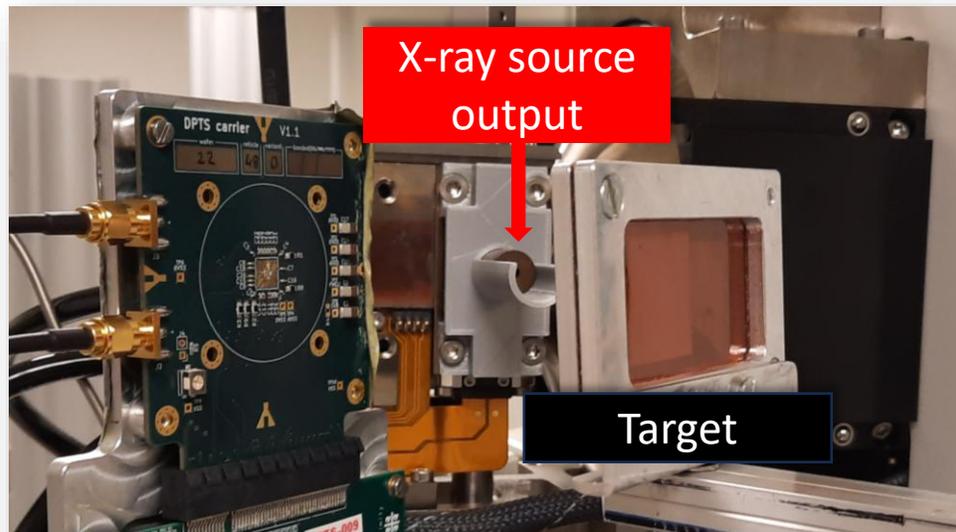
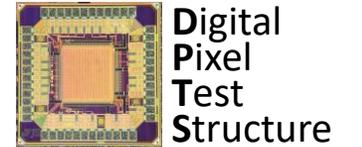
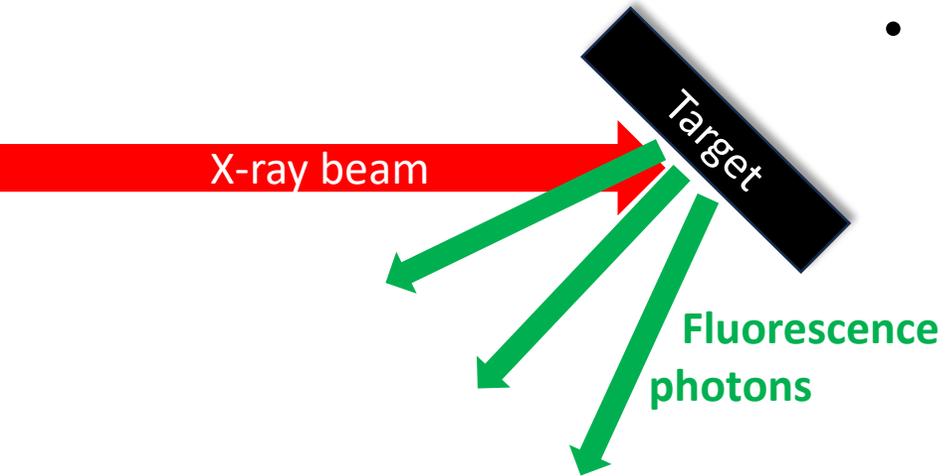


Energy calibration



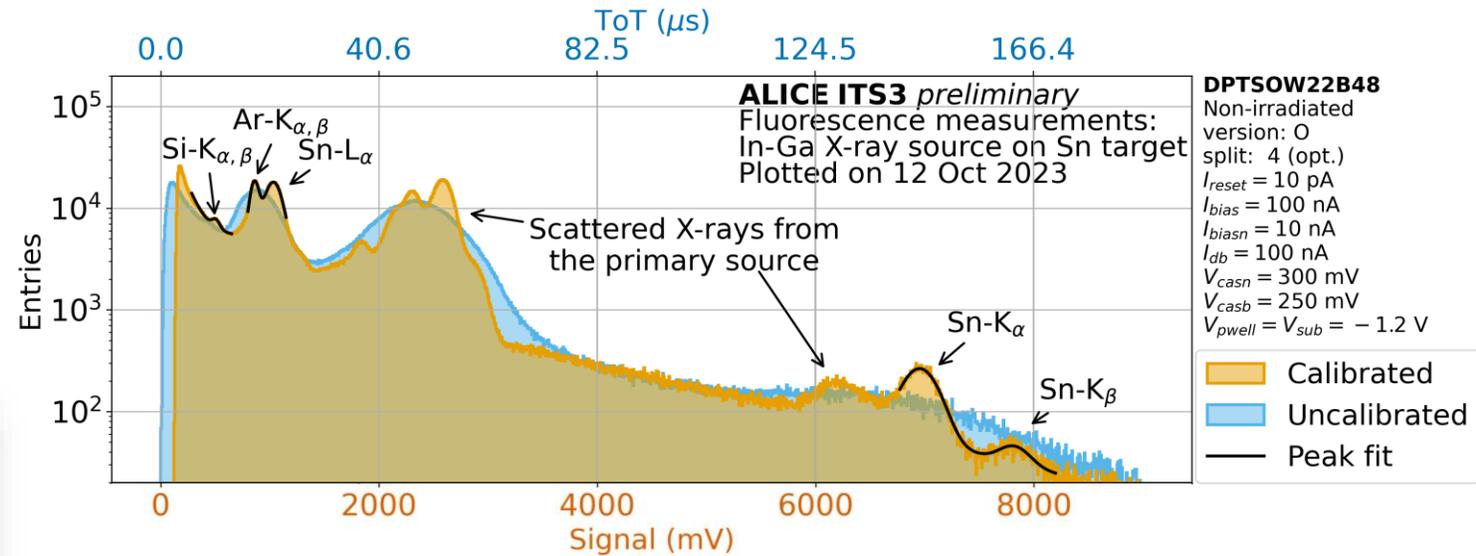
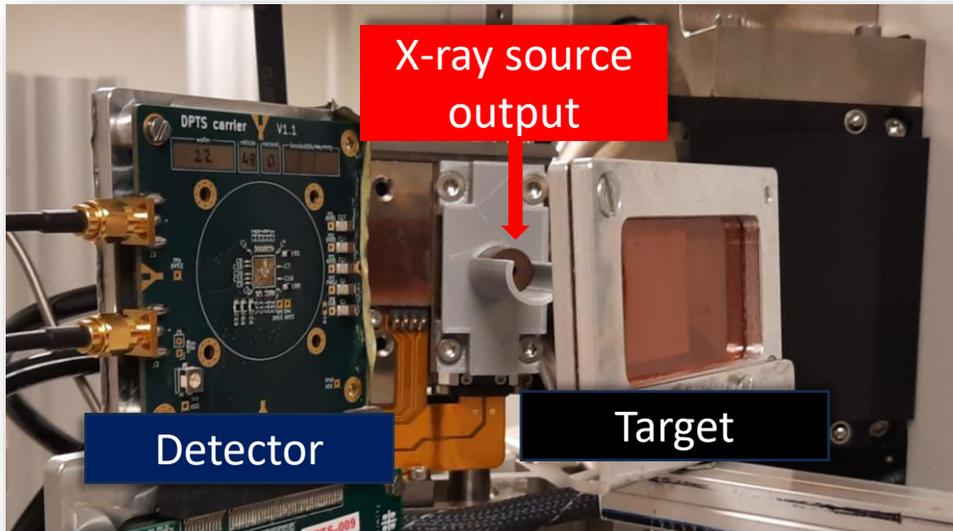
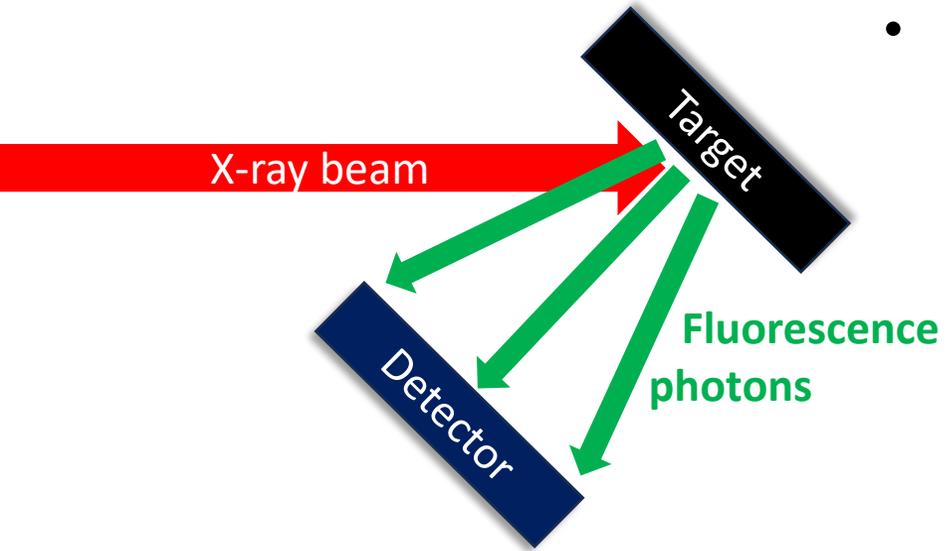
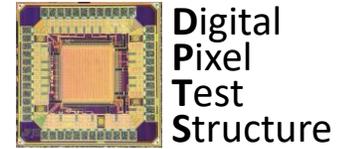
DPTS: X-ray fluorescence

- Fluorescence photons from Sn target

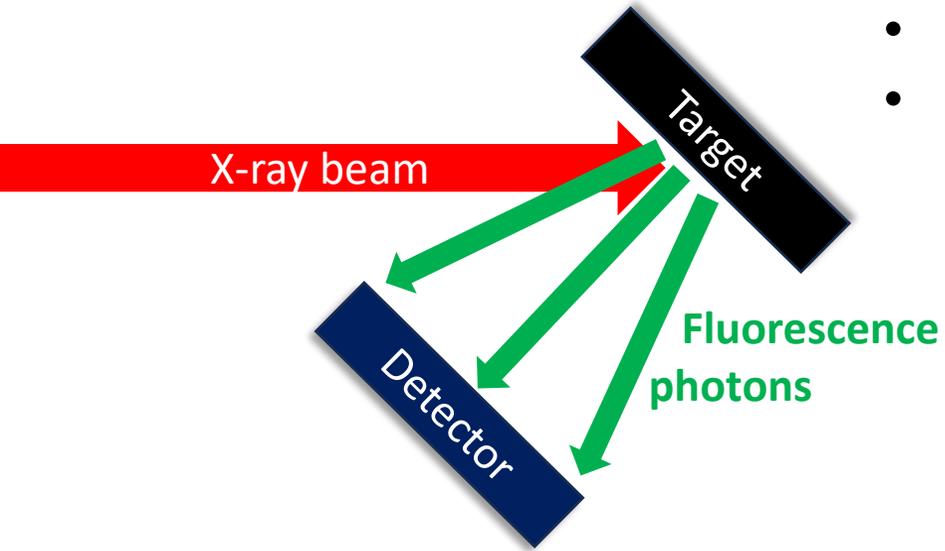


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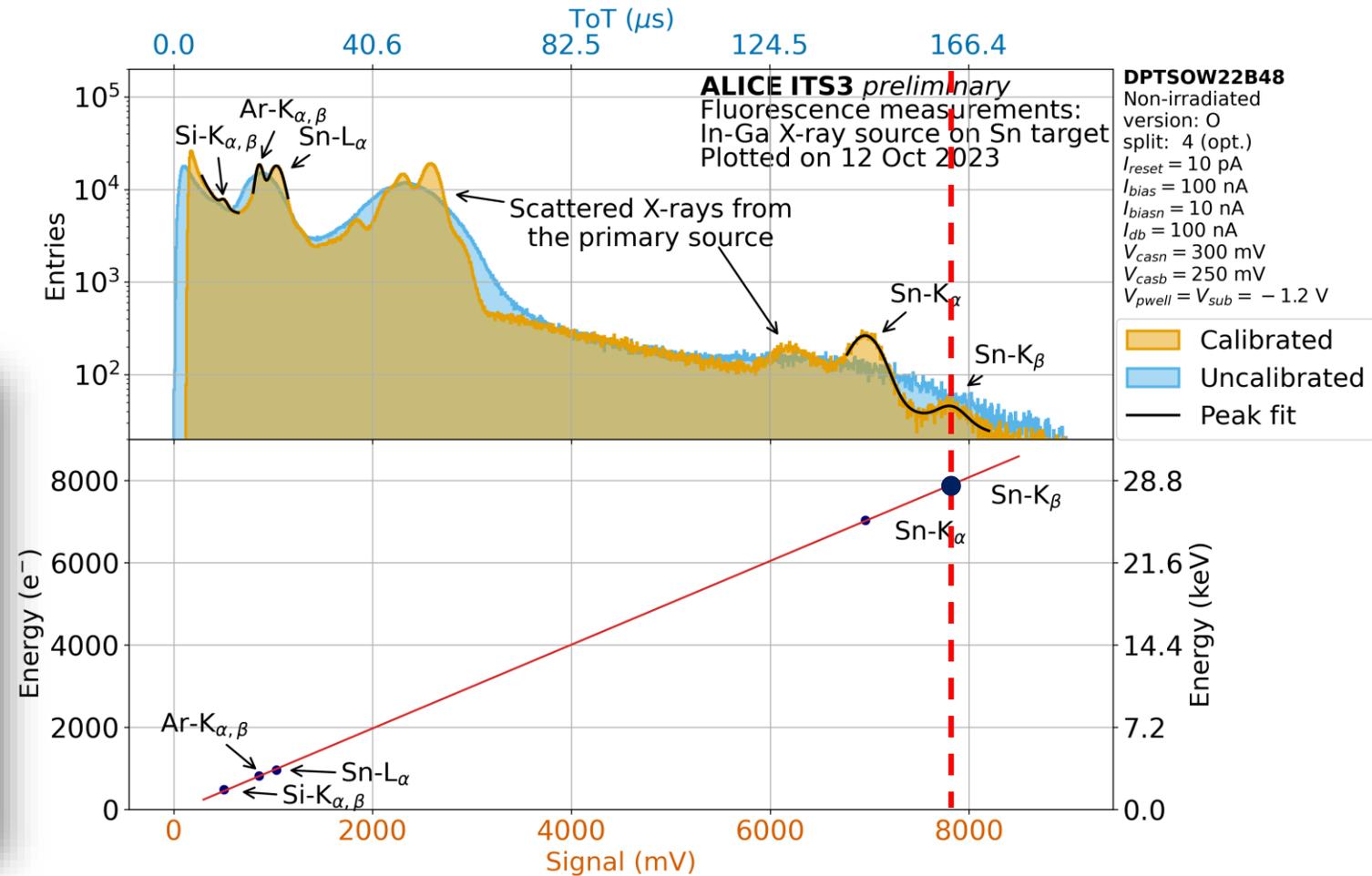
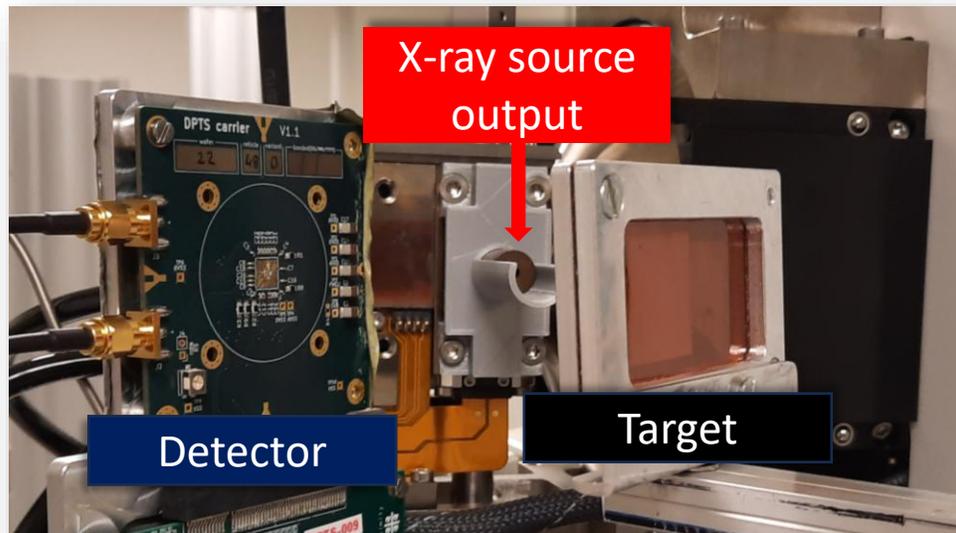
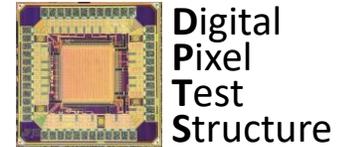
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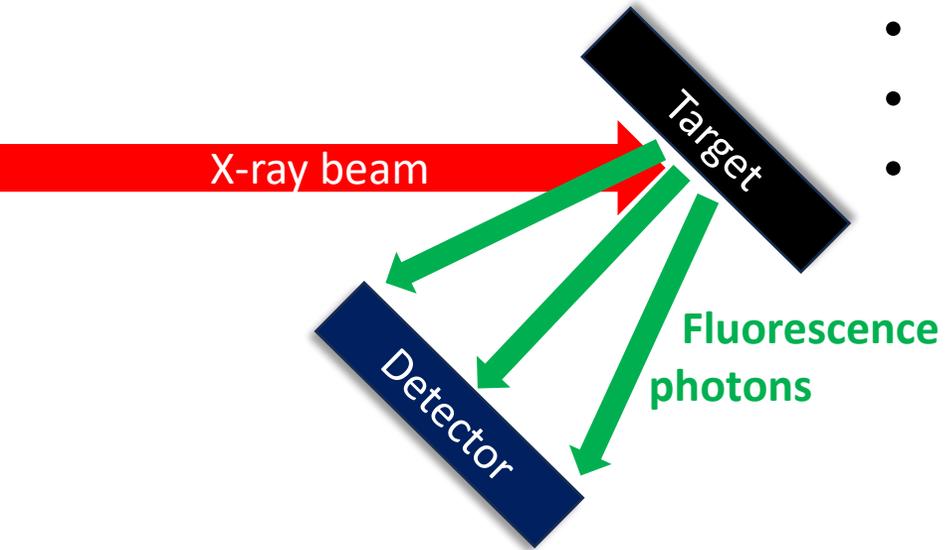


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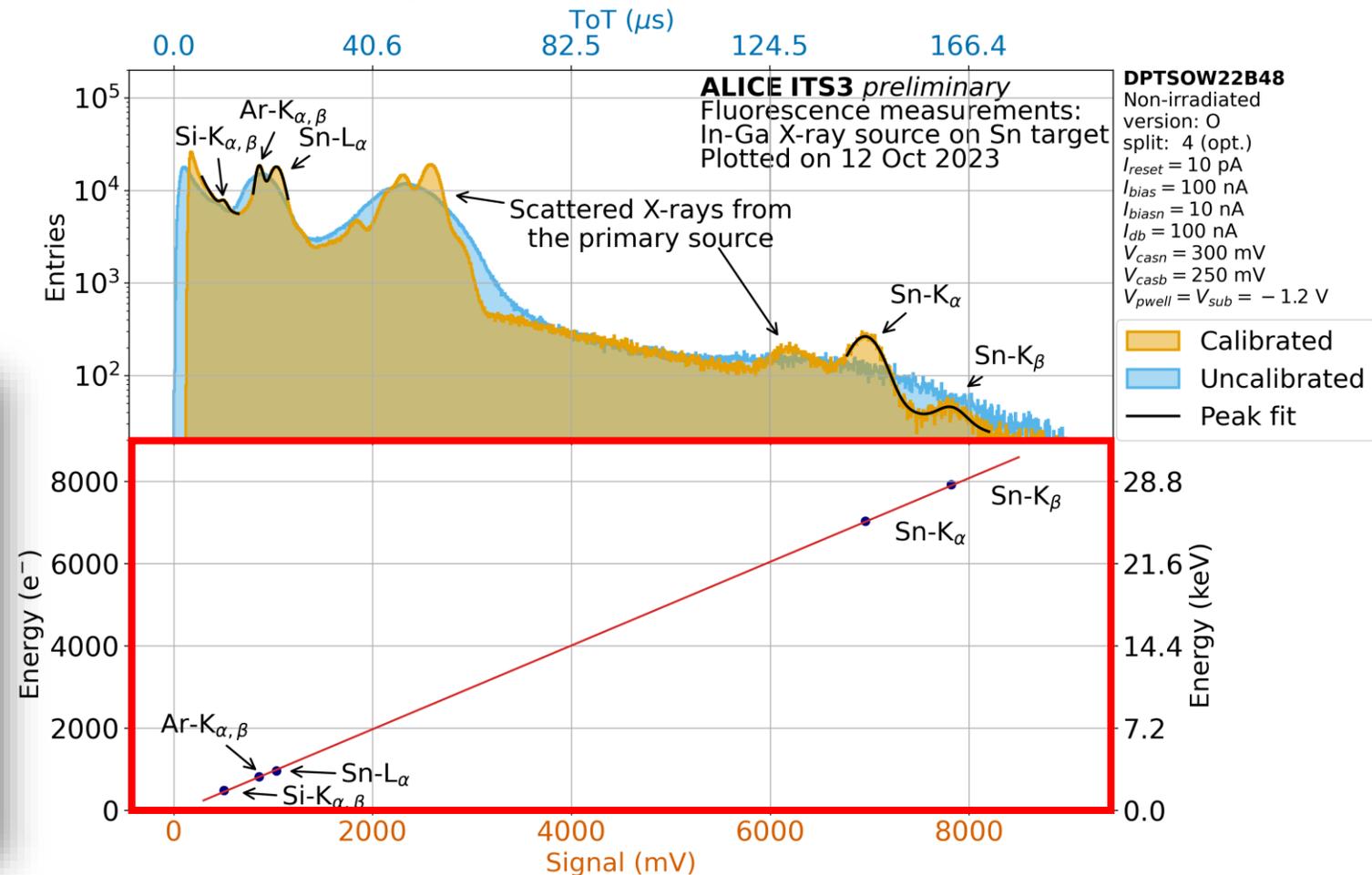
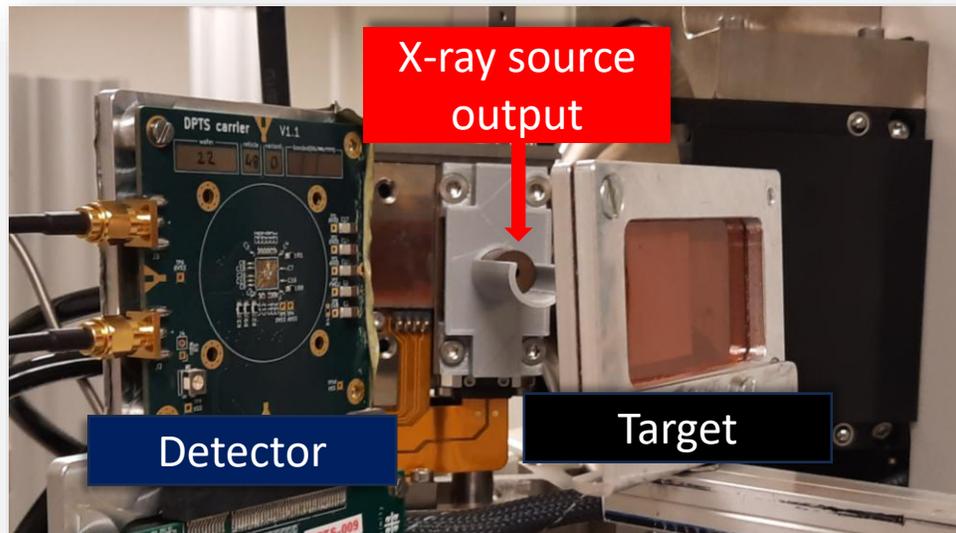
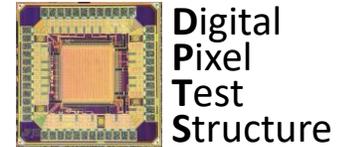


- Fluorescence photons from Sn target
- Energy calibration of the response up to **28.8 keV**



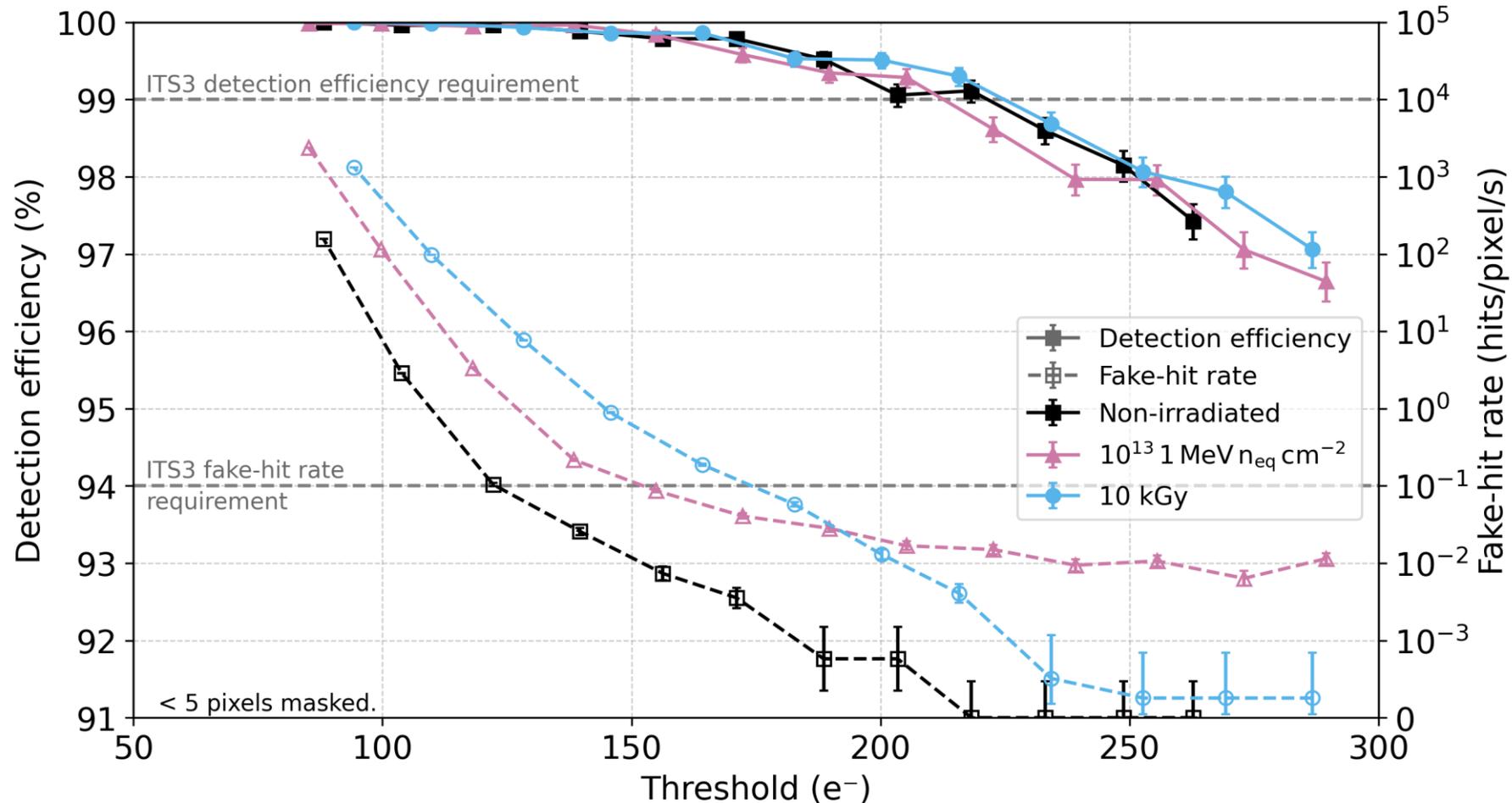


- Fluorescence photons from Sn target
- Energy calibration of the response up to **28.8 keV**
- Demonstrated **linearity** of the response

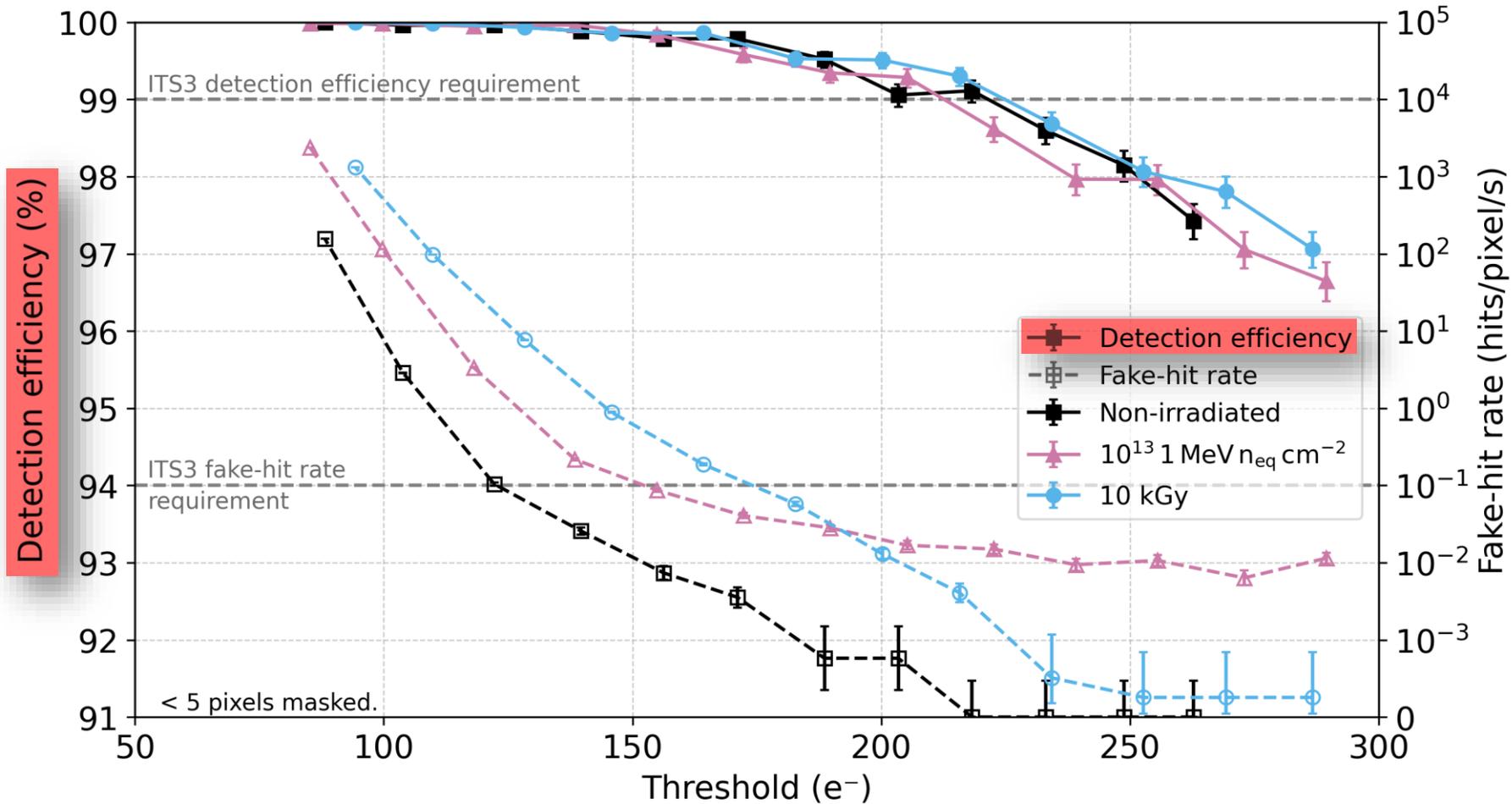


- Non-Ionizing Energy Loss (NIEL) affects mainly the charge collection process
- Total Ionizing Dose (TID) radiation affects the in-pixel front-end

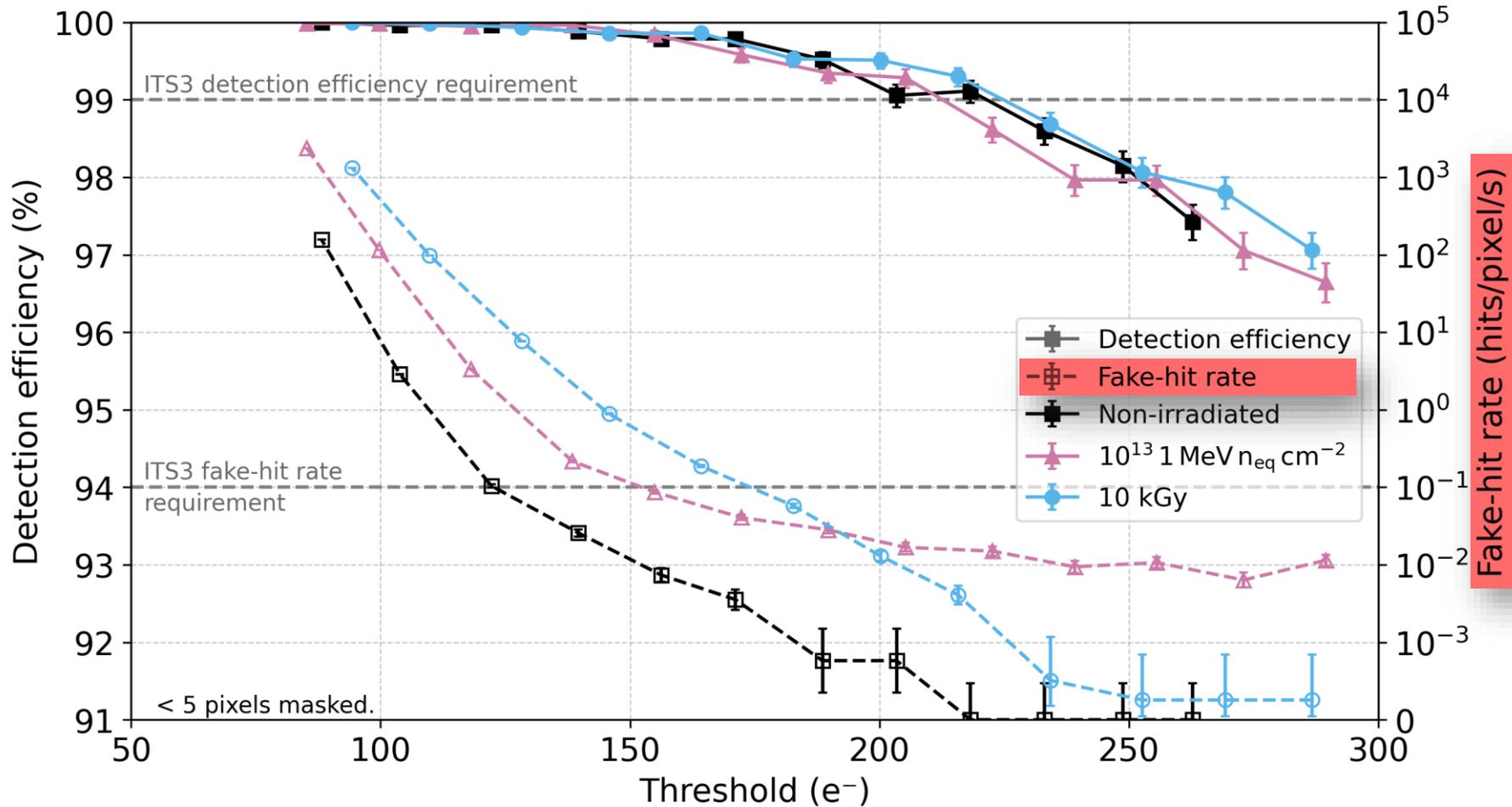
See A. Sturniolo poster



- In-beam measurements: **detection efficiency**

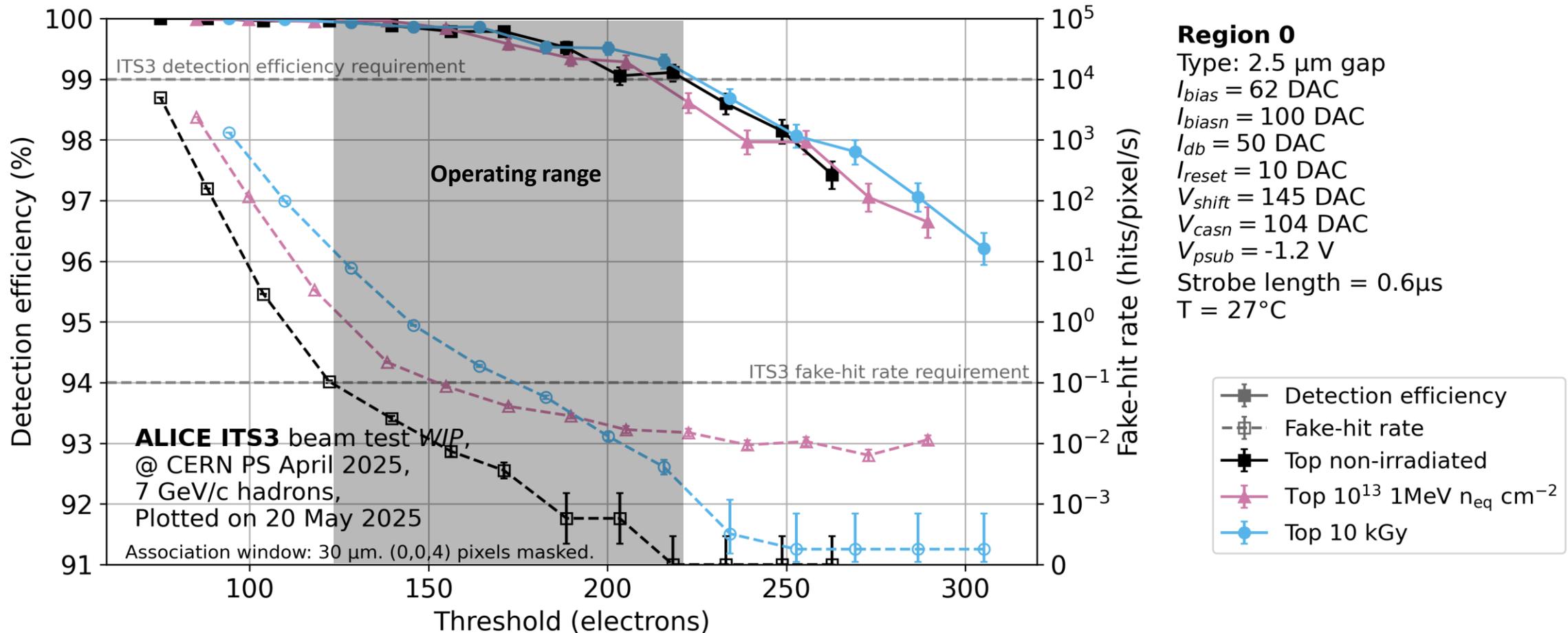


- In-beam measurements: detection efficiency
- Functional characterization: Fake Hit Rate (FHR)



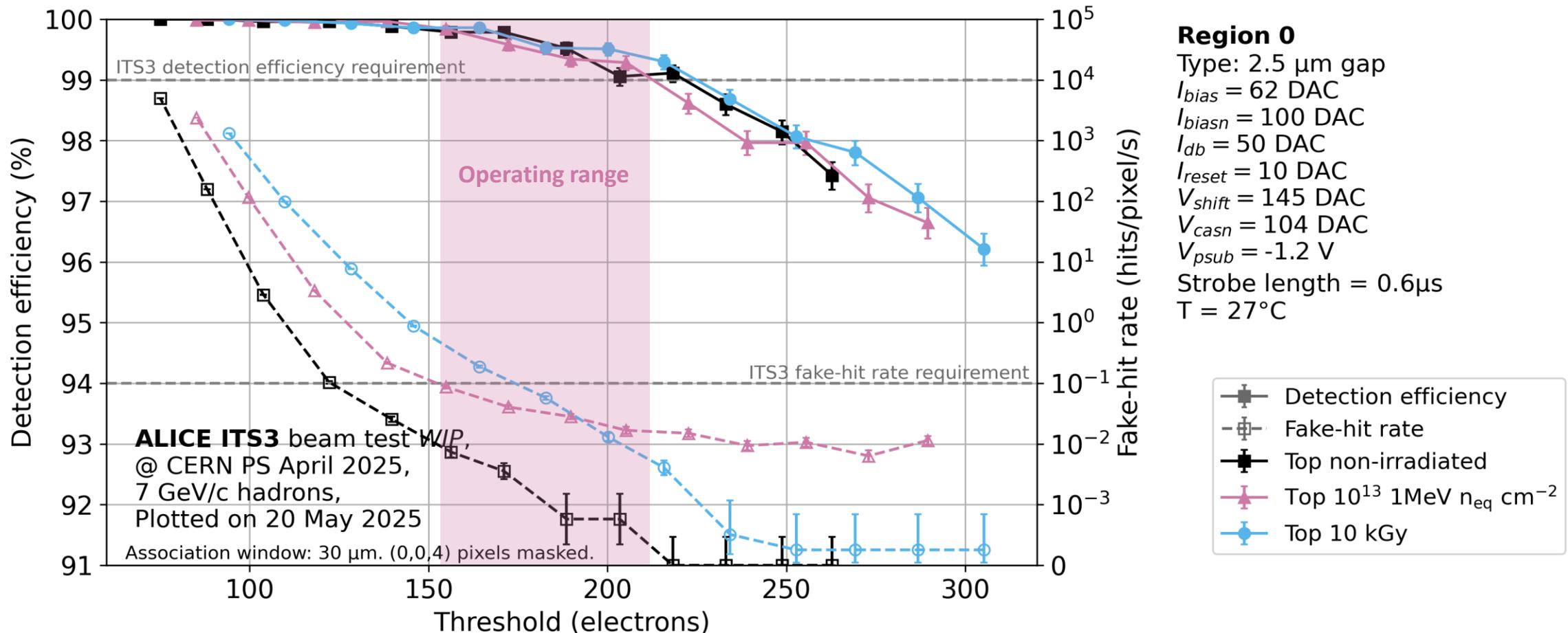
- Efficiency higher than 99% in a wide range of thresholds

See A. Sturniolo poster



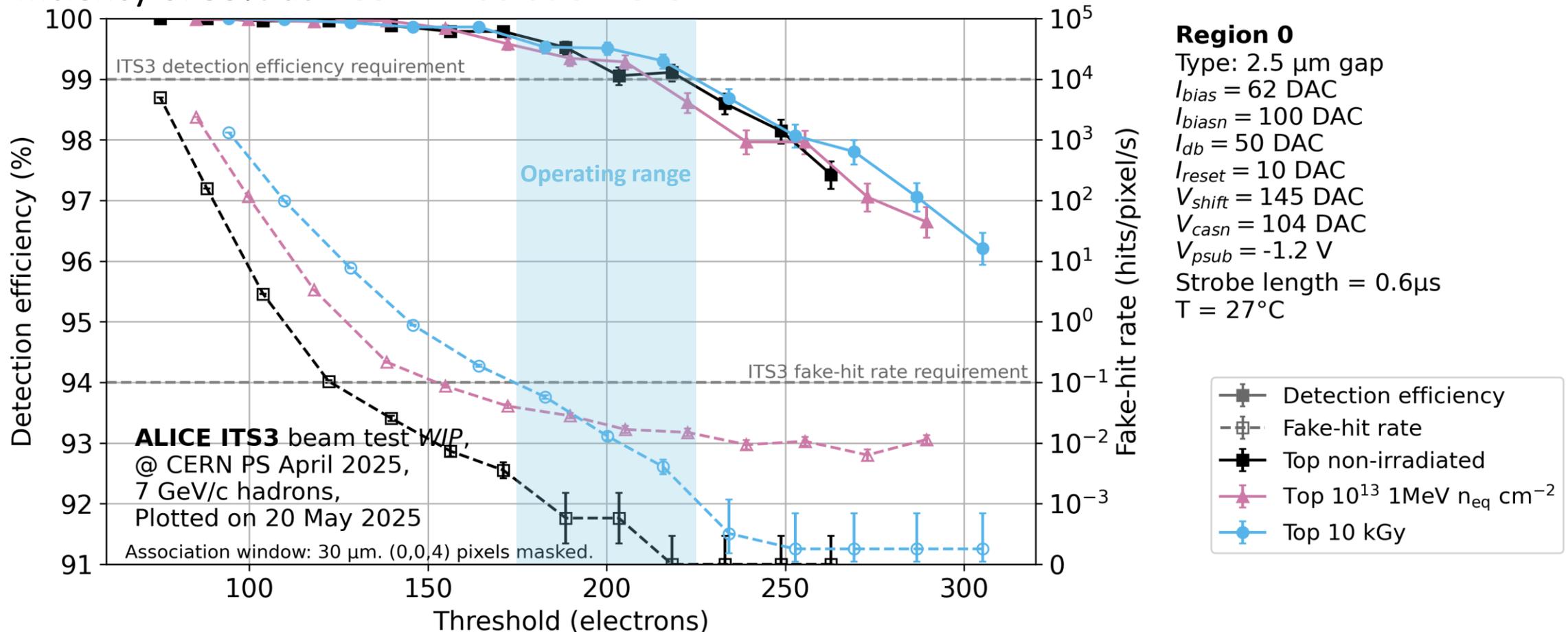
- Efficiency higher than 99% in a wide range of thresholds
- Efficiency of 99% at **ITS3 NIEL radiation level**

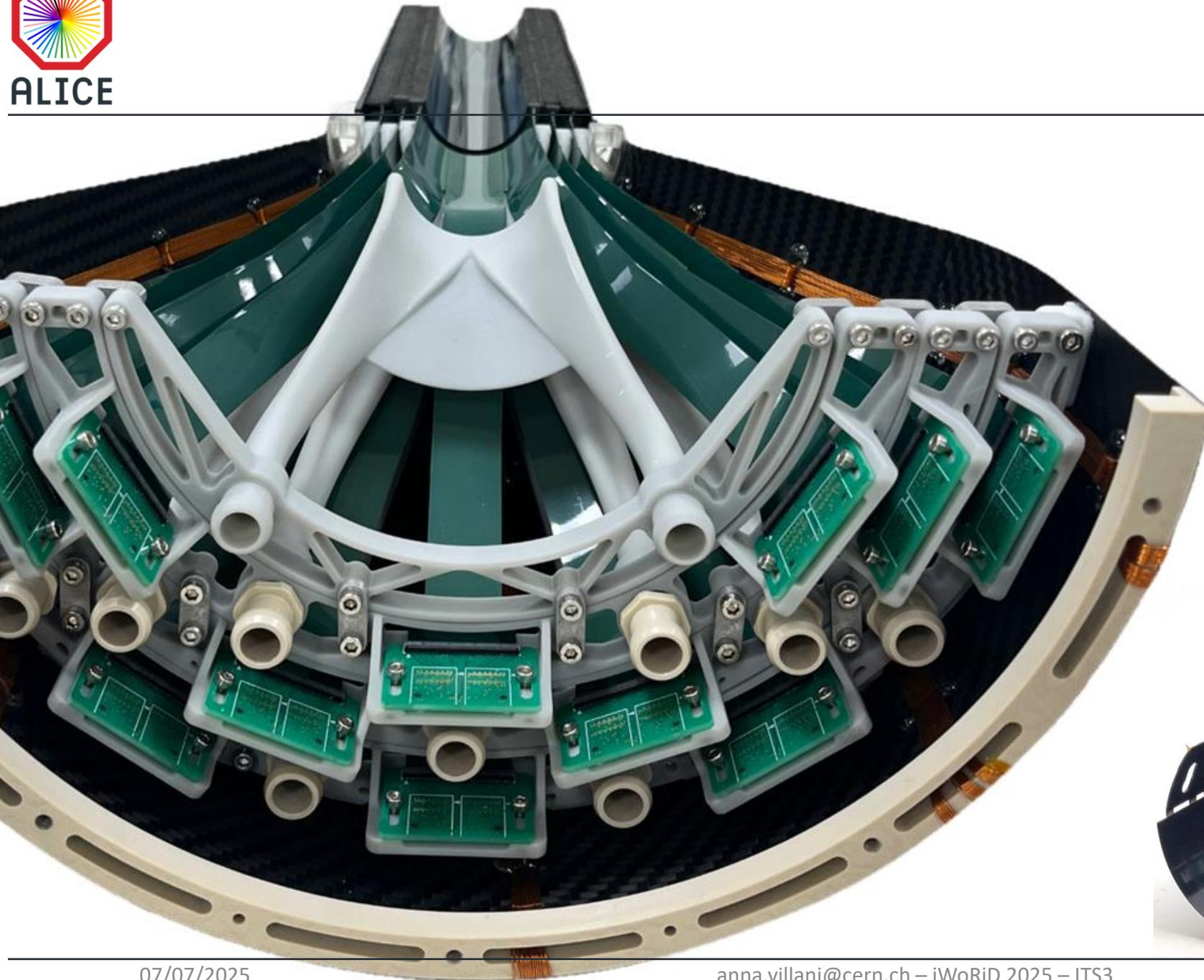
See A. Sturniolo poster



- Efficiency higher than 99% in a wide range of thresholds
- Efficiency of 99% at **ITS3 NIEL radiation level**
- Efficiency of 99% at **ITS3 TID radiation level**

See A. Sturniolo poster





Mechanics and cooling



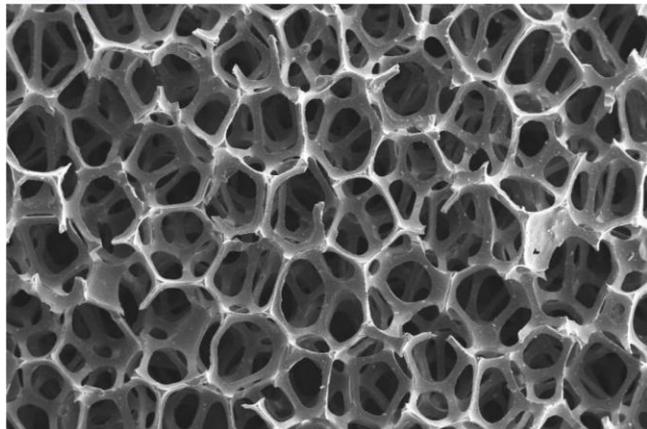
Ultra-light mechanics → material budget record

Carbon foam used as support and radiator:

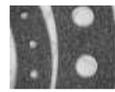
- Carbon (RVC) Duocel® for mechanical support
- Allcomp K9 standard density as cooling radiator



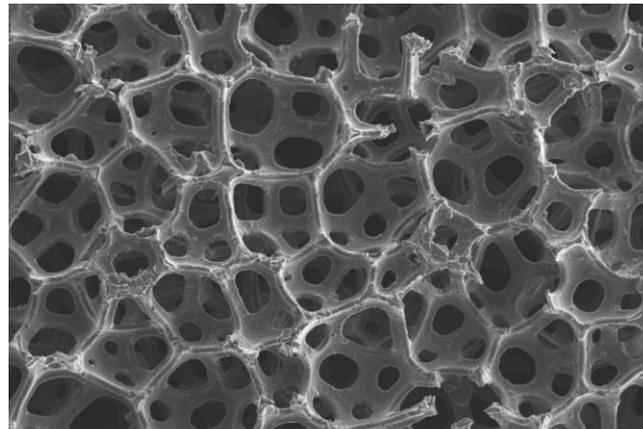
Carbon (RVC) Duocel®:
support



500 μm EHT = 10.00 kV WD = 11.5 mm Signal A = SE2 Sample ID = #2_ Anite Perez Fontenla Date: 18 Jun 2020 Mag = 30 X EN



Allcomp K9 standard density:
support and cooling

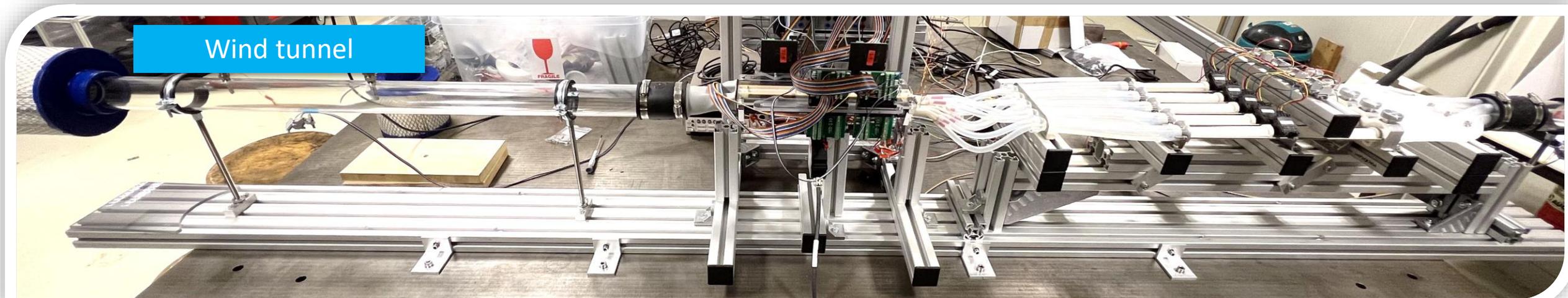


300 μm EHT = 10.00 kV WD = 10.6 mm Signal A = SE2 Sample ID = ALLCOMP#1_ Anite Perez Fontenla Date: 30 Jun 2020 Mag = 50 X EN

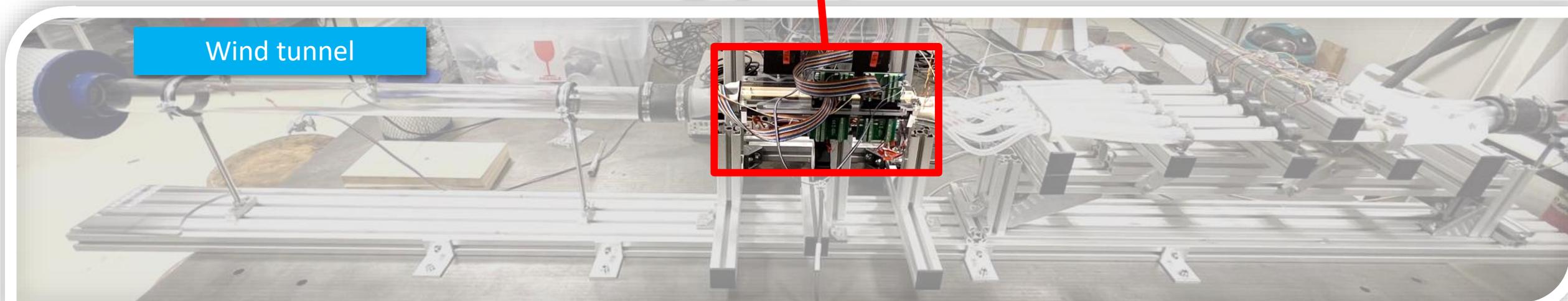
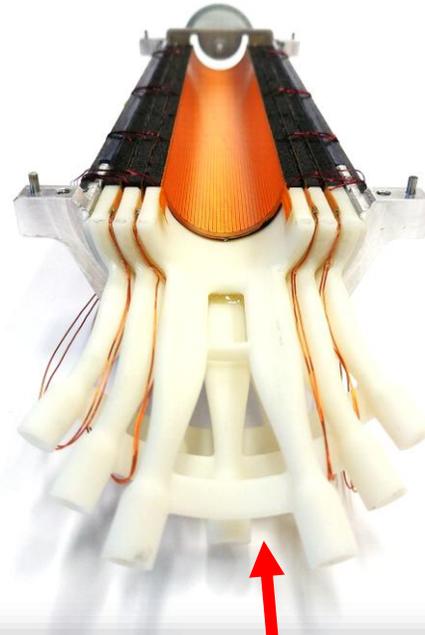


ITS3
Engineering
Model 2

Wind tunnel: cooling test

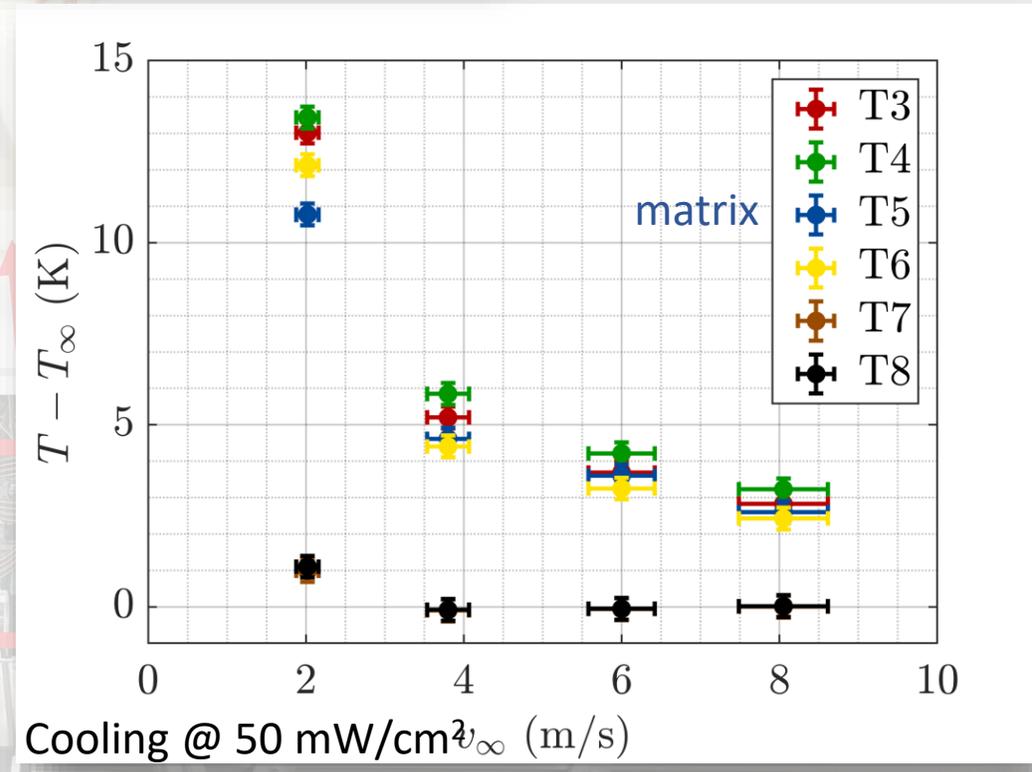
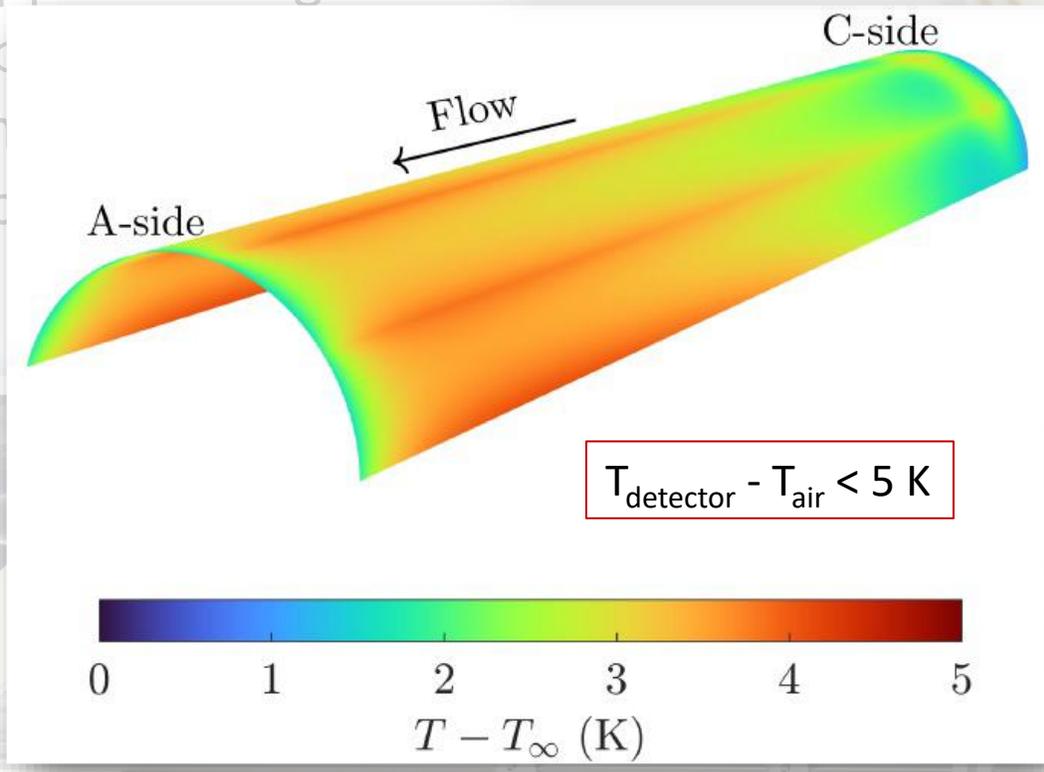
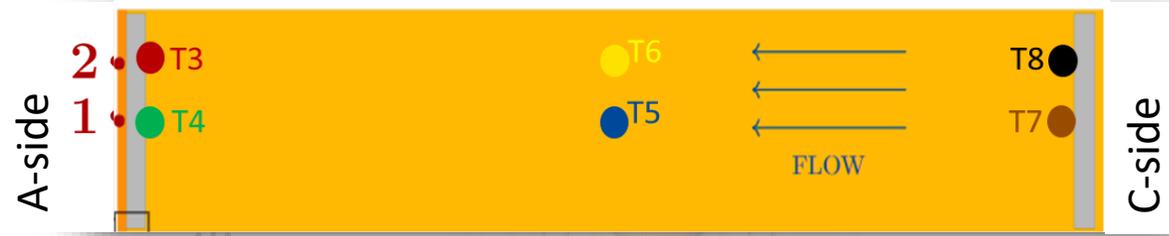


- ITS3 Breadboard Model 3 for thermal characterisation
- Copper heating traces on silicon in polyimide
- Temperature variation can be kept $<5\text{K}$



Wind tunnel: cooling test

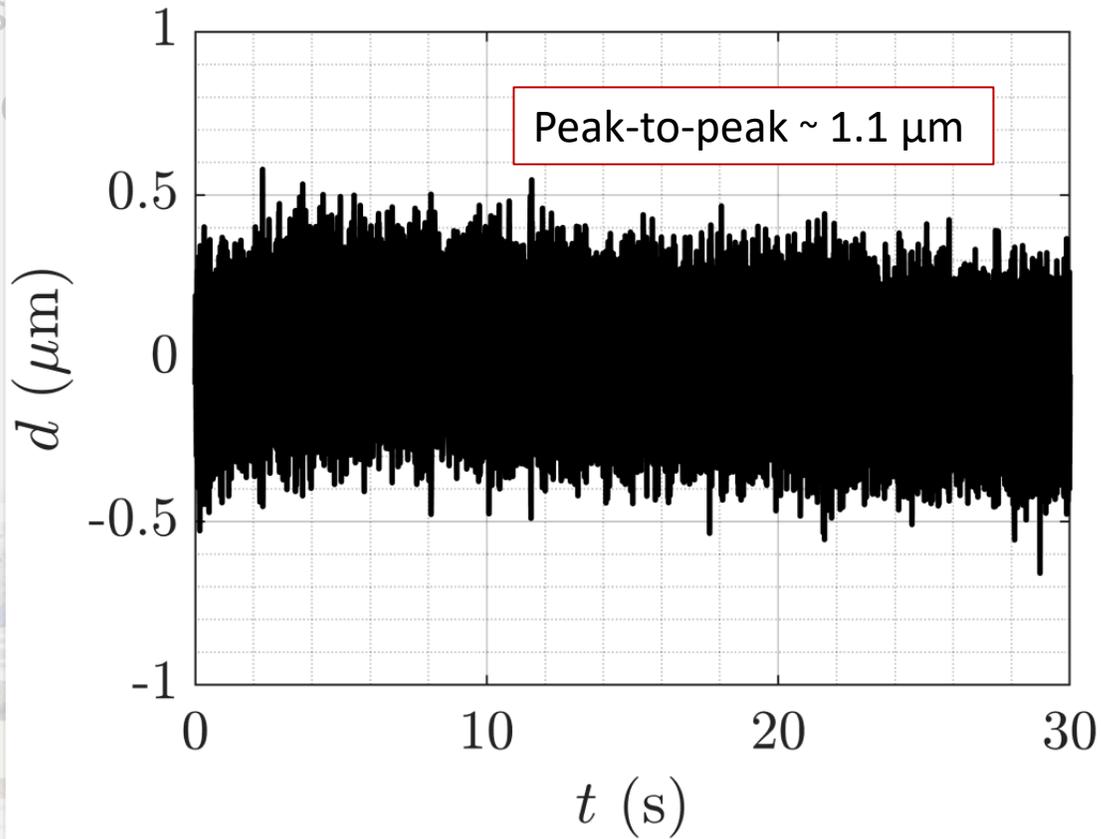
- ITS3 Breadboard M for thermal character
- Copper heating traces on silicon
- Temperature kept



Very good results with quite some margin: current target 40 mW/cm²

- ITS3 Breadboard Mode for thermal characteris
- Copper heating traces in polyimide
- Temperature variation kept $<5\text{K}$

Vibrations, center (8 m/s)

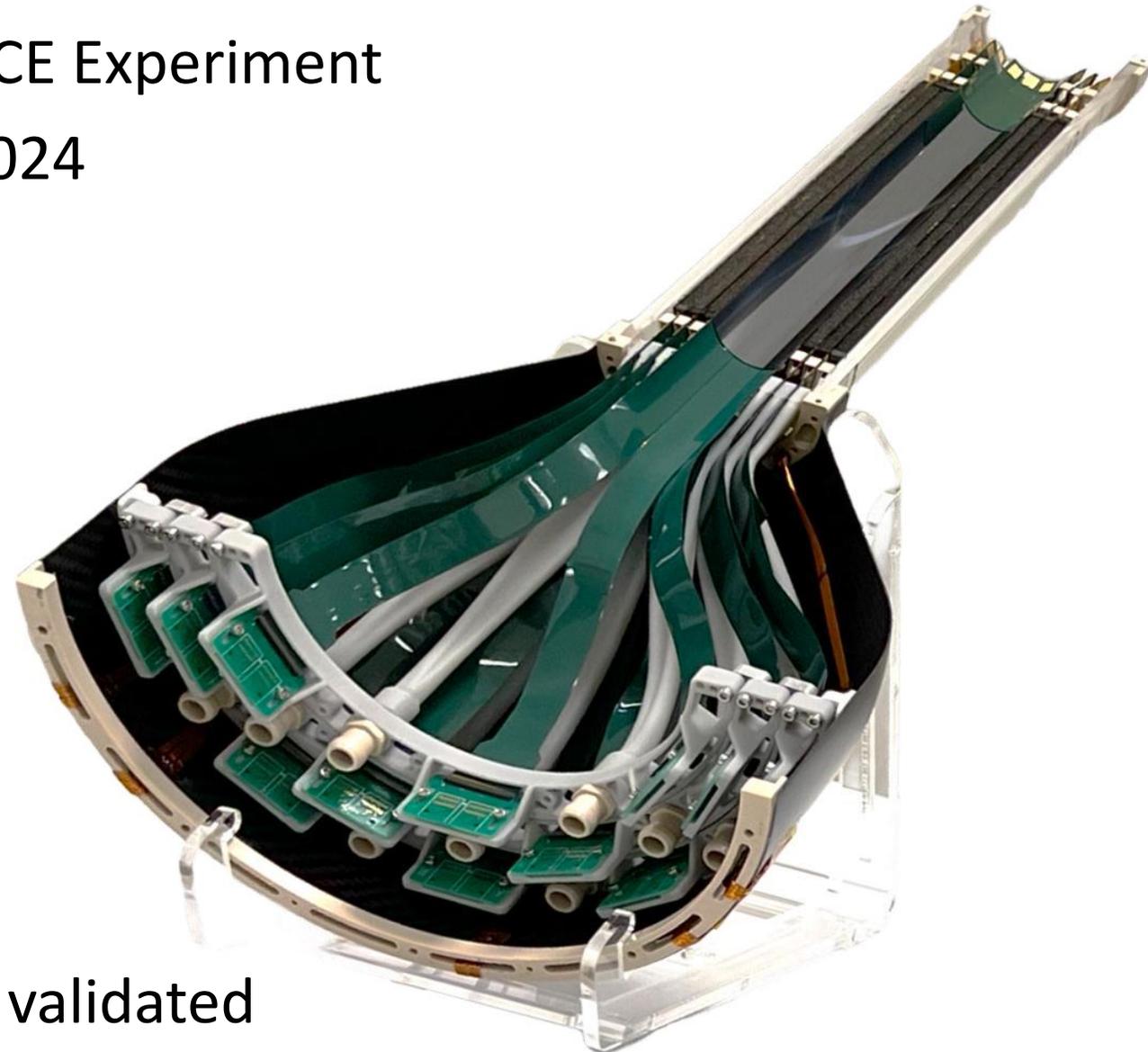


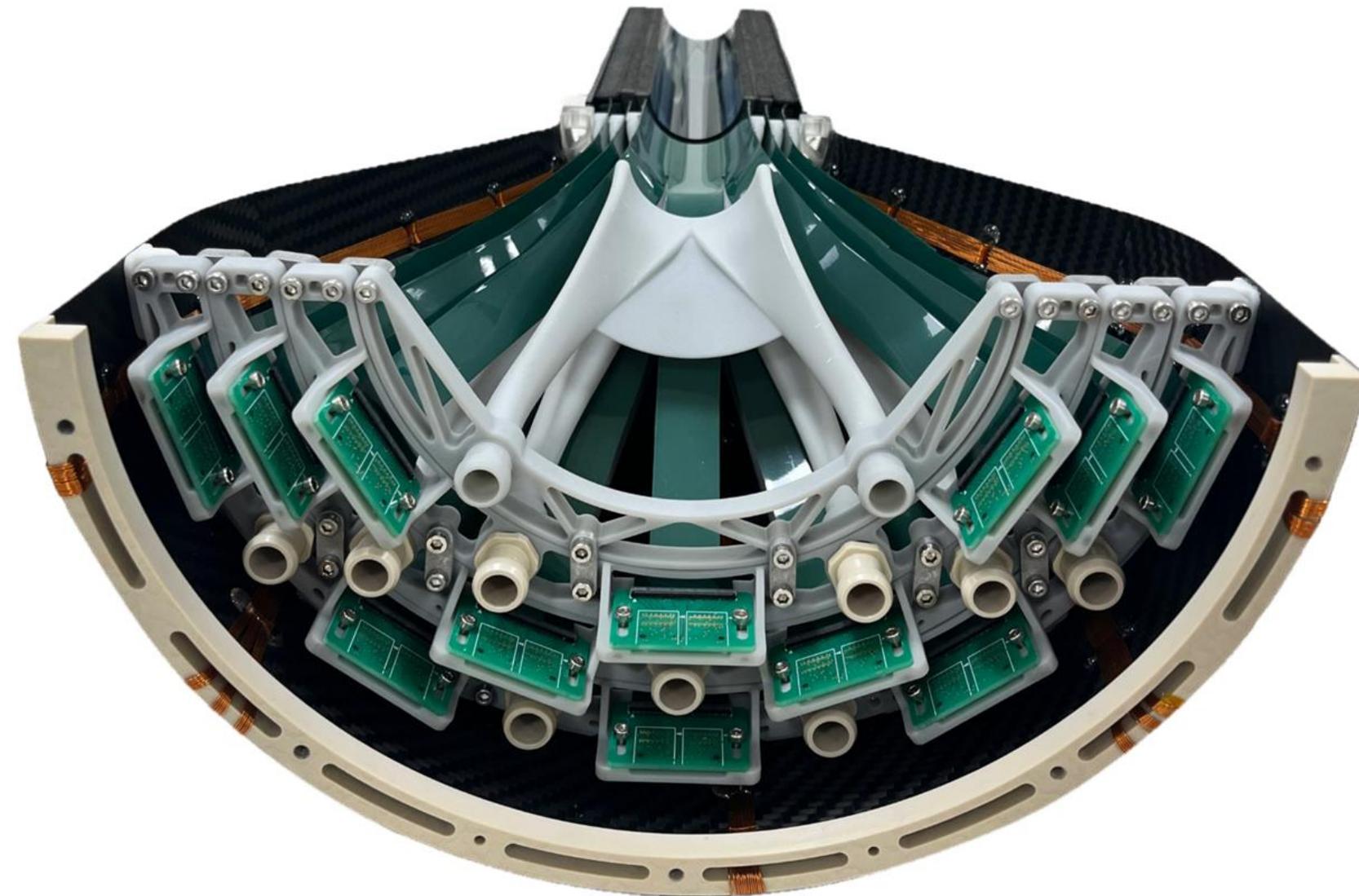
Wind tunnel

- ITS3 will be installed in 2028 in the ALICE Experiment
- Technical Design Report approved in 2024
- 6 MAPS sensors bent around the beampipe:
 - Area up to $10 \times 27 \text{ cm}^2$
 - Inner radius of 19 mm
 - $0.09\% X_0$ per layer



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 - Area up to $10 \times 27 \text{ cm}^2$
 - Inner radius of 19 mm
 - $0.09\% X_0$ per layer
- Demonstrated operability of **bent MAPS**
- **65 nm CMOS process** validated
- **Stitching** qualification ongoing
- **Mechanical and thermal** performance validated





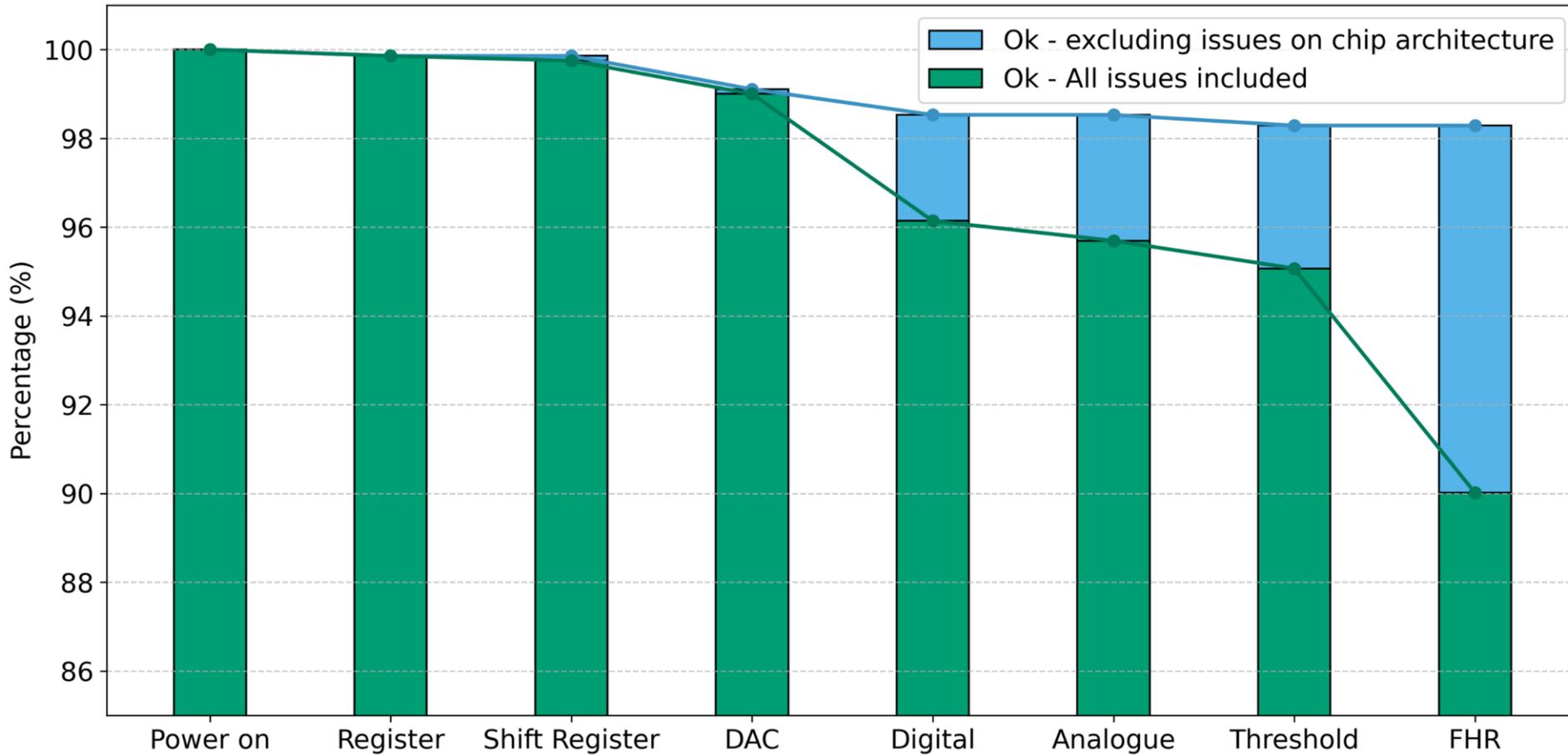
Thanks!



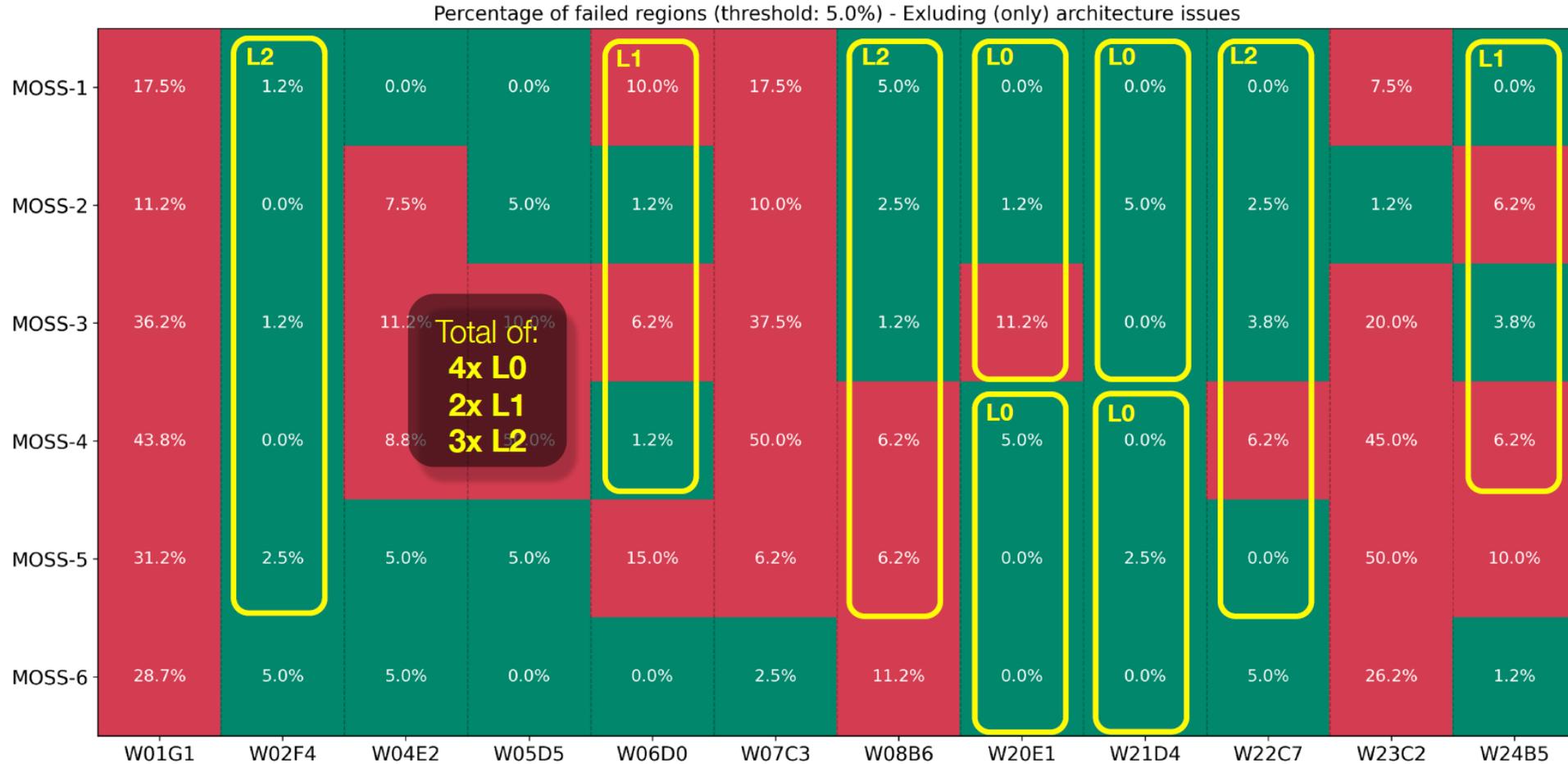
Backup

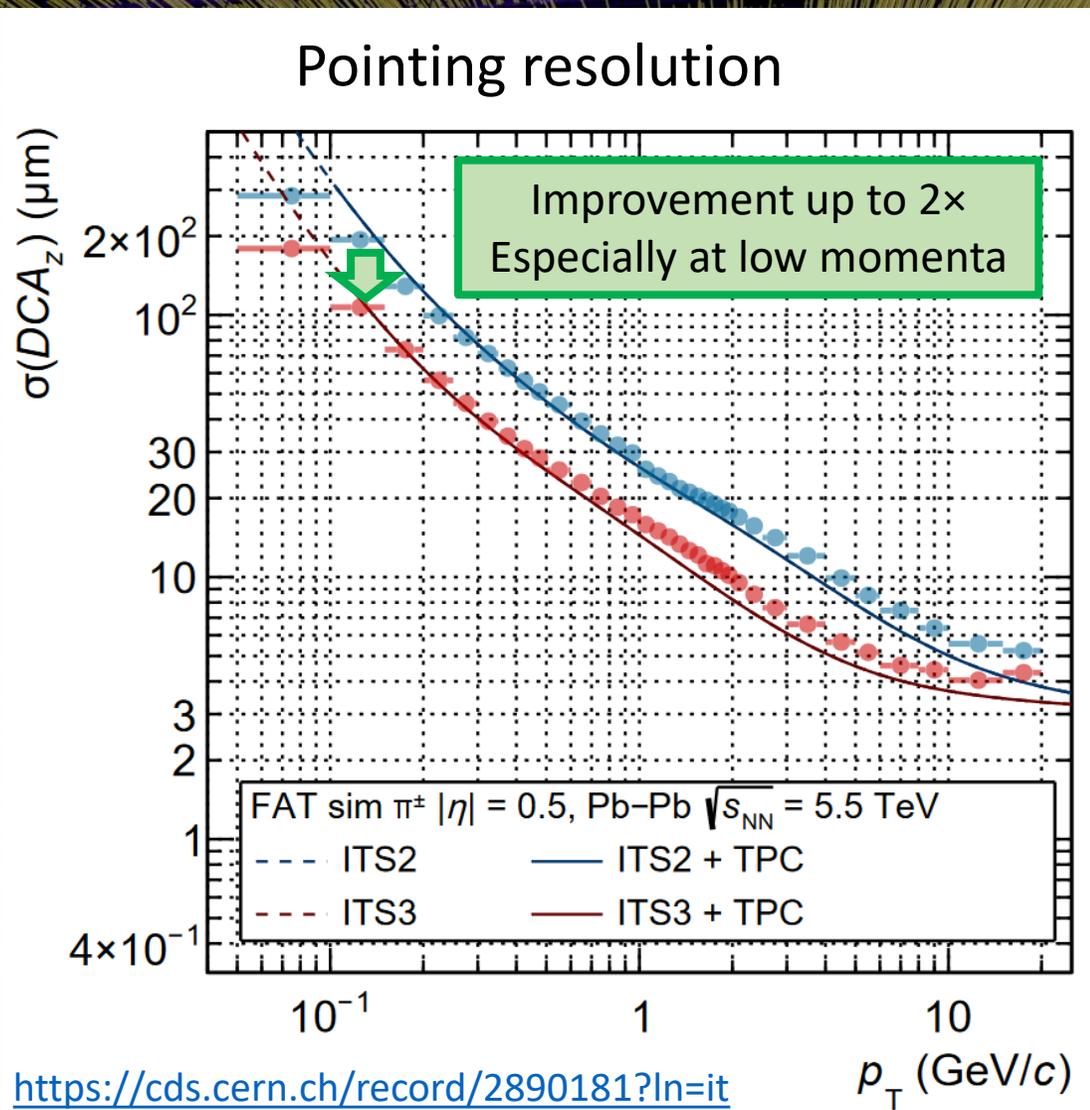


Yield of stitched prototype



Yield of stitched prototype





ITS3 Performance improvements:

- Tracking efficiency
- Pointing resolution

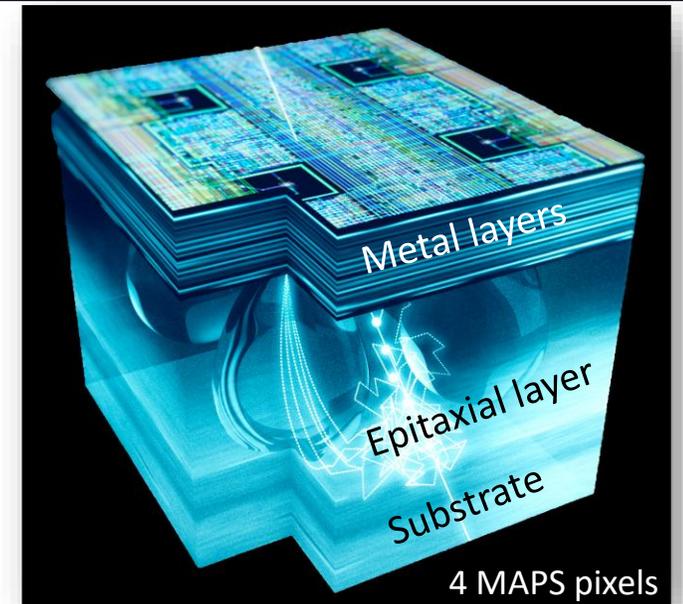
Will allow to

- Improve the measurement precision for the **heavy-flavour sector** in the low-momentum region, especially for B_s^0, Λ_b^0
- Bring **another set of fundamental observables** into reach (non prompt D_s^+, Ξ_c^+ decays)

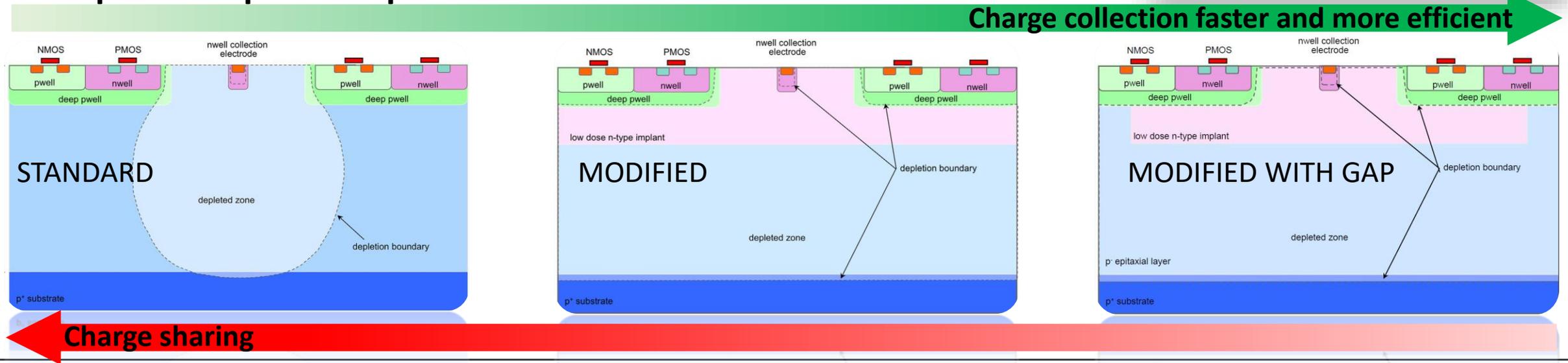
- Tower Partners Semiconductor Co. ([TPSCo](#)) 65 nm CMOS imaging process for Monolithic Active Pixel Sensors (MAPS)
- Chosen for ALICE ITS3 detector and under study by the [CERN EP R&D](#) on monolithic pixel sensors

Key advantages:

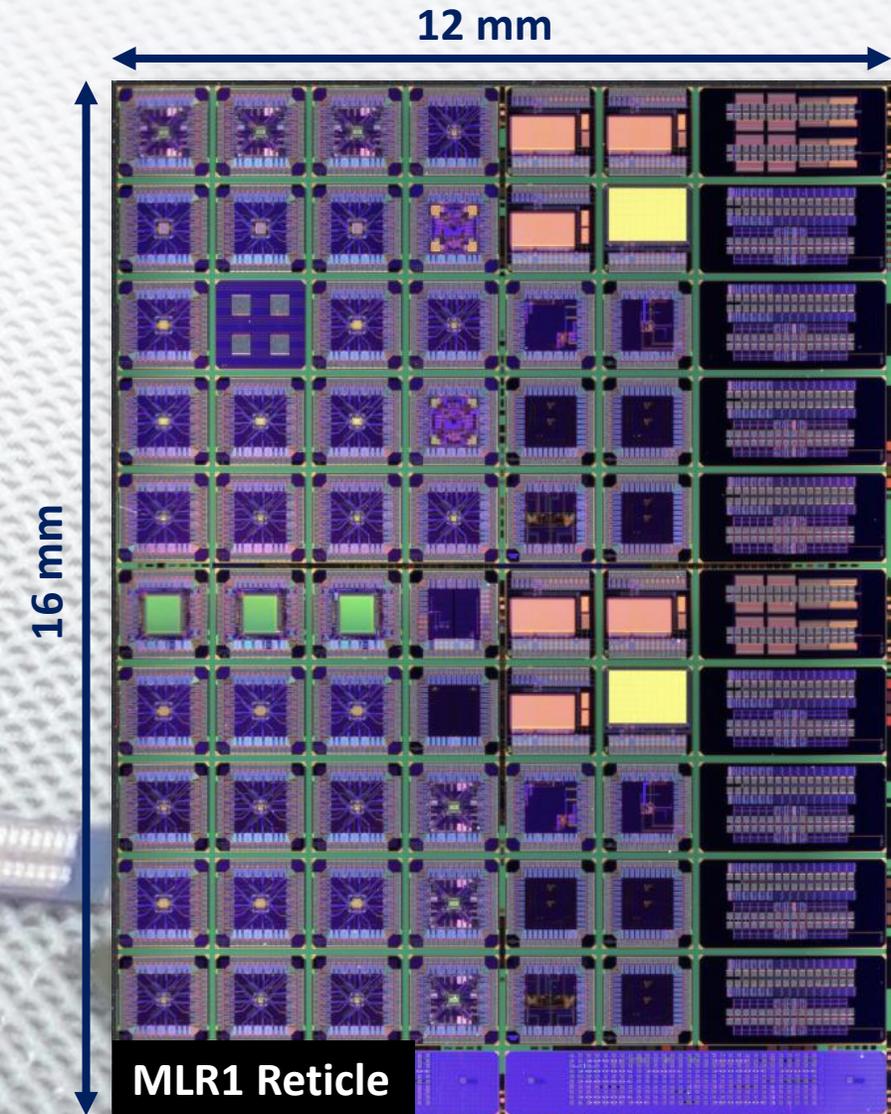
- High radiation hardness
- Low power consumption
- 5 μm 2D spatial resolution
- Large wafers (\varnothing 300 mm)



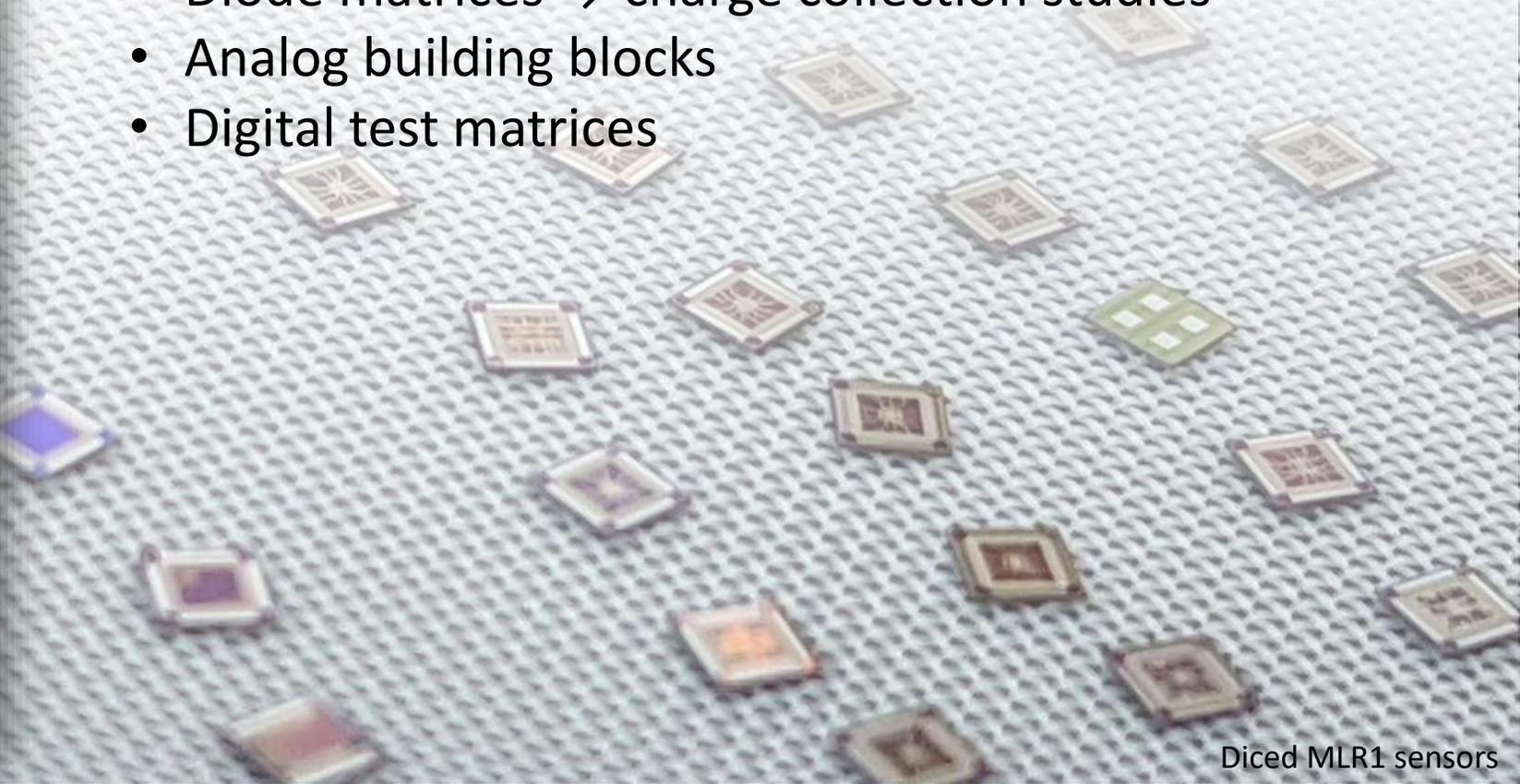
Three process options explored:



MLR1: first submission in 65 nm



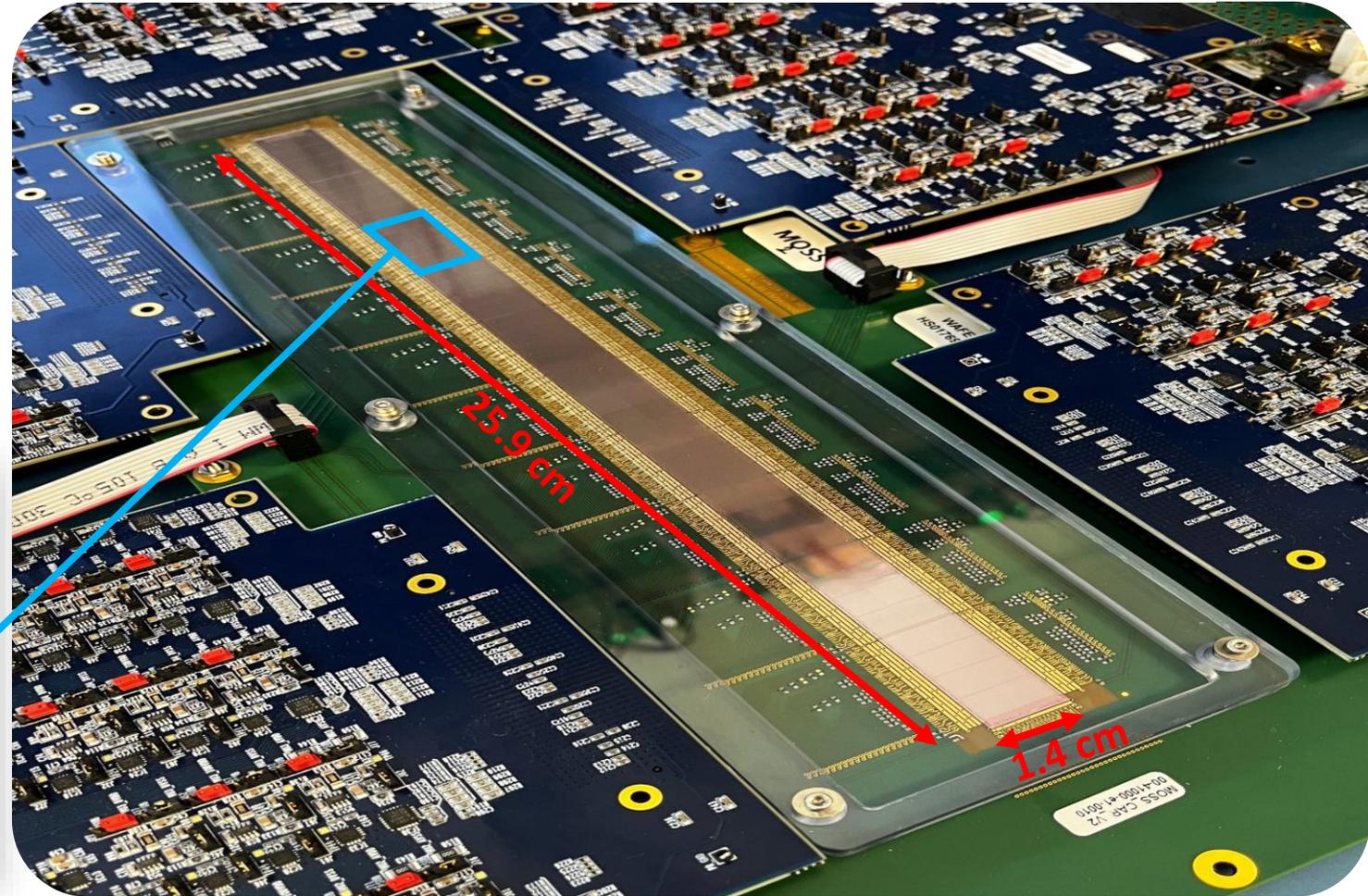
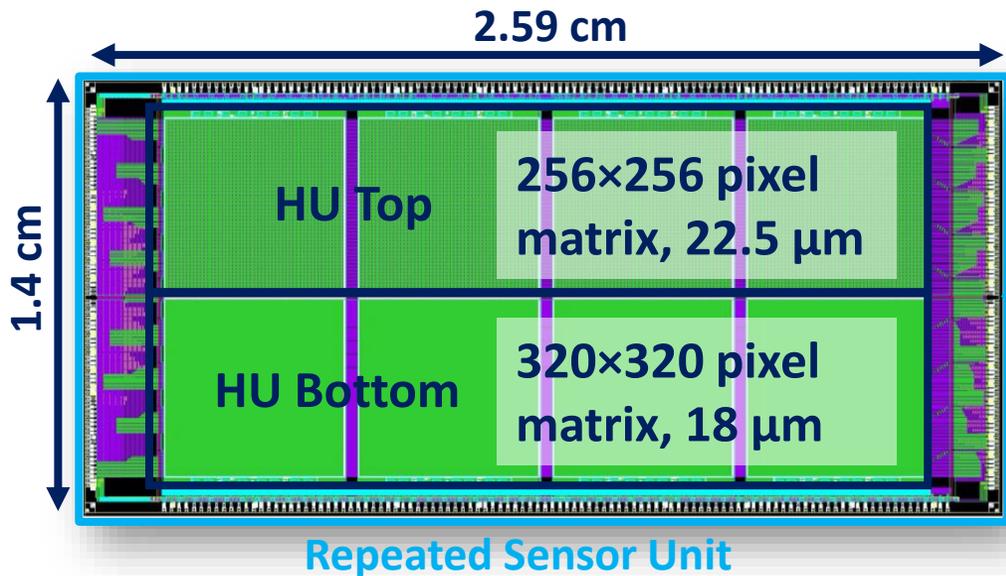
- **Multiple Layer Reticle 1 (MLR1)**, received in Sep. 2021
- Many small-scale ($O(1 \text{ mm}^2)$) prototypes:
 - Transistor test structures \rightarrow radiation hardness studies
 - Diode matrices \rightarrow charge collection studies
 - Analog building blocks
 - Digital test matrices





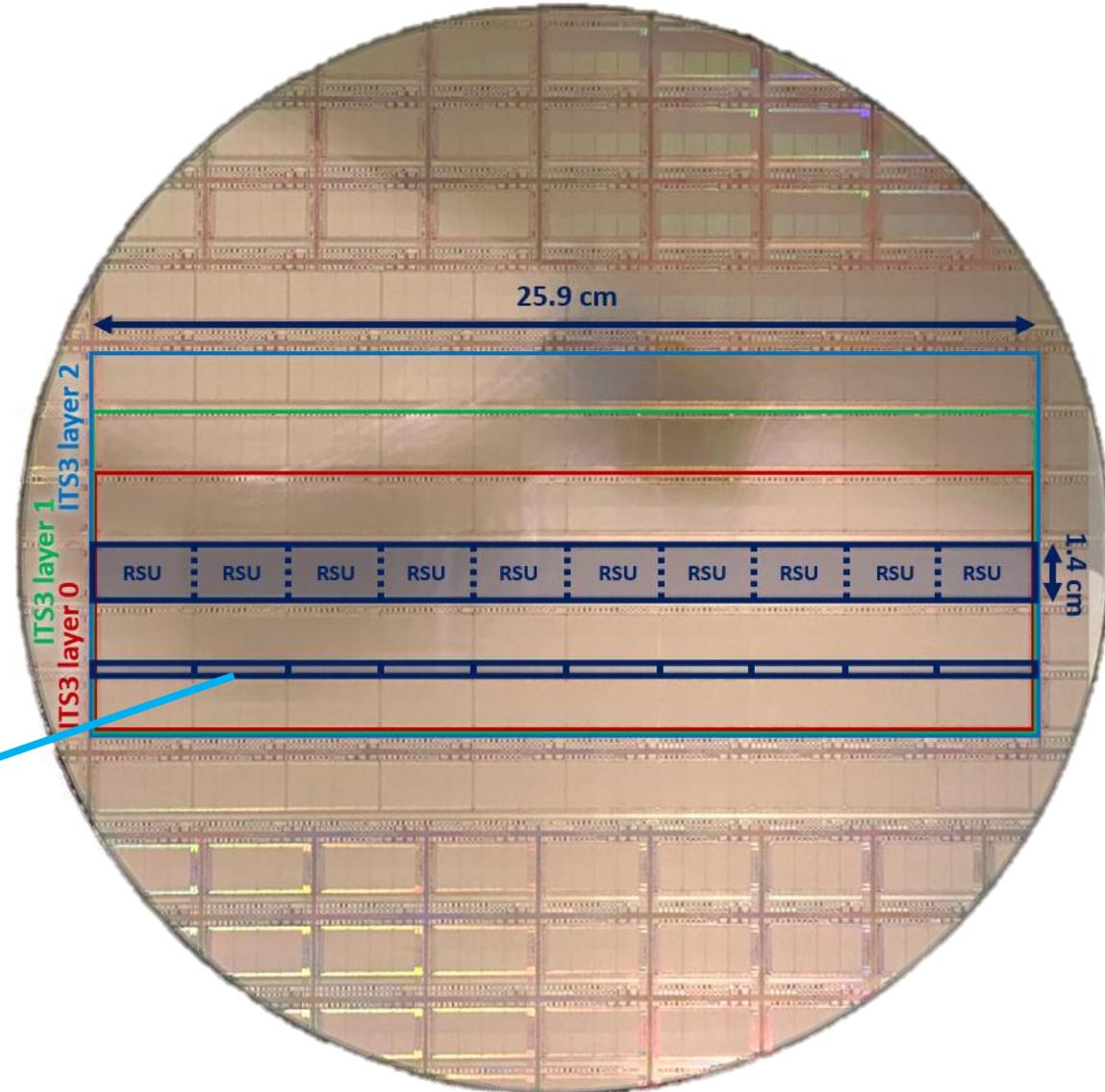
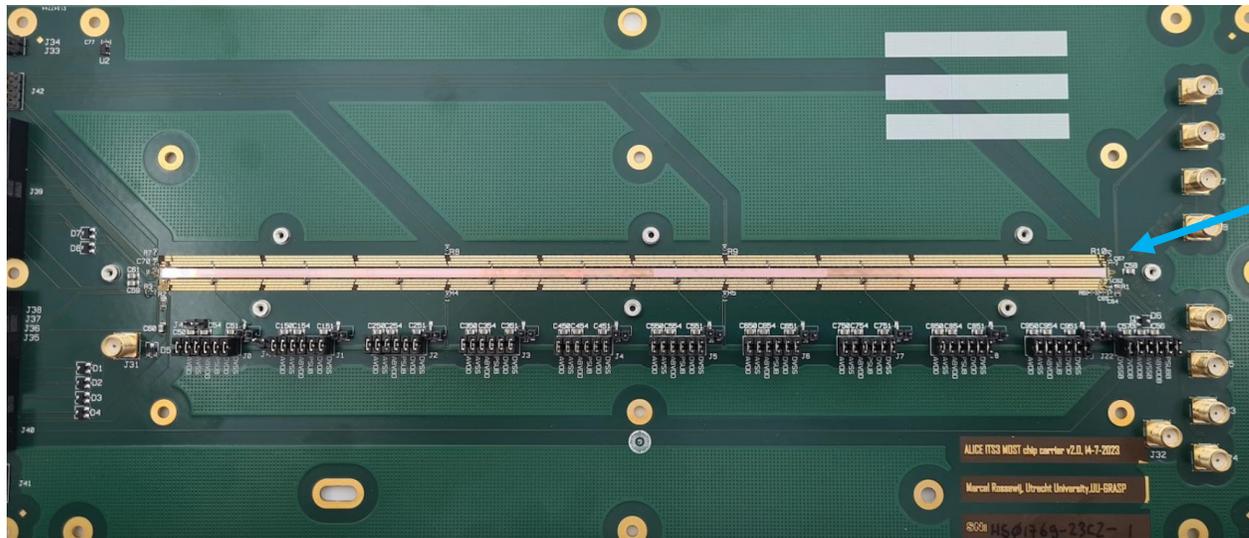
ER1: **MO**nolithic **S**titched **S**ensor, MOSS:

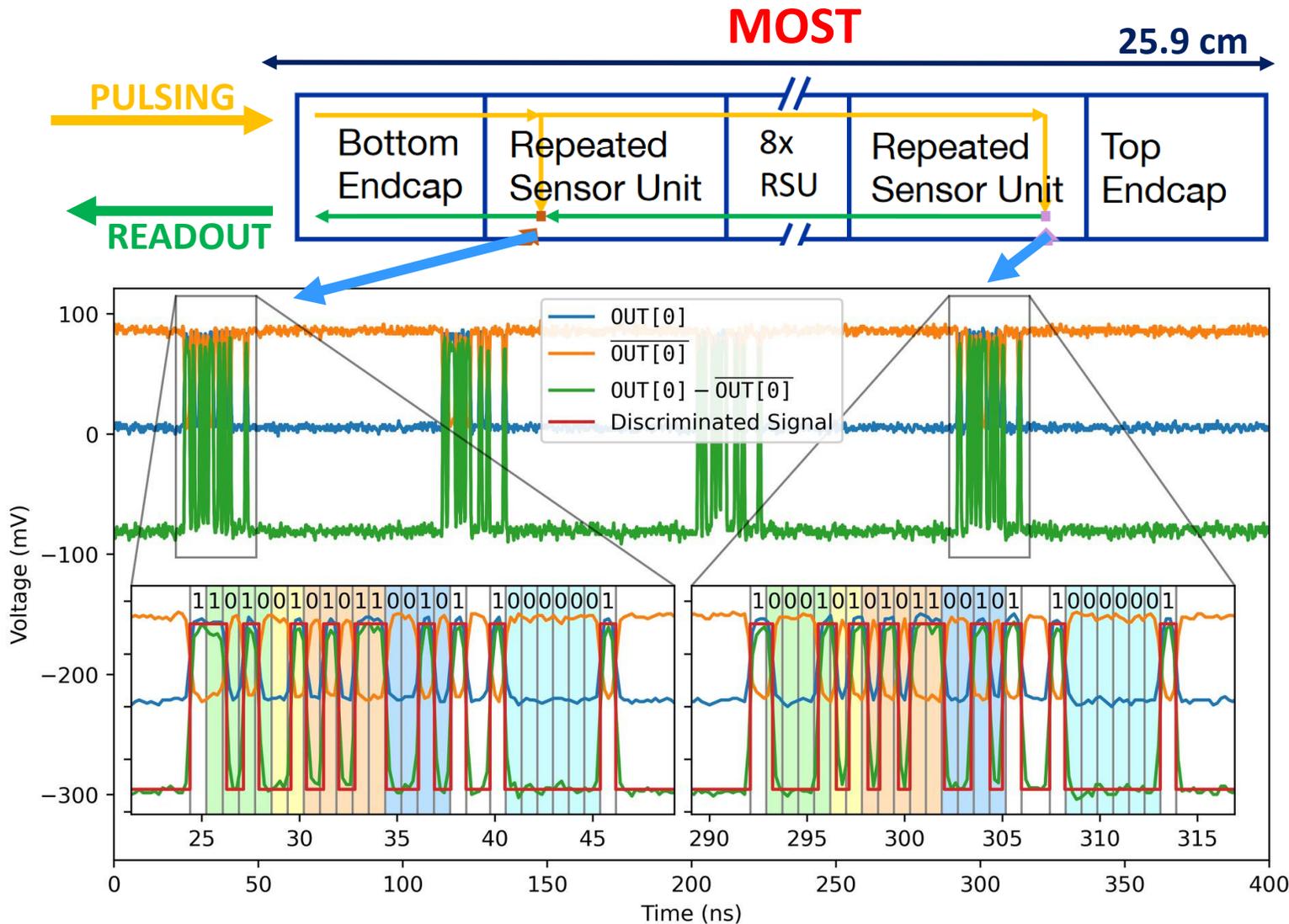
- $25.9 \times 1.4 \text{ cm}^2$
- 10 **Repeated Sensor Units** (RSU)
 - 2 Half Units (HU) with 4 regions (each with different electronics)



MOonolithic Stitched sensor with Timing (MOST)

- $25.9 \times 0.25 \text{ cm}^2$
- 0.9 million pixels, $18 \mu\text{m}$ pitch
- Aimed at testing the transmission quality of high-speed data over the full length of the ITS3
- Data transmission verified:
 - 1) 1Gbit/s
 - 2) over 25.9 cm
 - 3) across 10 stitched RSU





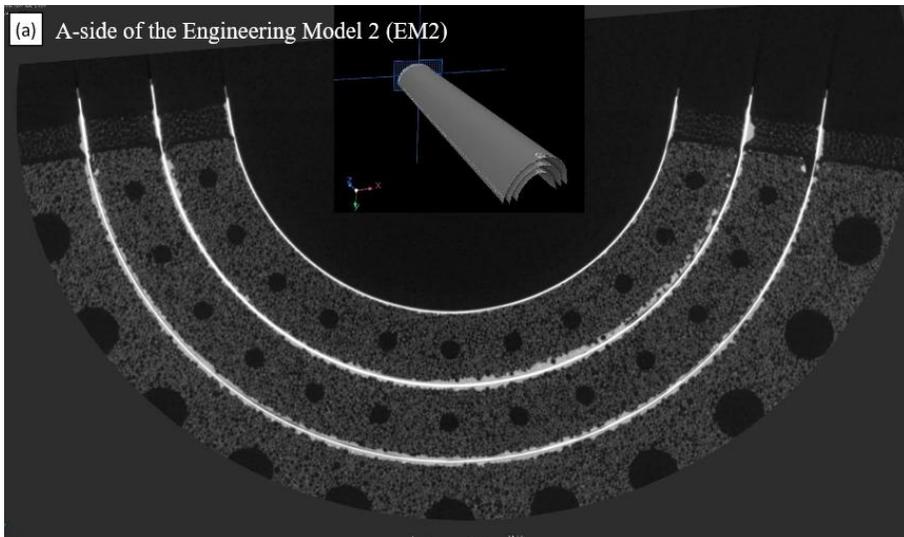
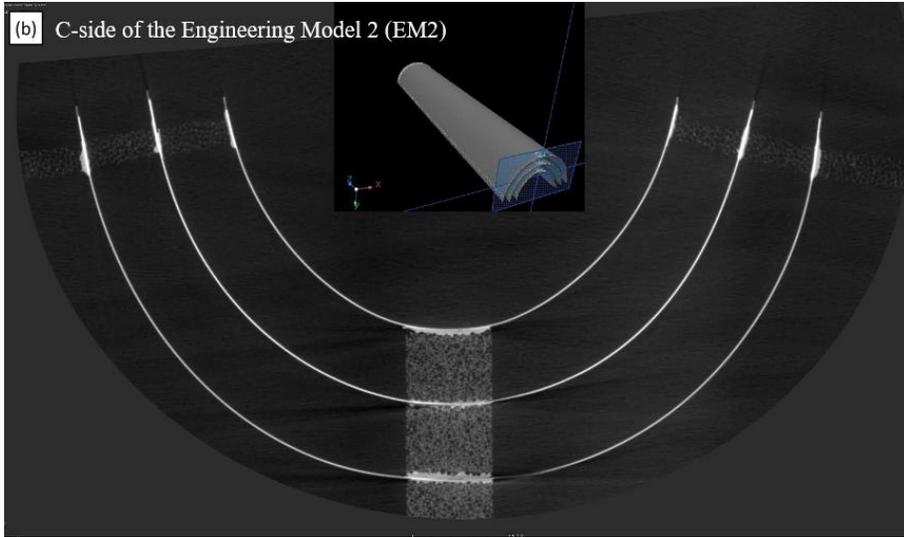
Test of the **data transmission across the full length**

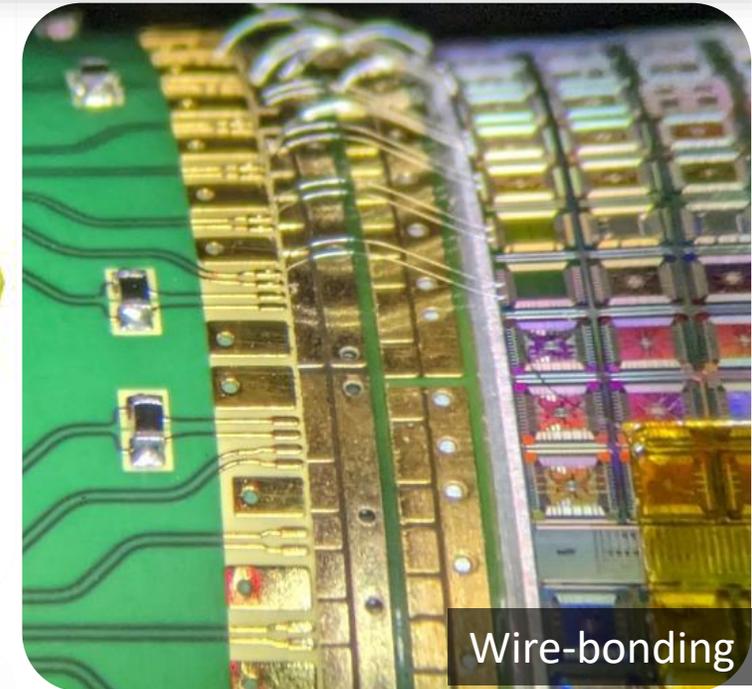
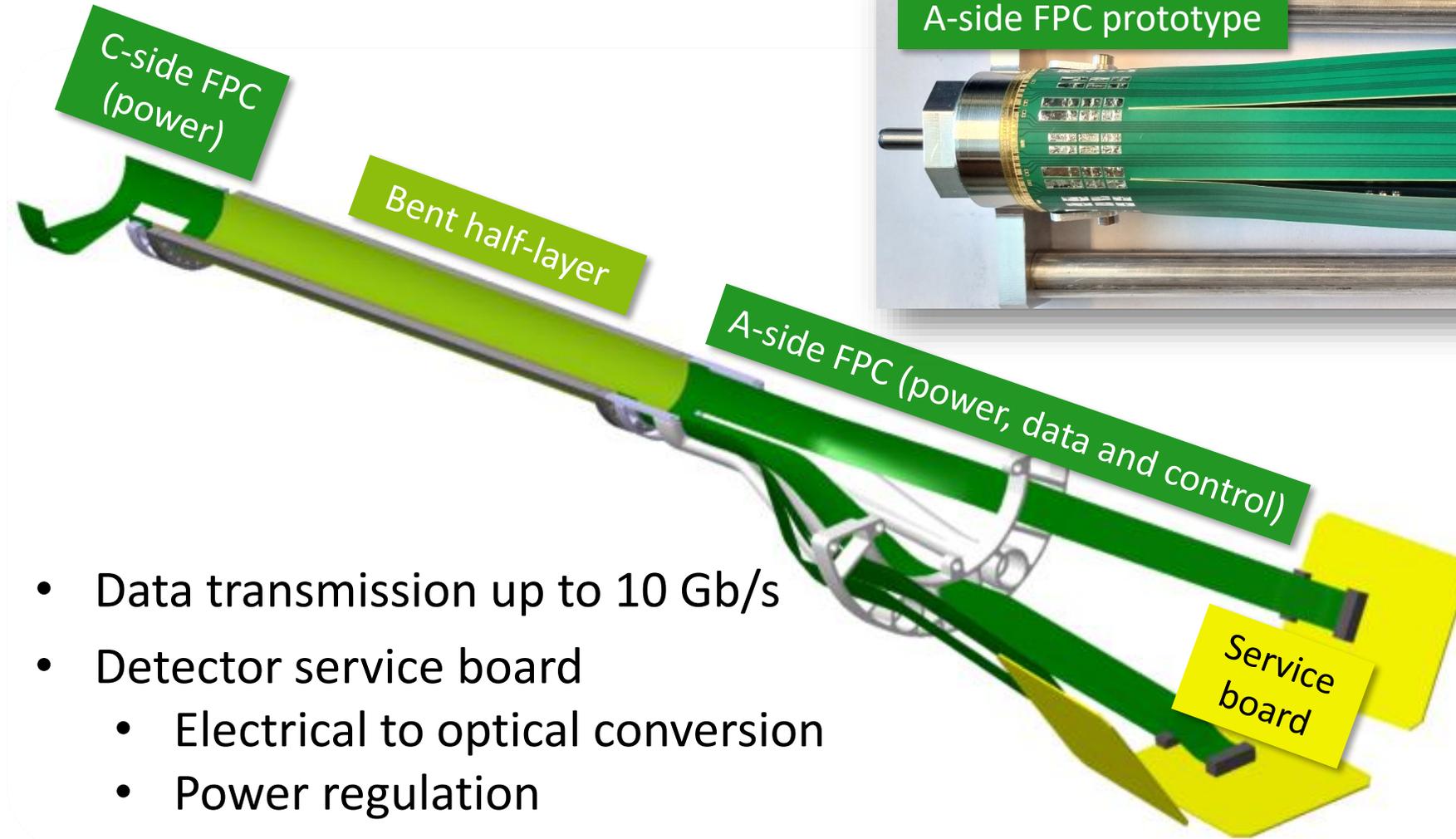
- Pulsing and readout of different MOST RSUs



- Data transmission verified:
 - 1) 1Gbit/s
 - 2) over 25.9 cm
 - 3) across 10 stitched RSU

ITS3 mechanical model

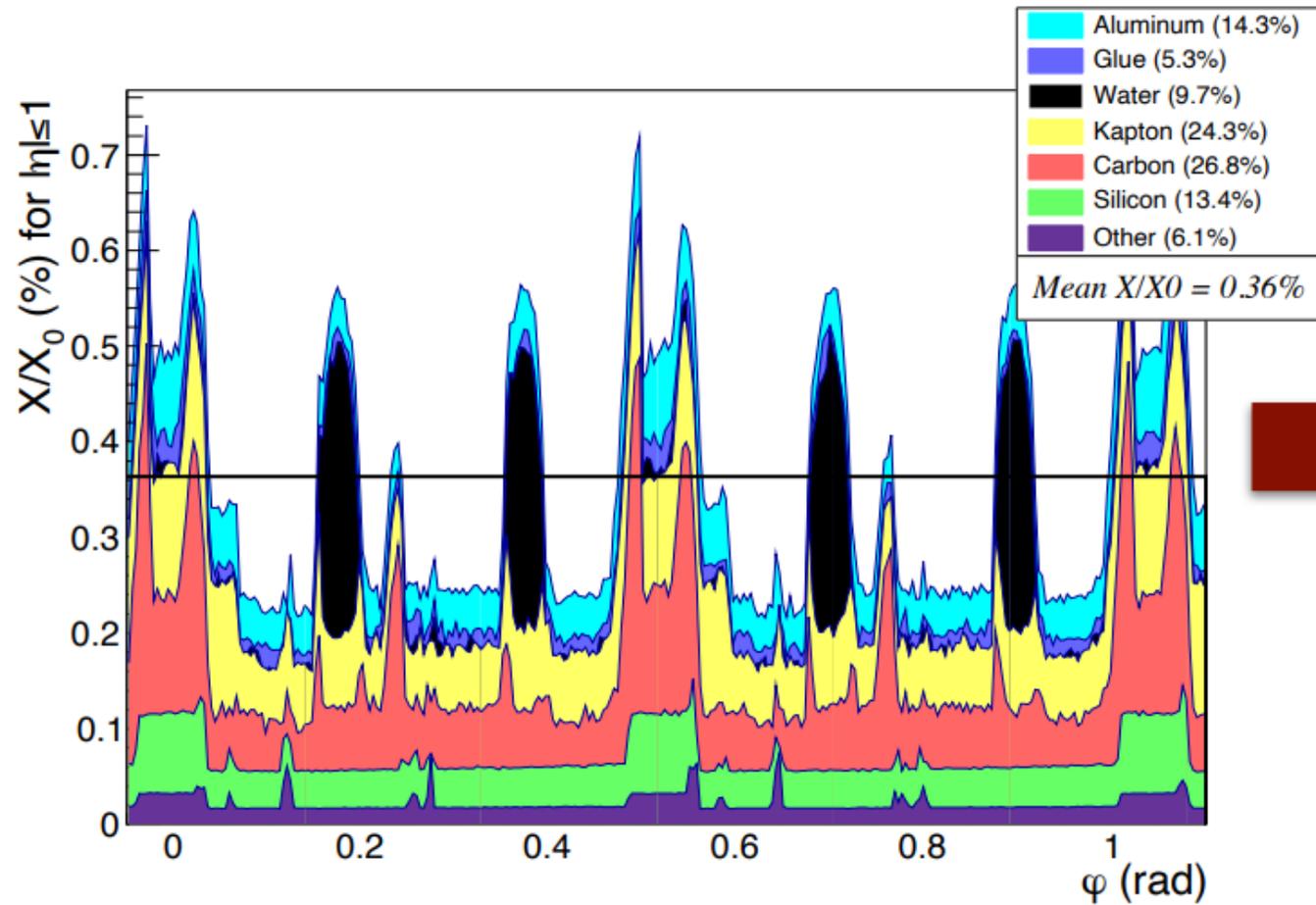




- Data transmission up to 10 Gb/s
- Detector service board
 - Electrical to optical conversion
 - Power regulation
- Reusing existing electronics

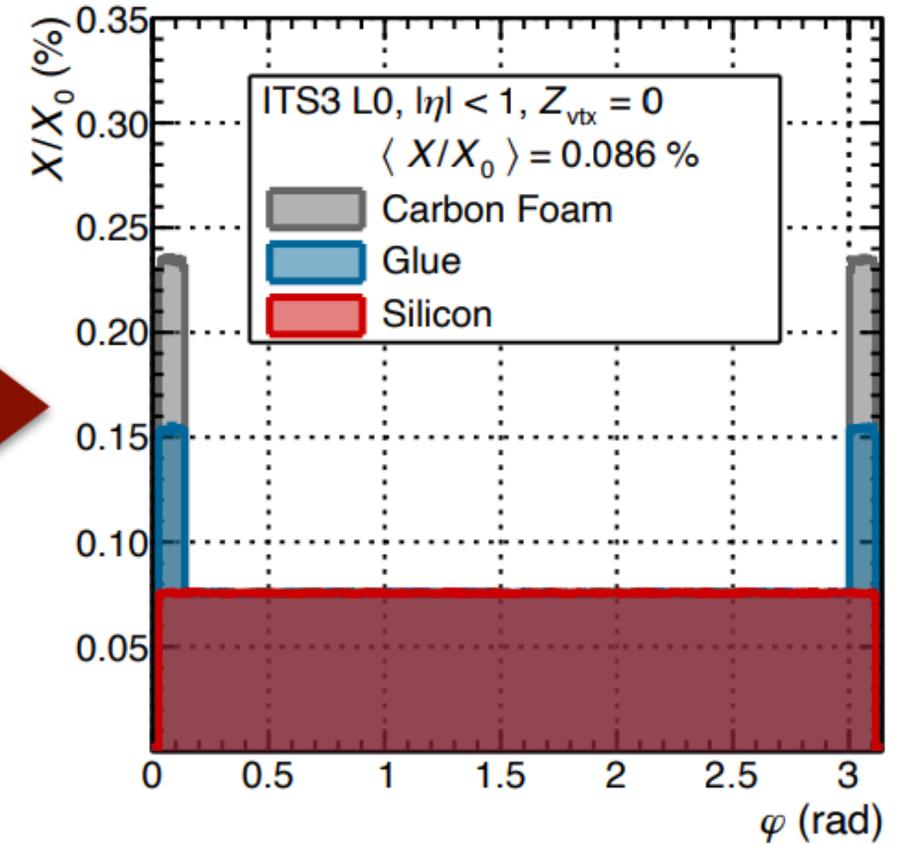
From ITS2 to ITS3

ITS2 innermost layer



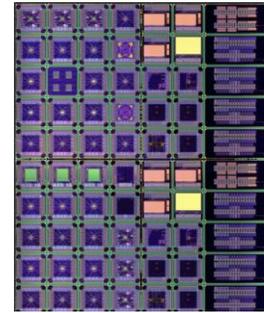
ITS2 Layer 0

ITS3 single layer model

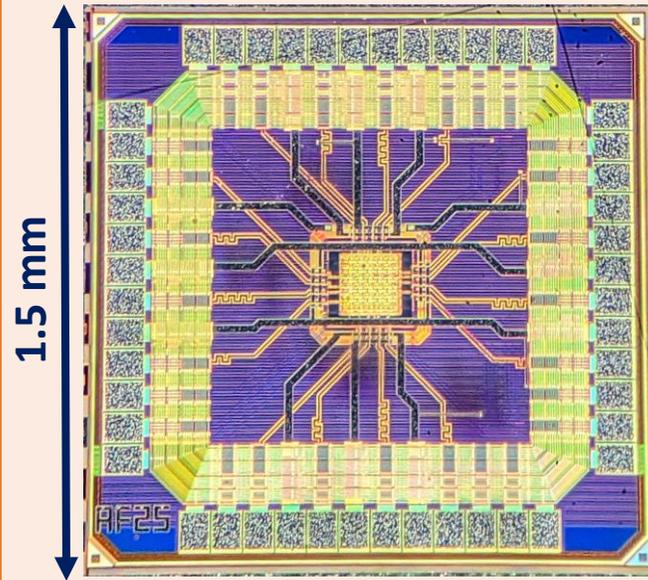


ITS3 Layer 0

MLR1 sensor prototypes

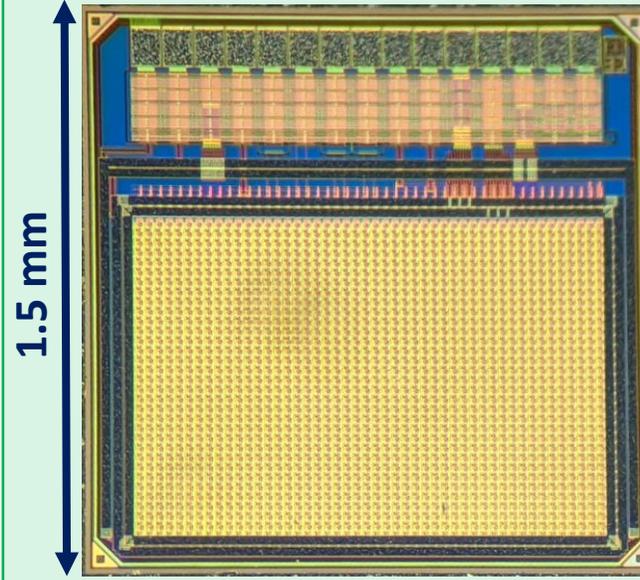


APTS: Analog Pixel Test Structure



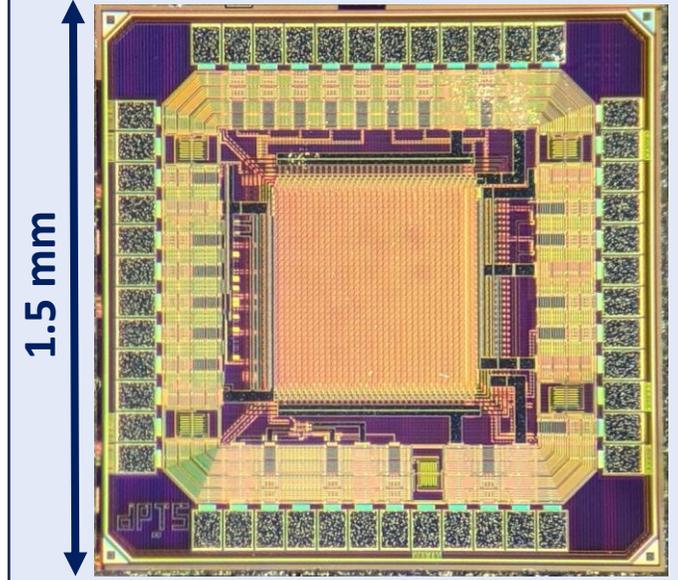
- 6x6 pixel matrix
- Pitch: 10, 15, 20, 25 μm
- Analogue readout of central 4x4 submatrix
- Output buffer in two versions: Source Follower (SF) and Op Amp (OA)
- **Goal:** explore pixel designs

CE65: Circuit Exploratoire 65

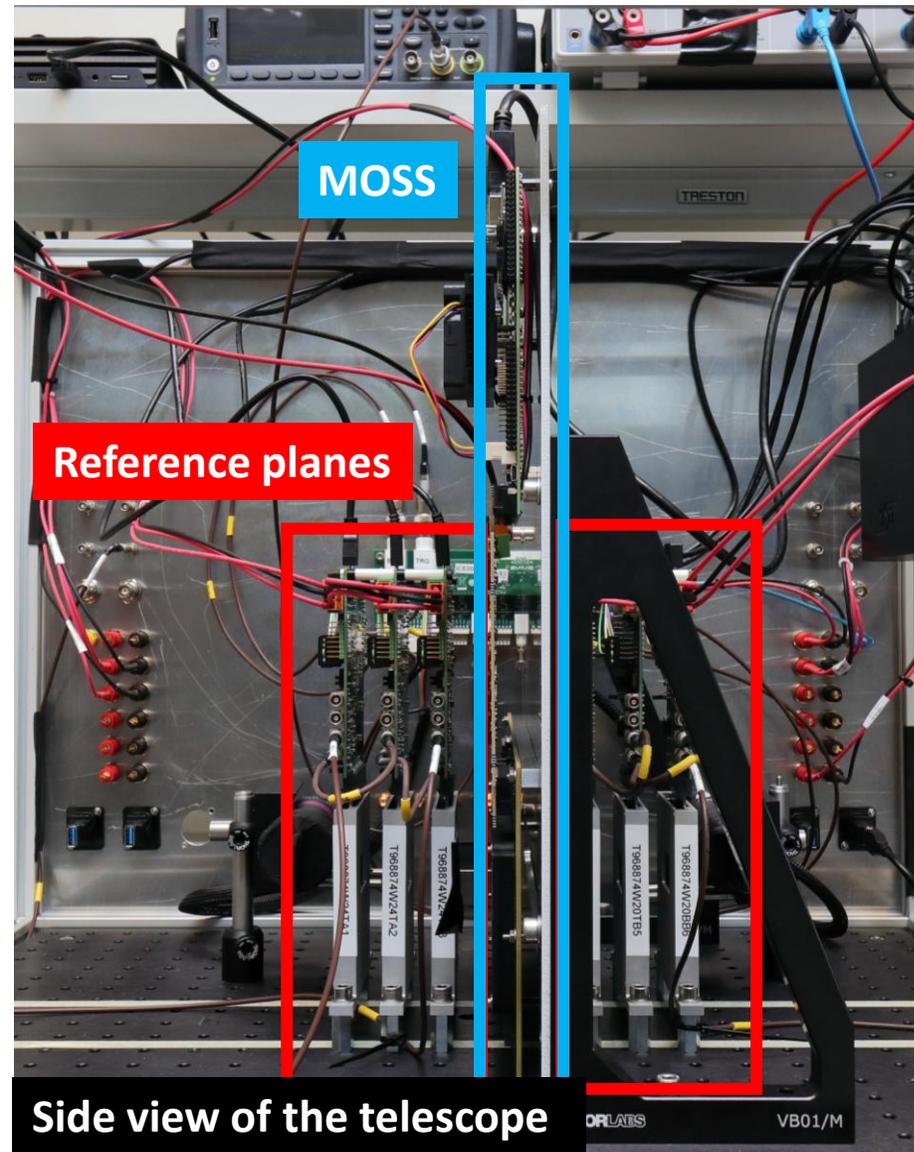


- 64x32 pixel matrix, 15 μm pitch (3 subvariants: AC, DC and SF)
- 48x32 pixel matrix, 25 μm pitch
- Rolling shutter readout (50 μs integration time)
- **Goal:** explore pixel matrix uniformity and rolling shutter

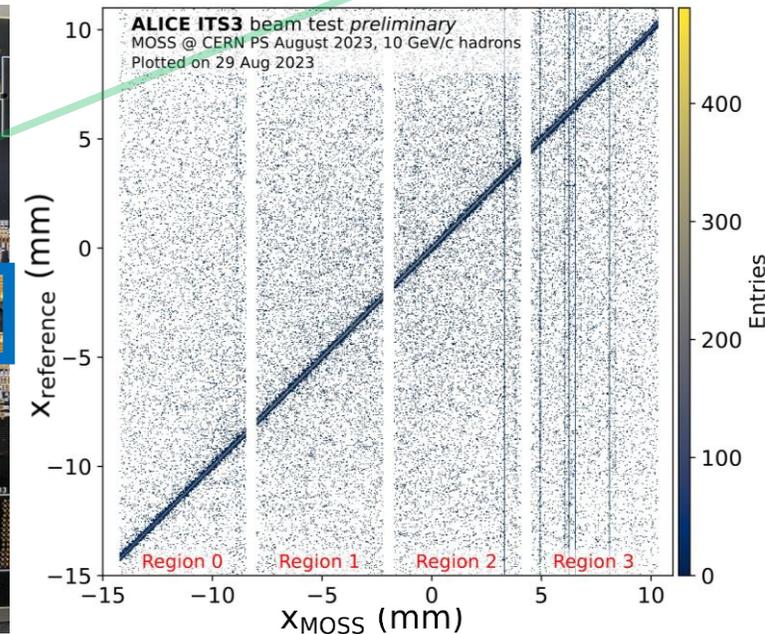
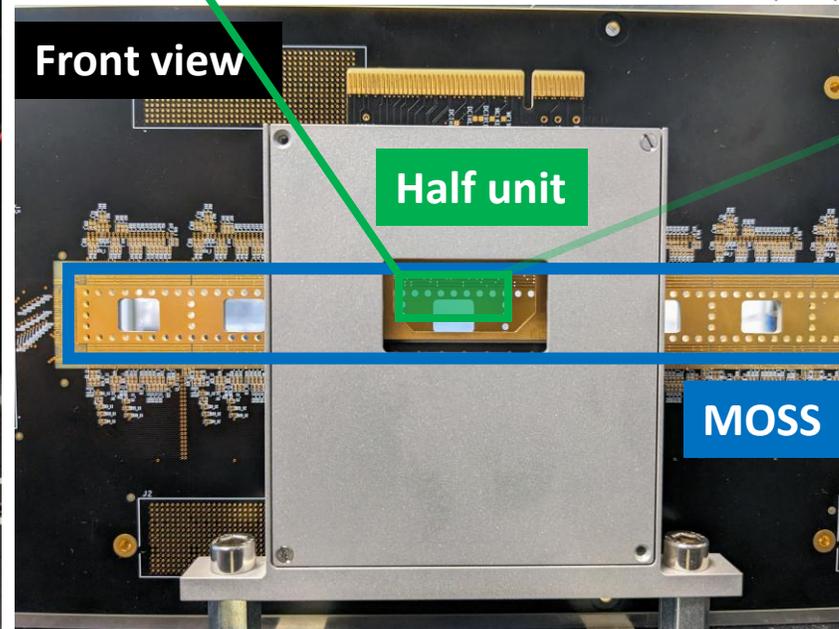
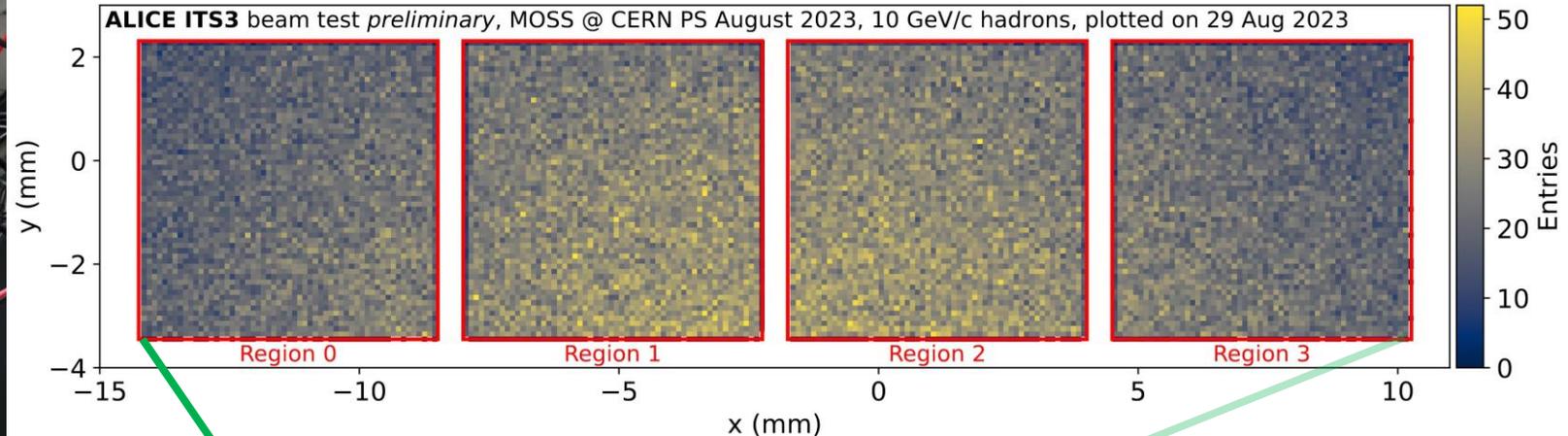
DPTS: Digital Pixel Test Structure



- 32x32 pixel matrix, 15 μm pitch
- Asynchronous digital readout
- Time-encoded pixel position
- Time-over-threshold measurements
- **Goal:** study the in-pixel front-end



- Testbeam @ CERN PS: hitmaps and correlations



MOSS test system

