

# Characterization and Performance Evaluation of ITk Pixel Production Modules for the ATLAS Upgrade

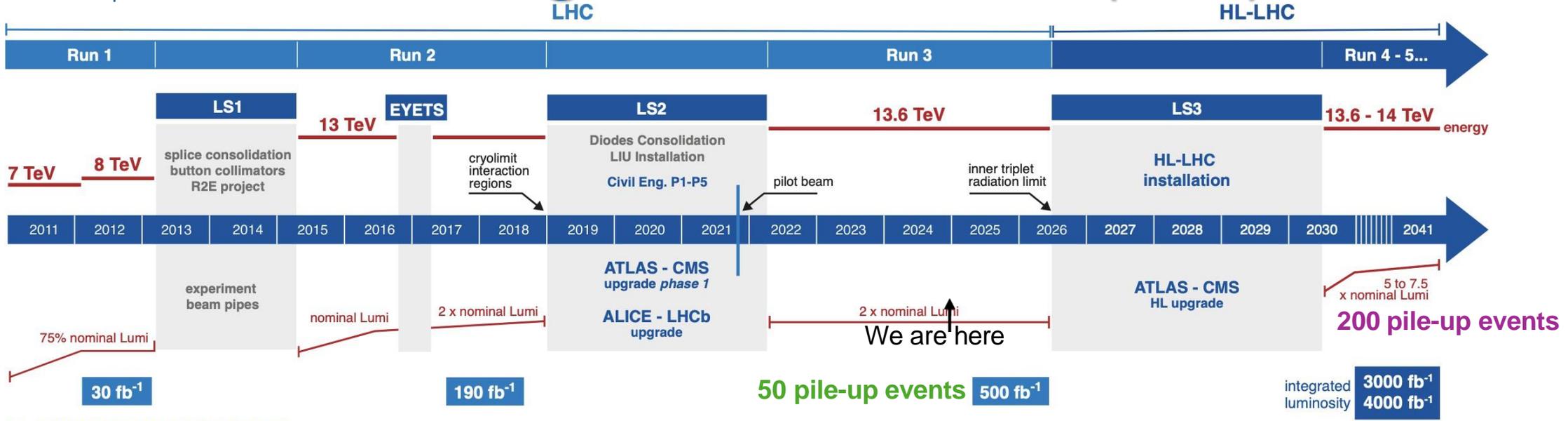
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University  
of Glasgow

Last update: Oct 2024

# Large Hadron Collider (LHC)



## HL-LHC TECHNICAL EQUIPMENT:

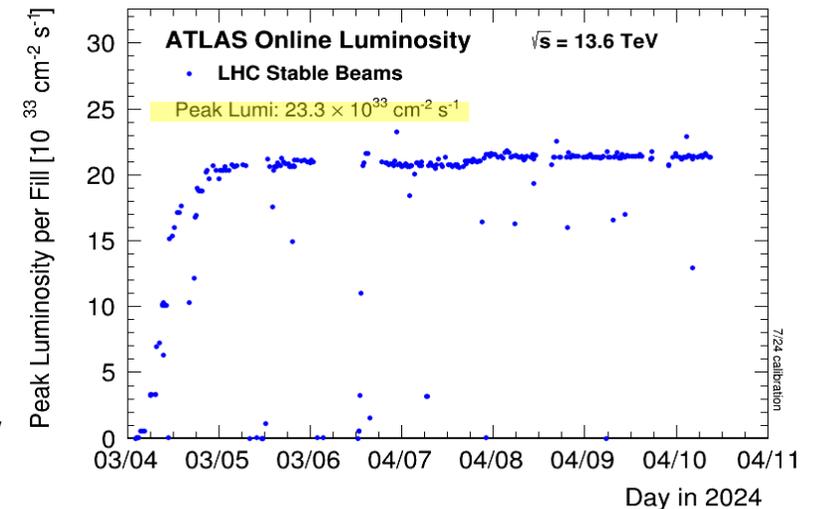


[https://hilumilhc.web.cern.ch/sites/default/files/2024-10/HL-LHC\\_October2024.pdf](https://hilumilhc.web.cern.ch/sites/default/files/2024-10/HL-LHC_October2024.pdf)

## High-luminosity large hadron collider (HL-LHC) :

- integrated luminosity: more than 250 fb<sup>-1</sup>/year
- instantaneous luminosity expected to be 75 x 10<sup>33</sup> cm<sup>2</sup> s<sup>-1</sup>

Source: <https://home.cern/resources/faqs/high-luminosity-lhc> / NIMA 1070 (2025) 169978



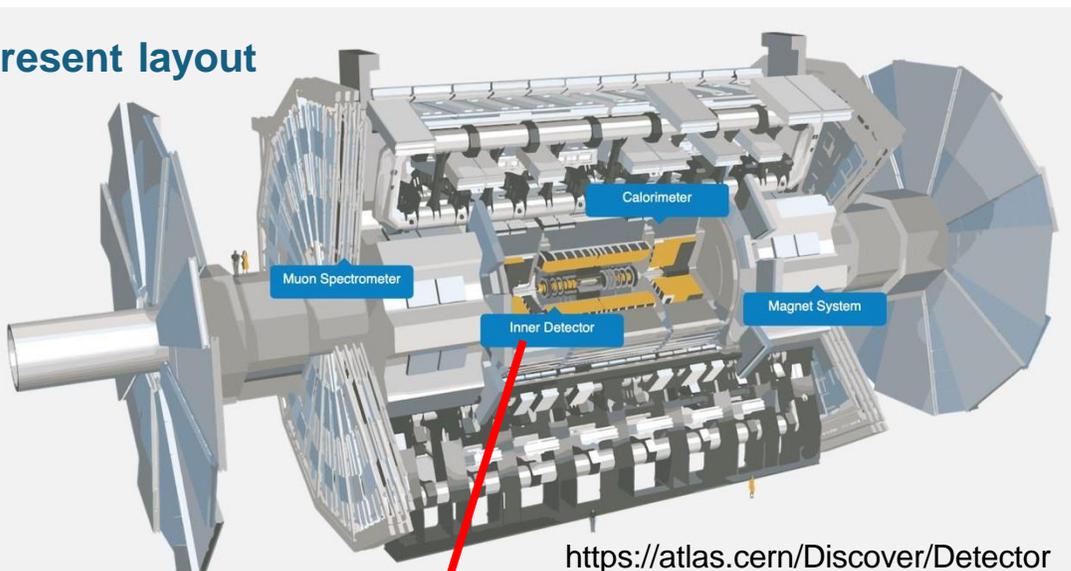
<https://atlas.web.cern.ch/Atlas/GROUPS/DATAPREPARATION/PublicPlots/2024/DataSummary/figs/peakLumiByFill.png>

Md Arif Abdulla Samy

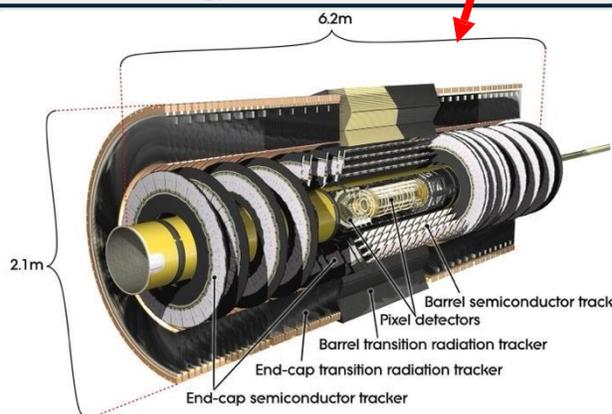
# ATLAS update for HL-LHC

The current innermost detection system of ATLAS is the Inner Detector

## Present layout



<https://atlas.cern/Discover/Detector>



### Inner Detector (ID)

Max Acceptance  $\eta = 2.5$

Pixel Detector: 92 million channels

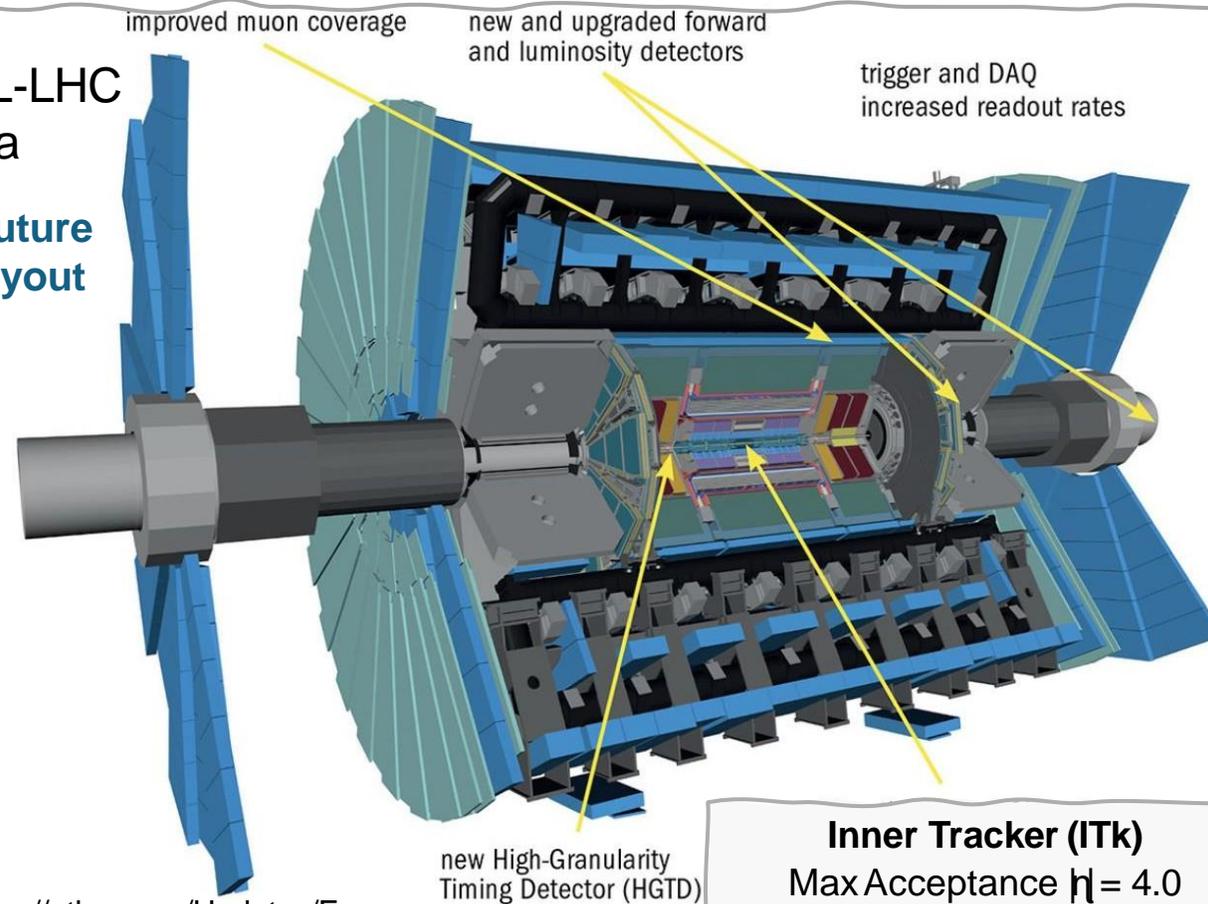
Semiconductor Tracker: 6 million channels

Transition Radiation Tracker: 350.000 channels

<https://atlas.cern/Discover/Detector/Inner-Detector>

## HL-LHC era

## Future layout



<https://atlas.cern/Updates/Future/High-Luminosity-ATLAS>

### Inner Tracker (ITk)

Max Acceptance  $\eta = 4.0$

ITk Pixel Detector: 5 billion channels

ITk Strip Detector: 60 million channels

ID will be replaced by the all-Si tracker ITk

# Inner Tracker-ITk

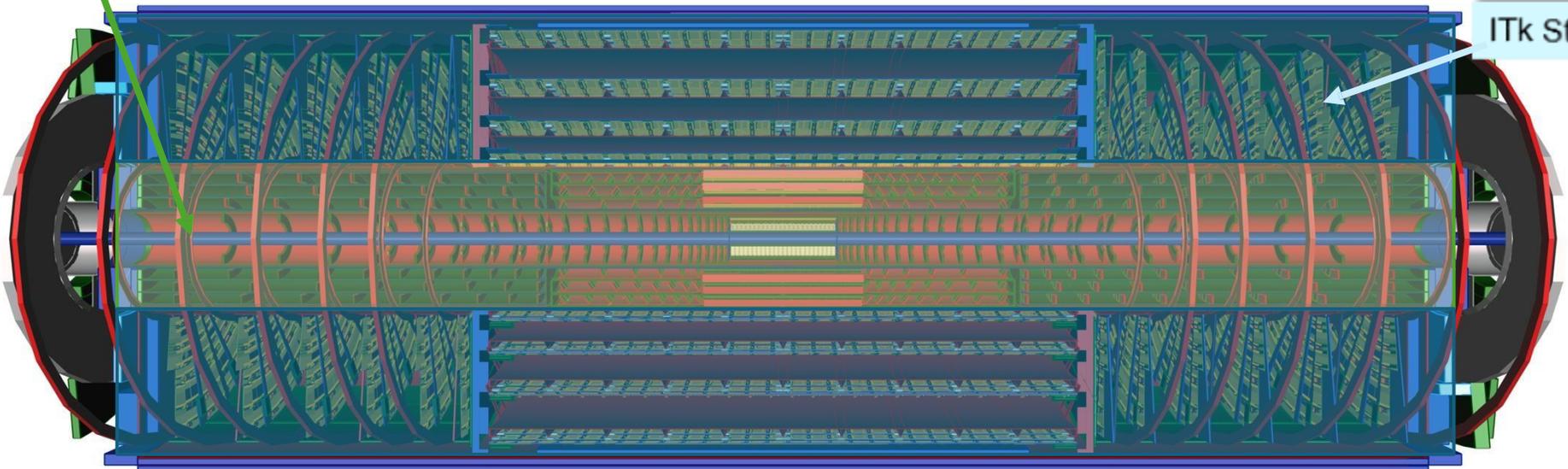
ATL-PHYS-PUB-2021-024

ITk Pixel

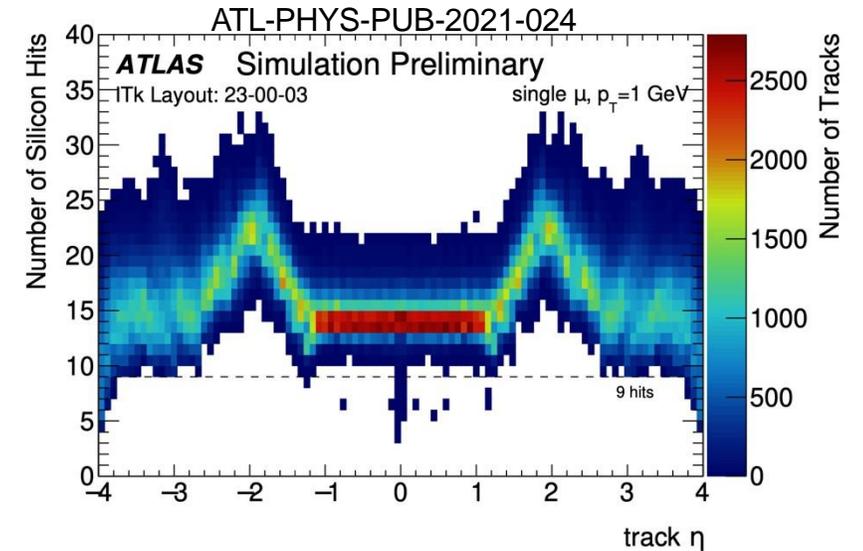
ITk Strip

For Pixel overview-  
see the talk of  
Umberto M.

For Strip overview-  
see the talk of  
Marta B.

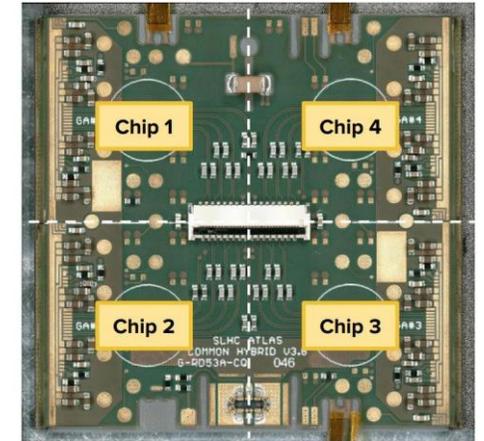


- Closest to the interaction point
- At least 9 hits/track
- Occupancy kept  $< 1\%$  thanks to the higher granularity
- Composed of two parts: **ITk Pixel** with 5 pixel barrels and rings and **ITk Strip** with 4 strip barrels and strip disks
- Replaceable two innermost layers at half of the lifetime: **ITk Pixel Inner System (IS)** with Endcaps and Barrels

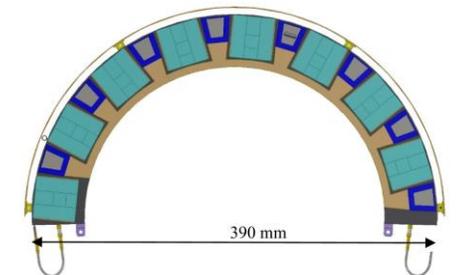
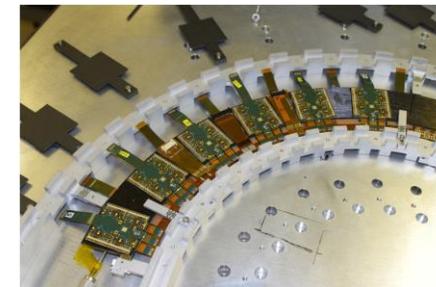


# Pixel Module Sites

- 10 clusters for pixel module assembly (31 assembly sites) and testing across the globe
- United Kingdom Pixels is one of the clusters
- UK cluster is responsible for assembly endcap quad pixel modules with planar sensors, QA/QC them, load them in half ring and deliver them to CERN
- UK cluster has three assembly and testing sites:
  - University of Glasgow
  - University of Liverpool
  - University of Oxford
- These three site will assemble and test about 600 modules each
- University of Glasgow has finished their pre-production batch with ITkPixV1.1 chip, and started their production batch of pixel modules with ITkPixV2 chip

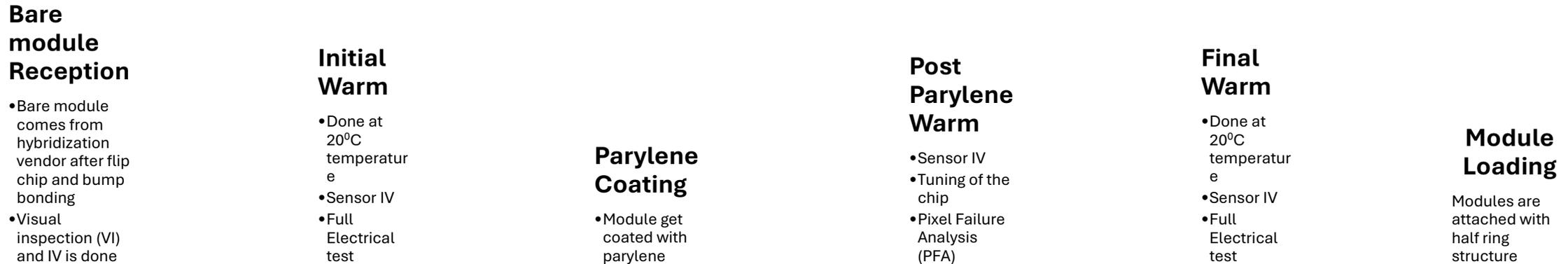


Quad module from top



Quad module half ring

# Pixel Module workflow



## Assembly

- Flexible PCB is glued with bare module
- Wirebonding is done
- Pull test is done
- Final VI

## Parylene Masking

- VI
- Mask put on module to prevent parylene to cover unwanted places
- Caps on connectors

## Parylene unmasking

- Masks are taken out
- Caps are taken out
- VI

## Thermal Cycle

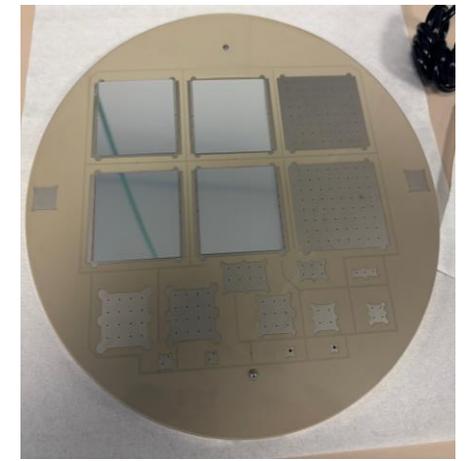
- Thermally cycle the for 10 cycles from 40°C to -45°C

## Final Cold

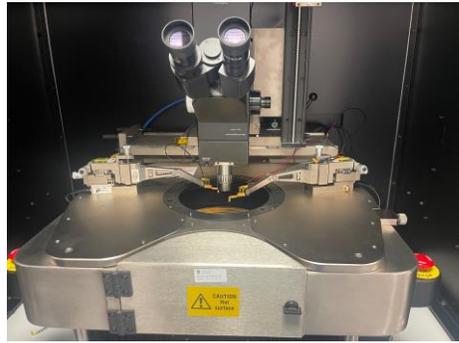
- Done at -15°C temperature
- Sensor IV
- Full Electrical test

# Bare Module reception

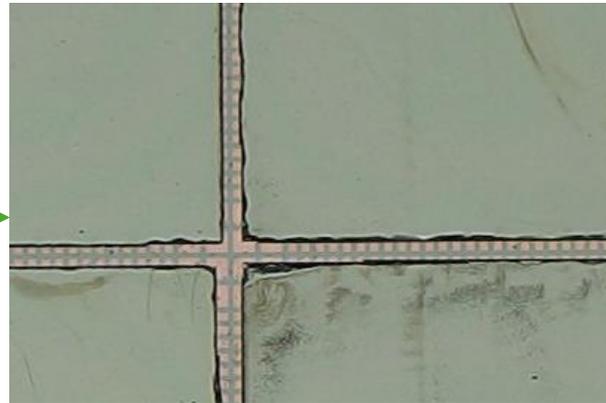
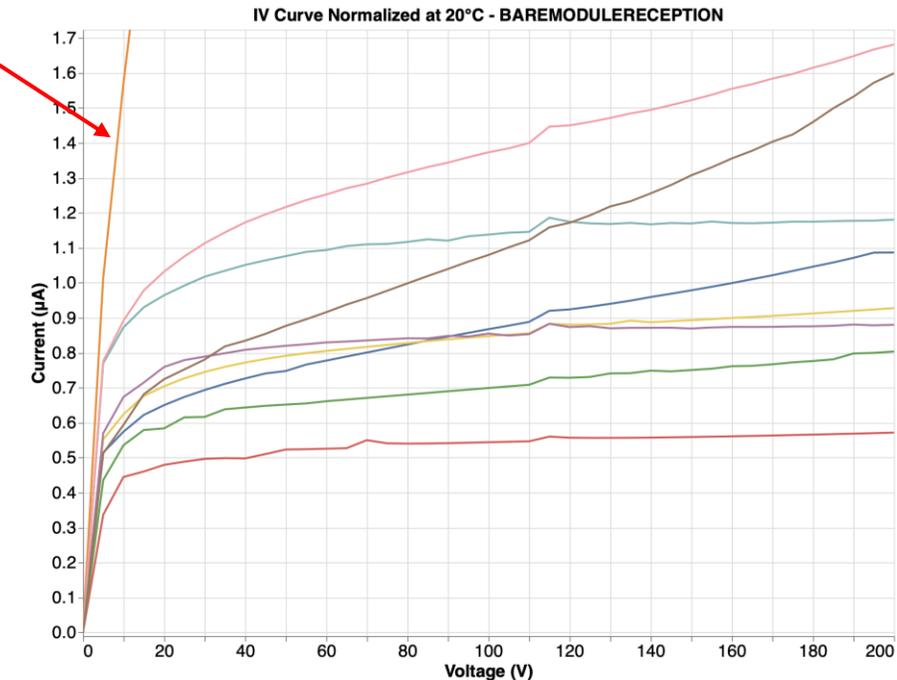
- Bare module comes from hybridization vendor after flip-chip of sensor and FE-chips
- Manually probed at probe station with specialized chuck
- Probed 26 bare modules with visual inspection, all with 150  $\mu\text{m}$  sensor
- One module has been failed for bad IV (greater than  $1.5 \mu\text{A}/\text{cm}^2$ )
- Automatic probing being developed



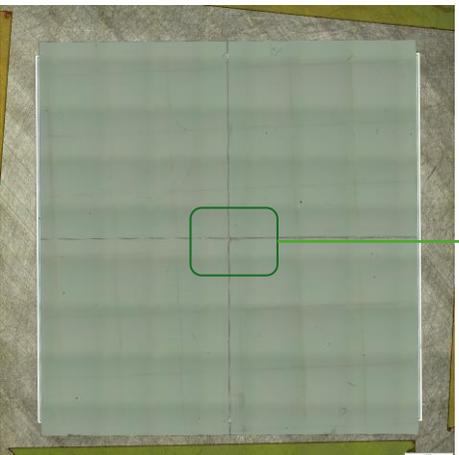
Specialize chuck for multi-module probing



Wentworth AVT702 probe station

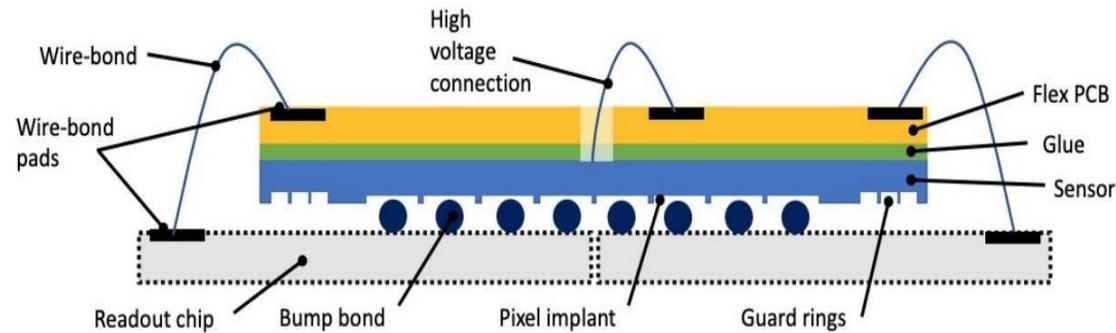
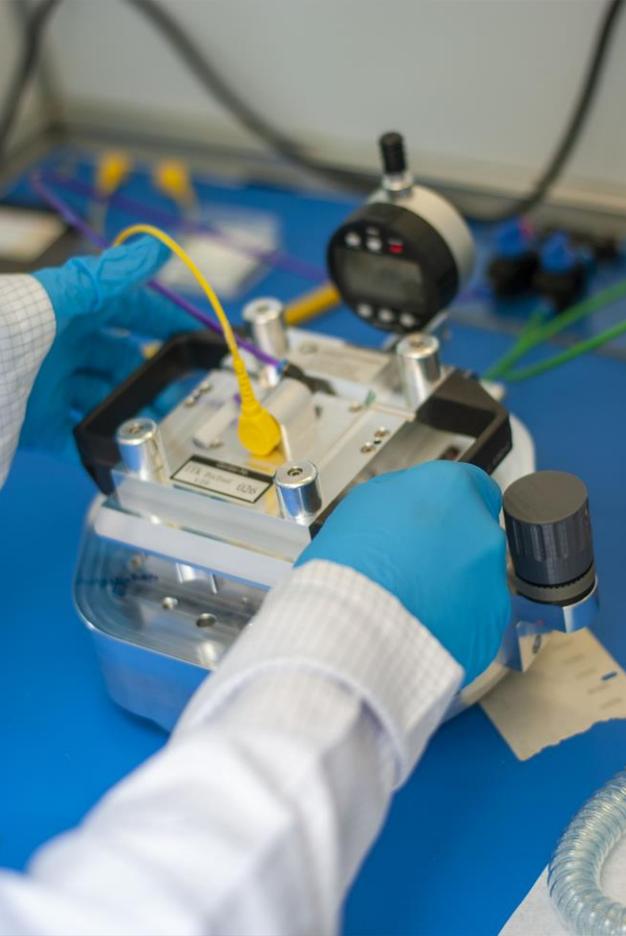


20UPGB43200139: an example of passed module

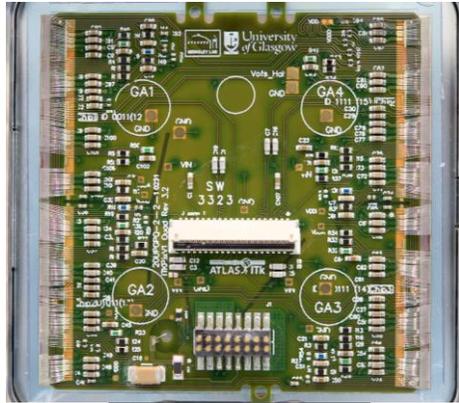


# Assembly

- Glasgow has four assembly stations, with four assembly jig
- It takes about 30 minutes to assemble a module, but about 24 hours to cure the glue in jig, wirebonding, pull test, visual inspection needs additional time
- assembly jig has been designed to minimize variation due to operator. It controls relative position of bare module and flex PCB and glue thickness.
- With four jigs, four modules can be made at a same time
- Glasgow has committed to produce 8 modules in a week with wire bonding, pull test and visual inspection



# Quality Control Testing



Quad Module

- After assembly, a visual inspection is done
- An **Initial Warm** test is done maintaining warm temperature (20°C)- a series of tests including module IV
- Again Visual inspection is done, connectors on module are masked in preparation for parylene coating of module and shipped to Liverpool for coating → Liverpool is going to parylene coat all the modules in UK cluster



Visual Inspection

- Module is shipped back to Glasgow, unmasked and visually inspected again, and made ready for **Final Test**:
  - **Post-parylene warm** test (20°C) is done, module is thermally cycled for 10 cycles from +40°C to -45°C
  - **Final Warm** test is done at warm temperature (20°C), and **Final Cold** test is done at cold temperature (-15°C) with a source scan with Mini X2 X-ray gun



Masking process



Masked Module

# Module testing setup (warm)

Vacuum

DAQ PC

- Card 1
- Card 2
- Card 3
- Card 4

DMM 6500  
(10 Ch)

HMP 4040  
LV

DCS  
GOLD

DCS  
GREEN

Wiener crate HV supply

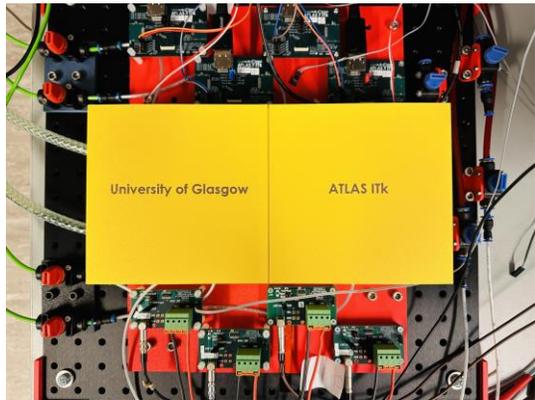
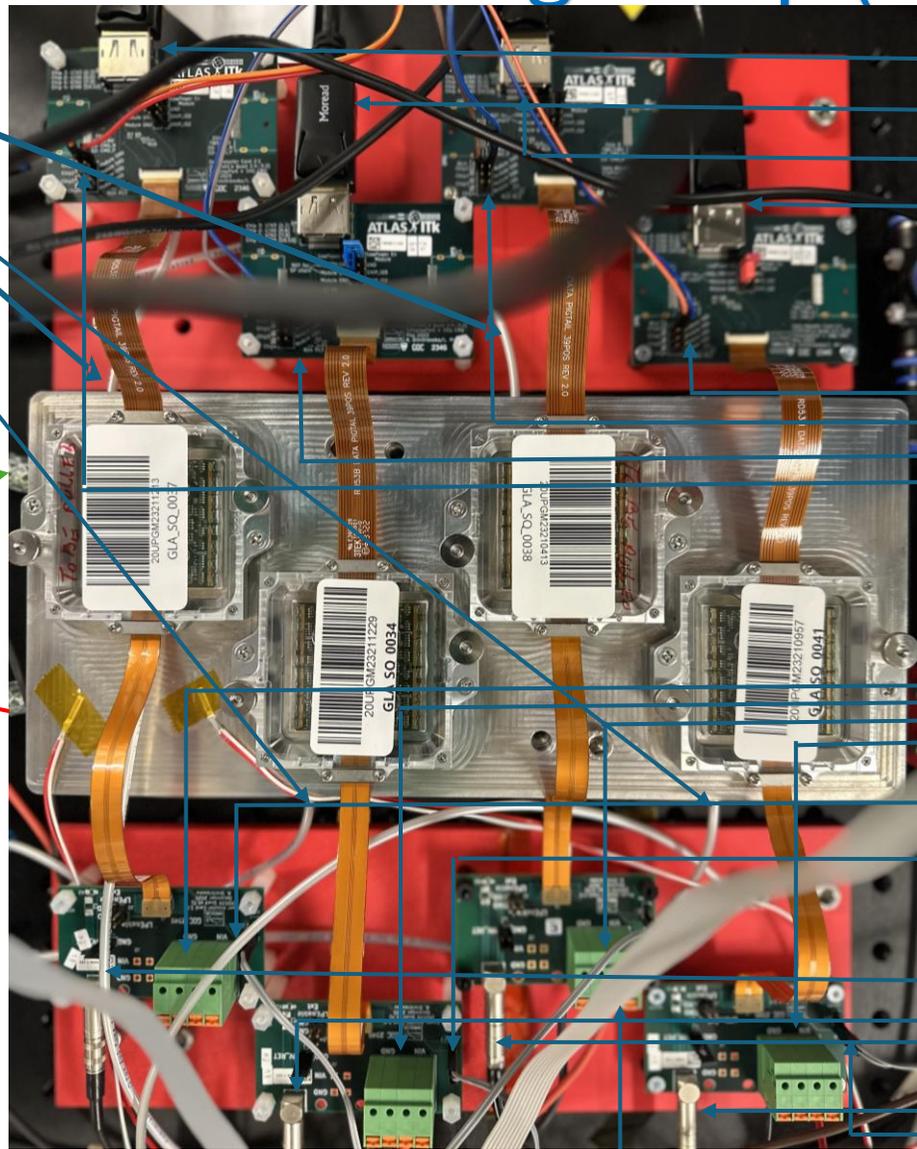
DCS  
Blue

DCS  
ORANGE

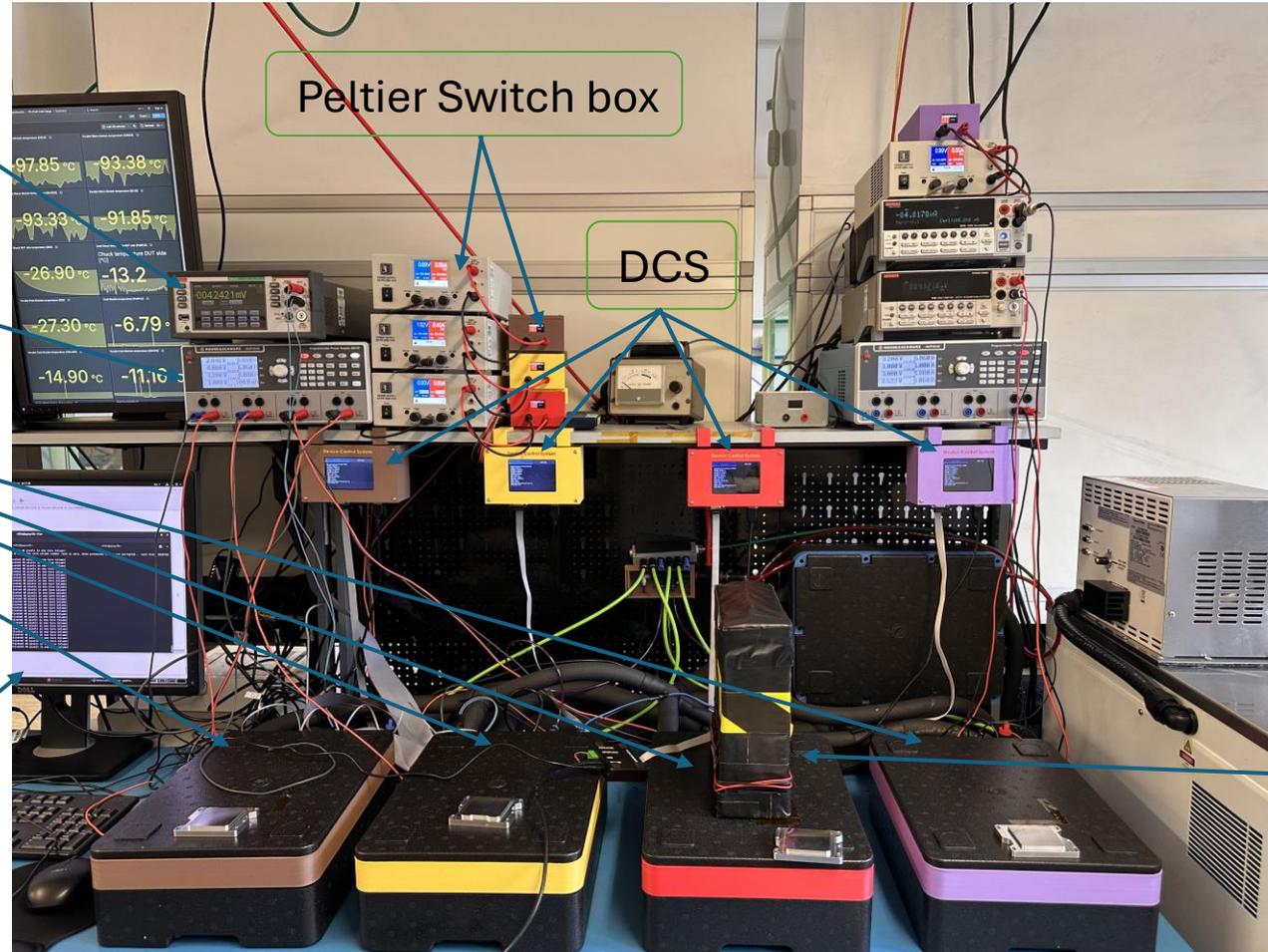
Warm parallel Setup

Chiller

- Chiller is always set to 14°C
- Four modules can run parallelly
- Four Device Control Setup (DCS) is there to read temperature and humidity of the four modules
- Initial warm test can be done in four modules by ~ 3 hours



# Module testing setup (Cold)



DMM 6500  
(10 Ch)

HMP 4040  
LV

Peltier Switch box

DCS

Wiener crate HV supply

DAQ PC

Card 1

Card 2

Card 3

Card 4

- Chiller is always set to -40°C
- Four modules can run parallelly
- Thermal cycle of 10 (+40°C to -45°C) takes almost 7 hours
- Final test takes almost two days

Chiller

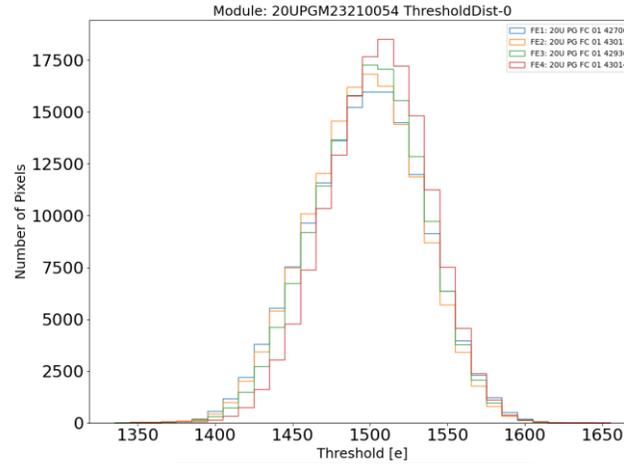
Mini X2 X-ray gun

Cold parallel Setup

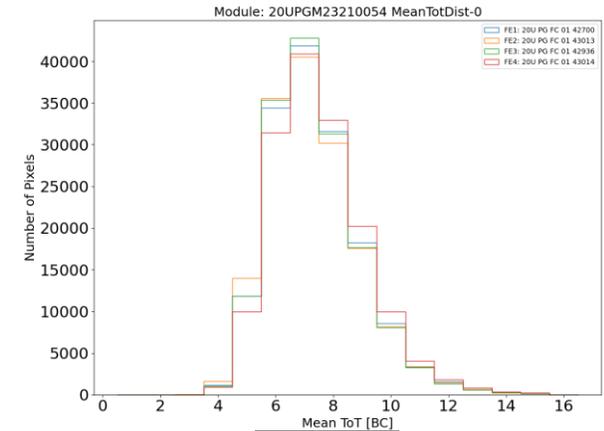
# Module test results

- In each stage of quality control process, a series of tests are repeated including IV at the different stages
- Electrical tests include trimming of different internal circuits and registers, evaluation of internal currents and voltages
- Tests also includes scanning of all pixels, tuning , disconnected bump scan and source scan with X-ray gun
- To pass, a module has to pass in all the tests (green) at all stages

Key	Data			
MODULE_TEMPERATURE	20			
ANALYSIS_VERSION	localdb-tools v2.5.0			
QUAD-MODULE_ADC_CALIBRATION	1	2	3	4
QUAD-MODULE_SLDO	1	2	3	4
QUAD-MODULE_VCAL_CALIBRATION	1	2	3	4
QUAD-MODULE_ANALOG_READBACK	1	2	3	4
QUAD-MODULE_LP_MODE	1	2	3	4
QUAD-MODULE_INJECTION_CAPACITANCE	1	2	3	4
QUAD-MODULE_MIN_HEALTH_TEST	1	2	3	4
QUAD-MODULE_TUNING	1	2	3	4
QUAD-MODULE_PIXEL_FAILURE_ANALYSIS	1	2	3	4
MODULE_BAD_PIXEL_NUMBER	62			
MODULE_ELECTRICALLY_BAD_PIXEL_NUMBER	57			
MODULE_DISCONNECTED_PIXEL_NUMBER	5			
QUAD-MODULE_DATA_TRANSMISSION	1	2	3	4
MODULE_DISABLED_COLUMNS_NUMBER	0			



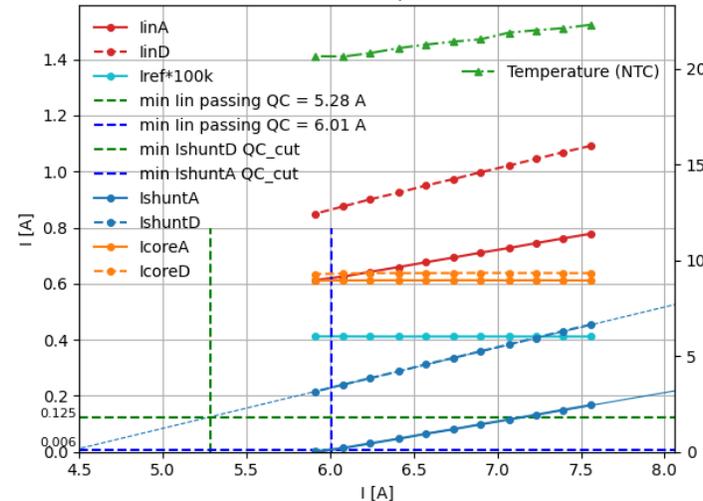
Threshold scan after tuning



ToT scan

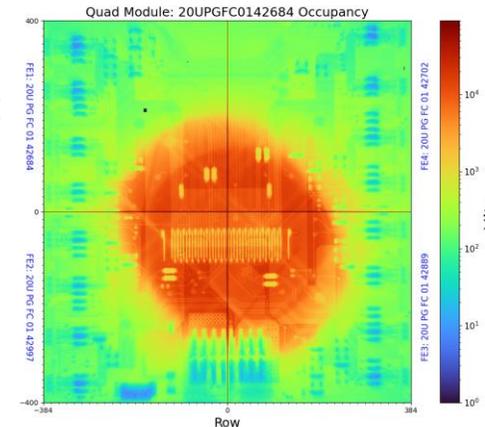
SLDO

Currents for chip: 0x22ea5

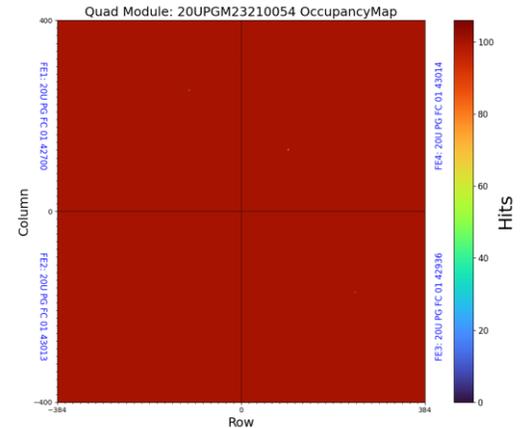


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Source scan

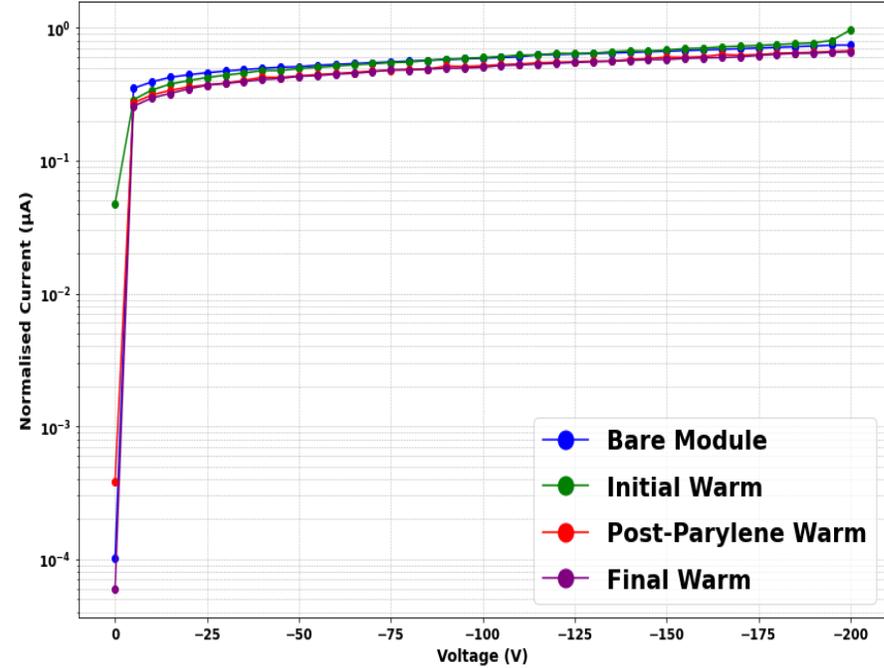


Disconnected Bump scan



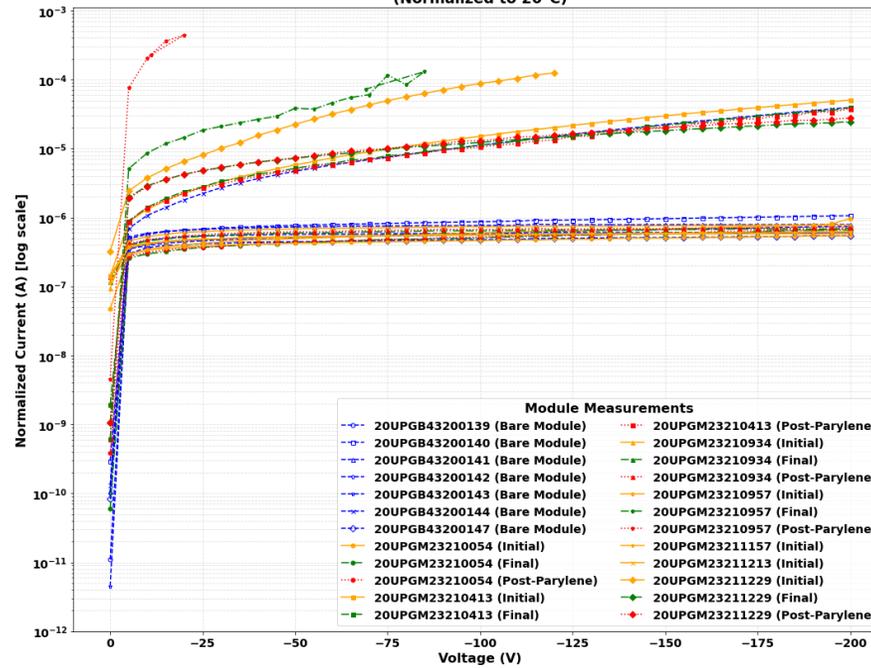
# Module IV yield

Module 20UPGM23210054 — Comparison of Warm Normalized IV Curves (at 20°C)



IV of one good module on all stage

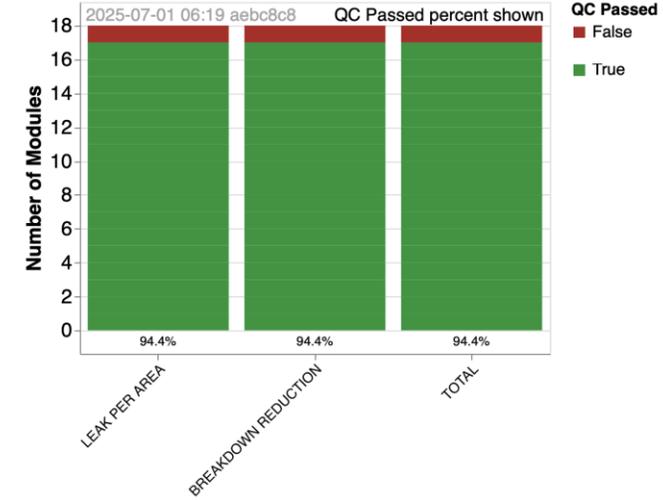
Comparison of Initial vs. Bare Module vs. Final vs. Post-Parylene I-V Curves (Normalized to 20°C)



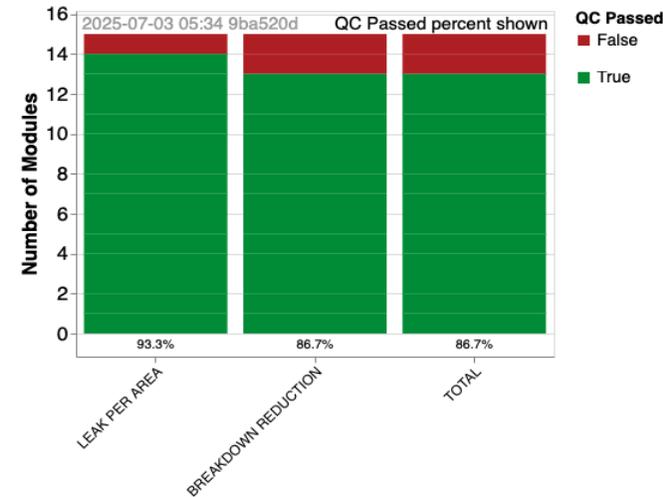
IV of all module on all stage

- 26 bare modules received, and reception tests done, 18 have been assembled into modules and went through initial test. 14 were tested through final stage
- At initial test, one module breaks down early
- At Final test, another module recorded reduction in breakdown voltage (reduction more than 10 V)
- All other module has leakage current less than  $1.5 \mu\text{A}/\text{cm}^2$ , and breakdown voltage more than 200 V

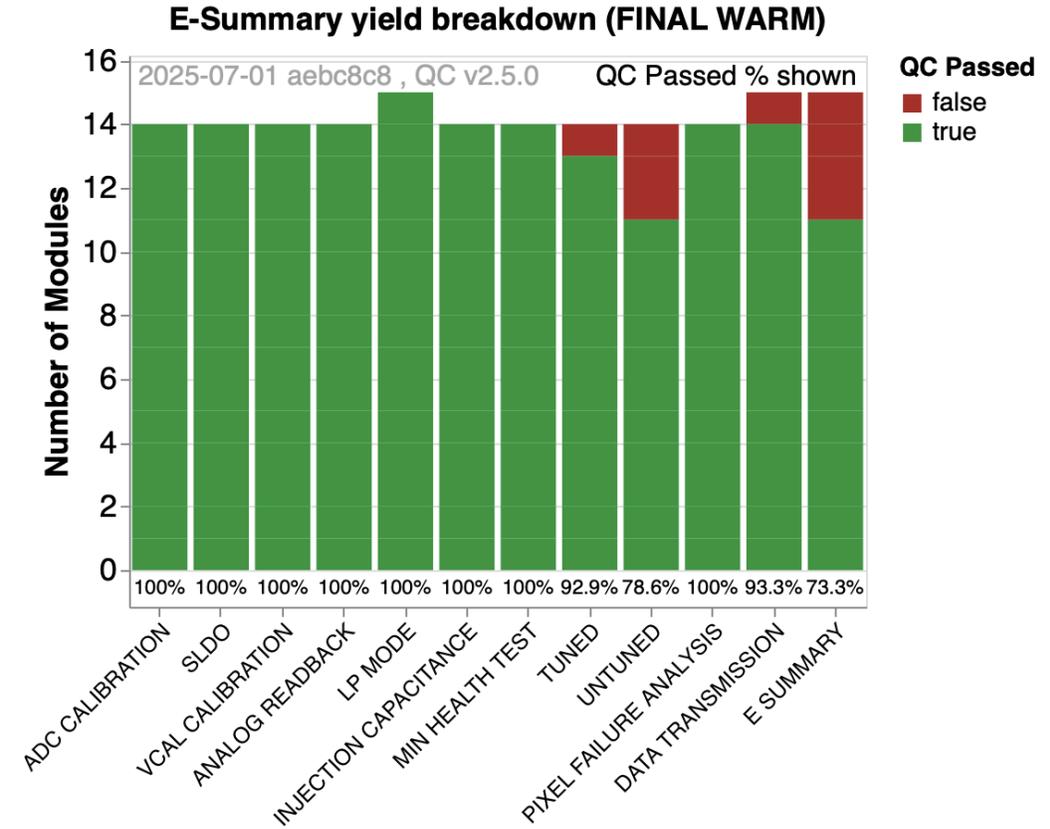
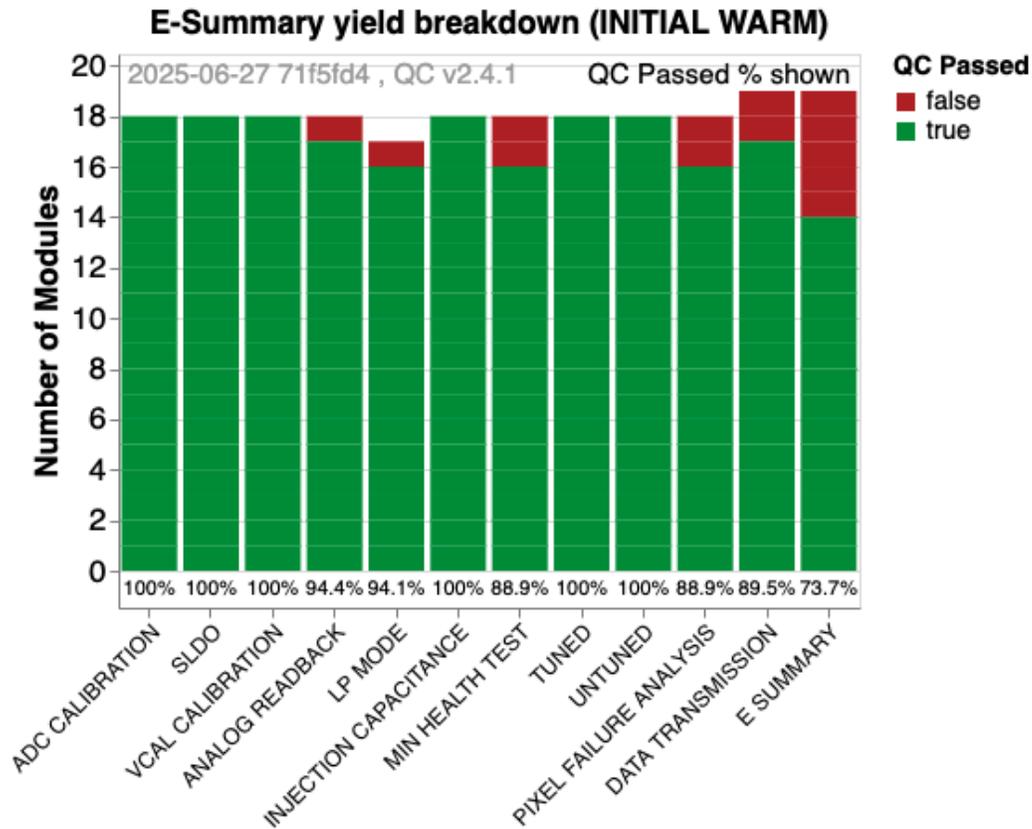
Breakdown for IV\_MEASURE at INITIAL\_WARM



Breakdown for IV\_MEASURE at FINAL\_WARM



# Module Electrical QC yield



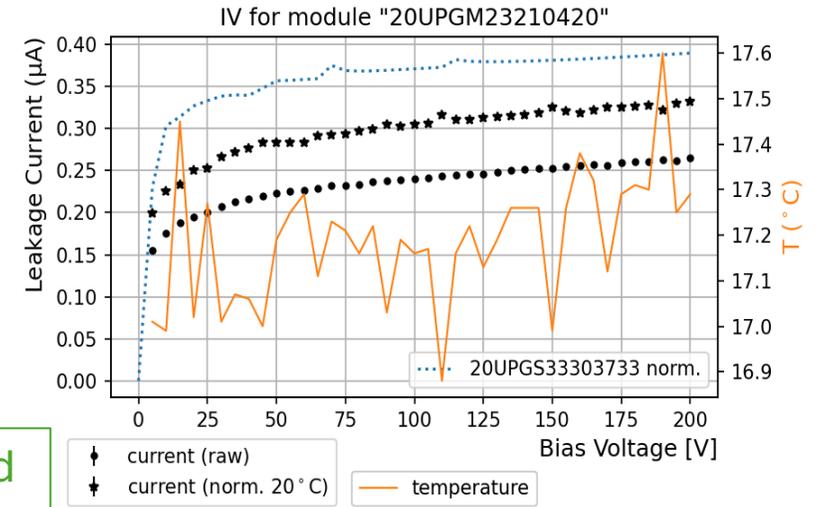
- One of the modules have one chip (chip 4) disabled
- Some of the modules are yet to be finished testing after parylene coating
- Overall yield ~73% , which is much better then pre-production yield (53.8%)

# Before and after extensive Thermal cycle

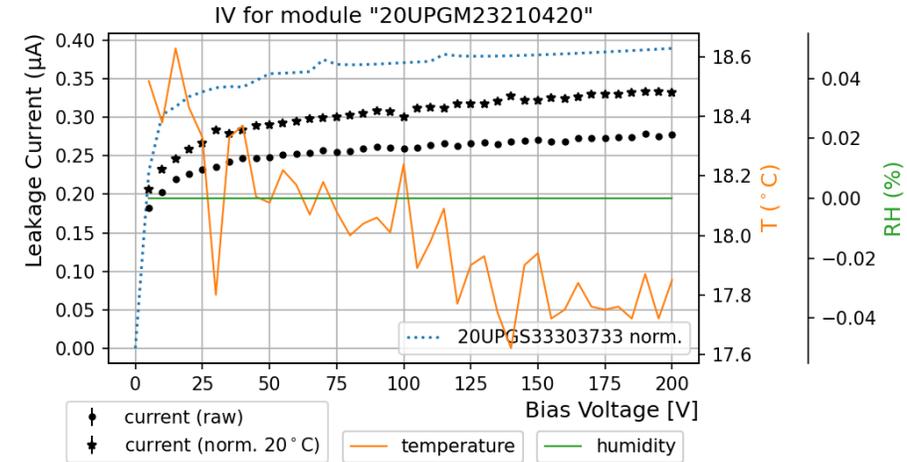
- One module was considered to perform long Thermal cycles (normal thermal cycle consist of 10 cycles)
- Cycled within +40°C to -45°C
- Cycled 70 time over two days
- Intention is to stress the module thermally to see any deviation in module characteristics, specially bump bond delamination

	Before Thermal Cycle	After Thermal Cycle		
MODULE_BAD_PIXEL_NUMBER	91326	91326		
MODULE_ELECTRICALLY_BAD_PIXEL_NUMBER	91321	91321		
MODULE_DISCONNECTED_PIXEL_NUMBER	5	6		
QUAD-MODULE_PIXEL_FAILURE_ANALYSIS	1	2	3	4

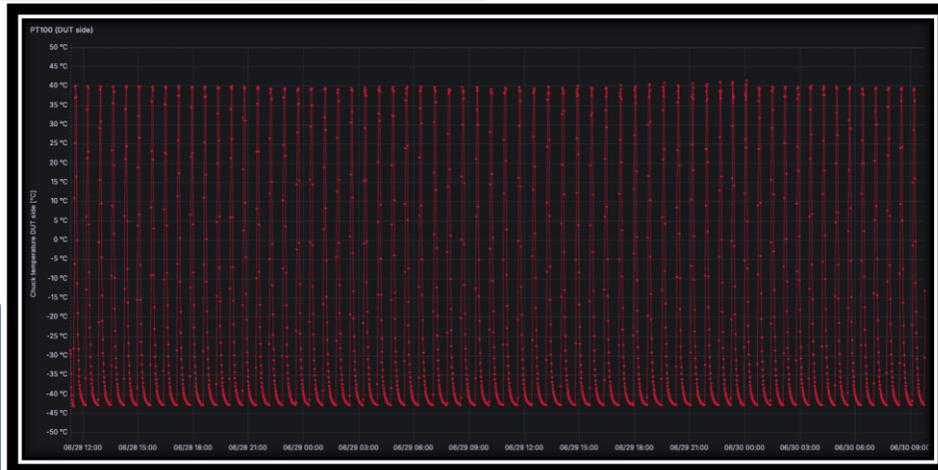
No Difference is detected in terms of IV and Bump delamination



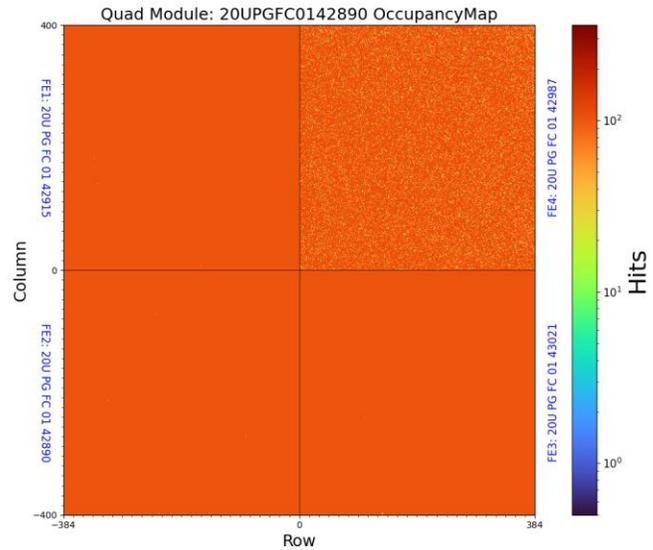
Before TC



After TC

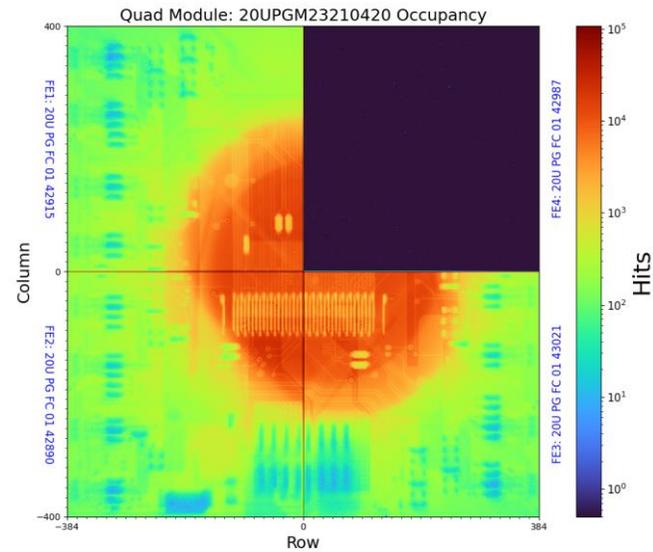


# Before and after extensive Thermal cycle-continued



Before TC

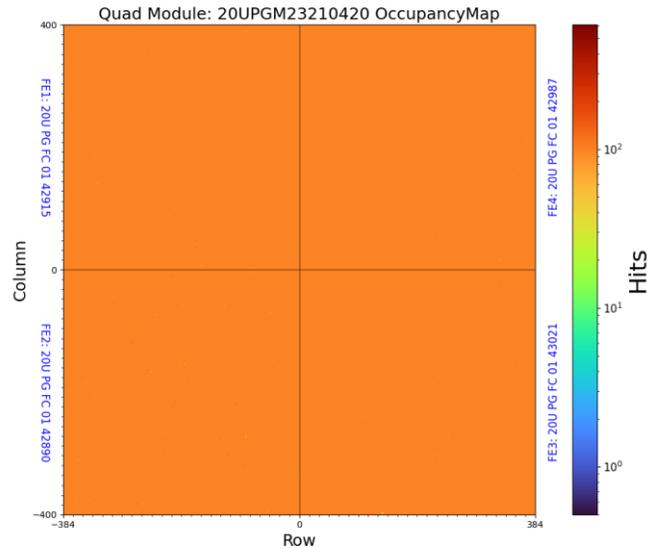
Disconnected  
Bump Scan



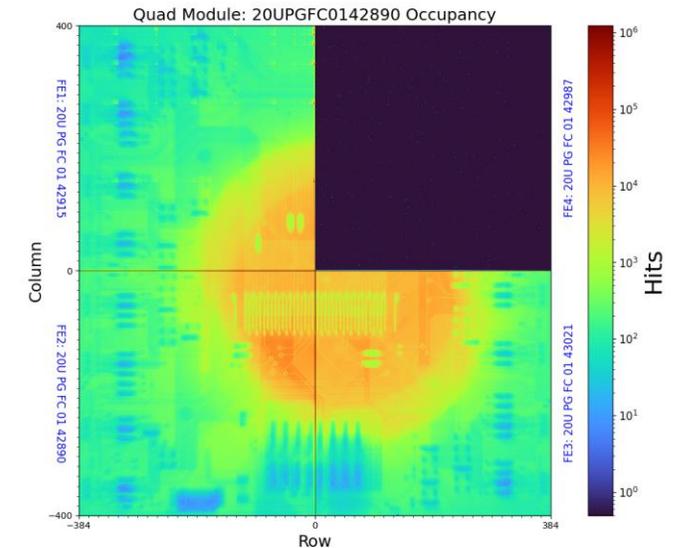
After TC

Before TC

Source Scan



- Chip 4 has bad communication, do not record any hits in source scan
- No significant changes can be seen, other than reduction of noise in chip 4



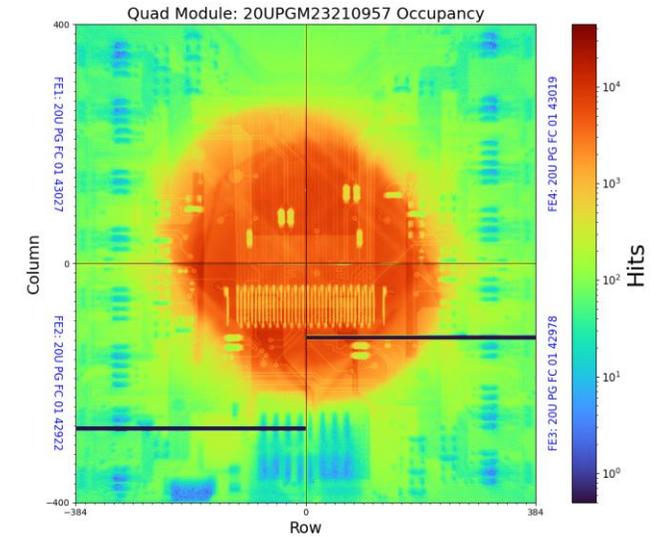
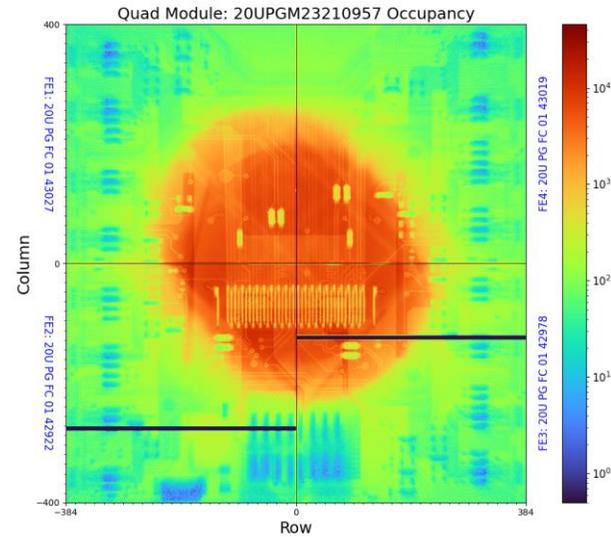
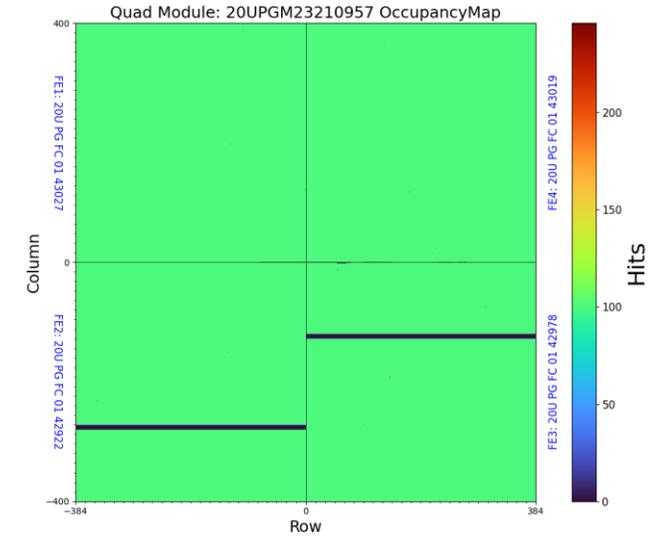
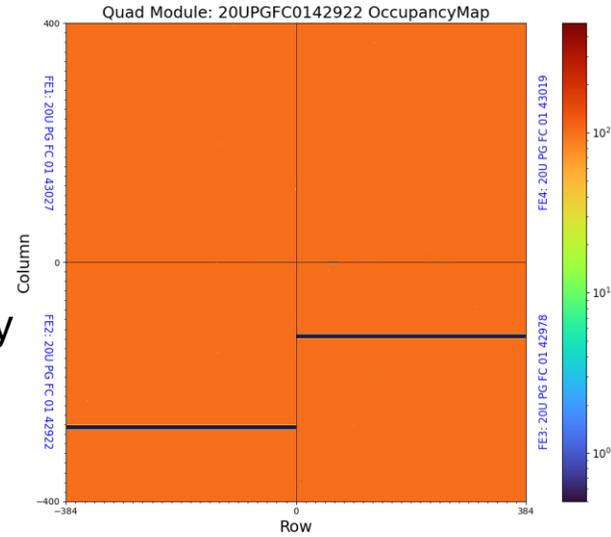
After TC

# Before and after extensive Thermal cycle-CC module

- Another module was considered to perform long Thermal cycles with broken core column (known as *Core Column* issue)
- Cycled within +40°C to -45°C
- Cycled 70 time over two days
- Intention is to stress the module thermally to see any deviation , or increase in more broken columns

No Difference is detected in terms of bump delamination or increase of core column problem

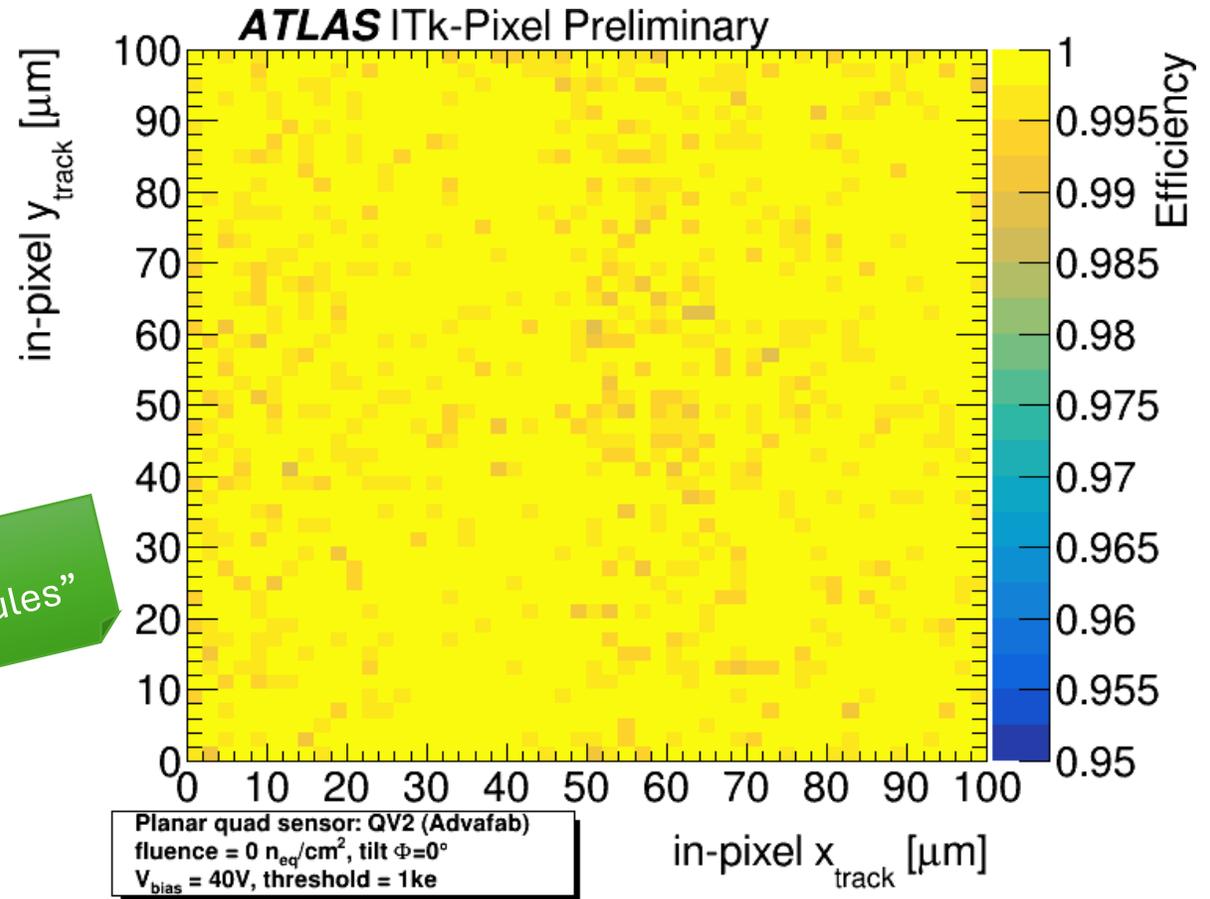
	Before Thermal Cycle		After Thermal Cycle	
MODULE_BAD_PIXEL_NUMBER	6554		6553	
MODULE_ELECTRICALLY_BAD_PIXEL_NUMBER	6296		6301	
MODULE_DISCONNECTED_PIXEL_NUMBER	258		252	
QUAD-MODULE_PIXEL_FAILURE_ANALYSIS	1	2	3	4



# Test beam result

- One module was tested under 120 GeV pion beam at CERN
- Module was tested before irradiation
- It showed more than 99 % hit efficiency at 20 V bias at sensor
- More study will be done after irradiation

“Up-to-date test beam results of ATLAS ITk Pixel sensors and modules”  
More information at poster session



[https://indico.cern.ch/event/1455346/contributions/6323044/attachments/3006994/5300730/Trento\\_2025\\_ITk\\_Pixel\\_Testbeam\\_CKrause.pdf](https://indico.cern.ch/event/1455346/contributions/6323044/attachments/3006994/5300730/Trento_2025_ITk_Pixel_Testbeam_CKrause.pdf)

# Conclusion

- Production has started slowly, but progressively
- No significant bump delamination was seen in any module
- Though we have a bit less yield (~73%) than the target yield (78%), we are trying to improve
- Maximum failure came from core column, software and a bit handling
- Have identified some problems in process, and learning more and adapting
- With more experience predicting to be much better in future production batches

