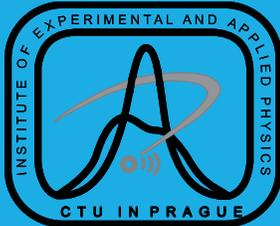




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# KATHERINE READOUT FOR TIMEPIX4: A NOVEL ACQUISITION ECOSYSTEM FOR TIMEPIX4-BASED DETECTORS

International Workshop  
**26th iWoRiD**  
on Radiation Imaging Detectors



# MOTIVATION – KATHERINE'S SHOW MUST GO ON...

- **Timepix4 ASIC**

- Developed in Medipix collaboration, CERN
- 512 x 448 pixels, 55  $\mu\text{m}$  pixel pitch
- 195 ps time binning
- 16x 10 Gbps fast output lines  $\Rightarrow$  2.5 Ghits/s per chip
- Digital pixels (great feature for a triggering)
- TSV support

- **Katherine readout for Timepix2/3**

- Chipboards, software, methodology....
- Ethernet, USB interface
- Long distances, installation in CERN (ALTA, LHCb, ALICE, ...)

**Our goal: User-friendly readout system for general purpose**



# WHY “ECOSYSTEM“?



- Why the title of this talk is: **”A novel acquisition ecosystem for Timepix4...”**
- **Ecosystem** - it might sound a bit pretentious, maybe even too marketing-driven
- **Because we are talking about:**

**Chipboard and cabling**

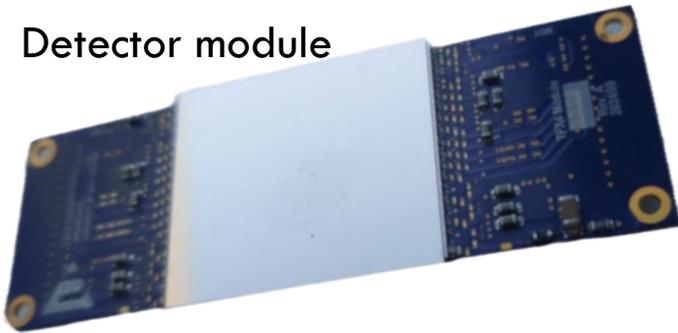
**Readout device**

**Control SW**

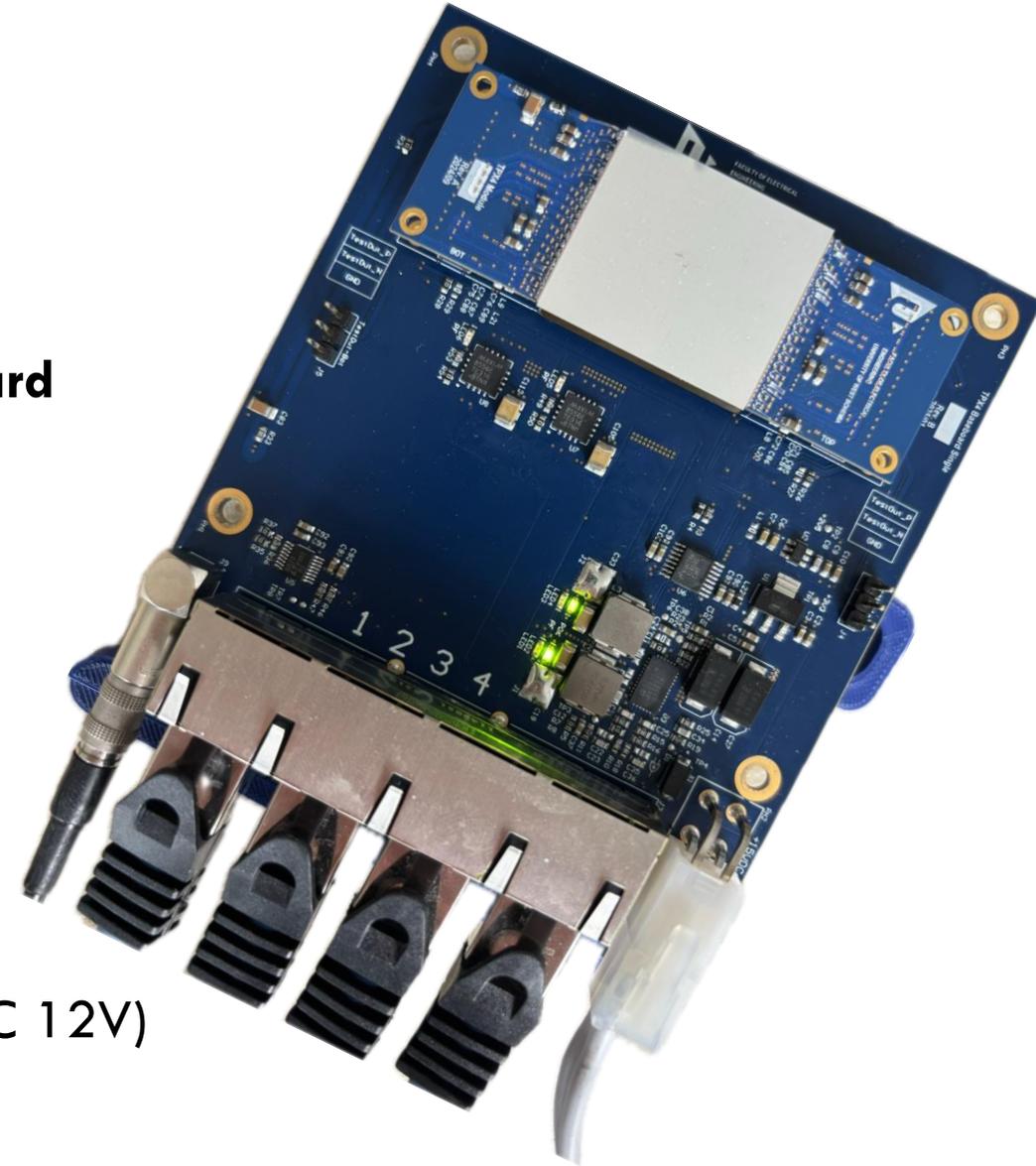
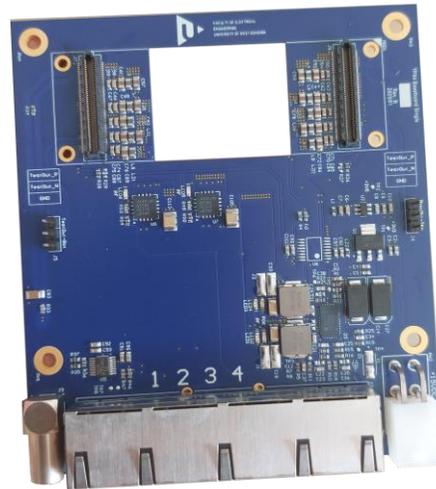
# TIMEPIX4 – CHIPBOARD

- Our solution? Fully modular approach...
- **Modular chipboard = detector module + base board**
- It is fine to reuse chips and share them via projects....

Detector module



Base board



- **Connectors:** 4x RJ45 (data), Lemo (bias), Molex (DC 12V)
- **Module:** 8x fast serial lines; **Base board:** 4x

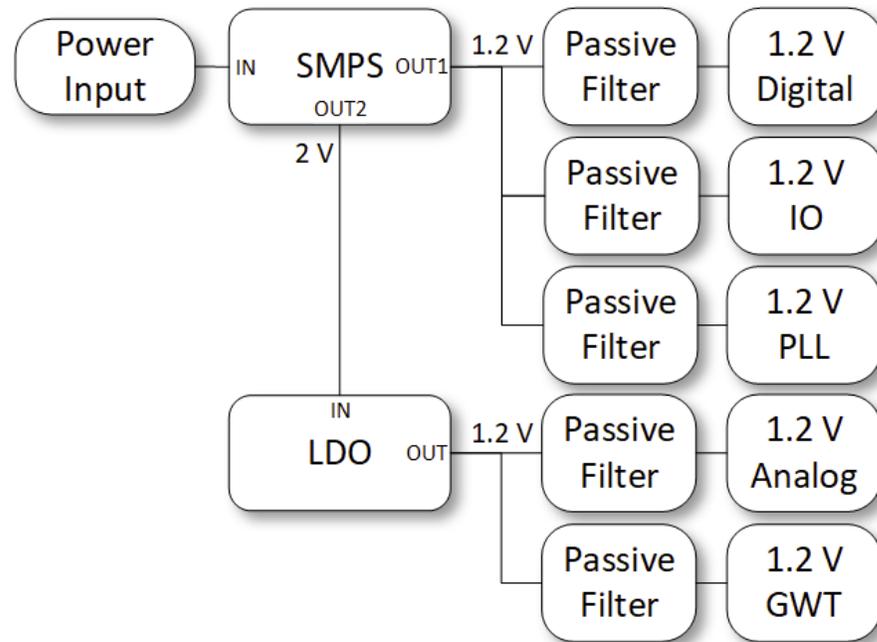
Now: version for wire-bonded chip ready and tested, TSV ready for testing

# TIMEPIX4 – CHIPBOARD

- Switched-mode **pre-regulation** of voltage (from 12V)
  - Less demands on cabling, better stability...

„fixed“ prototype

Prototype in housing



- Speed? 2.5 Gbps/line in 5 m cable length (cat 8.1)

# READOUT DEVICE — BASIC FEATURES

## KATHERINE FOR TIMEPIX4

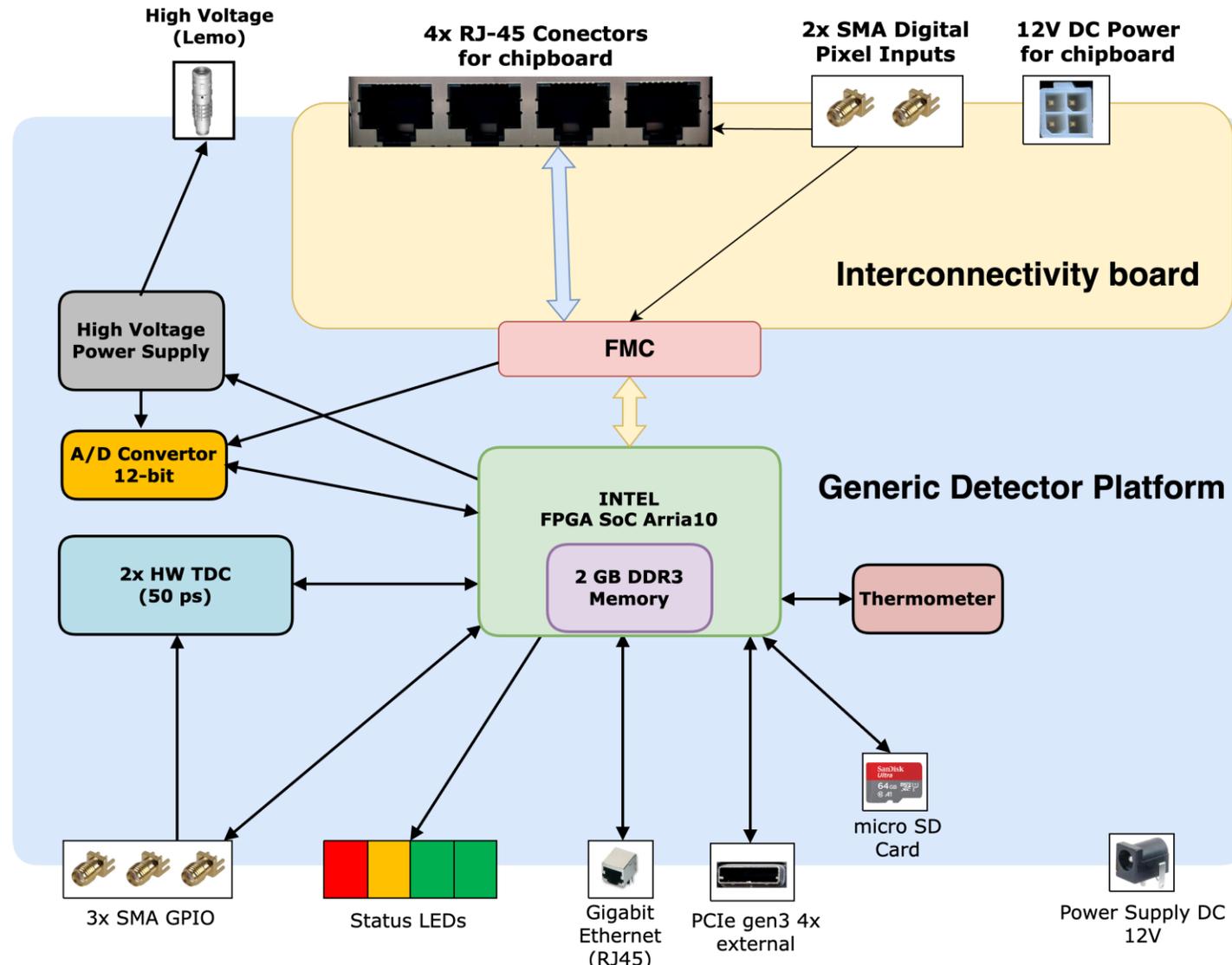
- Modular concept: **Generic Detector Platform (mainboard) + interconnectivity board** (for specific detector/configuration)
  - Currently only interconnectivity board for single chip; version for a pair of chipboards during summer.
- Based on Intel **SoC FPGA Arria10 (dual-core Cortex-A9 + FPGA), 2 GB DDR4** memory
  - CPU can come in handy for data processing
- Bias voltage source in the **range of  $\pm 1$  kV**, including leakage current measurement
  - Wide support of sensors
- Providing with power supply voltage (1.2V) for at least a single-chip chipboard
  - User does not want to use external power supply!
- GPIO ports for straightforward integration into existing measurement chains
  - Key factor for adoption of the readout system
  - On-chip termination, time-stamping, digital pixel feeding, start/stop trigger, external clock input

# READOUT DEVICE — BASIC FEATURES

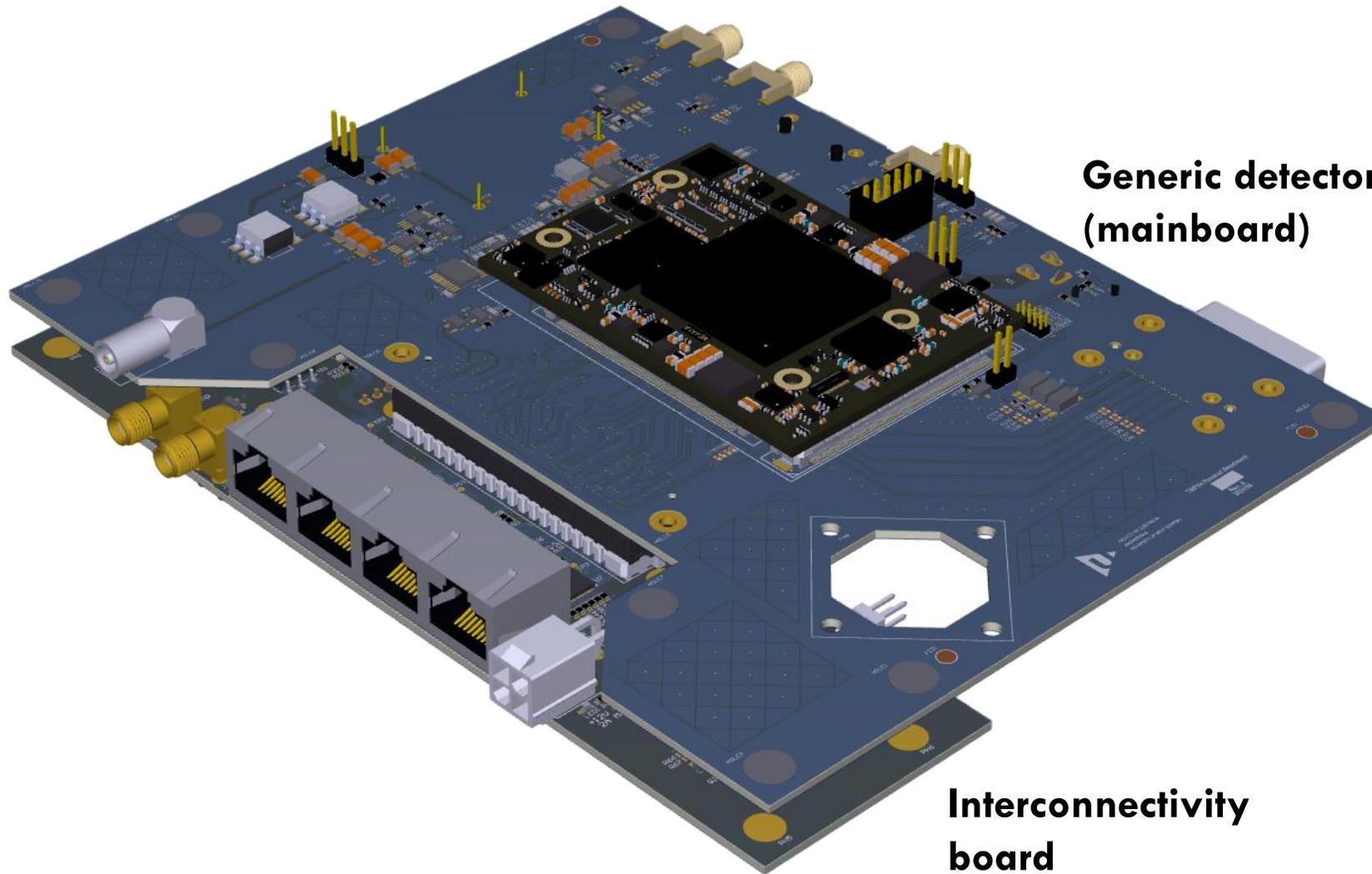
## KATHERINE FOR TIMEPIX4

- TDC components for precise time-stamping of external trigger signals
  - TDC is implemented in an FPGA, **hardware TDC on board (50 ps time binning)**
- **Timepix4 connectivity: 8x 2.56 – 5.12 Gbps** (can be shared within more chips)
- Low level data processing – decoding ToT/ToA => recalculation inside device
- Smart commands:
  - Control SW does not take care of internal Timepix4 registers
  - Configuration of pixels is accessible in logical addressing X[0; 511] Y[0, 447], not in raw Timepix4 address approach
- Extra ToA bits (32 bits) – automatically added into data stream
  - Only small influence on bandwidth; **Max. acquisition ~ 80 days**
- **Communication interfaces: 1 Gb Ethernet (UDP), PCIe Gen3 4x**

# READOUT DEVICE — CONCEPT SCHEME

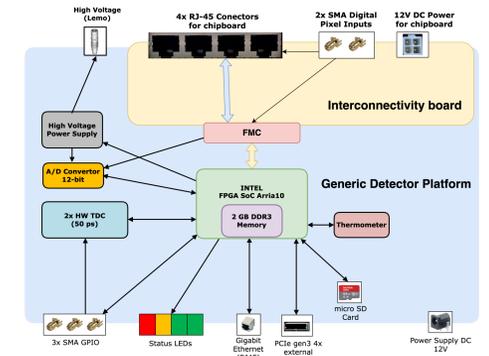


# READOUT DEVICE — 3D MODEL

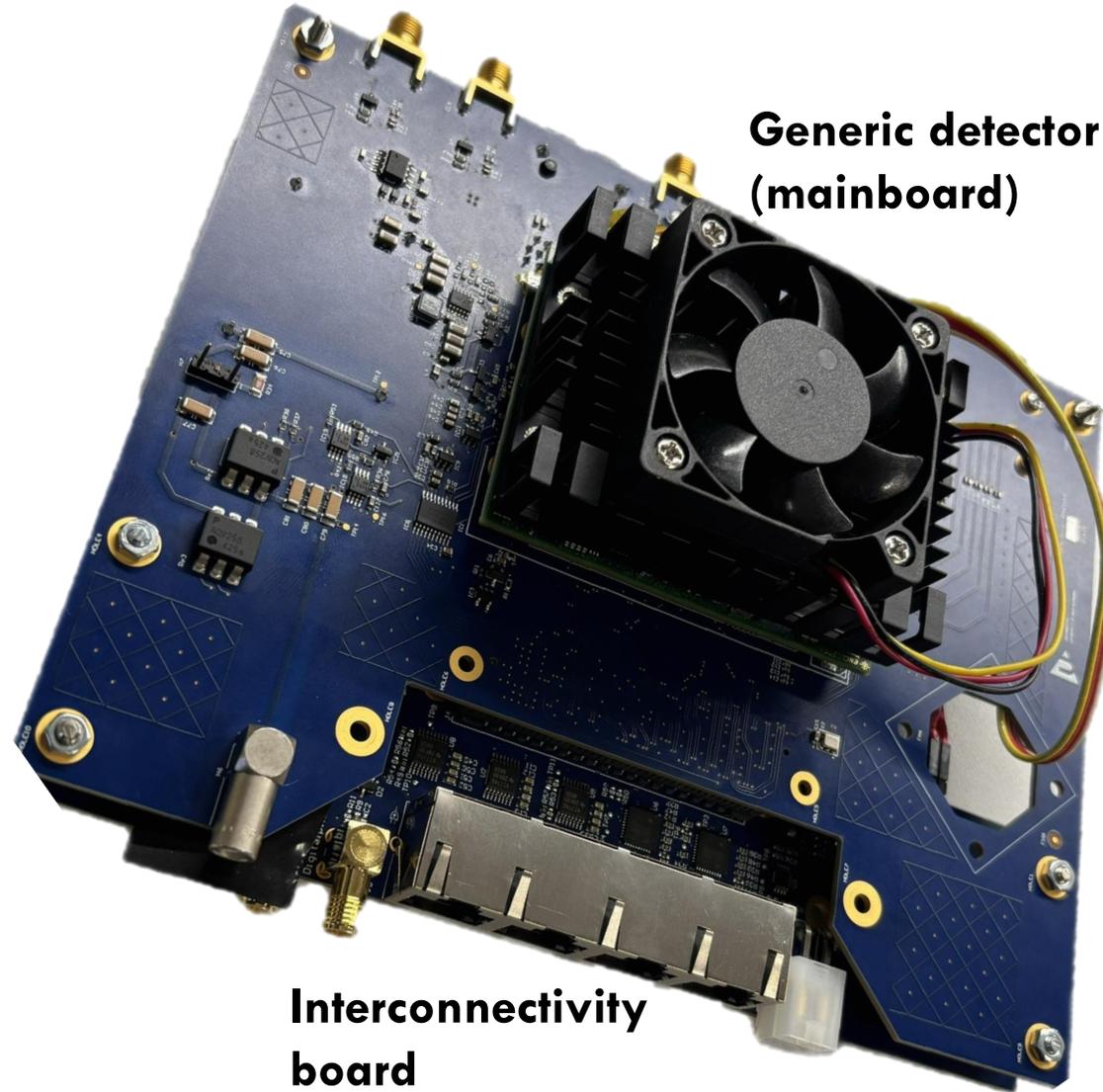


**Generic detector platform  
(mainboard)**

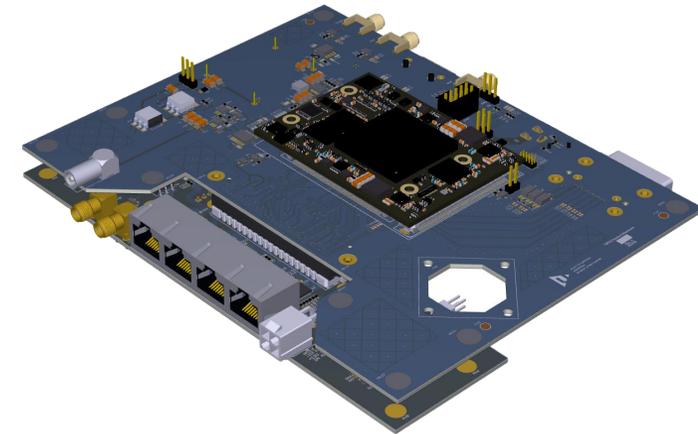
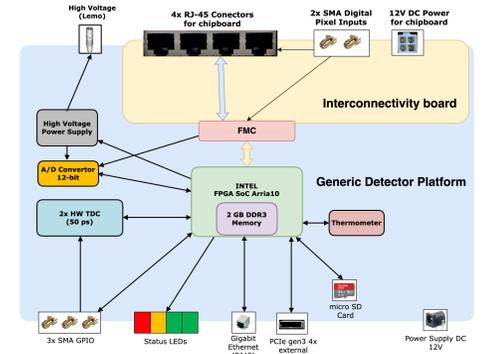
**Interconnectivity  
board**



# READOUT DEVICE — COMPLETED

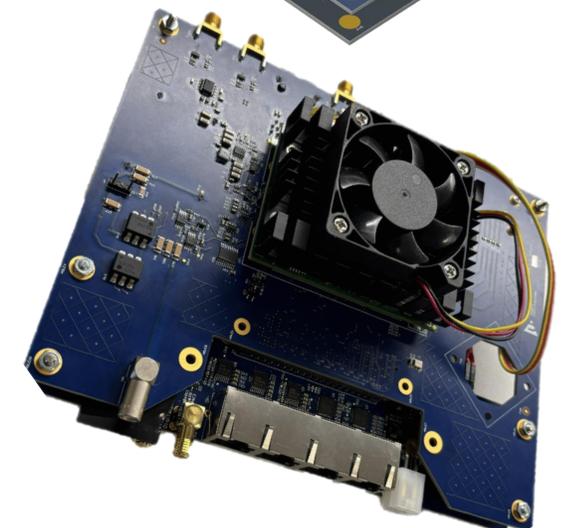
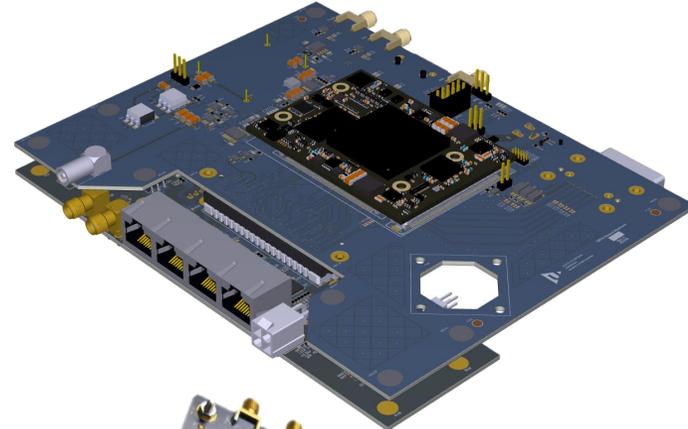
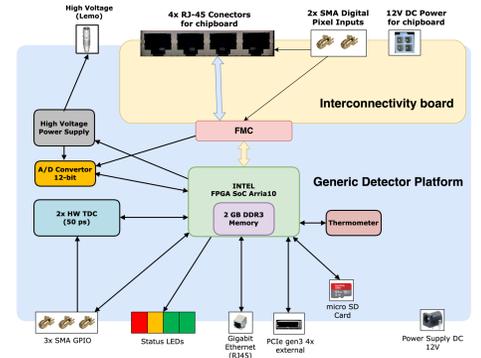


**Generic detector platform  
(mainboard)**



**Interconnectivity  
board**

# READOUT DEVICE — HOUSING



# READOUT DEVICE — INTERFACES WITH COMPUTER

- Communication interfaces
  - **Gigabit Ethernet** (11 MHit/s) - fully working
  - **PCIe Gen3 4x** (up to 350 MHit/s) – working with limited speed (30 MHit/s), still under development
- In first release, PCIe only for pixel data, ETH for control & pixel data



# SOFTWARE SUPPORT — CONTROL SOFTWARE

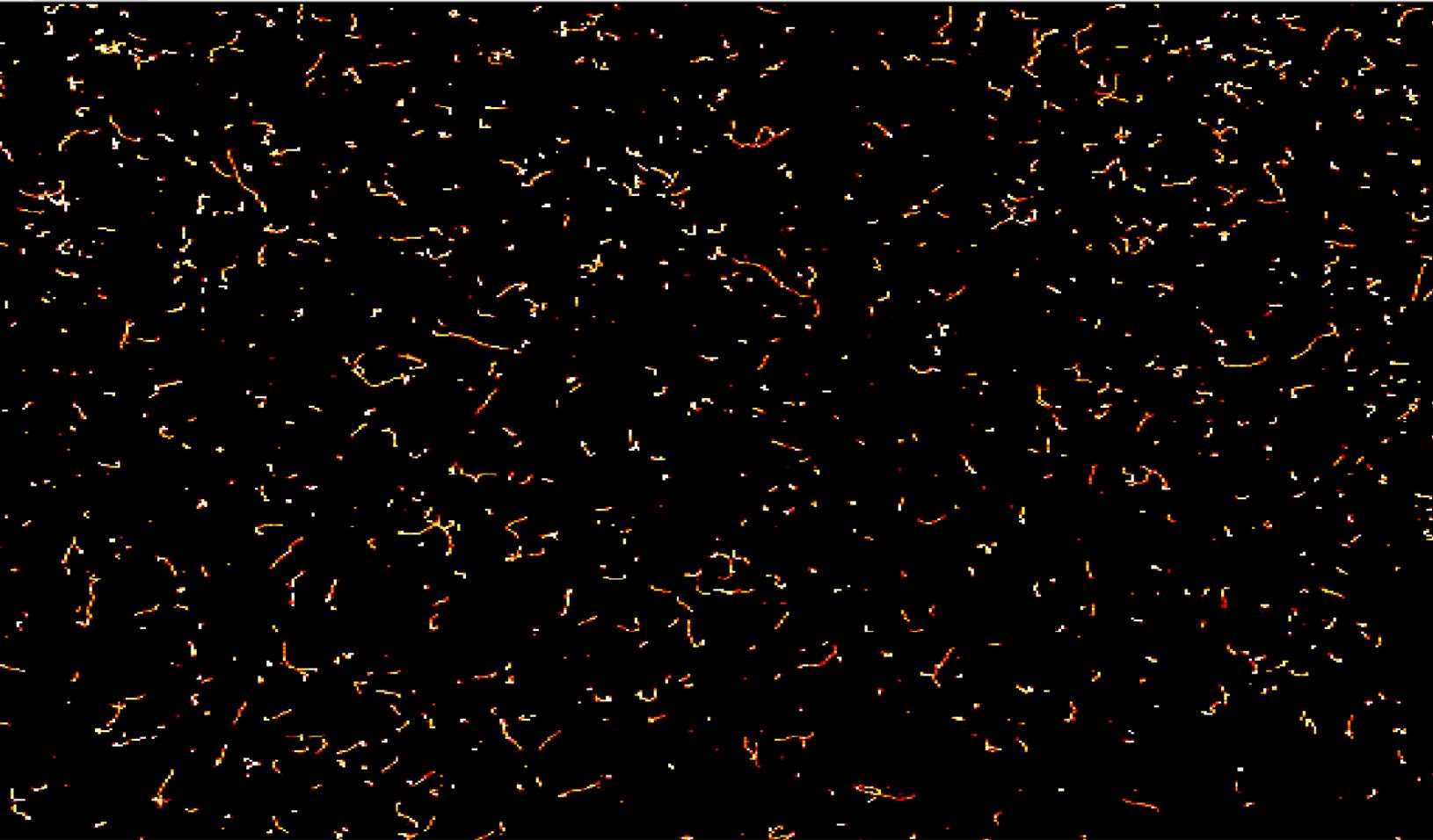
- Two branches of development...
- **Burdaman SW for Timepix4:** Tool for control and data acquisition
  - First version released
  - Based on Burdaman for Timepix2/3; Windows platform only
  - Output to text file
  - Internal DAC settings, DACs scanning
  - Equalization of pixel matrix; Threshold scanning (for threshold calibration)
  - GPIO settings, LEDs settings, external triggering of acquisition
- **Track Lab SW** (created by Petr Mánek)
  - Great tool for detector control, data acquisition and for data analysis
  - Support for all version of Katherine and all IEAP/UWB devices
  - <https://software.utef.cvut.cz/tracklab/>
  - ***Katherine for Timepix4 should be added withing Q4/2025***



# SOFTWARE SUPPORT — BURDAMAN SW

---BurdaMan--- Chip ID: chip was not found | IP address of readout: 192.168.1.40

Chip: chip was not found  Multiview



Energy  Time  Count  Mask Bits  Pixel Th

X: 454 Y: 430

Measurement Chip Settings Readout HW

Digital Test

Grid  Ratio

**Acquisition settings:**

Time [s] 40 Frames 1

**Start**

Repeat  Save to RAM

Z:\temp\tpx4\\_calibratio ..

Save Results to File

**Detector mode:**

ToA & ToT

PC24b Threshold: 0

**Threshold 0:** 605 - keV

**Threshold 1:** 1000 - keV

**Threshold 2:** 1000 - keV

**Threshold 3:** 1000 - keV

**Bias Voltage A [V]:** 120 **Bias Voltage B [V]:** 150

**Frames** 1/1 jump to: <=>

Frames Auto Update

Frame statistic

Pixel count:	9,187
Max ToT:	571
Min ToT:	0
Average ToT:	63.28
Total ToT:	581317
Deadtime [ms]:	0
UDP Transfer:	100%

**Color Map** Hot

Min 0 Max 80

Under Warning Over Warning

Frame progress 40.0

Acq. progress 40.0

# SOFTWARE SUPPORT — BURDAMAN SW

The screenshot shows a software interface with several sections:

- Measurement** tab: Chip: chip was not found
- Internal DACs** table:

Parameter	Value	Voltage
VbiasPreamp	128	0.831 V
VcasPreamp	170	0.594 V
VbiasLevelShift	88	0.847 V
Ikrain	3	1.014 V
Vfbk	200	0.786 V
VTpulseCoarse	255	0.817 V
VTpulseFine	8	0.037 V
VBiasDiscTailNMOS	100	0.842 V
VBiasDiscPMOS	90	0.294 V
VBiasDiscTRAFF	32	0.253 V
VCascDisc	160	0.524 V
VTreshold	128	0.692 V
VbiasDAC	90	0.900 V
VControlVCO	134	0.066 V

- Analog Voltage Supply**: 1.122 V
- Digital Voltage Supply**: 1.171 V
- Temperature**: 30 °C
- DAC Scan**: VBiasPreamp selected
- Chip Settings**: Analog Mode: High-Gain hole
- Threshold Energy**: a0 coeff. 0, a1 coeff. 0

Settings of DACs

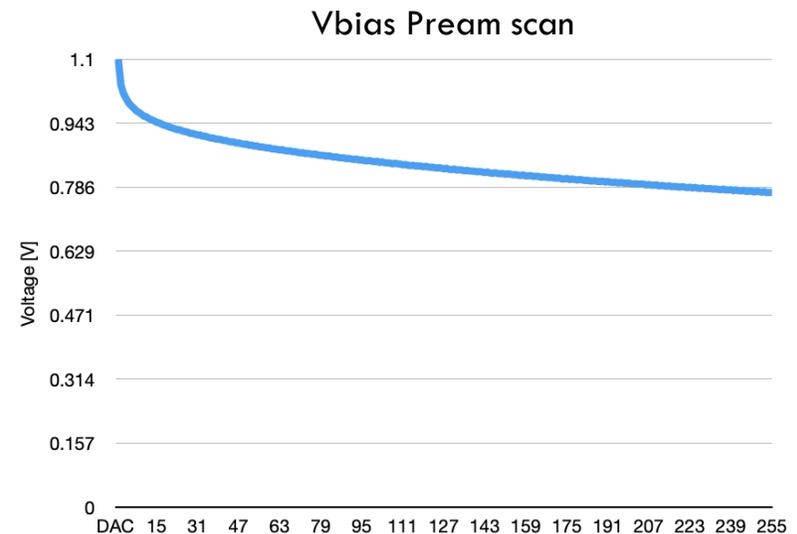
Scan of DAC's analog value

Scan of the current voltage supply

Chip temperature

DACs scanning

Analog mode setting



# SOFTWARE SUPPORT — BURDAMAN SW

The screenshot displays the Burdaman SW software interface. The main window is currently black, indicating that the chip was not found. The interface includes a top menu bar with options like 'Measurement', 'Chip Settings', and 'Readout HW'. On the right side, there are several control panels:

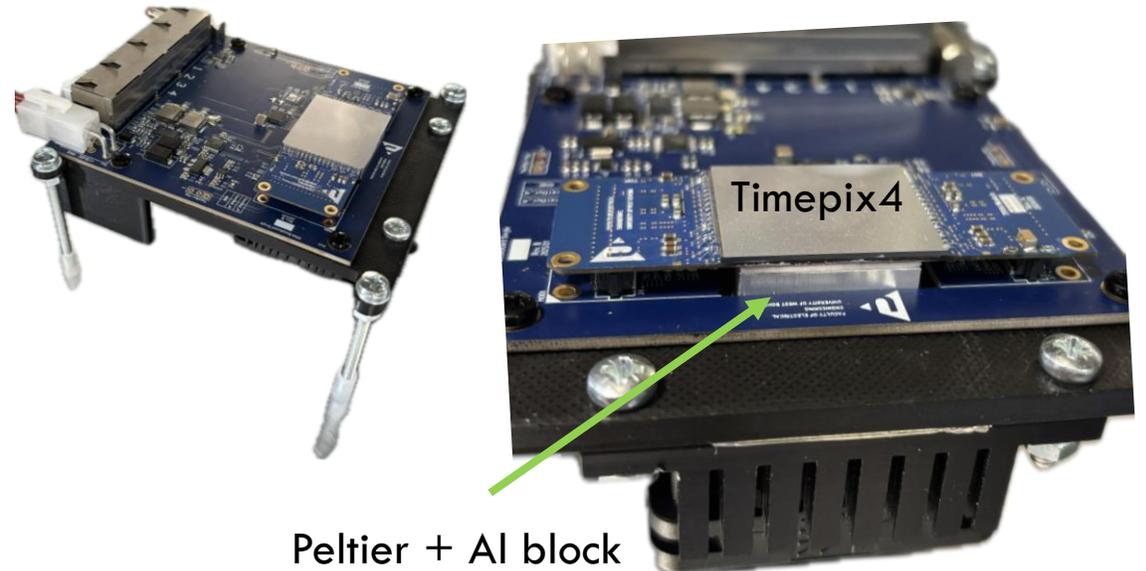
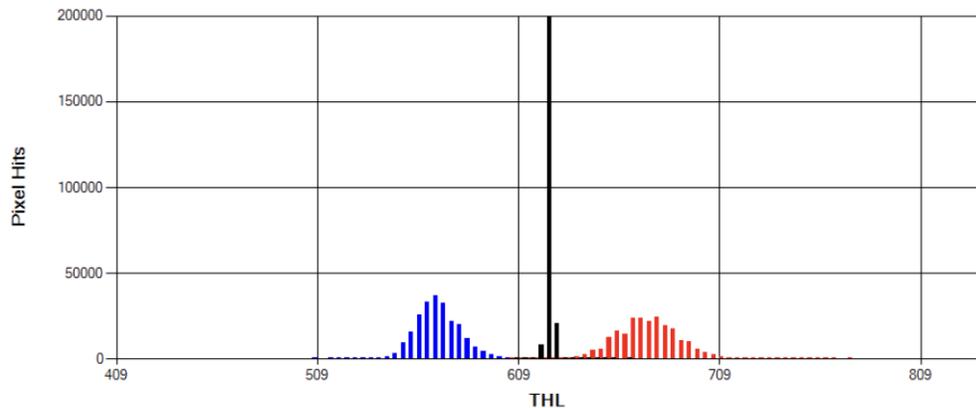
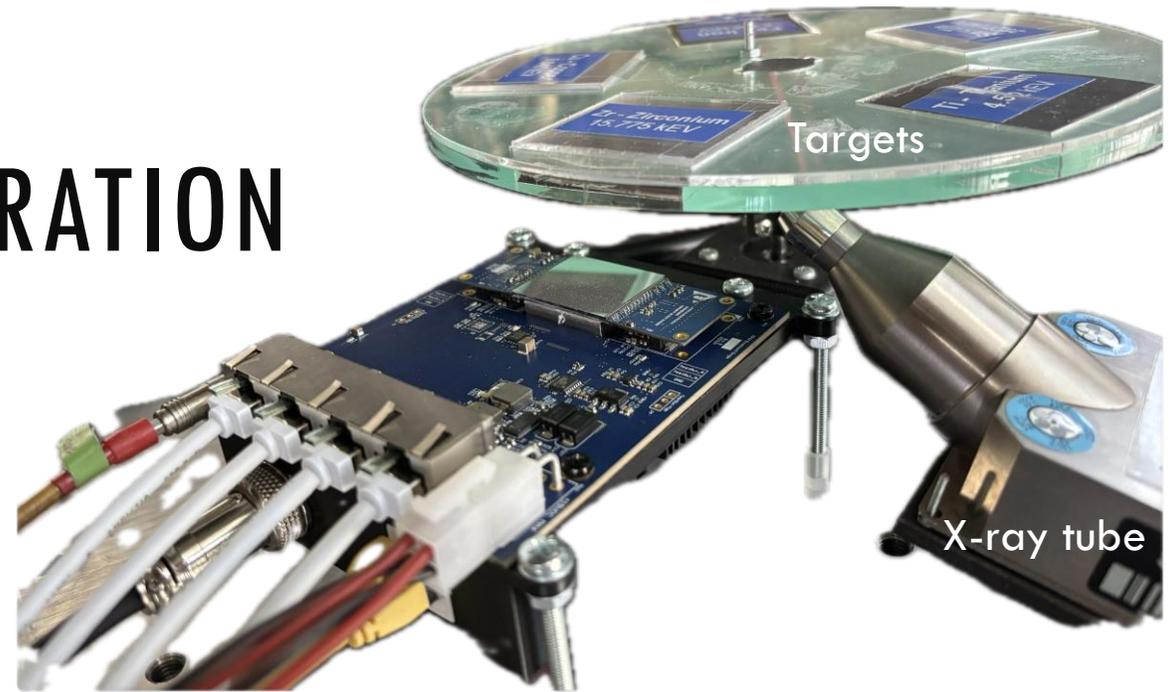
- Acquisition settings:** Includes fields for 'Time [s]' (10) and 'Frames' (1), a 'Start' button, and checkboxes for 'Repeat', 'Save to RAM', and 'Save Results to File'. A file path 'Z:\temp\tpx4\\_calibratio..' is also visible.
- Detector mode:** Set to 'ToA & ToT'.
- Thresholds:** Four thresholds are set to 1000 keV.
- Bias Voltage:** 'Bias Voltage A [V]' is 120 and 'Bias Voltage B [V]' is 150.
- Frames:** Shows '1/1' frames with navigation buttons.
- Frame statistic:** A table of statistics:

Pixel count:	0
Max ToT:	0
Min ToT:	0
Average ToT:	0.00
Total ToT:	0
Deadtime [ms]:	0
UDP Transfer:	100%
- Color Map:** Set to 'Hot', with 'Min' at 0 and 'Max' at 80. 'Under Warning' and 'Over Warning' buttons are present.

At the bottom of the interface, there are checkboxes for 'Energy' (checked), 'Time', 'Count', 'Mask Bits', and 'Pixel Th'. The status bar at the bottom right shows 'X: 469 Y: 255'.

# TIMEPIX4 ASSEMBLY CALIBRATION

- Timepix4 Si-300 $\mu$ m module on base-board
- Active cooling – Peltier module  $\sim 18^{\circ}\text{C}$
- Bias = 120 V
- Targets: V, Ca, Ti, Fe, Cu, Zr, Sn +  $^{241}\text{Am}$
- Edge noise equalization in PC24 mode + optimizing loops

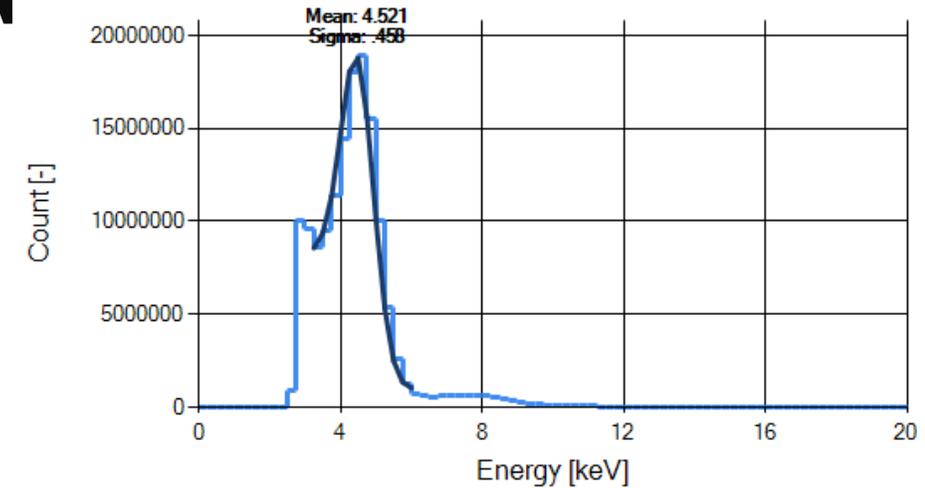


	Mean	Std. Dev.	Pixel Hits
Low Th	570.55	11.02	229372
High Th	672.27	15.49	229370
Final Th	621.23	1.48	229346

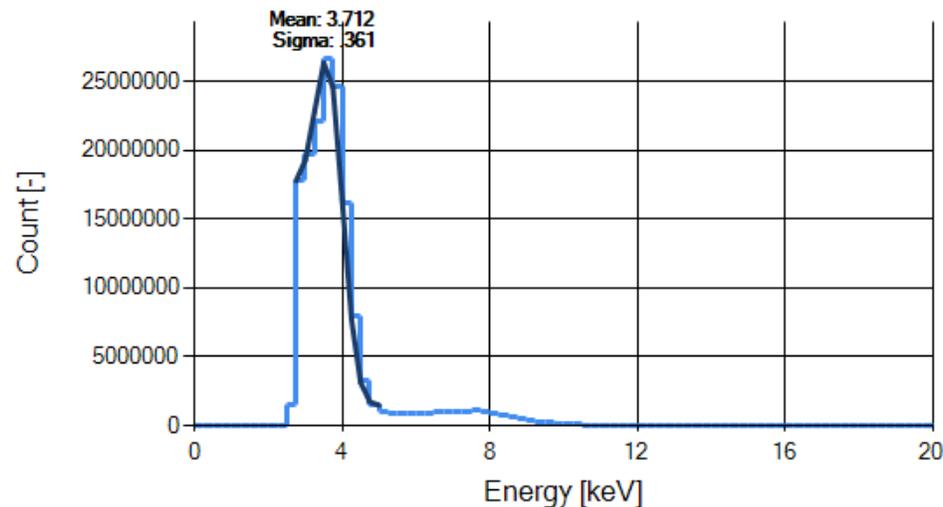
# TIMEPIX4 ASSEMBLY CALIBRATION

- Temperature  $\sim 18^{\circ}\text{C}$
- Bias = 120 V
- $\text{THL}_{\text{low}} \sim 2.8 \text{ keV}$
- 60 keV peak ( $^{241}\text{Am}$ ): Sigma 1.3 (all cluster), 1.1 (single-pix)

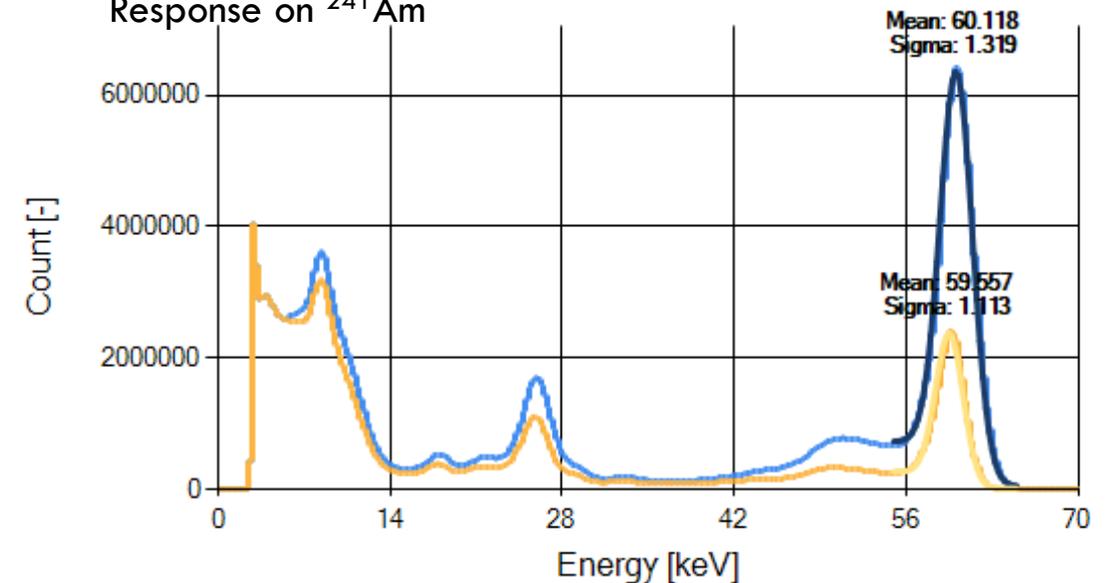
XRF Titanium



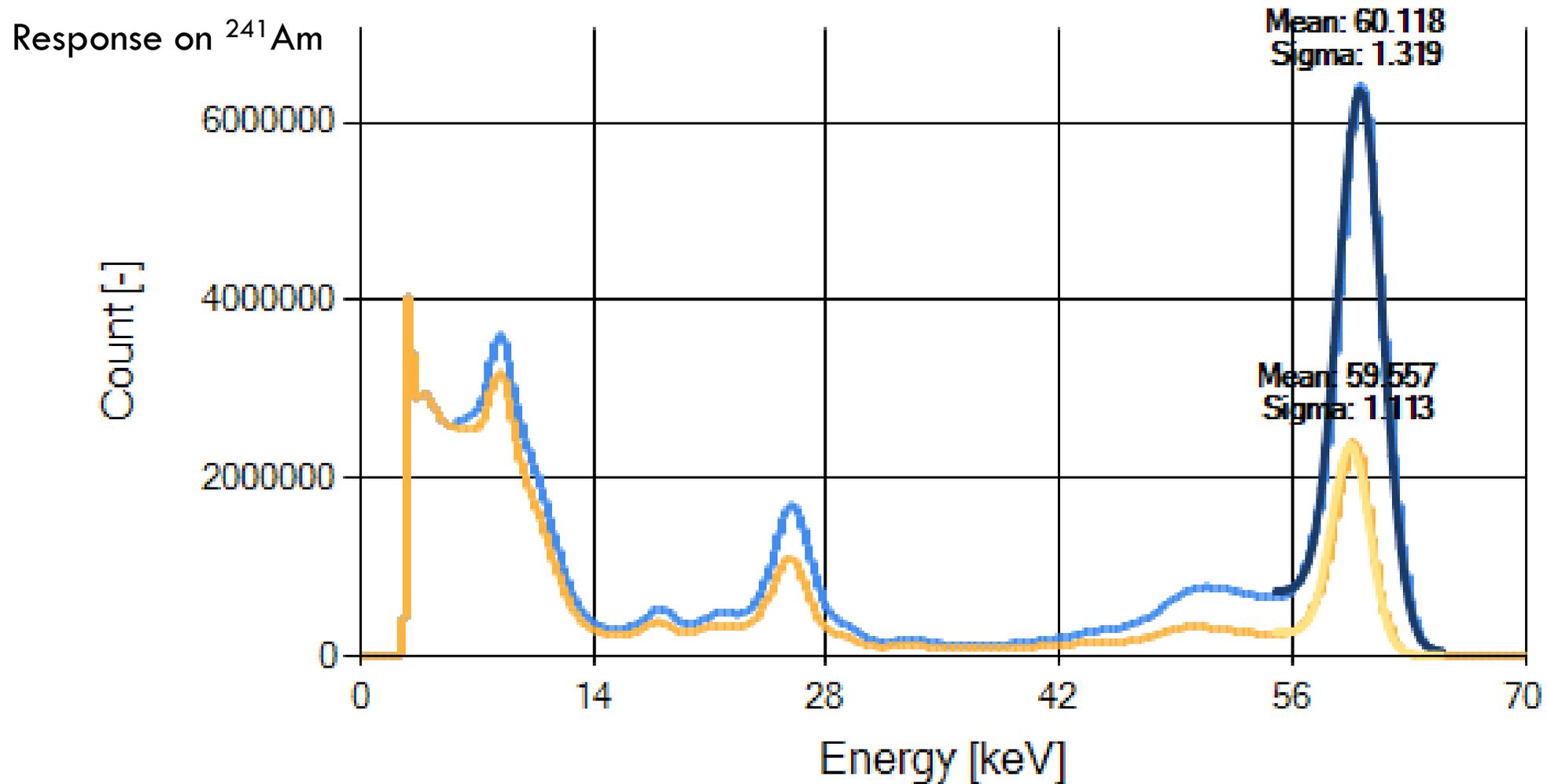
XRF Calcium



Response on  $^{241}\text{Am}$



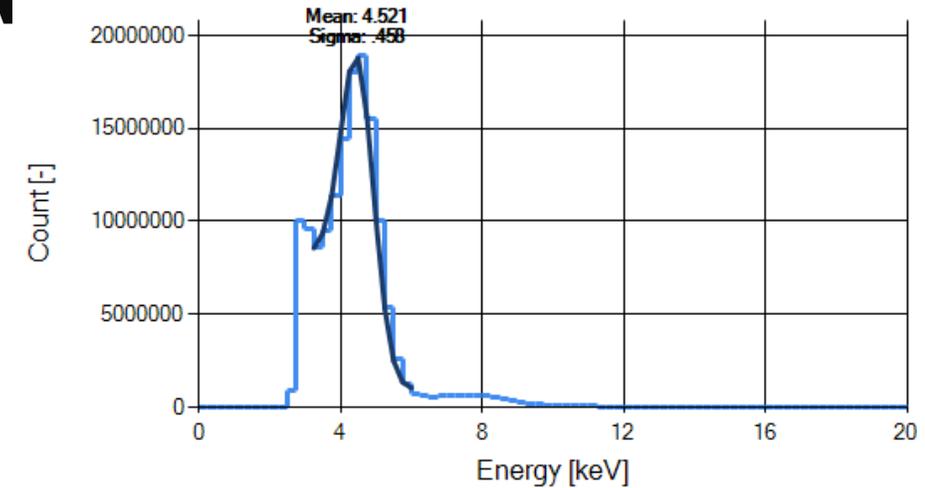
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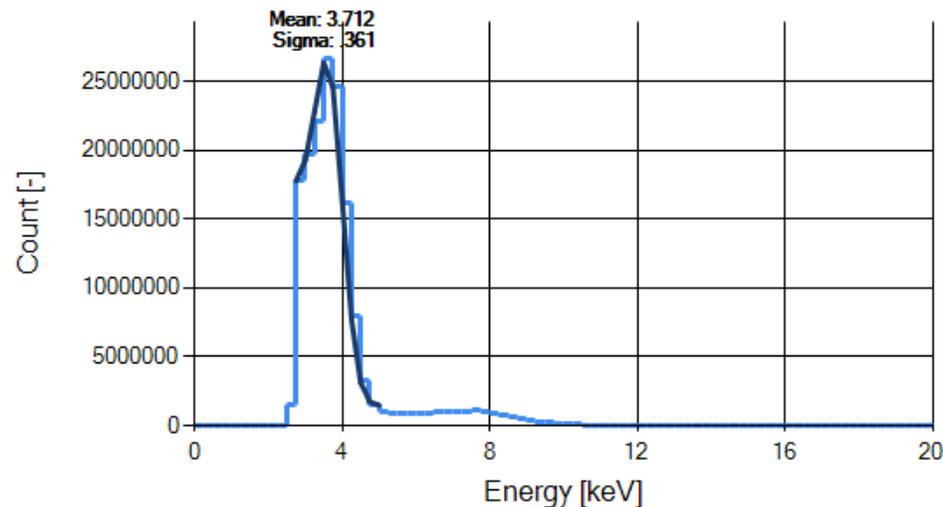
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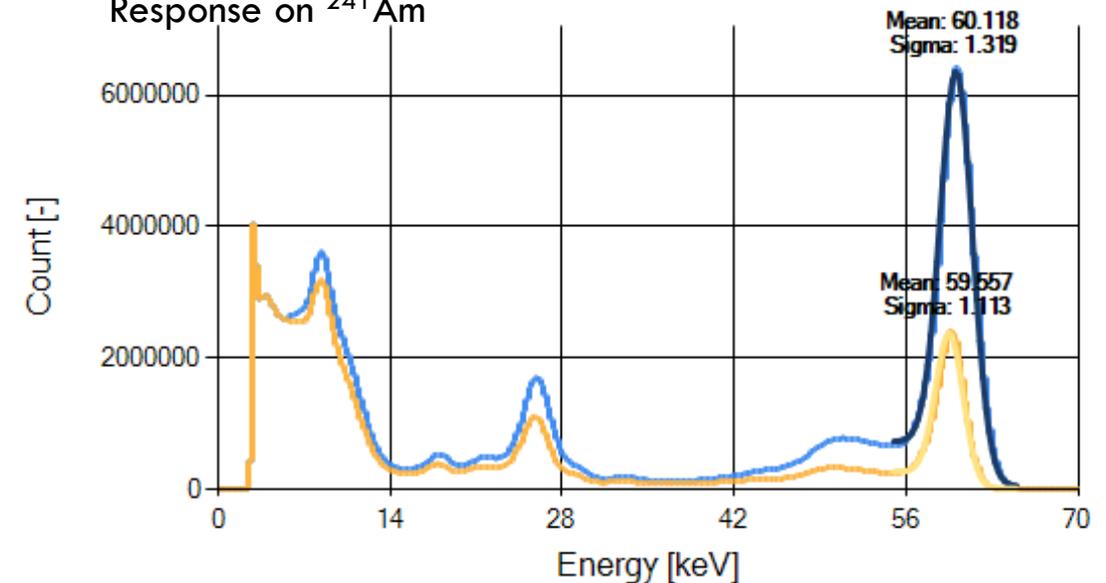
XRF Titanium



XRF Calcium

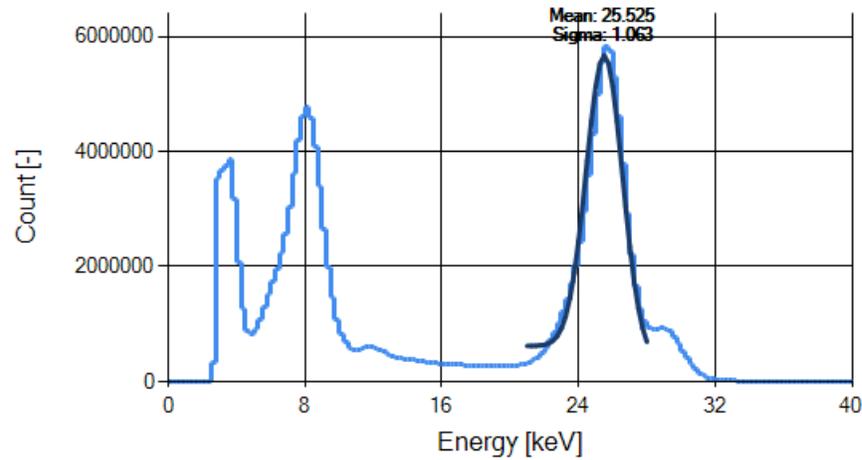


Response on  $^{241}\text{Am}$

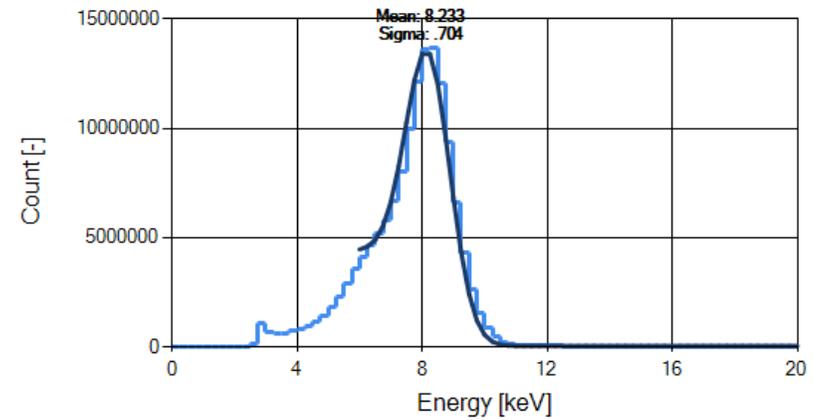


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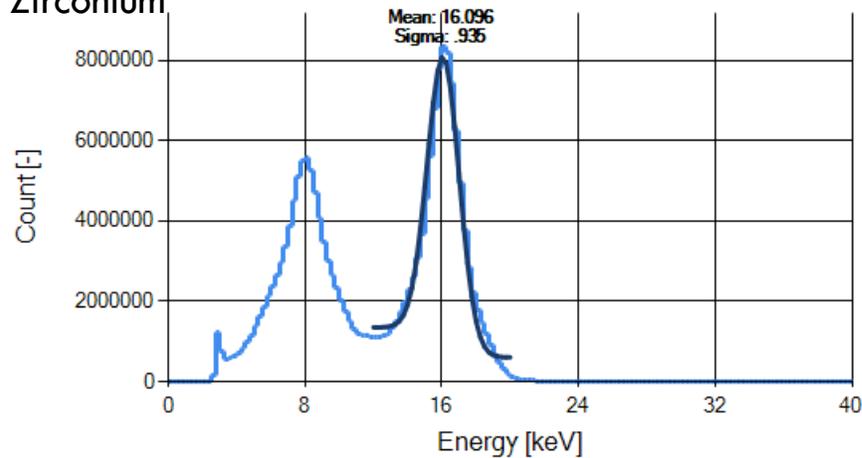
XRF Tin



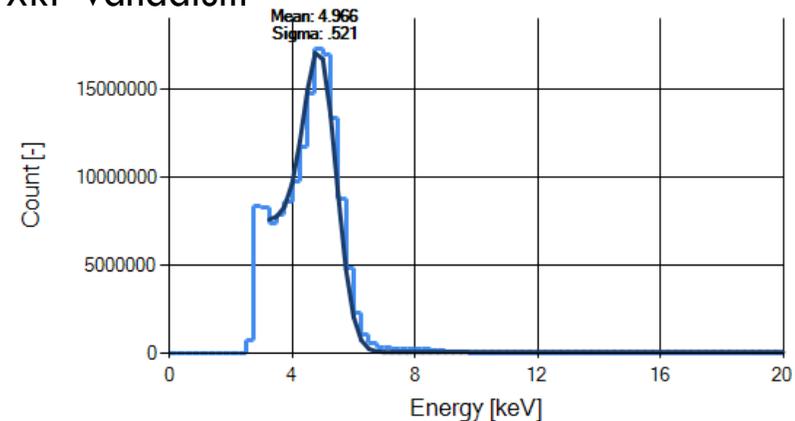
XRF Copper



XRF Zirconium

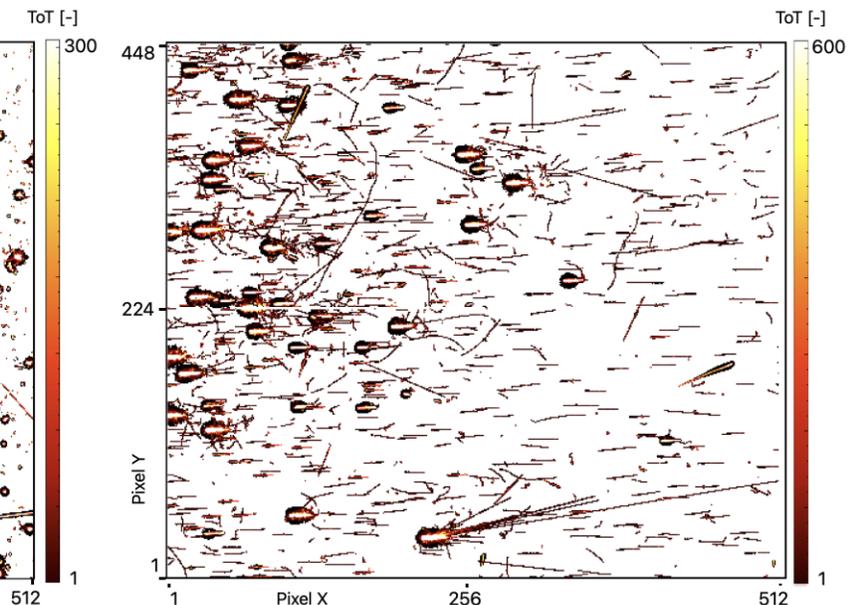
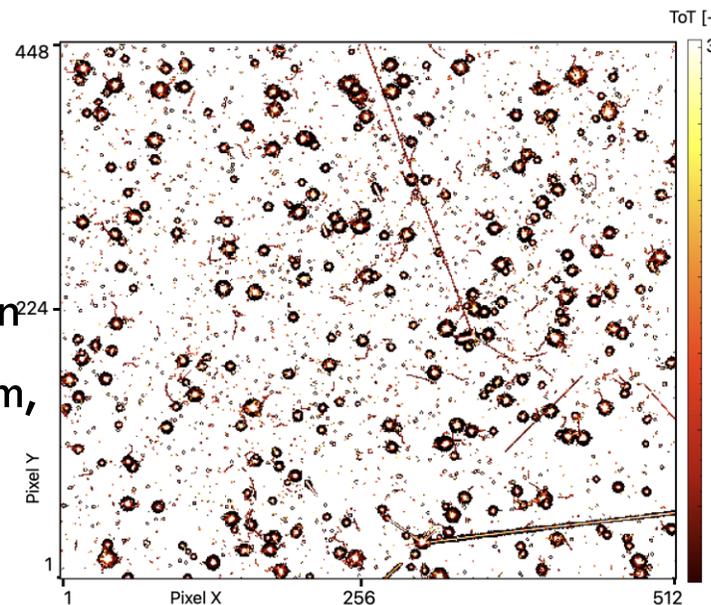
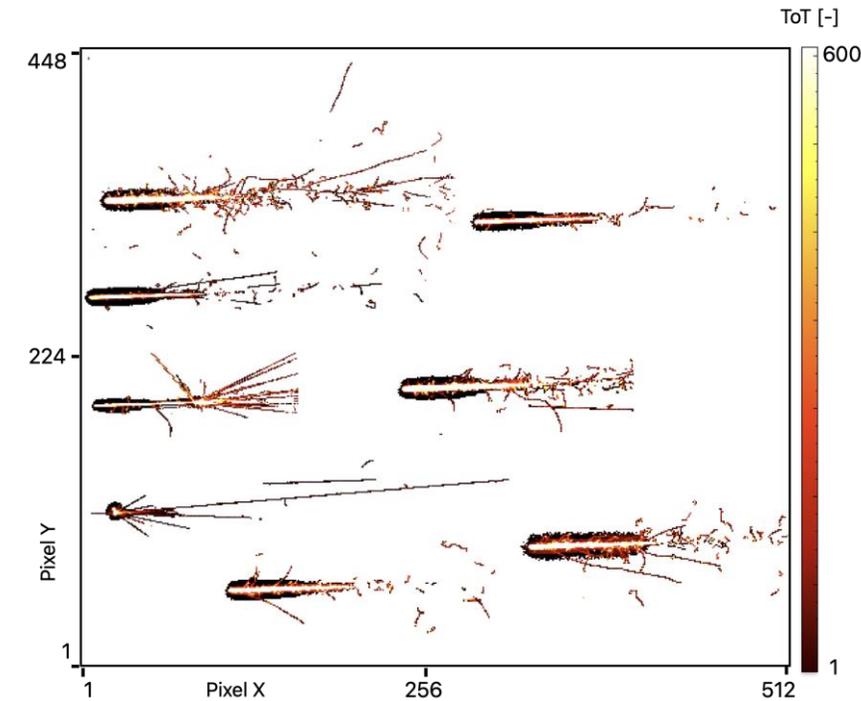


XRF Vanadium



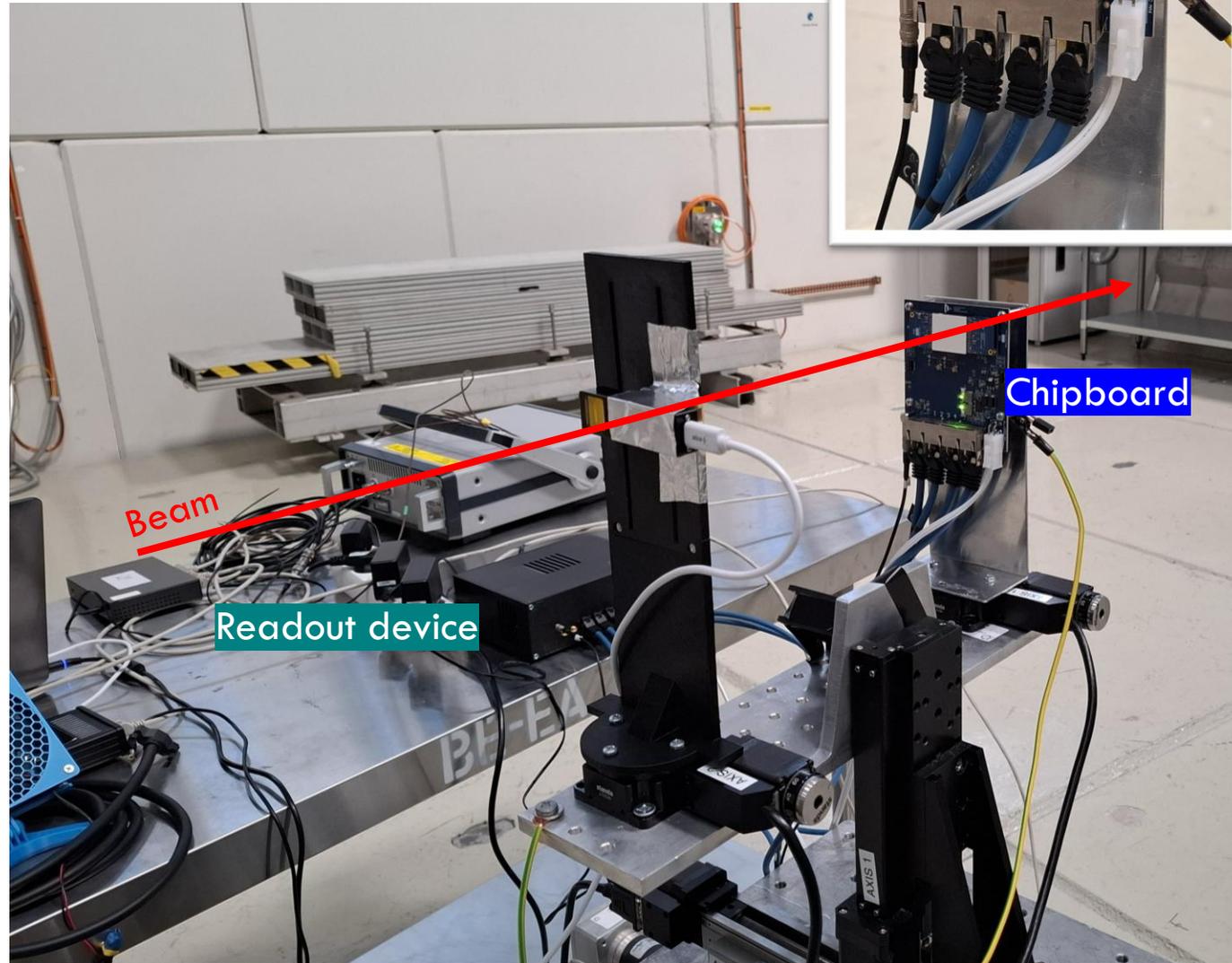
# TESTING – LEAD ION BEAM

- Very first testing on test beam
- Super Proton Synchrotron, CERN. November 2024.
- 350 GeV/c lead ion/fragmented
- Timepix4 Si-300 $\mu$ m glued on PCB (preliminary version of chipboard)
- Not ideal solution of power supplies
- 3 m cabling (4x cat 6a, power, bias)
- 1 Gb Ethernet used for communication
- Detector placed in centre of the beam, irradiated under several angles
- Several SEUs detected
- No volcano effect



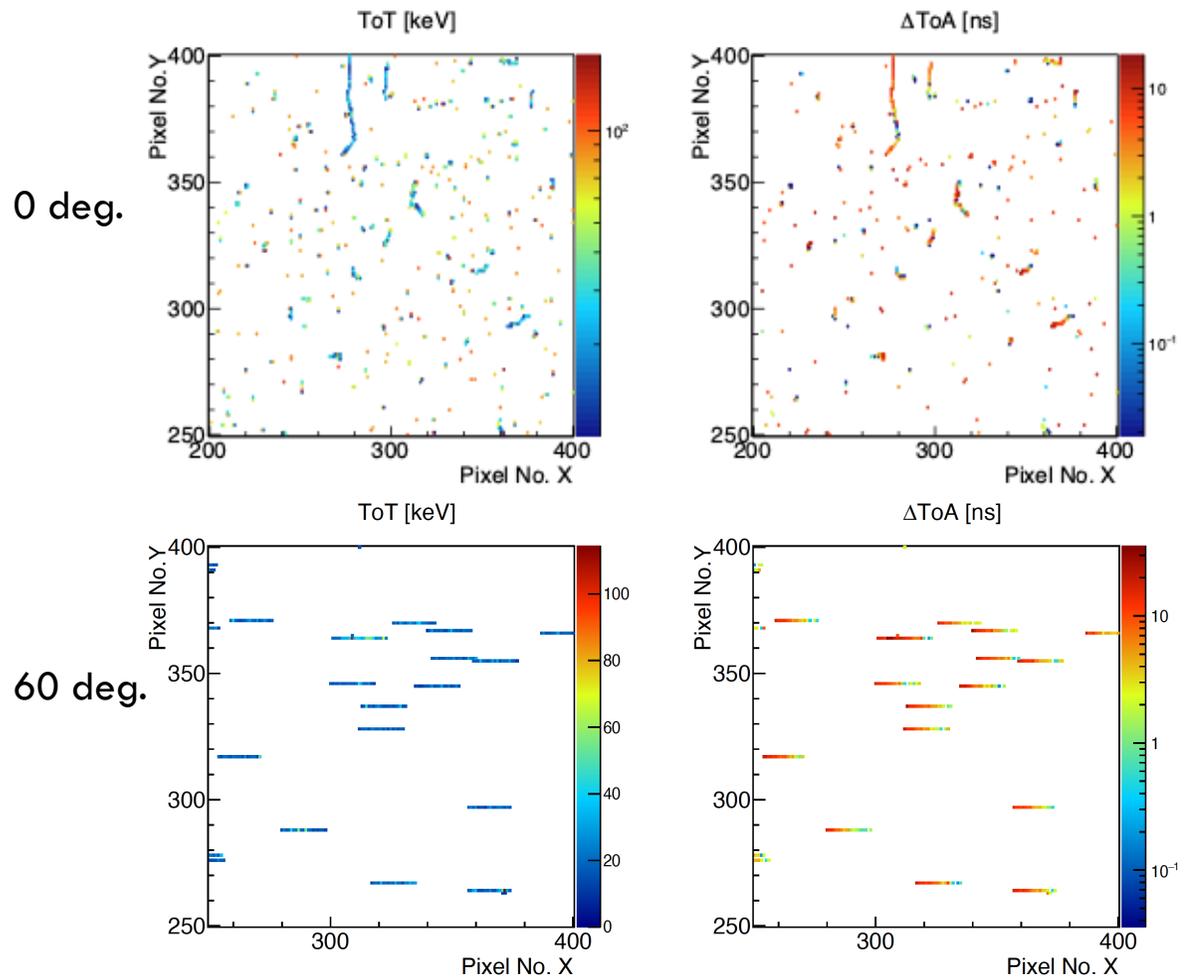
# TESTING — BEAM TEST - PIONS

- Proton synchrotron, CERN. April 2025.
- Muons, 10 GeV
- Timepix4 Si-300 $\mu$ m module on base-board
- Mounted on rotary stage
- 1 m cabling (4x cat 8.1, power, bias)
- 1 Gb Ethernet used for communication
- Detector placed in centre of the beam, irradiation under several angles

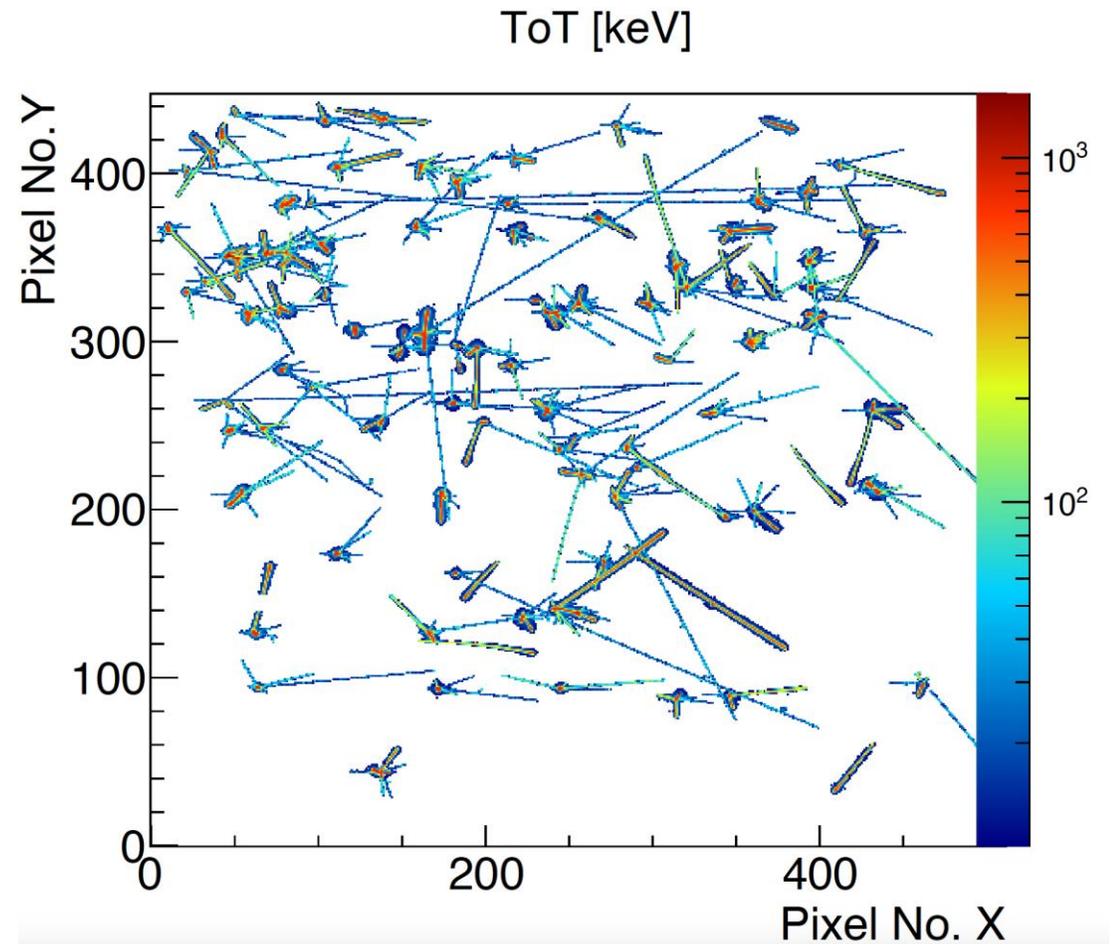


# TESTING — BEAM TEST — RESULTS

ToT and  $\Delta$ ToA hit maps

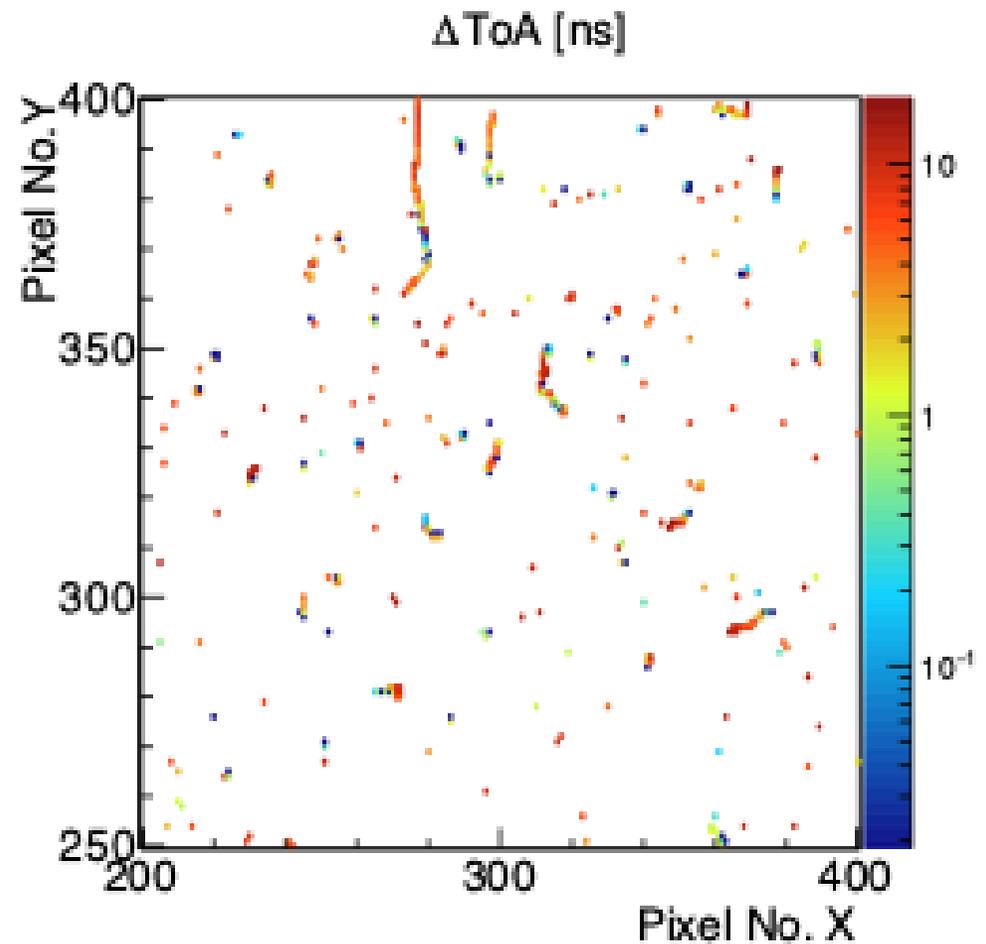
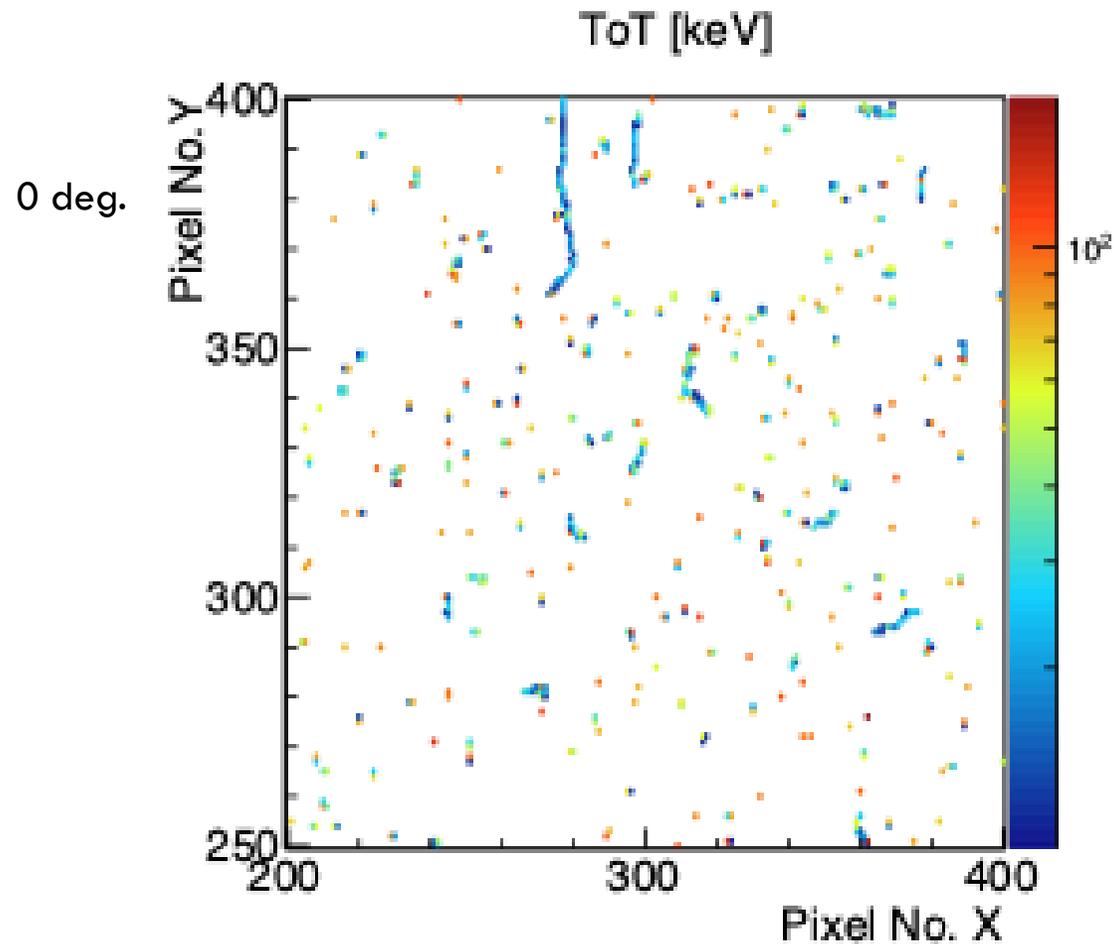


ToT hit map showing clusters with strong interaction in the sensor



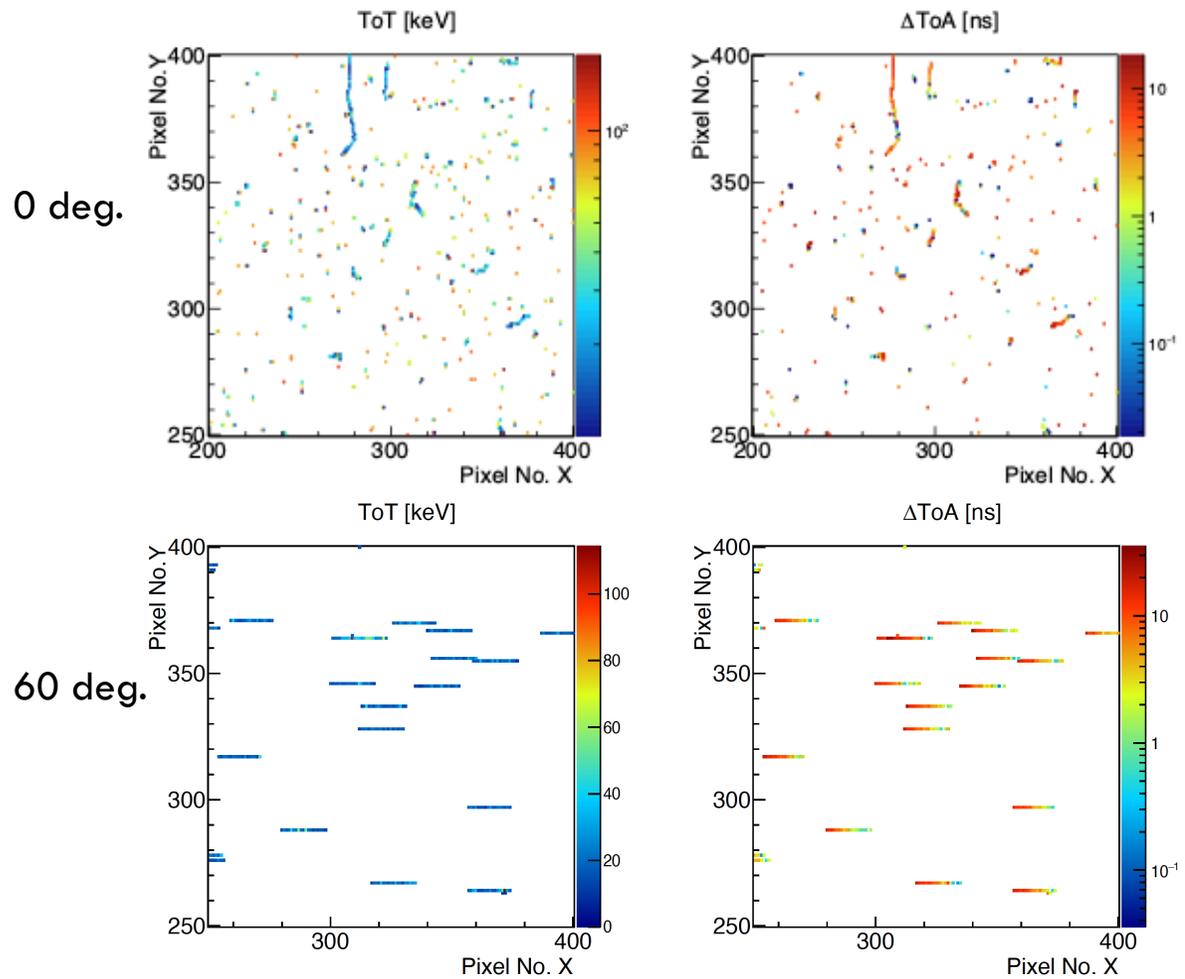
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ToT and  $\Delta$ ToA hit maps

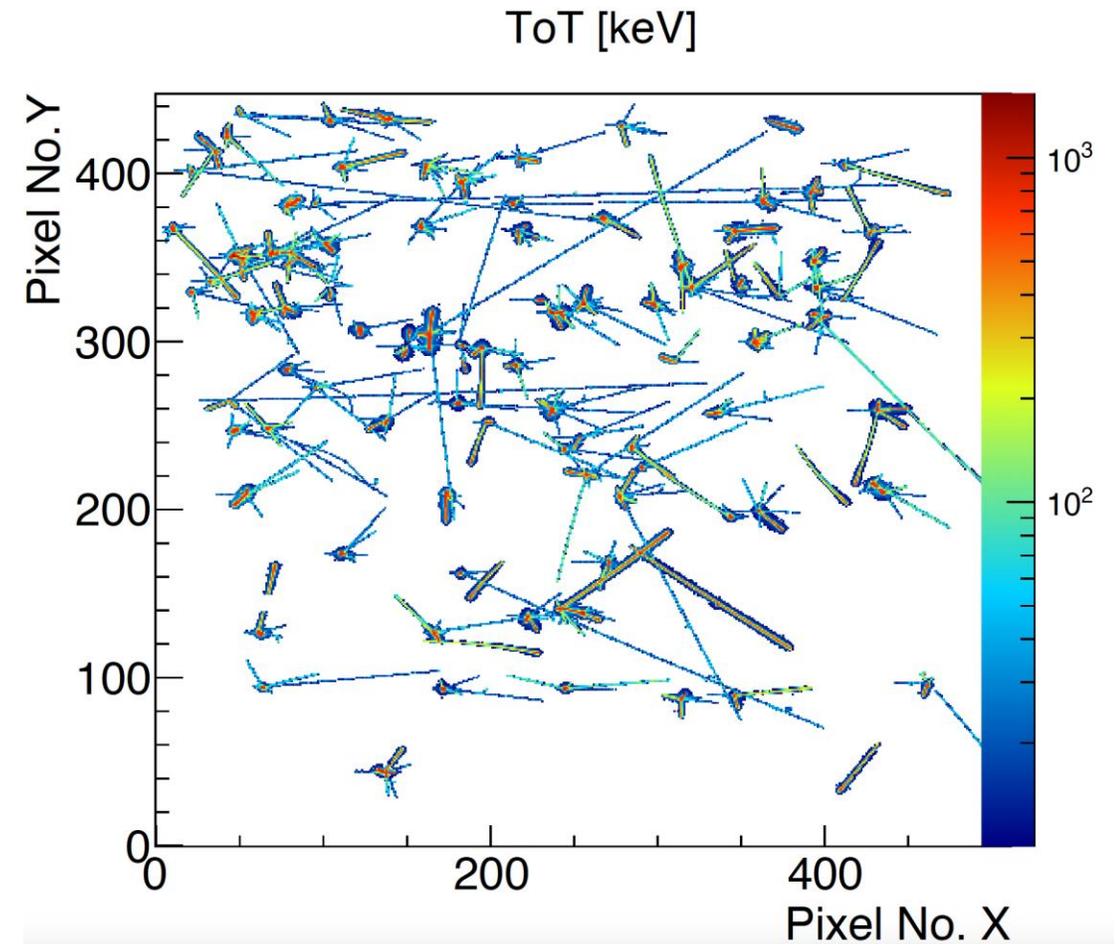


# TESTING — BEAM TEST — RESULTS

ToT and  $\Delta$ ToA hit maps

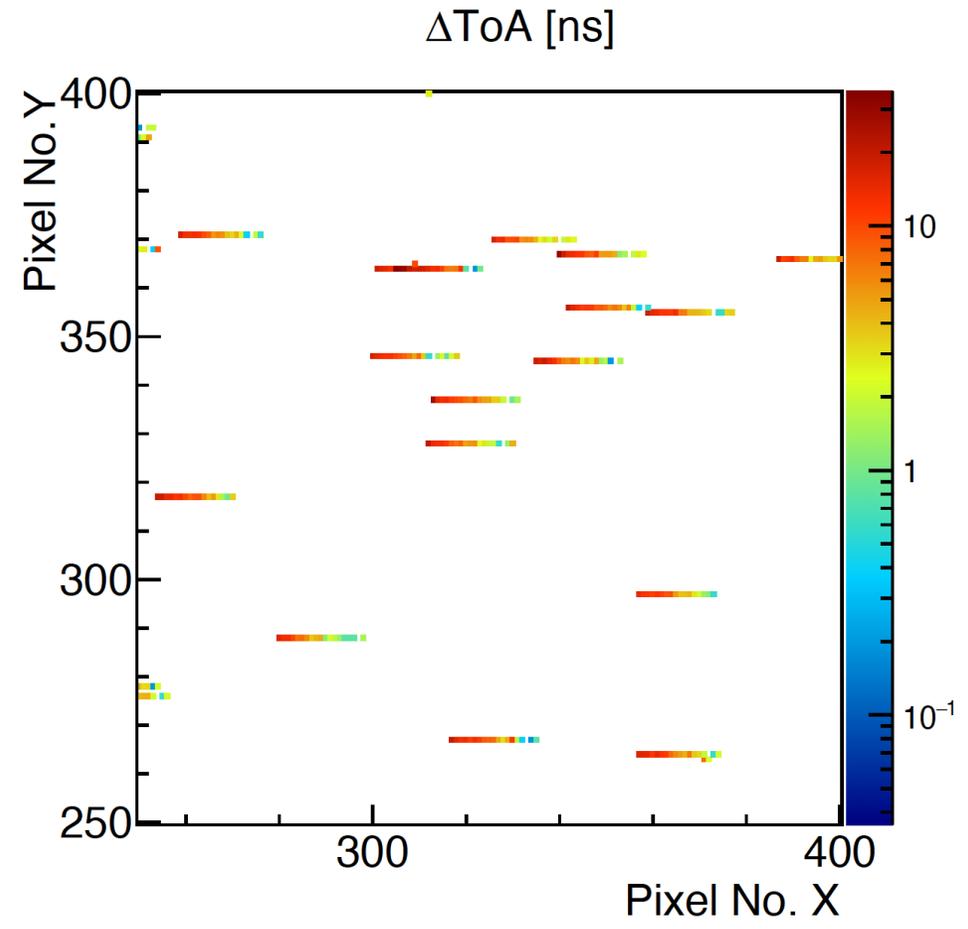
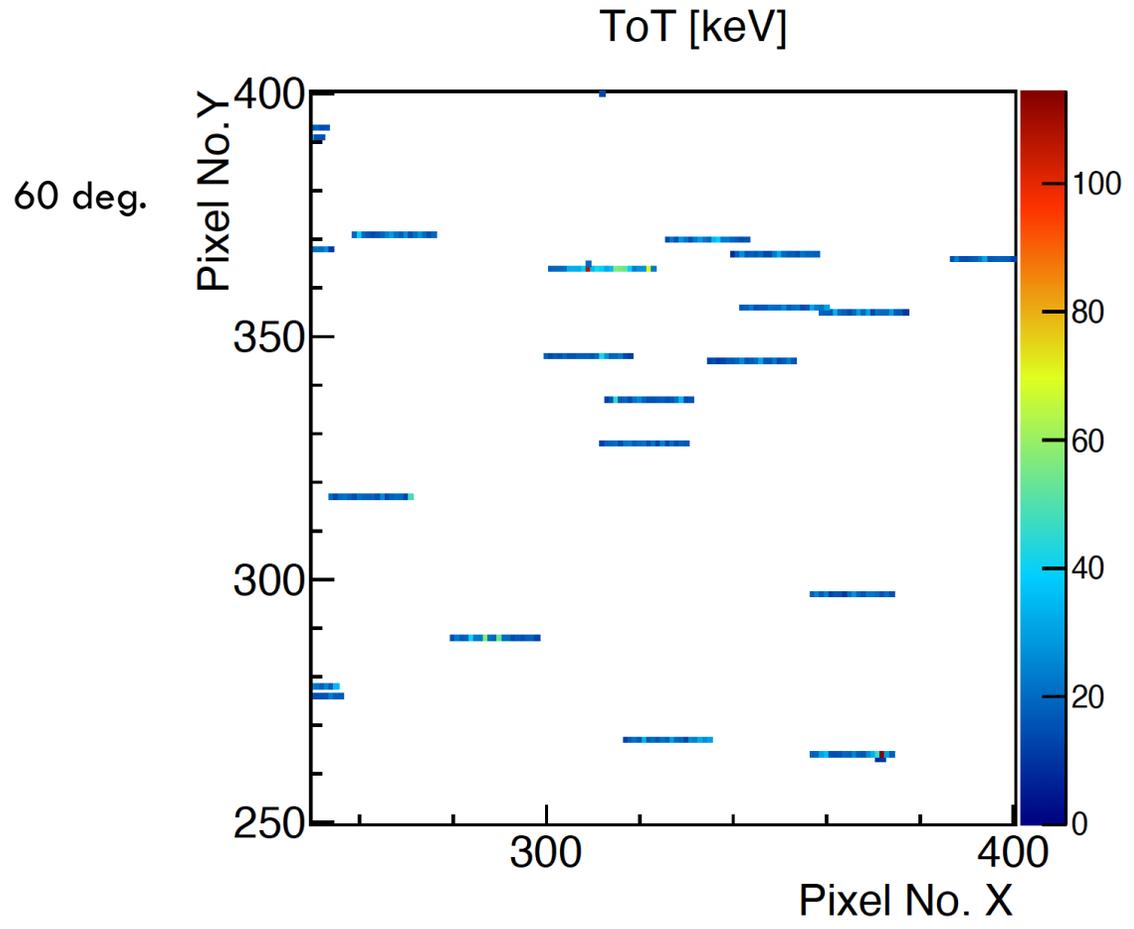


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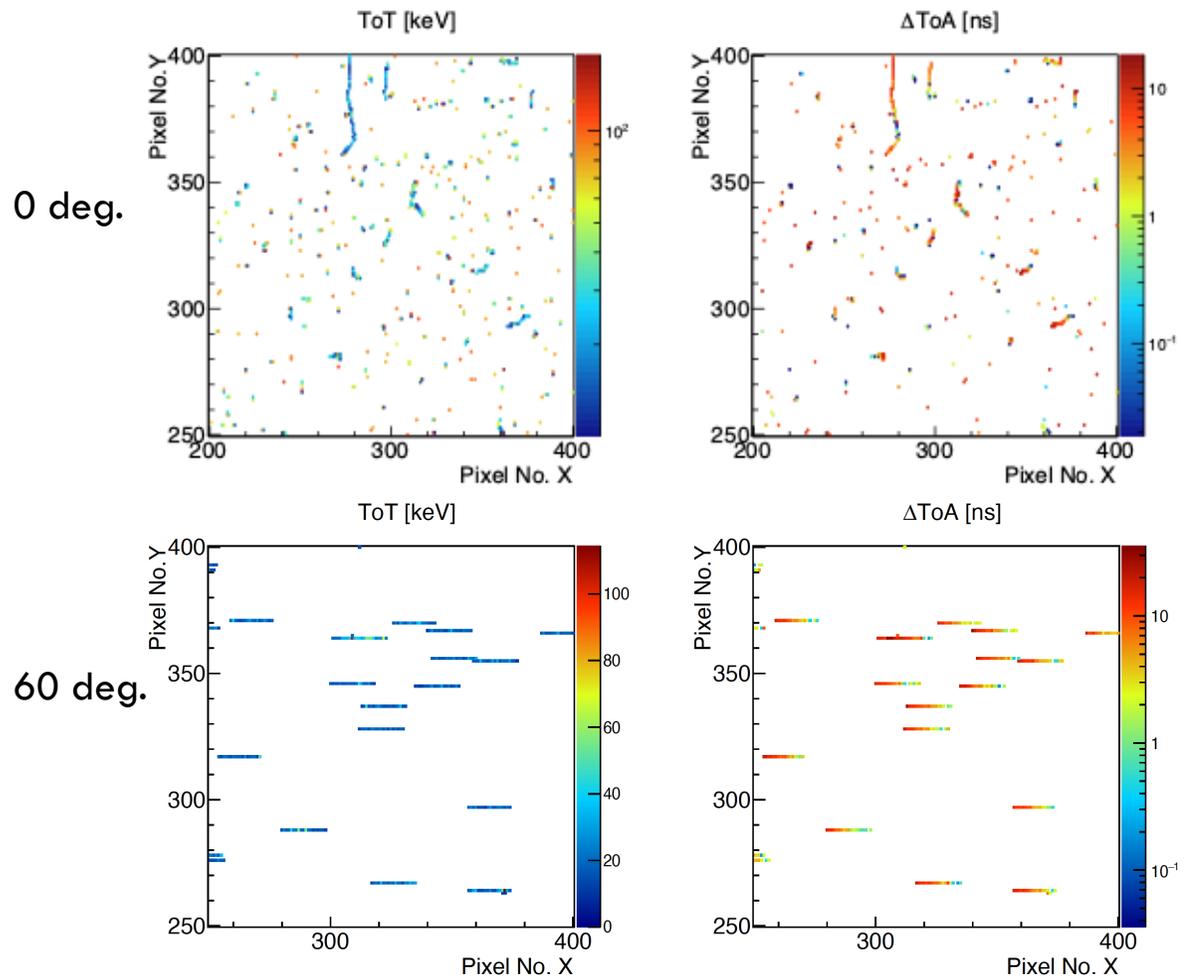
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ToT and  $\Delta$ ToA hit maps

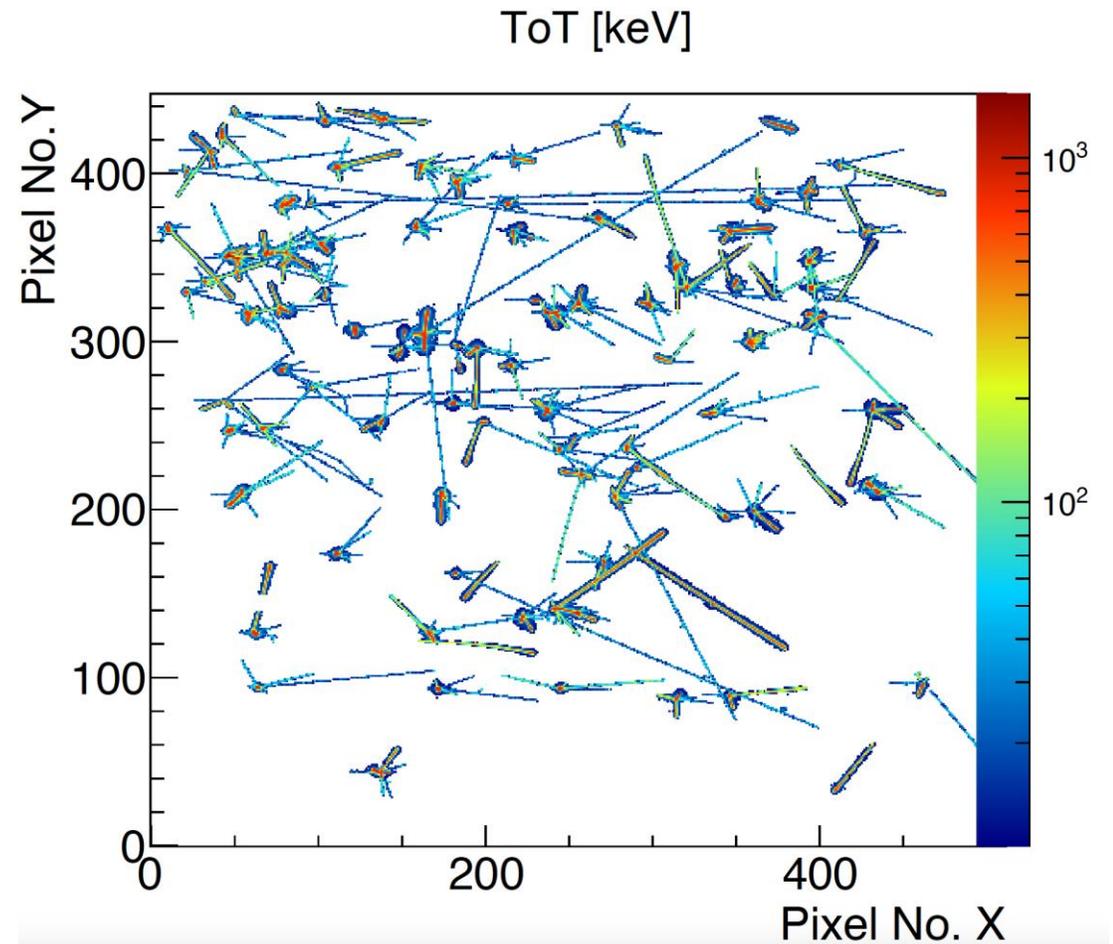


# TESTING — BEAM TEST — RESULTS

ToT and  $\Delta$ ToA hit maps

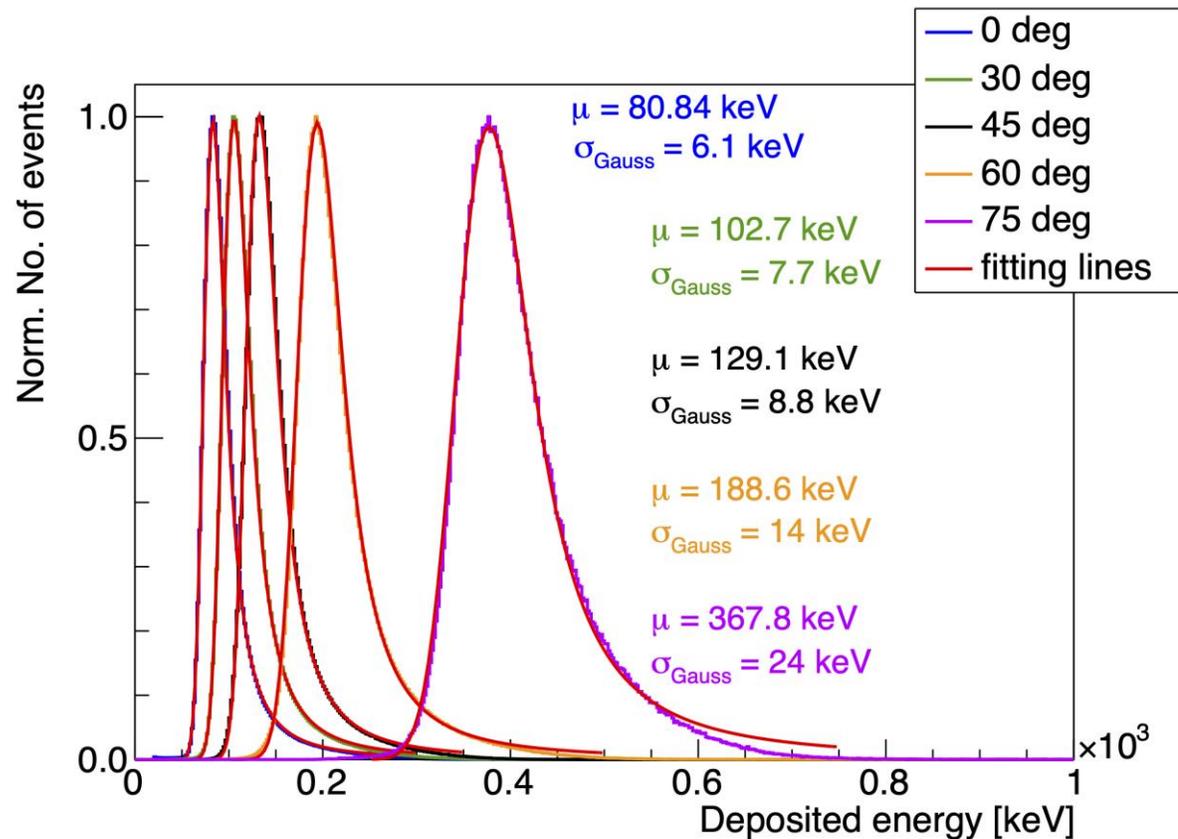


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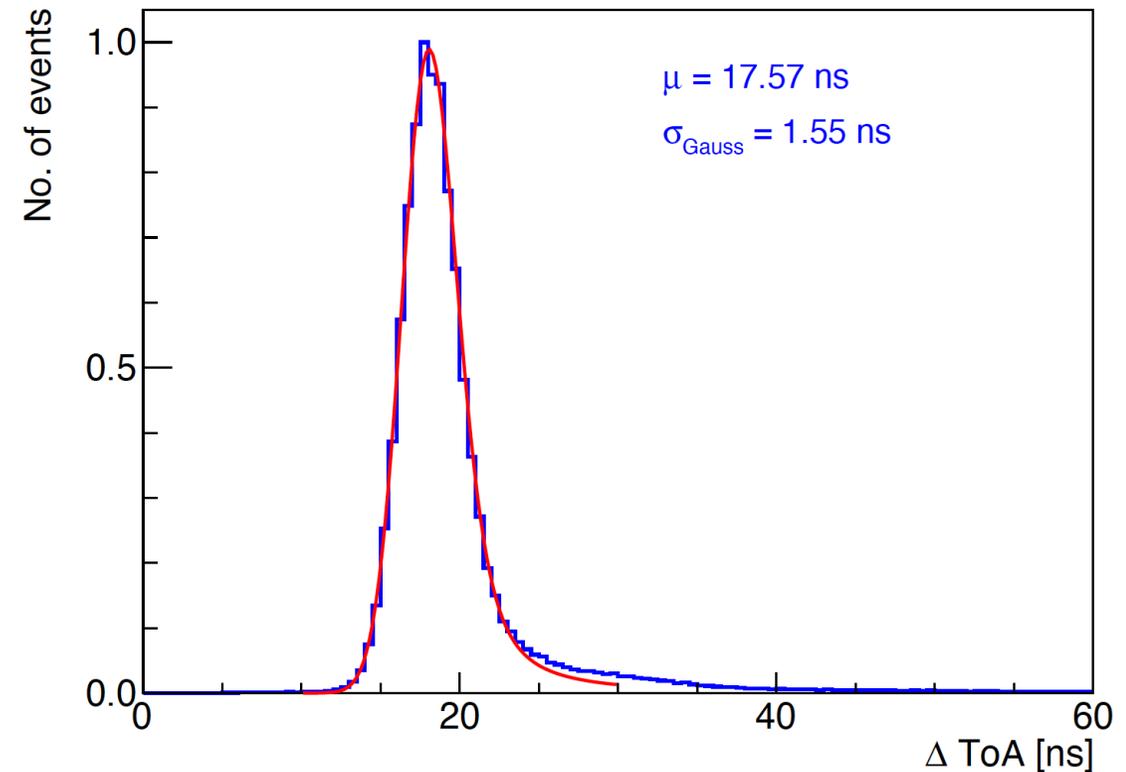


# TESTING — BEAM TEST — RESULTS

Deposited energies of clusters at different angles  
(with respect to the detector normal)



Cluster delta time (estimation of drift time)  
75deg, bias = 70V



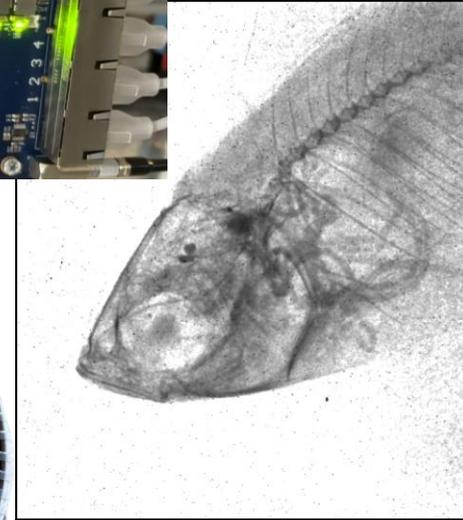
# CONCLUSION

- **What is now available?**

- Timepix4 modular chipboards (wire-bonding, TSV)
- Timepix4 readout device
- Control SW
- Data rate via Gigabit Ethernet  $\sim 11$  MHit/s

- **What's next?**

- Finish PCIe communication (350 MHit/s is goal)
- Multi-chip support (Timepix4 Quad should be goal)
- Track Lab support
- Adding “instrumentation” connector – support of specific devices: fans, peltier modules, stepper motor...
- Compact version (USB-stick size) – *P. Broulim's poster*
- Plug-in architecture for onboard data processing – *M. Farkas's poster*





**THANKS FOR YOUR ATTENTION...**

**PETR.BURIAN@CERN.CH**

# COMMANDS...

- **Pixel config command**

ID	Chip_ID	Coordinates	Config Value
[63..48]	[40..32]	[25..8]	[7..0]
		$= (y * 512) + x$	[7] = mask_bit
			[6] = test_pulse_en
			[5] = power_en
			[4..0] = adjust. bits

- **Internal DAC scan:**

63..48	47..8	7..0	63..48	47..32	31..0
0x000F (Cmd ID)	<i>unused</i>	Internal DAC ID	0x000F (Response Cmd ID)	<i>unused</i>	Analog Scan Value (float)

# TIMEPIX4 — CHIPBOARD — IDEAS

## Key ideas:

- Glory of VHDCI connector is over.
- What cabling do we need?
  - Have a chance to be far away from acquisition system
  - Reliability, cost, availability....
- FMC? Maybe good enough to the lab.
- Main power voltage level? Higher is better.
- How to reuse detector in other projects?
- How to debug boards after wire-bonding, or TSV mounting...?

# SOFTWARE SUPPORT — BURDAMAN SW

The screenshot displays the BurdaMan software interface. The main window shows a dark image with numerous small white specks, likely representing detected particles or defects. The interface includes several control panels and status indicators.

**Top Bar:** ---BurdaMan--- | Chip ID: chip was not found | IP address of readout: 192.168.1.40

**Left Panel:** Chip: chip was not found |  Multiview

**Right Panel (Measurement):**

- Acquisition settings:**
  - Time [s]: 40 | Frames: 1
  - Start** (green button)
  - Repeat |  Save to RAM
  - Z:\temp\tpx4\\_calibratio ...
  - Save Results to File
- Detector mode:** ToA & ToT
- PC24b Threshold: 0
- Threshold 0:** 605 - keV
- Threshold 1:** 1000 - keV
- Threshold 2:** 1000 - keV
- Threshold 3:** 1000 - keV
- Bias Voltage A [V]:** 120 | **Bias Voltage B [V]:** 150
- Frames:** 1/1 | jump to: <=>
- Frames Auto Update
- Frame statistic:**
  - Pixel count: 116,112
  - Max ToT: 2,047
  - Min ToT: 0
  - Average ToT: 108.12
  - Total ToT: 12554102
  - Deadtime [ms]: 0
  - UDP Transfer: 100%
- Color Map:** Hot
- Min: 0 | Max: 1
- Under Warning |  Over Warning
- Frame progress: 19.5
- Acq. progress: 19.5

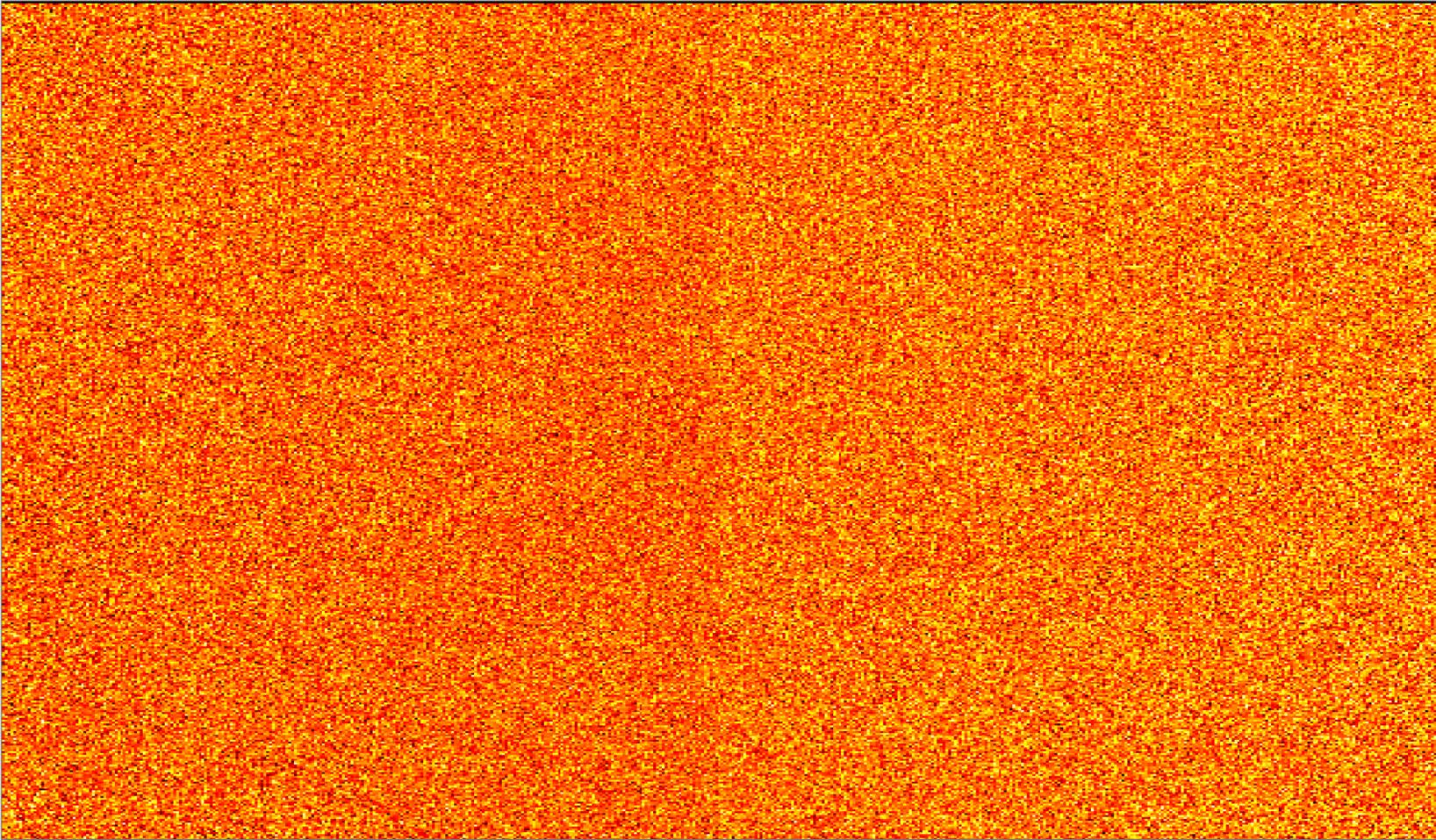
**Bottom Panel:**  Energy |  Time |  Count |  Mask Bits |  Pixel Th

**Bottom Right:** X: 498 Y: 54

# SOFTWARE SUPPORT — BURDAMAN SW

---BurdaMan--- Chip ID: chip was not found | IP address of readout: 192.168.1.40

Chip: chip was not found  Multiview



Energy  Time  Count  Mask Bits  Pixel Th

X: 330 Y: 6

Measurement Chip Settings Readout HW

Digital Test

Grid  Ratio

Acquisition settings:

Time [s] 40 Frames 1

**Start**

Repeat  Save to RAM

Z:\temp\tpx4\\_calibratio ...

Save Results to File

Detector mode:

ToA & ToT

PC24b Threshold: 0

Threshold 0: 605 - keV

Threshold 1: 1000 - keV

Threshold 2: 1000 - keV

Threshold 3: 1000 - keV

Bias Voltage A [V]: 120 Bias Voltage B [V]: 150

Frames 1/1 jump to:

Frames Auto Update

Frame statistic

Pixel count:	116.112
Max ToT:	2.047
Min ToT:	0
Average ToT:	108.12
Total ToT:	12554102
Deadtime [ms]:	0
UDP Transfer:	100%

Color Map

Hot

Min 0 Max 32

Under Warning Over Warning

Frame progress 19.5

Acq. progress 19.5

# CALIBRATION TOOLING

Katherine - Detector Tools for Timepix3 - petr.burian@cern.ch

Threshold Scan | **ToT Pixel Calibration** | Time-Walk Correction | Settings

**Calibration Points:**  
8) Americium 241 - Am: 59.5409 keV

Analysis + ToT Spectrum | Mean Calculation | THL Low: 2.8 | Calib Calculation | Calib Calculation with Test Pulses | Calculate Spectra

**Action:** IDLE - Calibration coefficients calculated!

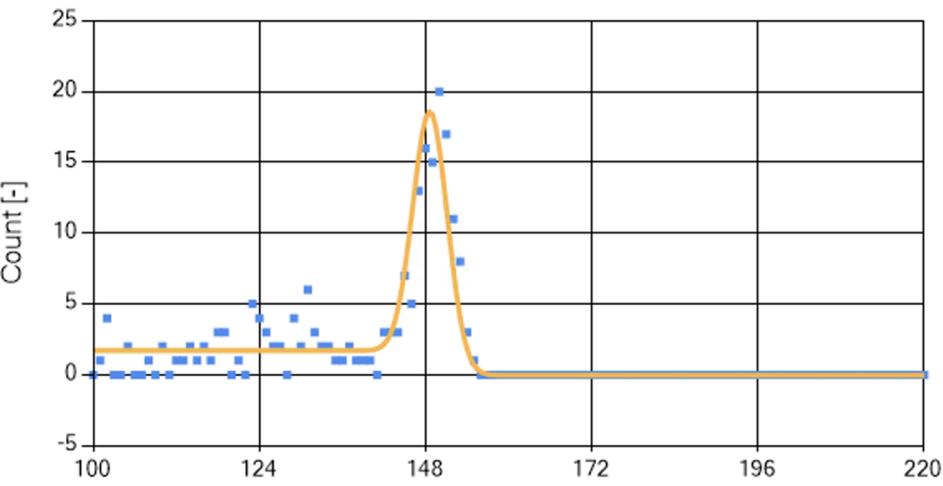
Data file: Z:\temp\tpx4\\_cilibration\_burda\peltier

Photons energy: Americium 241 - Am: 59.5409 keV

Processed pixels: 409,947,035  
Single-pixel events: 168,927,760  
Active pixels: 229,340  
Mean events/pixel: 736.58  
Min. events: 15  
Max. events: 2,011

Save

### ToT Spectrum of single-pixel clusters



Count [-]

ToT [-]

Total spectrum

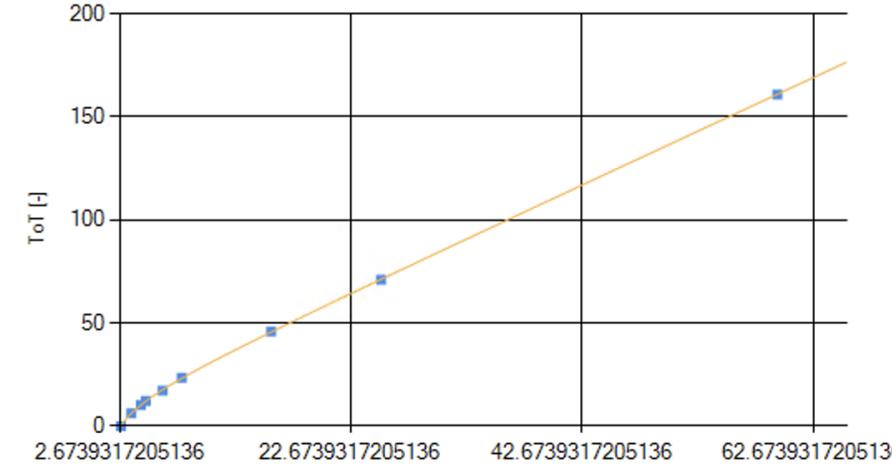
X: 200 | Y: 9 | Jump to random pixel | ToT Min: 100 | ToT Max: 220

### Calibration Curves

Energy Spectra | Coefficients Modification

Pixel coordinates: X: 8 | Y: 17 | Load cal. files

a: 2.594 | c: 39.181  
b: 3.198 | t: 1.543



ToT [-]

Energy [keV]

2.6739317205136 | 22.6739317205136 | 42.6739317205136 | 62.6739317205136