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A high throughput, radiation-hardened encoder/ decoder ASIC for the tracking system in HIAF

The High-Intensity Heavy-Ion Accelerator Facility (HIAF) is a next-generation heavy-ion accelerator currently under construction in China. A compact, large-acceptance spectrometer equipped with silicon pixel detectors will be constructed at HIAF to detect final-state particles at high event rates. The pixel-based tracking system, a key component of the spectrometer, is designed to precisely determine the spatial coordinates of collision points and secondary vertices from particle decays within the beam pipe. It must accurately track charged particles generated at collision rates of up to 100 MHz, while handling a data throughput exceeding 350 Gbps in a high-radiation environment. Serializer/Deserializer (SerDes) technology is widely used in such high-speed data links due to its ability to mitigate multi-channel skew. However, as transmission rates increase, DC imbalance and Single-Event Upsets (SEUs) can significantly elevate the bit error rate (BER). Encoding and decoding techniques provide a cost-effective solution to mitigate these errors. This study presents a radiation-hardened encoder/decoder ASIC, implemented in a 55 nm CMOS process, achieving a throughput of up to 20 Gbps. The chip employs an 84b/88b encoding scheme instead of the conventional 8b/10b encoding, enhancing efficiency while maintaining DC balance. Additionally, forward error correction (FEC) based on Reed-Solomon (RS) coding is integrated to detect and correct errors by appending redundancy bits, significantly reducing the BER. An optimized pipeline structure further enhances the throughput, meeting the stringent demands of large-scale data readout. To mitigate SEU-induced errors, triple modular redundancy (TMR) is implemented at critical nodes. Post-layout simulations demonstrate that, under a 1.2V supply, the encoder and decoder consume as little as 0.813 pJ/bit and 1.899 pJ/bit, respectively. The chip achieves a maximum error correction capability of 13.3% with 70% encoding efficiency and a 20 Gbps data rate, ensuring that the readout SerDes of the tracking system operates with high speed and low BER. Further test results will be presented in the poster.

Workshop topics

Front-end electronics and readout

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