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PIXCORE, a RISC-V microprocessor with an HPD management instruction set

Hybrid Pixel Detectors (HPD) are commonly used for X-ray imaging in both industry and medicine [1-2]. To this day, many approaches have been developed for managing such devices, such as the use of personal computers or FPGAs. Currently, one of the most interesting ones is the integration of the readout electronics for an HPD with the RISC-V microprocessor on the same silicon substrates.

In this article, we present PIXCORE, which is the application-specific integrated circuit block built of a RISC-V microprocessor with an HPD-managing extension, dedicated pixel matrix controller, memories, and some commonly used peripherals such as UART and GPIO. The designed device is the successor to HPSD [3] and is developed for manufacturing in a 16 nm CMOS process with an area of 410 x 210 μm.

Integration of a pixel matrix (PM) with a RISC-V microprocessor can significantly increase detector performance and improve its functionality. It allows the device to work without external assistive devices and execute many algorithms, such as discriminators offset calibration on the chip [4]. The predecessor of the presented solution (HPSD) implemented CPU-PM communication through the dedicated peripheral named pixel matrix controller (PMC) connected to the microprocessor data bus. It enabled fast inter-device communication but required an additional programmable unit named pixel matrix controller coprocessor (PMCC) executing programs written in a custom machine code. This solution required the implementation of synchronization mechanisms between the CPU and PMCC based on the PMCC status monitoring, which affected the overall performance of the device.

PIXCORE eliminates these restrictions through the implementation of the dedicated coprocessor tightly coupled to the RISC-V microprocessor. The CPU-coprocessor interaction is performed through the set of dedicated instructions allowing to manage the PM, such as pixels config setting or acquisition channels enabling. Additionally, usage of the more advanced semiconductor process enables the potential modification of the PM architecture and the replacement of long shift registers connecting neighboring pixels with independently addressed ones.

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[3] P. Skrzypiec and R. Szczygieł, Readout chip with RISC-V microprocessor for hybrid pixel detectors, Journal of Instrumentation, vol. 18, no. 1, C01030, Jan. 2023.

[4] P. Skrzypiec and R. Szczygieł, Development of On-Chip Calibration for Hybrid Pixel Detectors, 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), April 2021.

Workshop topics

Detector systems

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