

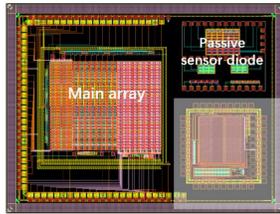
Test of COFFEE2, the first 55nm High Voltage CMOS sensor prototype

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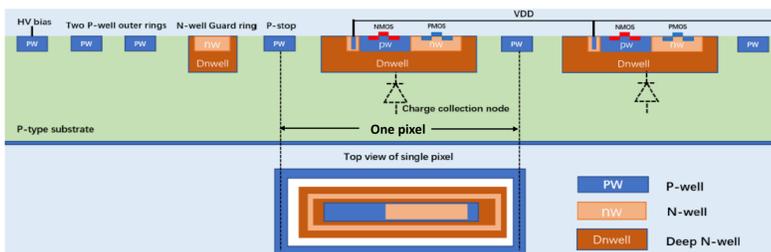
Introduction

To meet the increasingly demanding requirements of future tracking detectors for the LHCb Upgrade II and CEPC, advanced detector technologies with enhanced hit density processing capabilities and superior radiation tolerance are essential. To study the sensor performance and electronic response in the next generation process of HV-CMOS, the sensor chip called COFFEE2, which is the first prototype for process and circuit module in a 55 nm High-voltage technology is designed and tested. The "passive sensor diode" is designed to verify the characteristics of sensors with different gap and p-stop isolation structure. The "main array" features 20 * 32 pixels with 3 variations of pixel design. Preliminary test results are provided in the following session.



Process Features

- Dnwell-Sub junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- P-type substrate resistivity: 10 Ω·cm
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 50V with frontside HV bias
- More design details: Z. Chen et al., *Feasibility study of CMOS sensors in 55 nm process for tracking*, Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169905.



COFFEE2 Test System

PC + FPGA Board + Caribou Board + Dedicated Chip Carrier Board

Caribou system architecture

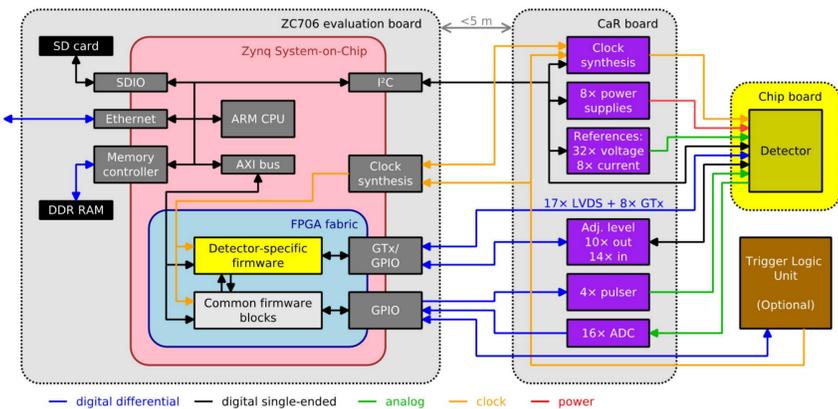


Fig2. Caribou test system architecture

Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulses	4 units
Full-Duplex High-Speed GTX Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



Resources for various target applications

Fig3. Control and Readout board

H. Liu et al., *Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade*, Journal of Instrumentation 12 (2017) P01008.

Main Results

Passive sensor diode results

- IV test: breakdown at **-70 V** (Fig4.a)
- CV test: single pixel ~50 fF at -70 V due to depletion (Fig4.b)
- Leakage current increased from 0.01 nA to ~1 nA after 10^{14} n_{eq}/cm² radiation Laser and α response observed (Fig4.d,e)

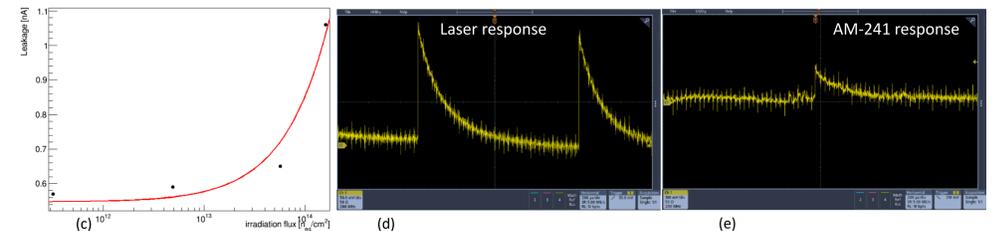
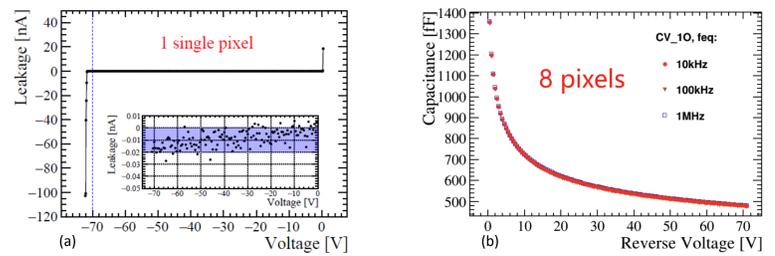


Fig4. IV test result (a) and CV test result before irradiation (b); test leakage current with irradiation (c); sensor responses to a laser (d) and AM-241 source (e) have been observed

Main array circuit results

- Charge injection test: Amplifier works well, response curve consistent with pre-simulation.

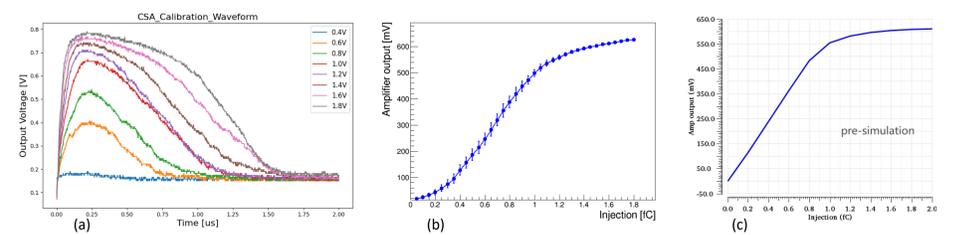


Fig5. CSA output with charge injection (a); response curve test (b) and simulation (c)

- Sensor test: red laser, beta ray from ⁹⁰Sr and X-ray from ⁵⁵Fe test sensor of pixel. The signal of red laser and beta ray are clear. The characteristic peak of X-ray from ⁵⁵Fe is also clear.

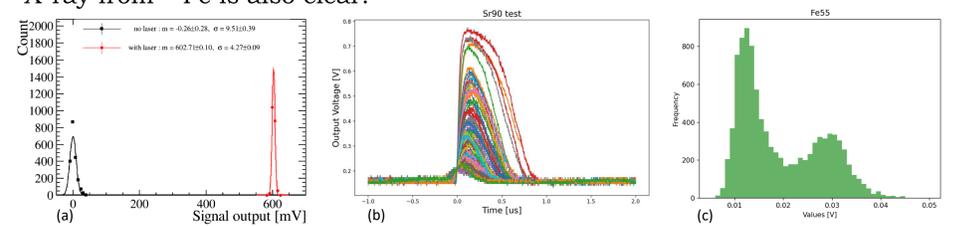


Fig6. red laser (a); beta ray (b) and X-ray (c)

- Comparator test: NMOS and CMOS comparator and its' amplifier output in red laser. CMOS comparator causes amplifier disturbance when on. This disturbance is caused by the absence of the deep p-well isolation layer in the triple-well process. However, through future process improvements in collaboration with the foundry, this effect is expected to be mitigated.

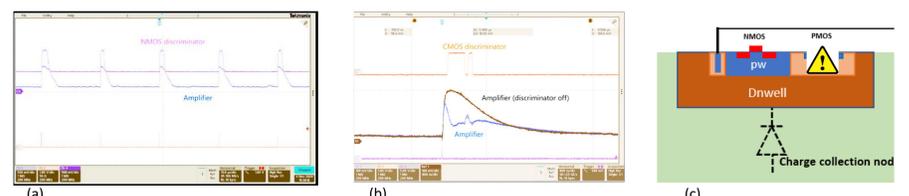


Fig7. NMOS comparator (a), CMOS comparator (b), PMOS cross talk (c)

Summary & Outlook

Preliminary measurements were carried out using injection circuits and radioactive sources. Results are in agreement with predictions. COFFEE2 demonstrates the feasibility of 55nm HV-CMOS technology for high-energy physics detectors. Future work will focus on collaborating with foundries to refine process capabilities, including optimizing substrate resistivity to enhance charge collection and introducing a deep P-well for pixel isolation. Sensor prototype with full readout functionality including in-pixel TDC are being designed with the same process.