

# ColorPix3 ASIC: Design of a Hybrid Pixel Readout Chip for High-Resolution Spectroscopic Imaging with CZT Sensors

The ColorPix3 ASIC represents an advanced hybrid pixel detector design tailored explicitly for high-resolution, color-sensitive X-ray imaging. Developed using a 65-nm CMOS process, this ASIC integrates a pixel matrix comprising of  $32 \times 32$  pixels, each sized at  $70 \times 70 \mu\text{m}^2$ , covering a sensitive area of  $0.05 \text{ cm}^2$ . In this technology demonstrator, the digital part of the readout system is being evaluated, which is capable of serving a  $256 \times 256$  pixel matrix. The future enlarged version of the chip is therefore able to cover a sensitive area of  $3.21 \text{ cm}^2$ .

The ColorPix3 ASIC features inter-pixel communication and implements a sophisticated Winner-Leader-Follower (WLF) summation algorithm, adjustable for clusters of either  $3 \times 3$  or  $5 \times 5$  pixels. **Each pixel in the matrix is equipped with ten independently controlled 12-bit counters with configurable equidistant thresholds**, supporting multi-color, custom-color, and monochromatic imaging modes. The ASIC further boasts a high-speed data readout capability of up to 3.2 Gb/s, safety low power mode, integrated current references, and on-chip debugging functionalities. Specifically engineered for bonding to a 2 mm thick Cadmium Zinc Telluride (CZT) sensor, the ASIC design significantly enhances performance in energy-sensitive photon detection applications.

## Workshop topics

Front-end electronics and readout

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