Contribution ID: **223** Type: **poster**

Performance of DC resistive read-out silicon sensors for future 4D tracking

In recent years, the innovative concept of low internal gain avalanche detector (LGAD) coupled with the resistive read-out (RSD) has significantly changed the performance of silicon detectors. By increasing the ratio signal-to-noise by a factor of around 20, the LGAD mechanism led to unprecedented time resolution, on the order of 30 ps for a 50 um active sensor thickness. The resistive read-out allows
instead to share the collected charge between several electrodes, achieving an excellent spatial resolution, order of 5% of the pixel pitch. These two concepts combined enable 4D tracking with silicon sensors.

This contribution presents the latest silicon sensor design based on these two concepts: a thin LGAD with a DC-coupled resistive read-out, the DC-coupled Resistive Silicon Detector (DC-RSD). This design aims at achieving controlled signal sharing through the implementation of isolating trenches (TI technology) amongst the electrodes that define the pixel.

Various structures are implemented in the wafer layout, manufactured at FBK as part of the 4DSHARE project. A subset of sensors have been characterised with a laser TCT system, equipped with a 5-um spot, to estimate the ultimate spatial resolution as a function of the pitch. Measurements at the TCT are also performed to evaluate how different values of the resistive layer impact the signal sharing. The spatial and temporal resolutions of sensors tested at DESY with an electron beam will also be presented.
This study will provide significant feedback on the capabilities and reliability of the DC-RSD design.

Workshop topics

Sensor materials, device processing & technologies

Author: BARDELLI, Giulio (Universita e INFN, Firenze (IT))

Presenter: BARDELLI, Giulio (Universita e INFN, Firenze (IT))