

Design of a HV-CMOS Prototype in 55nm process for the LHCb Upgrade II Upstream Tracker

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ABSTRACT

High-Voltage CMOS (HV-CMOS) pixel sensors are promising candidates for tracking applications in future high-energy physics experiments. Compared to the current mainstream 180 nm–130 nm processes, next-generation smaller technology nodes offer significant potential for improvements in power consumption, design flexibility, and overall performance. We have developed a prototype COFFEE3 based on a commercial 55 nm HV-CMOS process to meet the design requirement of the Upstream Pixel tracker in the LHCb Upgrade II.

INTRODUCTION

The LHCb Upgrade II, proposed for implementation during Long Shutdown 4 (LS4) of the LHC, aims to operate the detector at a maximum luminosity of $1.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. This necessitates the Upstream Pixel tracker (UP) to achieve a detection efficiency exceeding 99% under extreme hit densities of up to 100 MHz, provide nanosecond-level timing resolution to precisely tag collisions occurring at 25 ns intervals in the LHC, and maintain an average power density below 200 mW/cm².

To address these requirements, we propose a monolithic pixel sensors designed in 55 nm HV-CMOS technology. Building on the initial validation of the COFFEE2 prototype, the COFFEE3 chip prototype was designed and submitted in January 2025. At present, the chips have just been received and the testing work is in progress.

Process condition: affect design solutions

Several modifications of current process are desired:

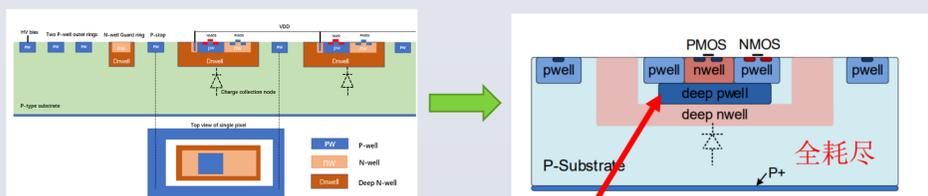


Figure 1. cross section of the current process (left) and desired process (right).

- **Triple-well:** transistors are enfolded by Dnwell
- **Wafer resistivity:** **10 Ω·cm;**
- **Metal layers:** 9 (1 top metal); **benefit for routing**
- The charge sensing diode formed by DNW & PSUB could be biased > 70V before breakdown;
- **Depletion depth about 10 — 20 μm;** (corresponding to 1k – 2k e⁻ total signal charges)
- **Replace the wafer for a higher resistivity substrate:** significantly increase the depletion depth, enhancing the total signal charge (2k – 20k e⁻) and reducing the front-end equivalent capacitance -> resulting in a higher SNR (signal-to-noise ratio);
- **Fine-tuning the well structure:** Adding an isolation layer between the Nwell and DNW allows for the integration of complex digital circuits within the pixel -> greatly increasing design flexibility and improving overall performance.

..... Efforts are still on going

Floorplan of COFFEE3

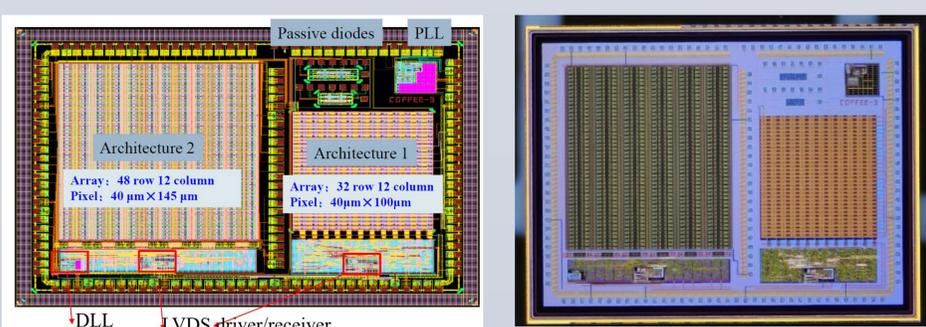


Figure 2. Layout (left) and picture (right) of COFFEE3 (left). The whole layout size is 4mm × 3mm, It contains two distinct pixel array readout architecture, the supporting digital circuits, necessary peripheral functional modules such as DLL, LVDS, PLL and a passive diode array for further research on the sensor and process.

Readout architecture 1

This architecture adopts a 32 × 12 pixel matrix where digitization is performed locally within pixels, with time-stamping executed at the array periphery to reduce intra-pixel complexity and power consumption.

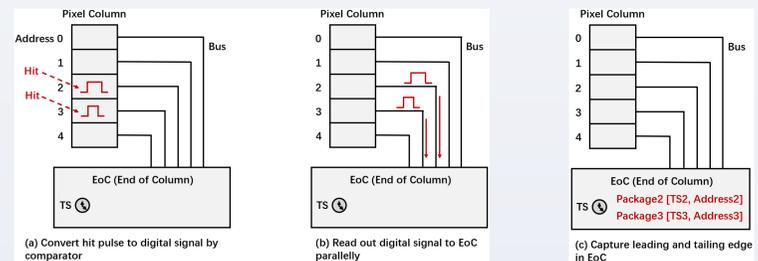
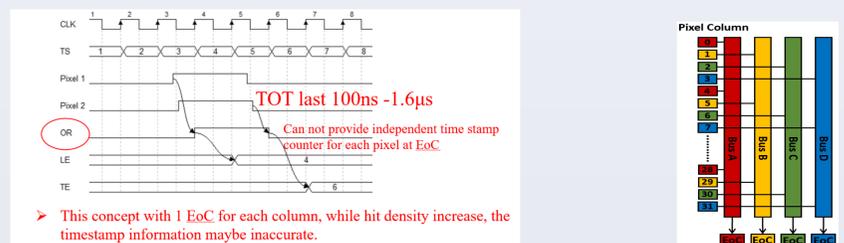


Figure 3. Readout concept of architecture 1. In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.



- COFFEE3 divides each column of pixels into 4 groups, which are input into 4 EoC modules. Each EoC also includes additional FSMs to handle higher hit rates. The area of the peripheral digital circuits does not significantly increase (less than 10% of the whole sensor).
- More EoC groups may be required for the most critical part of UP.

Readout architecture 2

This architecture integrates a 48 × 12 pixel matrix with in-pixel coarse-fine Time-to-Digital Converters (TDCs), enabling a data-driven prioritized readout scheme to optimize throughput and timing accuracy.

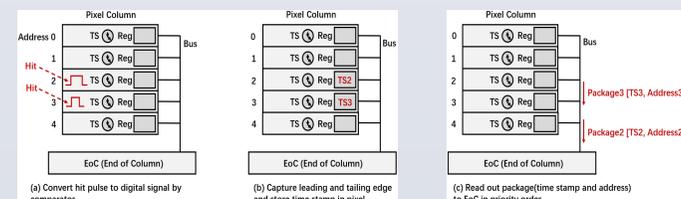


Figure 4. Readout concept of architecture 2. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.

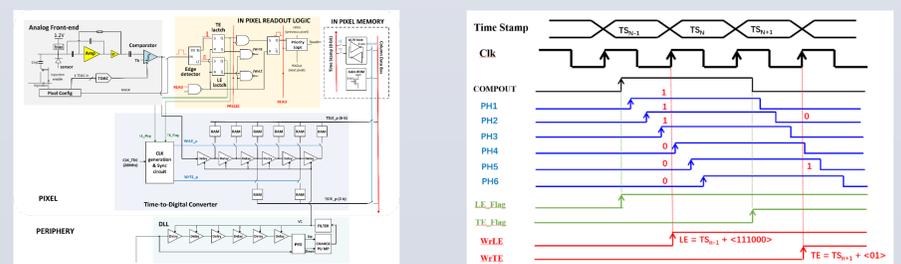


Figure 5. In-pixel schematic of architecture 2 (left). The pixel array employs a 40MHz coarse timestamp (25ns period). Within each pixel, a delay-line structure processes the comparator output to subdivide each coarse period into 6 bins, providing a 4.16ns fine timestamp for the leading edge (LE) of hit events (right).

Key performances from simulation

- **Noise:** The equivalent noise charge (ENC) of transient noise for three in-pixel FE architectures (two of them are for architecture 2) employed in COFFEE3 are ~160 e⁻, ~256 e⁻, ~97 e⁻ respectively;
- **Time resolution:** both the two architectures could provide a time resolution < 5 ns;
- **Power dissipation:** based on the design of architecture 2, estimate for a full size sensor (2cm*2cm), the power density would be ~ 150 mW/cm²;

CONCLUSION AND PERSPECTIVES

We have complete the design of COFFEE3 in a commercial 55nm HV-CMOS process to meet the specification required for the upstream tracker of the LHCb Upgrade II. The chips have been just received and the preparations for testing are currently underway. The test results from COFFEE3 will validate the design concepts and circuit performances, along with the possible process modifications will guide the design of the next version.