Fermilab

FERMI NATIONAL ACCELERATOR LABORATORY

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High frame rate Skipper CCD-in-CMOS imaging array

Farah Fahim

On behalf of Skipper CCD-in-CMOS (Fermilab, SLAC, Tower Semiconductor), SPROCKET (Fermilab, Northwestern University) and SparkDream (Fermilab, U. of Washington) projects

U.S. DEPARTMENT of ENERGY

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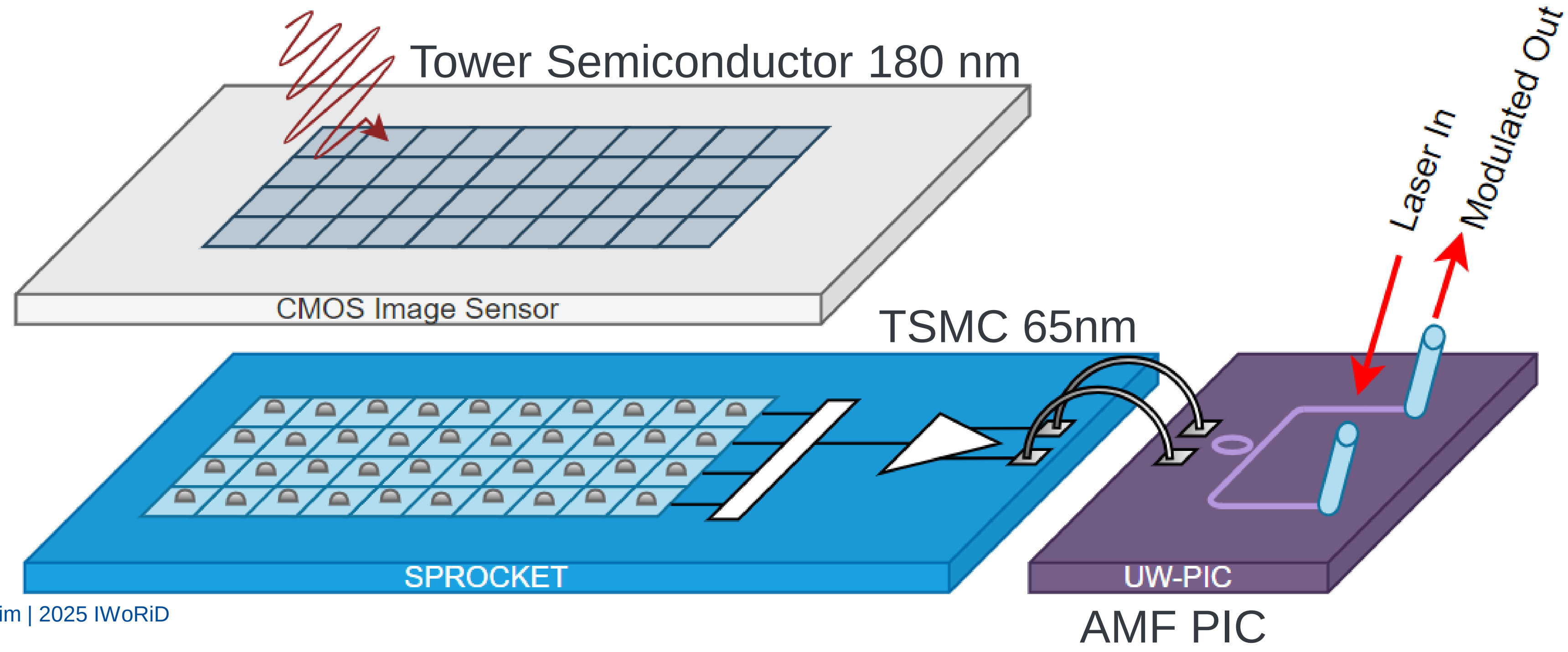
Physics Applications

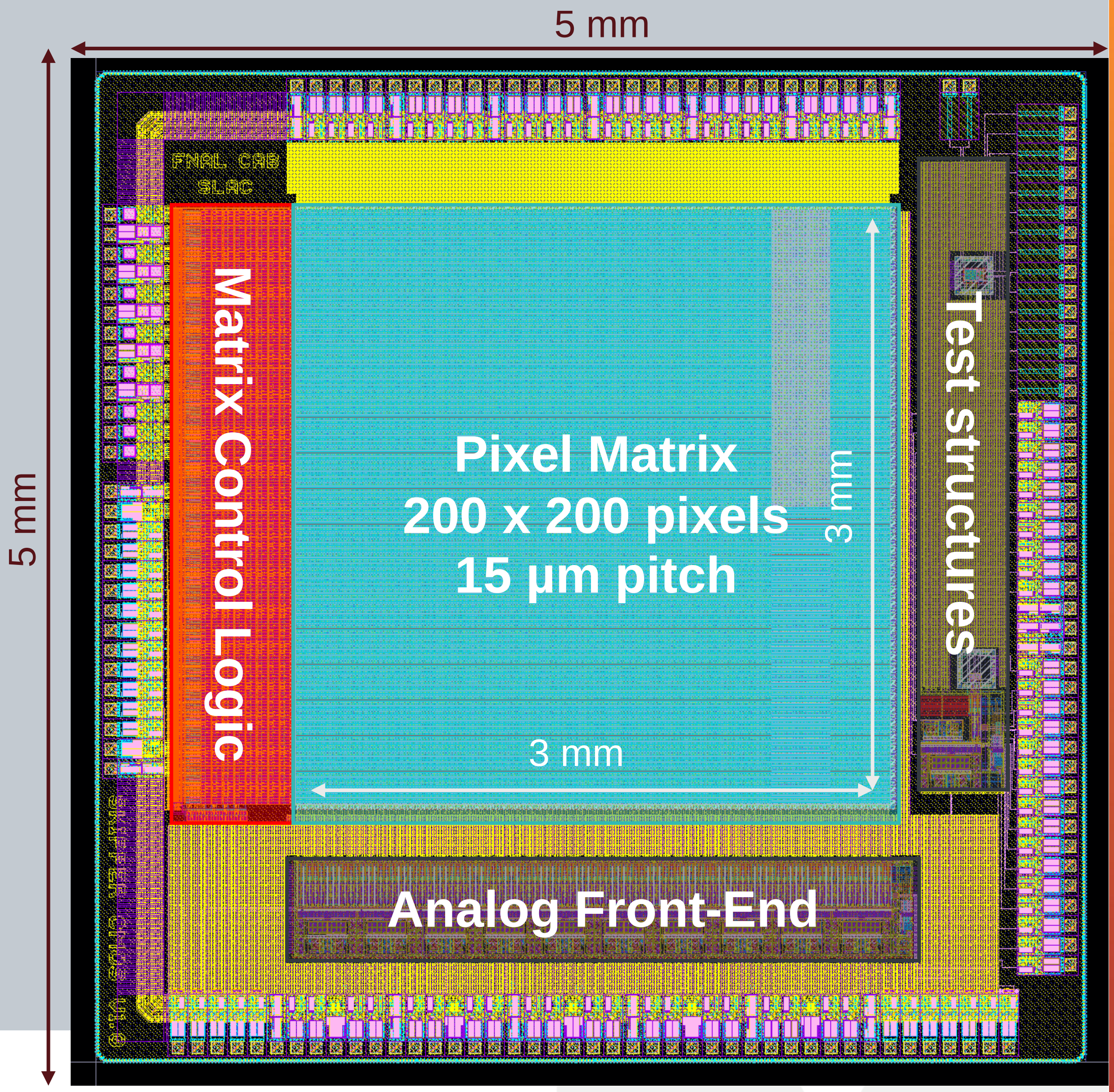
Development of Large Area Detectors for Ultra Low noise (< 1e-), High Speed (~ Mfps) and High Bandwidth Applications (> 100 Gbps) such as:

1. Low mass dark matter searches
2. Soft x-ray spectroscopy
3. Astrophysics: deep measurements of dark energy and dark matter signatures
4. Single-photon quantum sensing



Collaboration

Tower Semi: CMOS and Pixel Technology (CIS 180nm)
Centro Atómico Bariloche: Pixel and Matrix Implementation
Fermilab: Front End Readout Design
SLAC: Digital blocks and top-level implementation



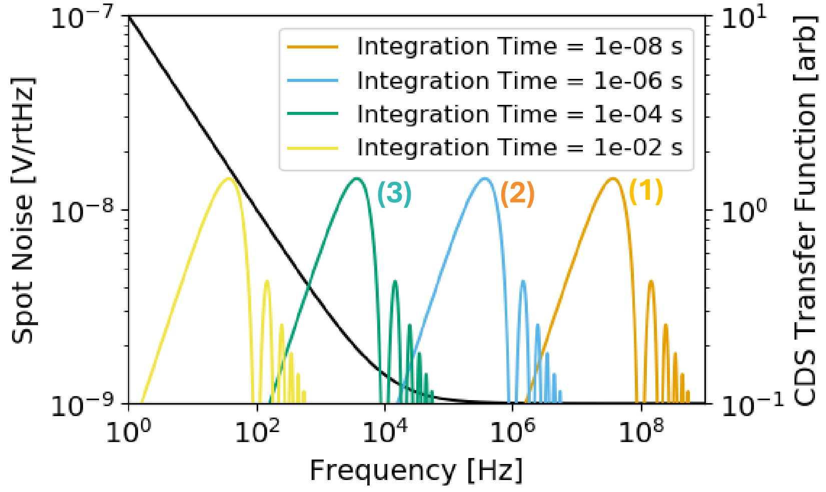
Tower Semiconductor 180 nm
CMOS Image Sensor

Skipper-in-CMOS Sensor

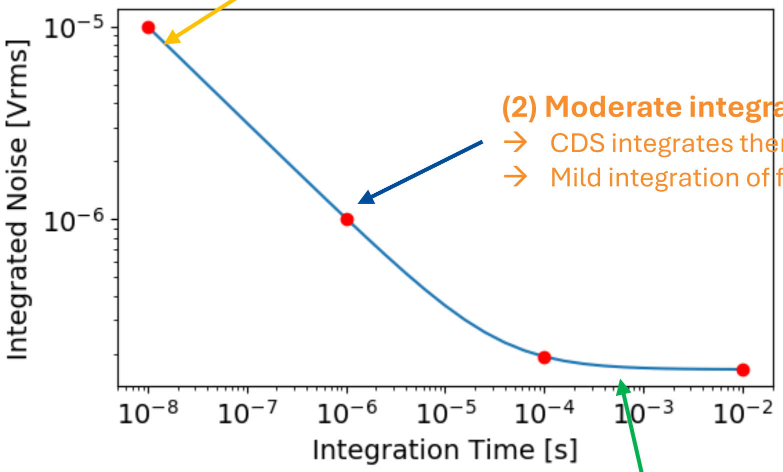
Pushing Noise Limits with Non-Destructive Readout (NDR)

Overcoming Limitation of Correlated Double Sampling

CDS



(1) Fast integration time:
→ CDS Integrates all the thermal noise over large bandwidth

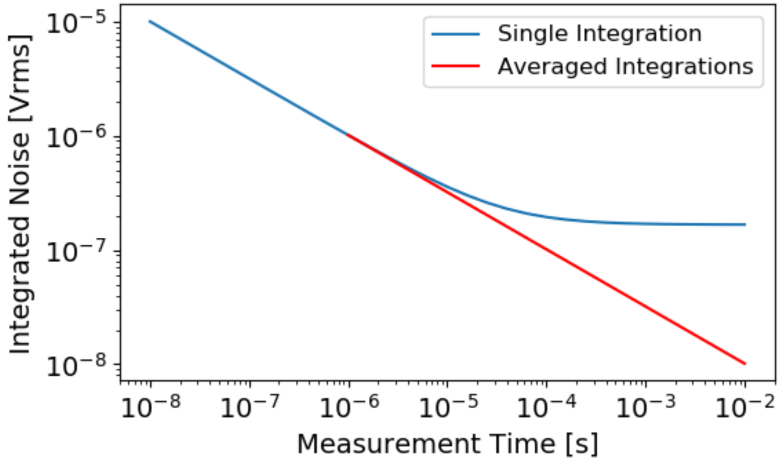


(2) Moderate integration time:
→ CDS integrates thermal noise over smaller bandwidth
→ Mild integration of flicker noise

(3) Slow integration time:
→ CDS integrates only flicker noise
→ The CDS bandwidth times 1/f noise is constant
→ We have reached the **limit** of the CDS

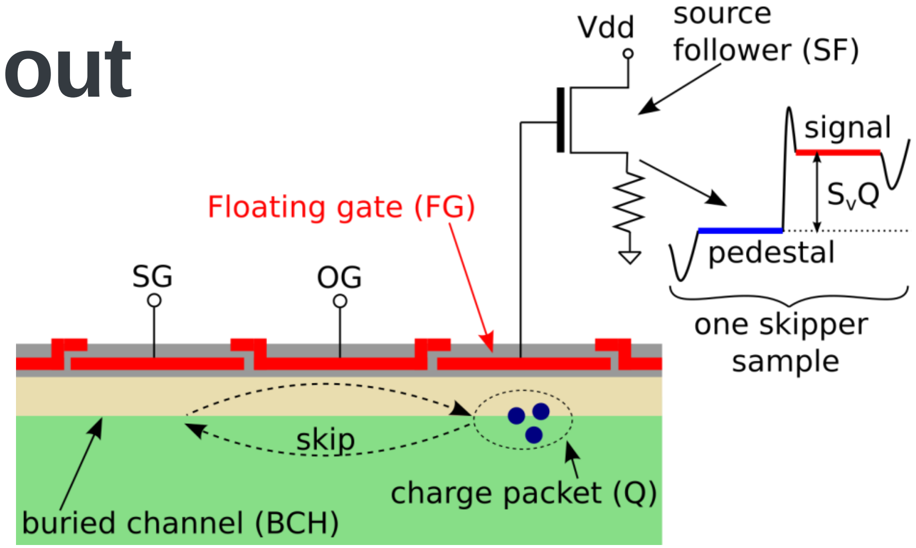
CDS + Skipping

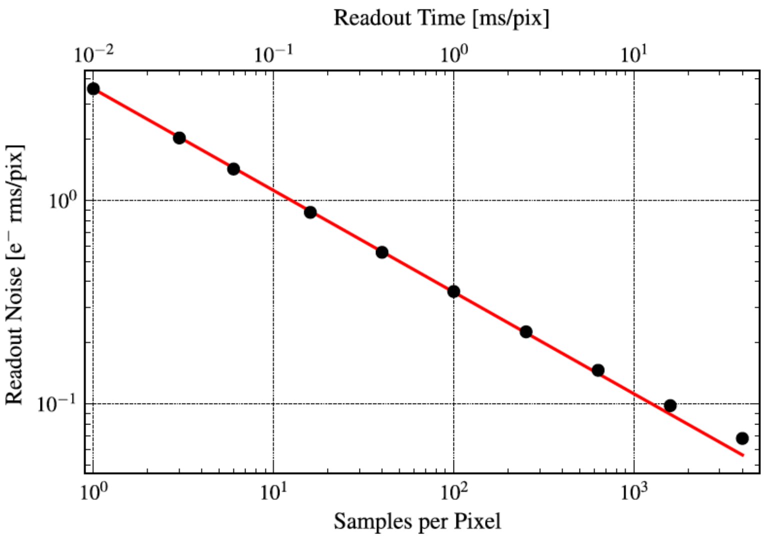
Successfully removes 1/f noise

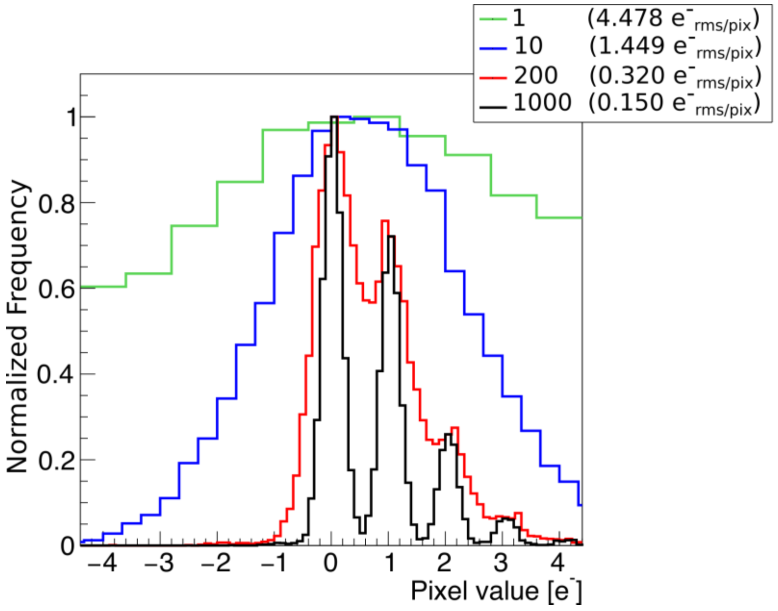


Skipper CCD for Non-destructive readout

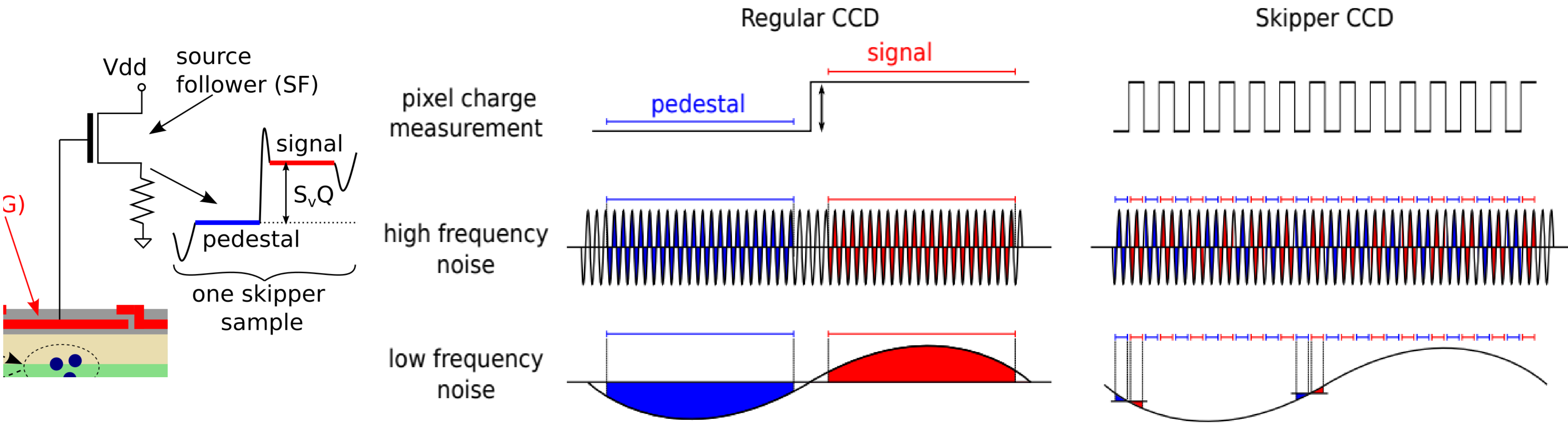
- Originally developed for CCD readout technique
- Allow to perform Non-Destructive Readout of the charge
- Signal is correlated, noise is not; improve SNR by $\sqrt{N}$
- Integrated noise < 1 e- is possible!
  ➔ Allow to do single photon imaging





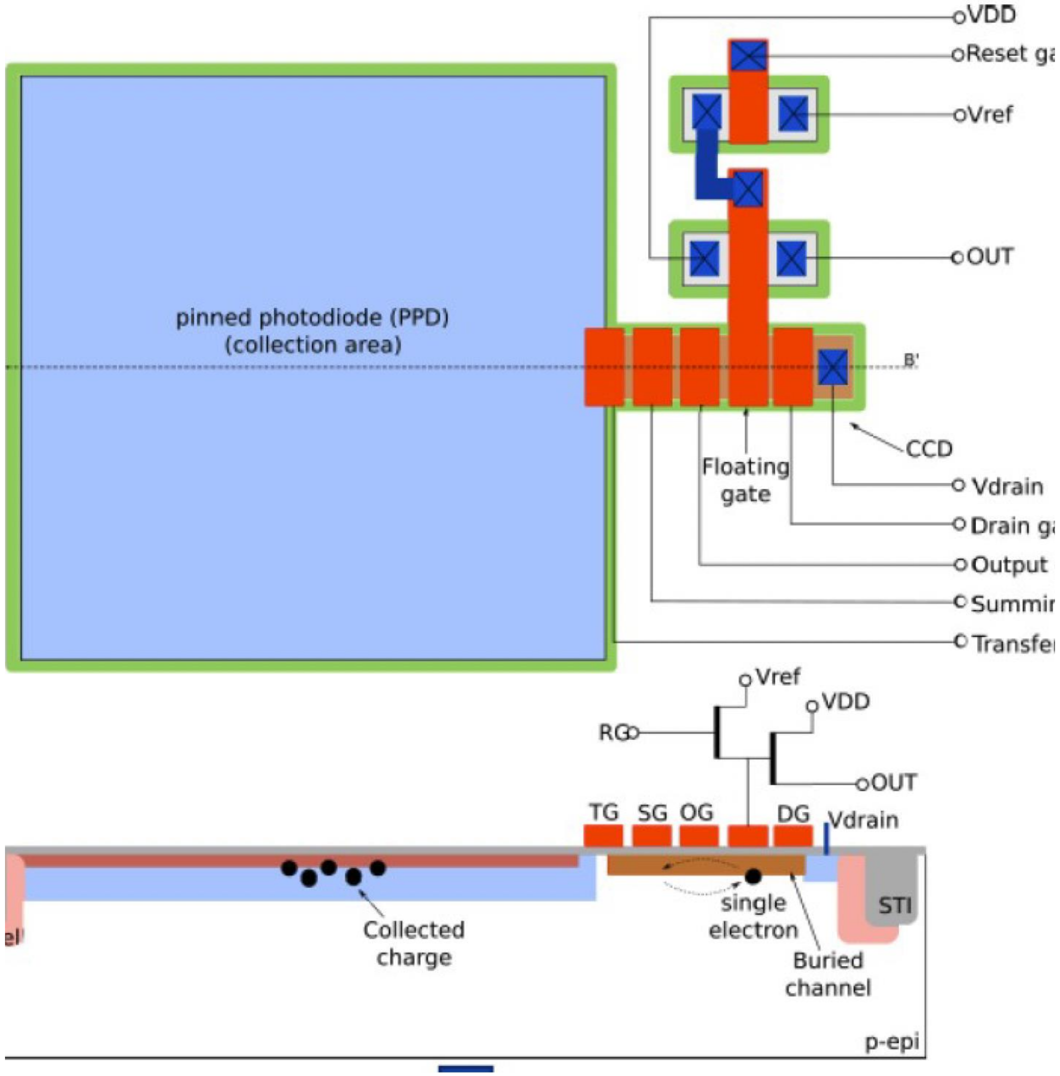


Skipping versus Correlated Multiple Sampling



- Final pixel value is *pix = avg(signal – pedestal)*, noise scales as *√#samples*
- Skipper readout is NOT the same as Correlated Multiple Sampling (CMS)
- Non-destructive read-out, pedestal and signal are sampled close to each other → filter low frequency noise too

Skipper CCD-in-CMOS



Pin-Photodiode for light collection

CMOS and Pixel structure from Tower

Expected conversion gain ~100 uV/e-

CCD structure charge-coupled to PPD

Expected single sample noise <1e-

Floating gate

For non-destructive multiple readouts

Concept Innovation

- **Sensor with Pinned PhotoDiode (PPD) for conversion**
  - ✓ Much higher Conversion Gain than CCD (100uV/e- vs 3uV/e-)
  - ✓ Low leakage
  - ✓ Lower noise per measurement than CCD

- **Skipper CCD for charge manipulation**
  - ✓ High charge transfer efficiency
  - ✓ Enables Non-Destructive Readout (NDR) capability
  - ✓ Enables noise averaging feature

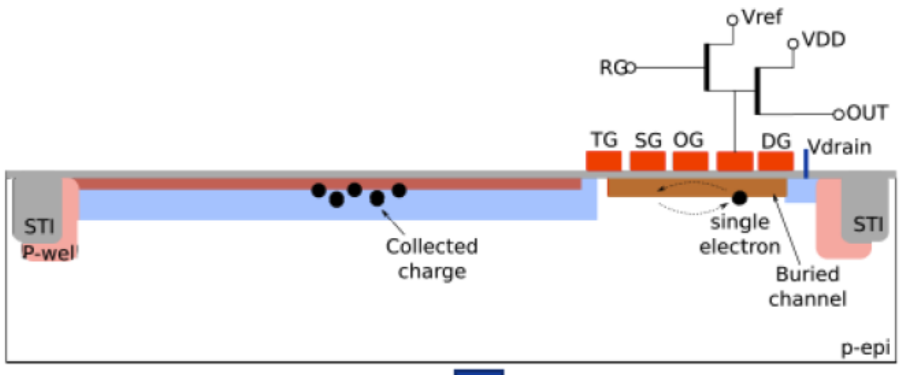
- **Co-integrated CMOS process**
  - ✓ Readout **parallelization** capabilities
  - ✓ Much **faster** readout time than CCD*
  - ✓ **Finer** feature size
  - ✓ **High-Volume** capability

Ref: Stefanov, K. D. (2020). Simulations and Design of a Single-Photon CMOS Imaging Pixel Using Multiple Non-Destructive Signal Sampling. Sensors , 20(7)

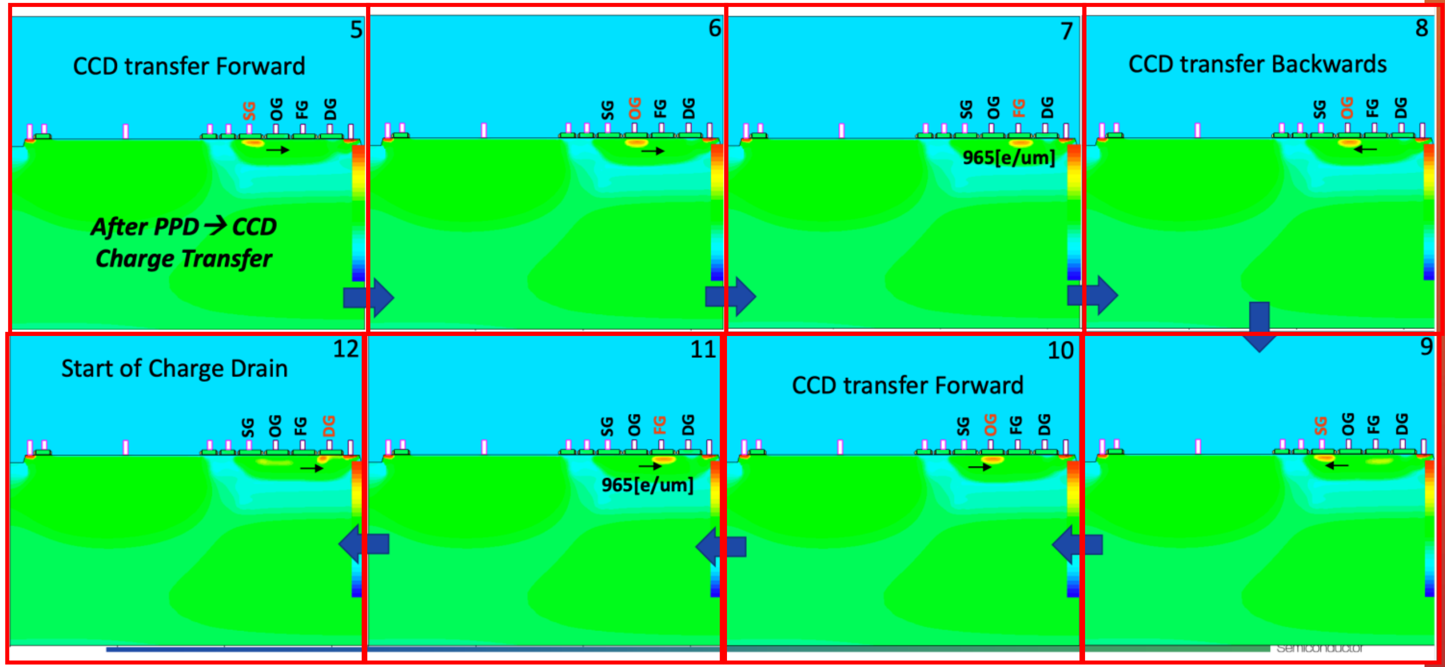
Non-Destructive Readout Operation

Operation:

1. Reset of the PPD and CCD
2. PPD charge integration
3. Pulse Transfer Gate (TG)



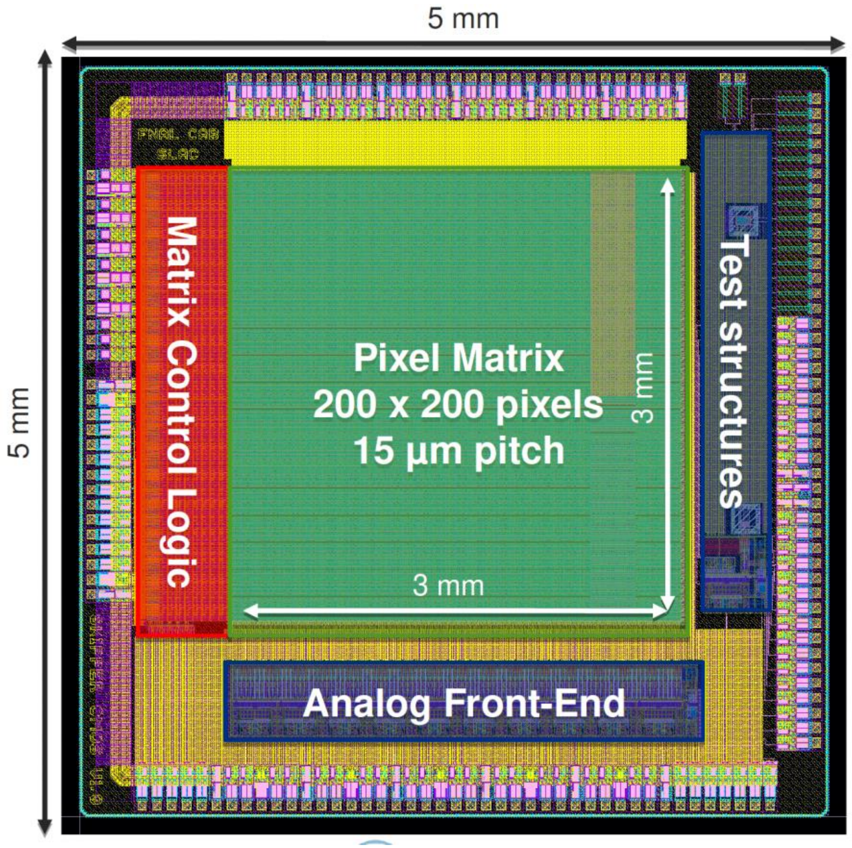
5. Transfer forward to the Summing Gate (SG)
6. Transfer forward to the Output Gate (OG)
7. Transfer forward to the Floating Gate (FG) for first NDR
8. Transfer back to OG
9. Transfer back to SG
10. Transfer forward to OG
11. Transfer forward to FG for second NDR
12. Transfer to the Drain Gain (DG) to flush the charges

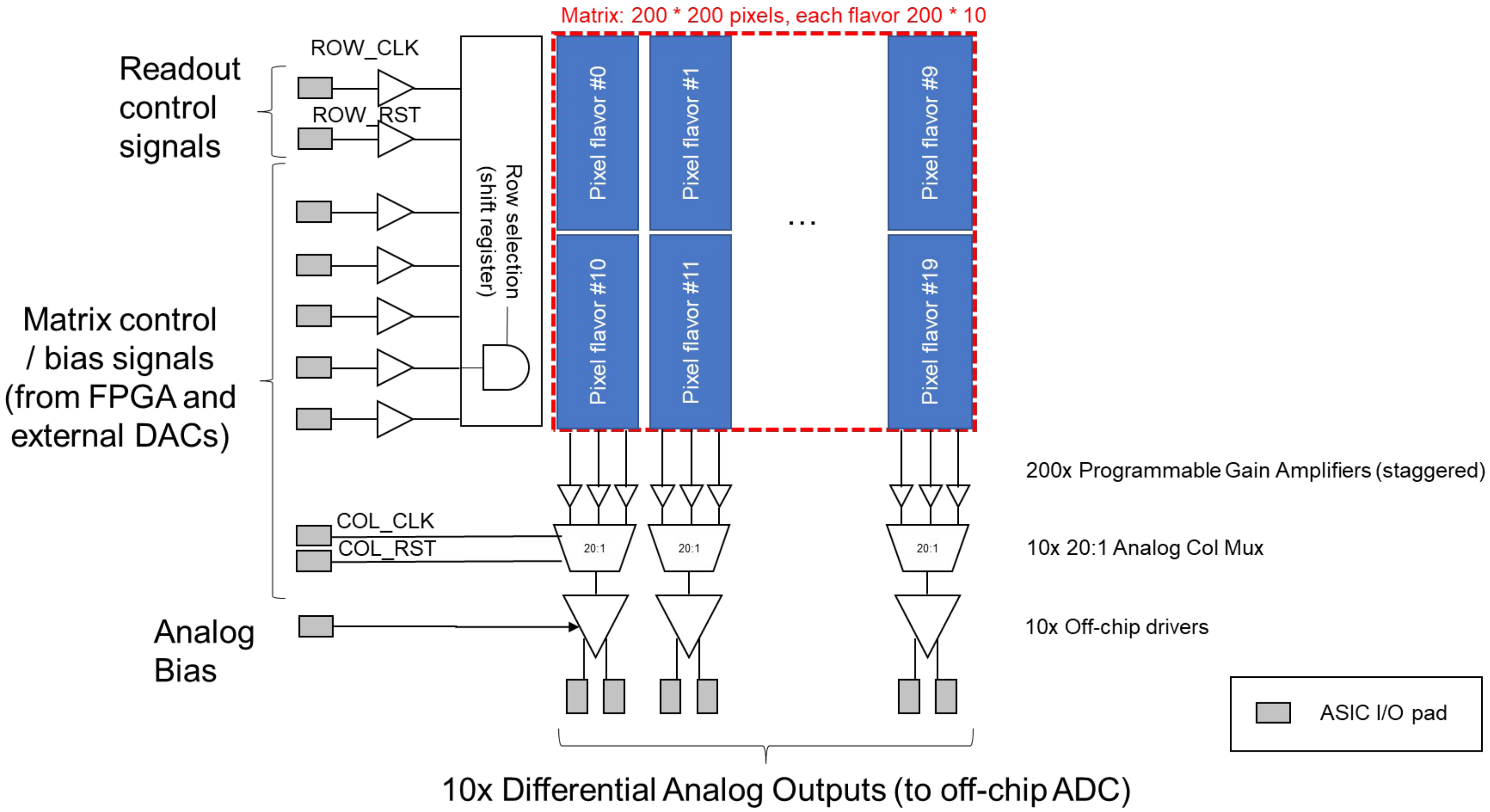


$$ENC_{final} = \frac{ENC_{initial}}{\sqrt{n}}$$

Device and redout system overview

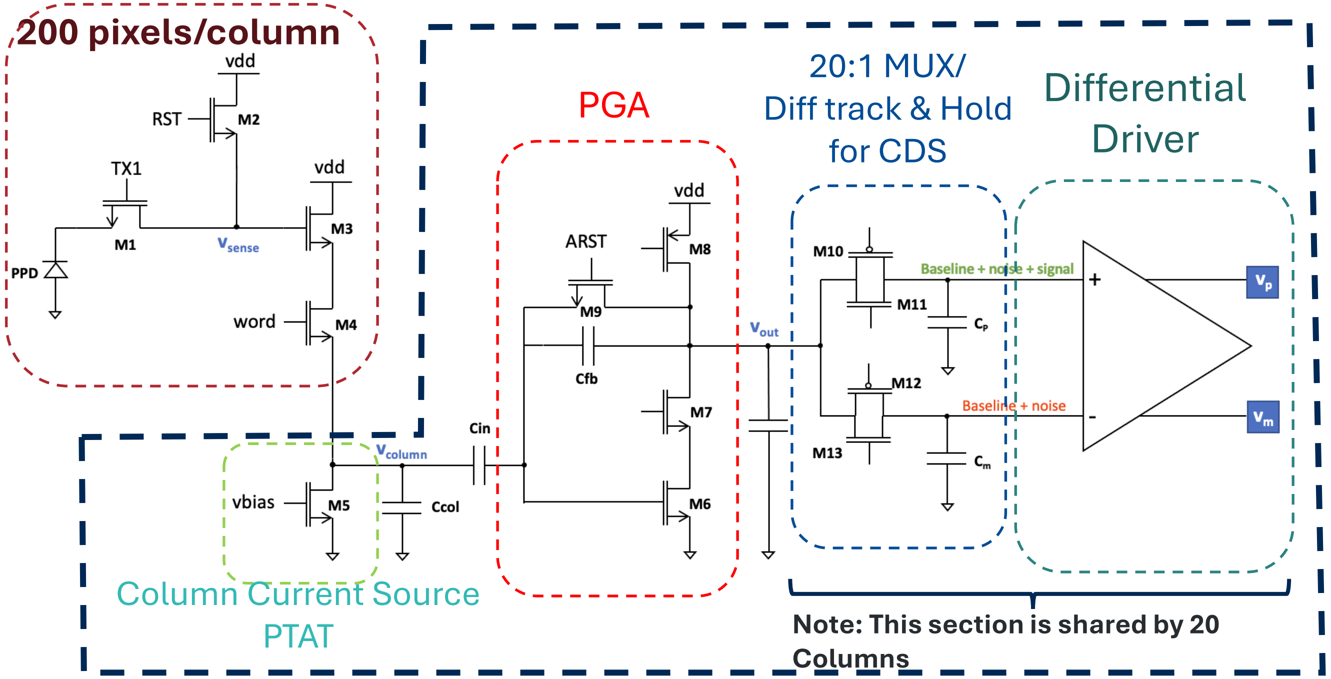
- PIXEL gates control are digital.
- PIXEL controlled thru level-shifers





1. Demonstrate low noise capabilities for a single measurement (< 2e- RMS including pixel and AFE)
2. Demonstrate **photon counting** with **micro-second scale readout time** capabilities
3. Fabricate and characterize pixel variations and AFE blocks:
   - → Identify pixel variant and split with best performance (Quantum Efficiency, Conversion Gain, Transfer efficiency)
   - → Identify AFE structures with best performance (noise, power, speed)
   - → Characterize and improve spice modeling of pixel

AFE Single Column Readout Chain Overview



To off-chip test board

Will perform readout, CDS and skipper operations

Spec	min	typ	max	unit	condition
IDC		24		mA	Nominal corner
Power		120		mW	Nominal corner
Output referred noise		188		uV	Noise tran, 0e-, cds=4pF, gain=1
ENC		1.6		e-	Noise tran, 0e-, cds=4pF, gain=1
ENC		<1		e-	Noise tran, 0e-, cds=4pF, gain=35
linearity: 1-R^2		9.8E-08		NA	gain =1, from 0e- to 11Ke-
Dynamic Range	1		11000	e-	Gain =1 and 2
Gain	1		35	V/V	

Key Specifications:

1. Small, Fast, Low noise
2. Gain tunable with Cin/Cfb capacitance ratio

   → High gain desirable in low light condition to improve SNR
3. Skipper operation effective up to the track & hold
4. Other noise sources (ie: KTC noise from track & hold, or sources from differential driver) are made insignificant due to the PGA gain

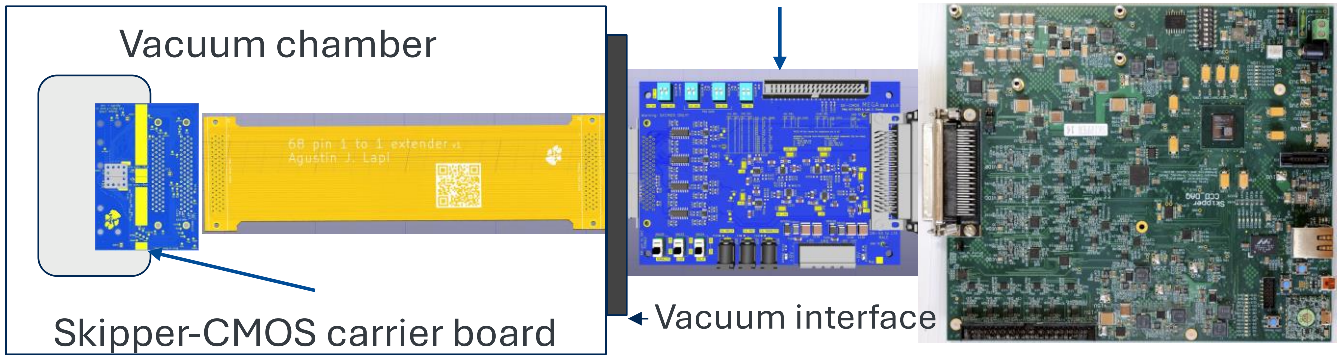
Single-photon Imaging – Peter Seitz/Boyd Fowler

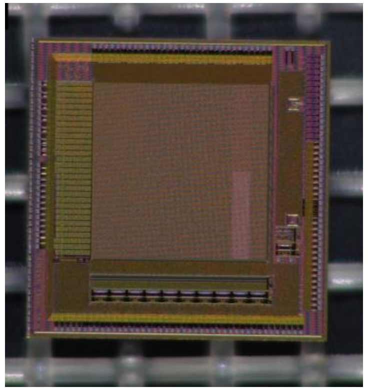
Springer Series in Optical Science 160

Testing system overview

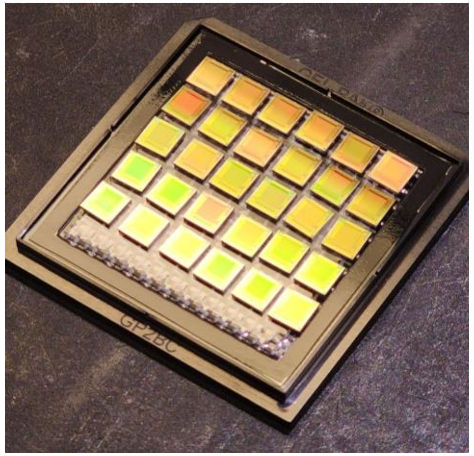
Interface board for
Bias, Multiplexing, digital buffers, 4 x 4:1 analog mux

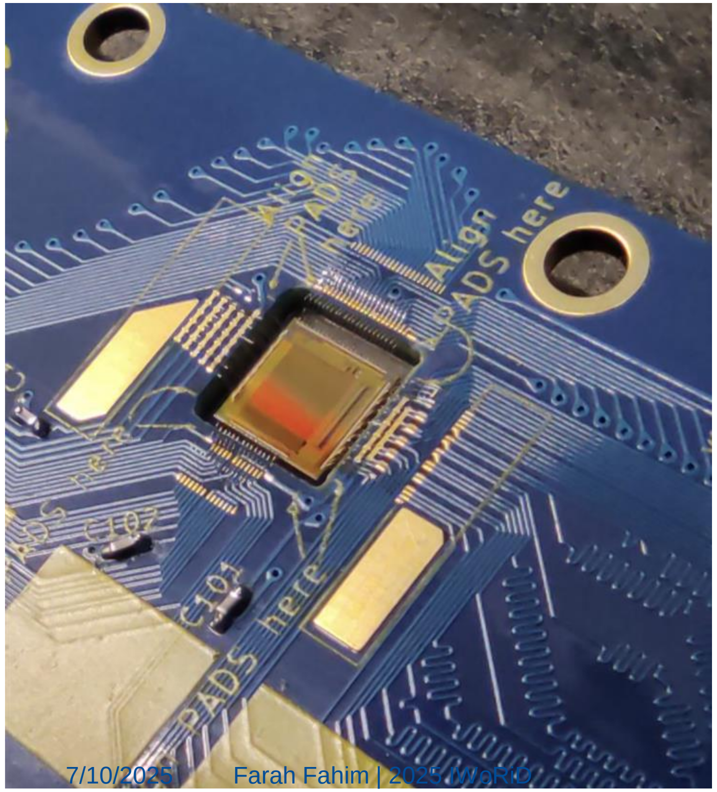
LTA (skipper Reaout- system)

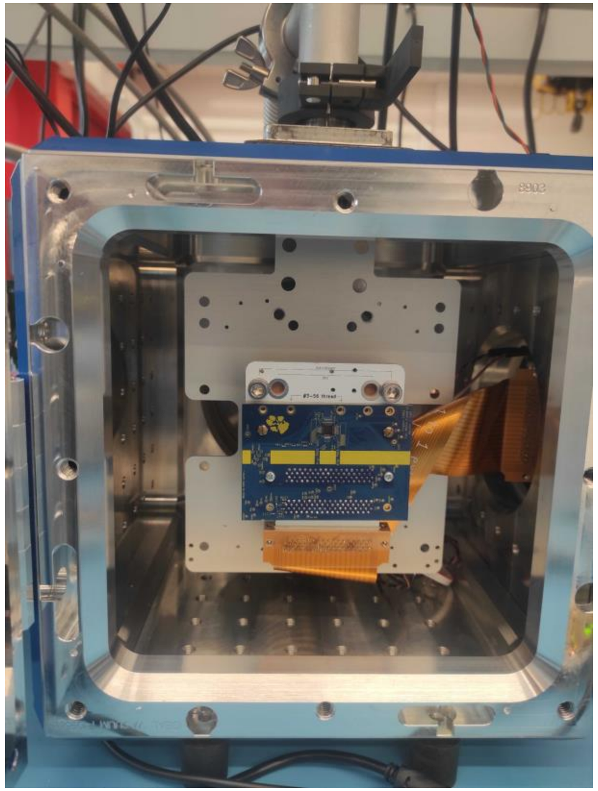


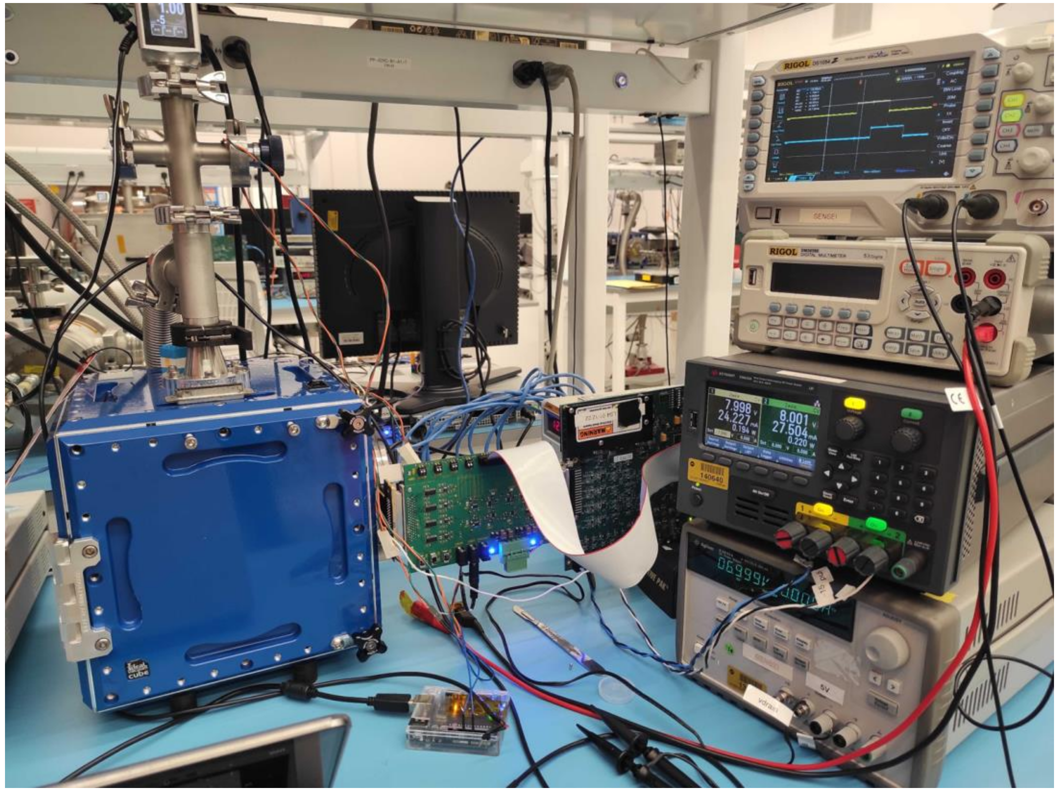


Chip Samples:
20 variants – 5 split









Stand-alone pixel structure

Charge transfer from PPD

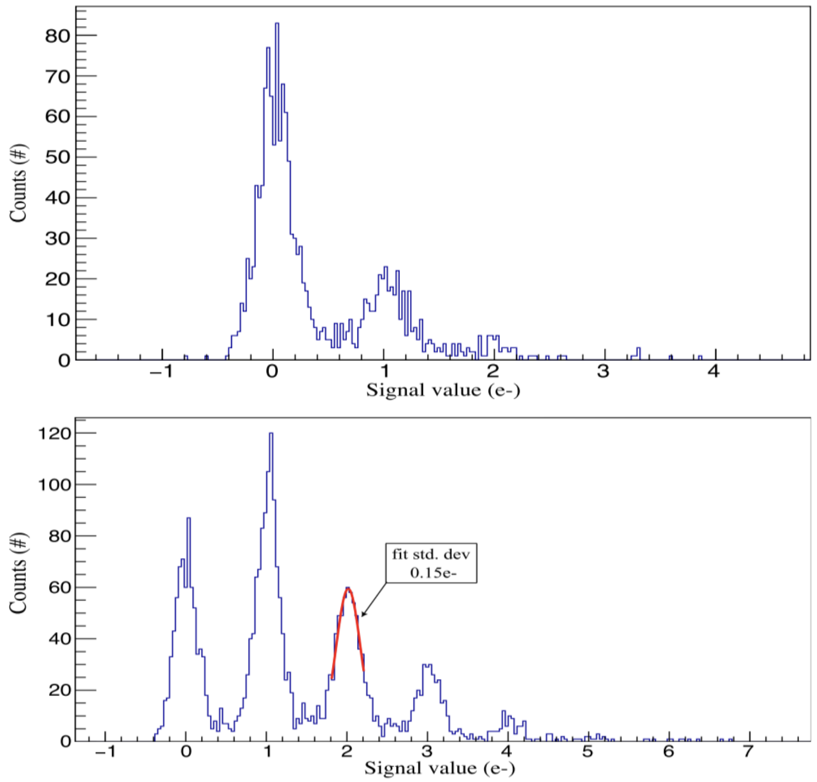
Successfully transfer charge from PPD to floating gate through charge-coupled CCD structure

Non-destructive readout

Up to 3000 skips tested

Sub-electron noise

0.15 e^- rms noise achieved



Stand-alone pixel test structure successfully demonstrate by Agustin Lapi [https://arxiv.org/pdf/2402.12516]

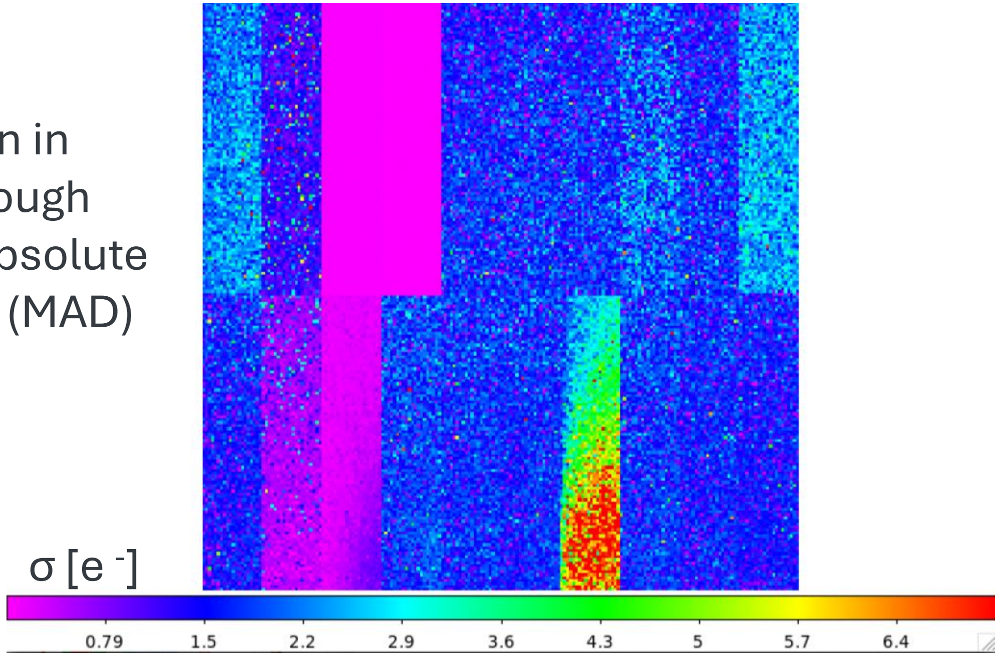
Matrix characterization

PRELIMNARY TEST RESULTS

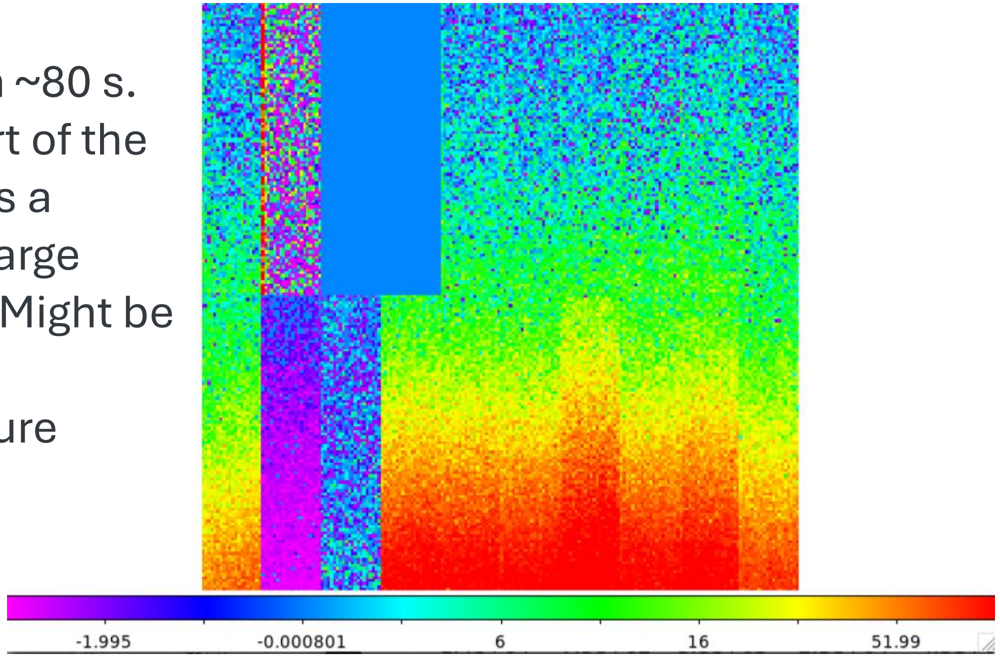
0:Case0	1:Case0_b	2:Case1_CTE_Lx0p7	3:Case1_CTE_Lx0p7_Wx1p5	4:Case0	5:Case2_TG1Wx2	6:Case2_TG2wCCD	7:Case3_Wx1p5	8:Case6_Wx0p5	9:Case4_sfLx1p5
10:Case0	11:Case1_CTE_Wx1p5	12:Case1_CTE_Wx0p5	13:Case1_CTE_noPWELL	14:Case0	15:Case2_TG1Wx2_TG2Wx1p5	16:Case2_TG1TG2wCCD	17:Case3_TG1wx2_TG2Wx1p5	18:Case6_Lx0p5	19:Case4_sfWx1p5

FOR THOSE IN RED, THEY DON'T ACHIEVE SUB-ELECTRON NOISE

Charge estimation in pixels through Median Absolute Deviation (MAD) image

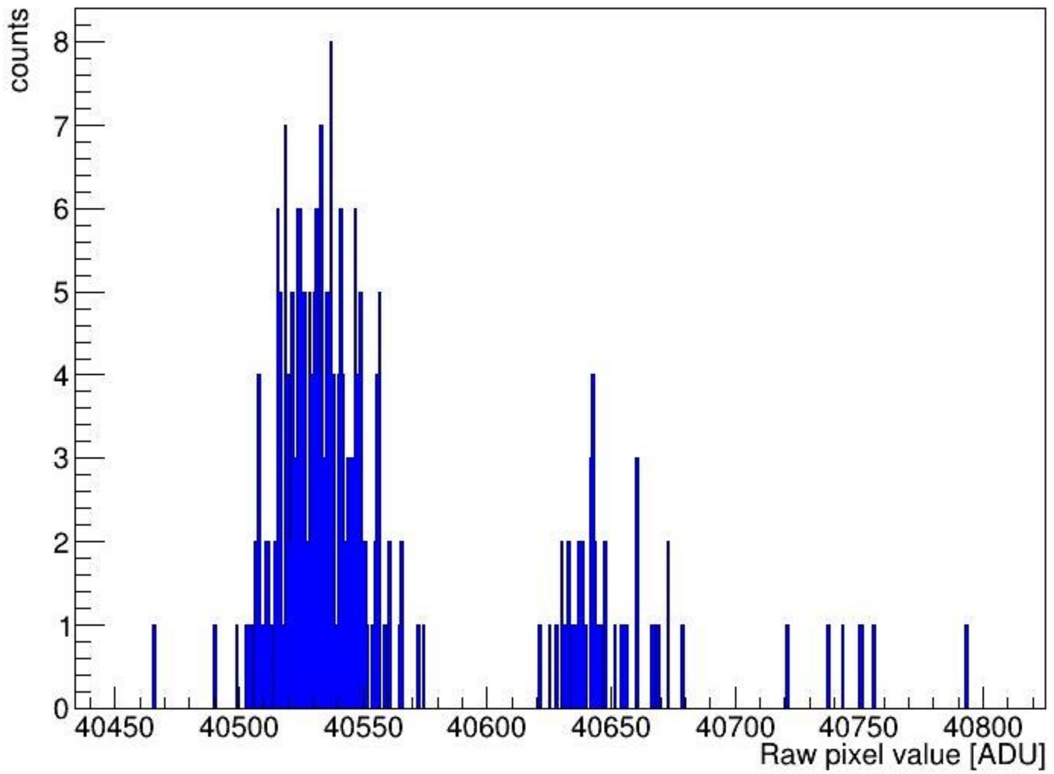


DC rate in ~80 s. Lower part of the matrix has a higher charge build-up. Might be related to temperature gradients



Case 12

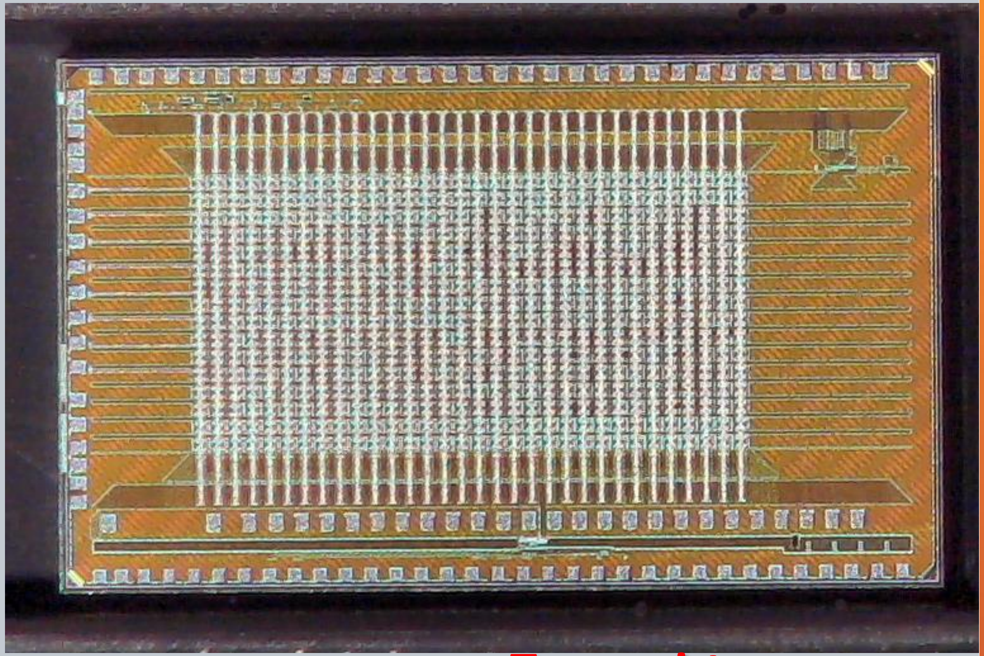
Most promising pixel structure

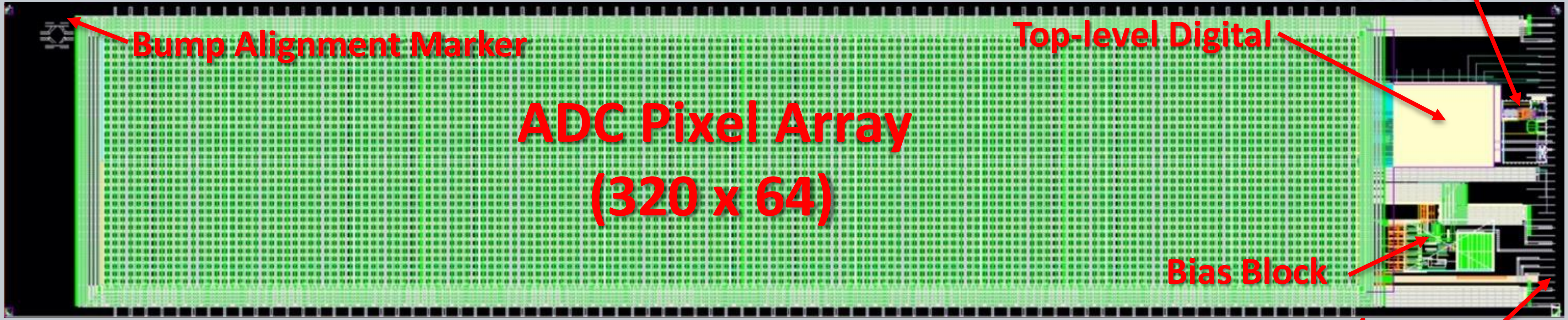


Slot:Flavor	Conversion Gain [uV]	Single skip noise [e-]	Mean STD in image [e -]	Average DC level after 80 s [e-]
12:Case1_CTE_Wx0p5	13.82	4.50	0.34	0.08

- Expected gain 100µV measured gain ~14µV. Probably transfer inefficiency from gates to drain.
- Expected single skip noise 1e-, measured noise 4.5e- (might be caused by higher floating gate capacitance
- Single measurement time (9µs), restricted by off-chip controls
- Issues with fully dumping the drain was observed
- We still have 5 other doping splits to measure

Collaboration
Fermilab: ASIC Design and Testing
Northwestern University: ASIC Design
TSMC 65 nm





SPROCKET
Accelerating Readout via Massive Parallelization

Pixel Electronics

- Key Specification:

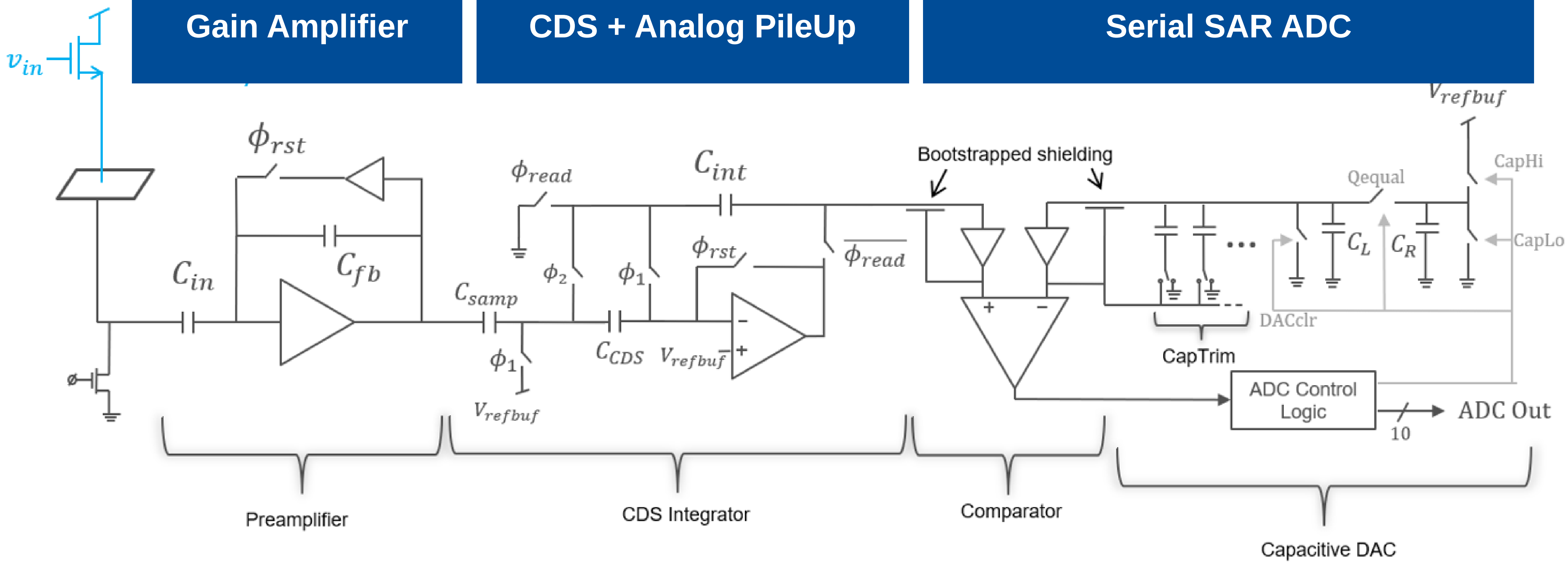
1. 1:16 readout electronics: sensor pixel ratio for highly parallel signal processing
2. Global shutter for sensor charge collection then approximately 1us charge integration time
3. 10b In-pixel compact serial SAR ADC with 6b trimming @ 100KHz
4. ~10us analog pileup (for small signals); 10us ADC conversion; 10us full frame readout

Source Follower

Gain Amplifier

CDS + Analog PileUp

Serial SAR ADC



Analog Pile-up

Observations:

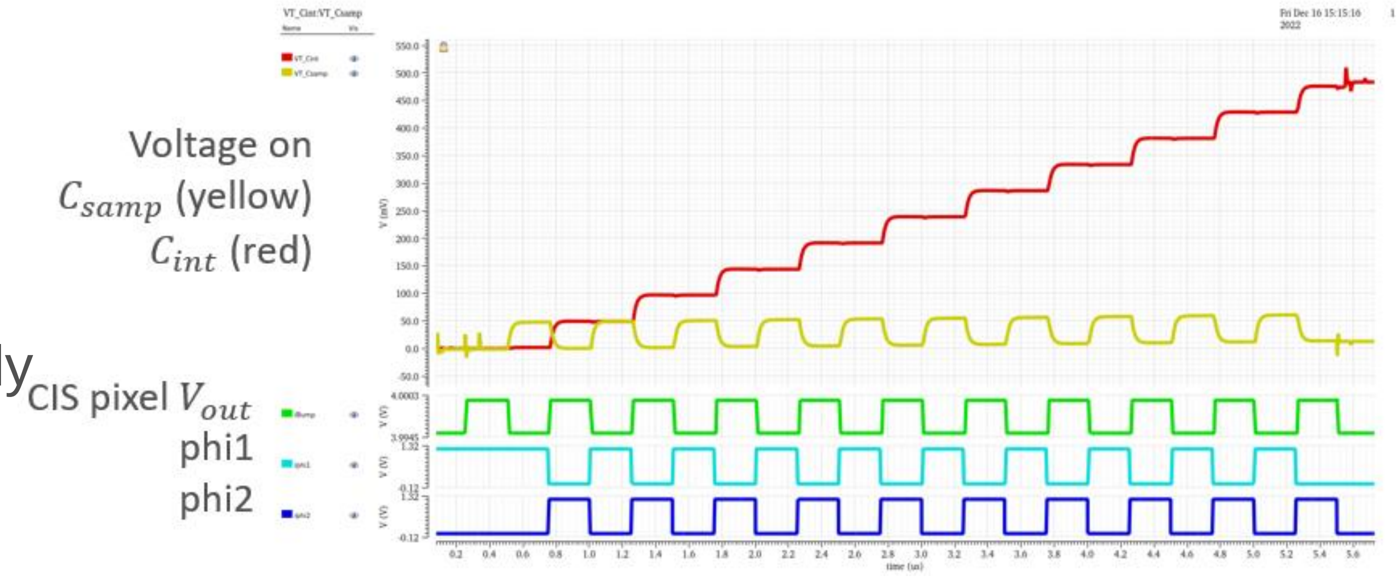
- A-to-D Conversion takes time + energy
- In Skipper-CMOS readout, we sample the same voltage multiple times; we only care about the average.

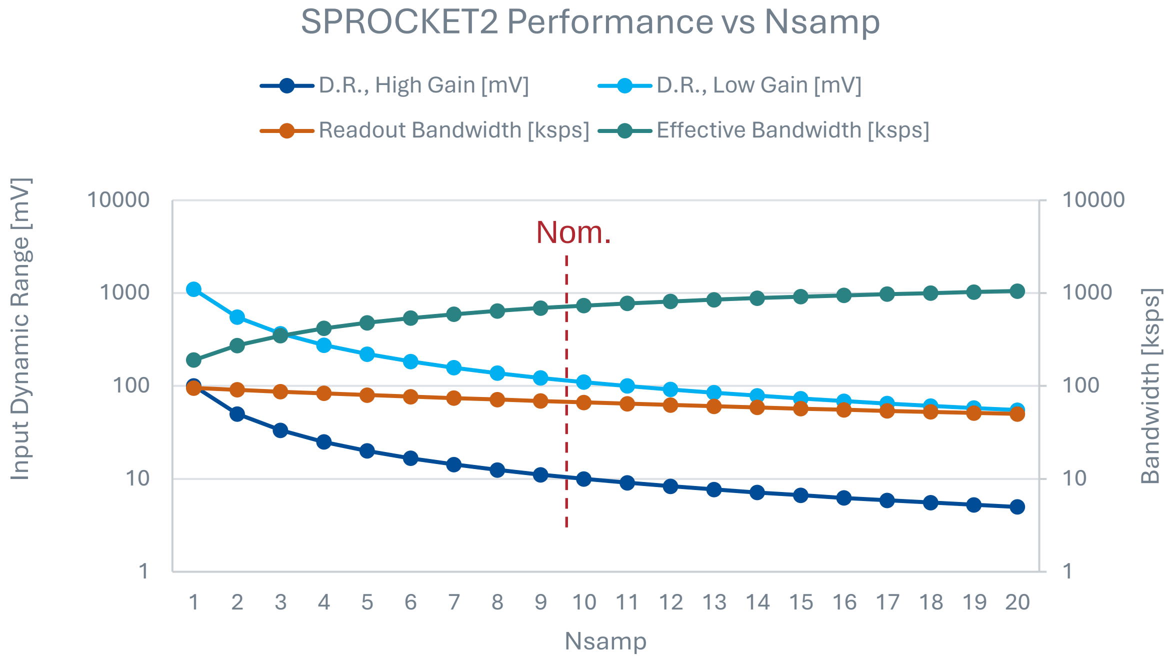
Therefore:

- Pile up multiple samples in analog, digitize the sum.
- For large signals above certain threshold we skip analog pileup
- **Intelligent data compression at the edge (not included in this prototype).**

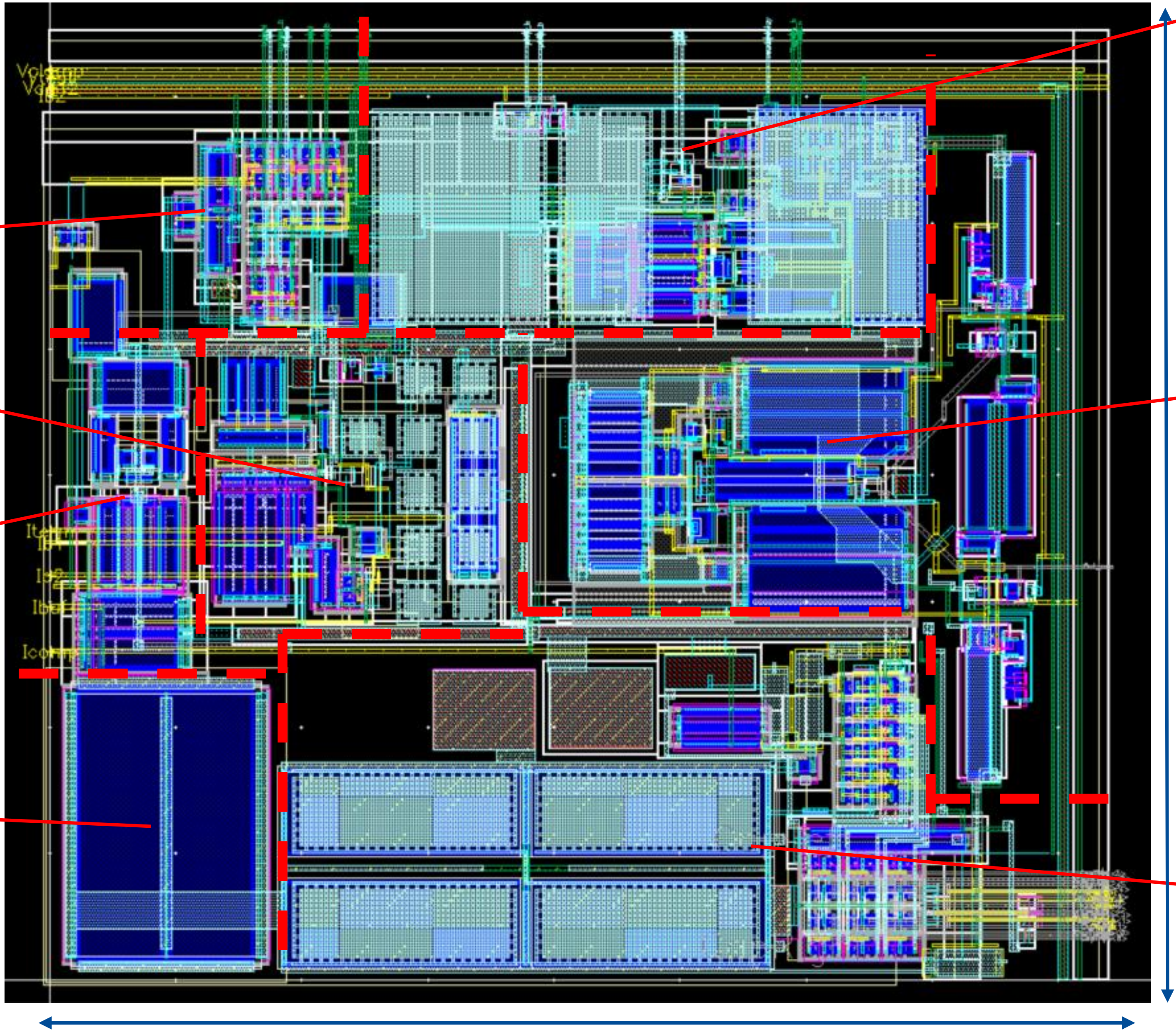
$$T_{readout}[\mu s] = 0.5 \times N_{samp} + 10$$

$$DR\ [mV\ V_{in}] = \frac{1000}{N_{samp}}$$



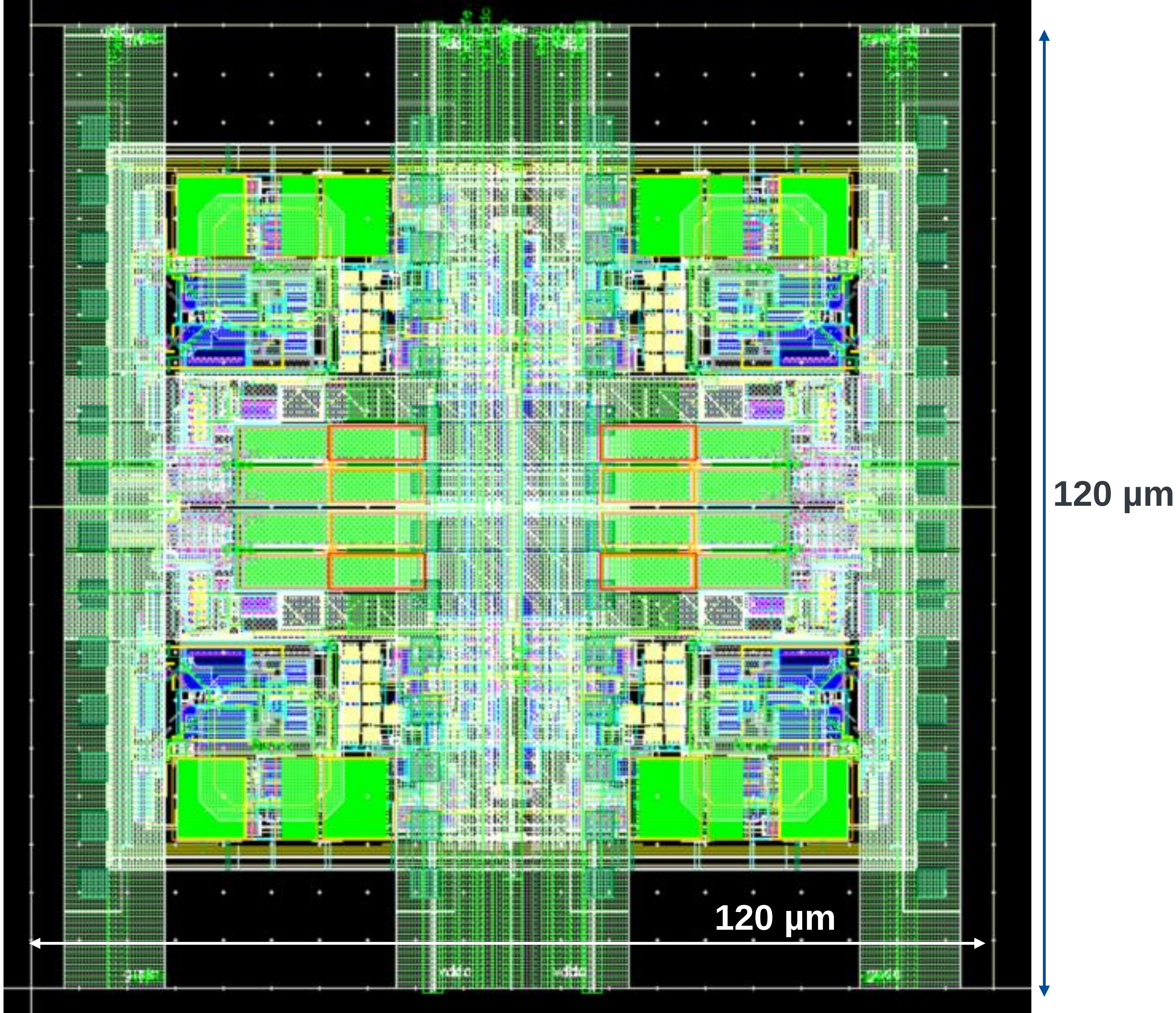


S2_PIX_ANA (blocks highlighted)



4 analog pixels with reserved area for digital processing and readout

- 4 analog frontends & 4 ADCs are shown



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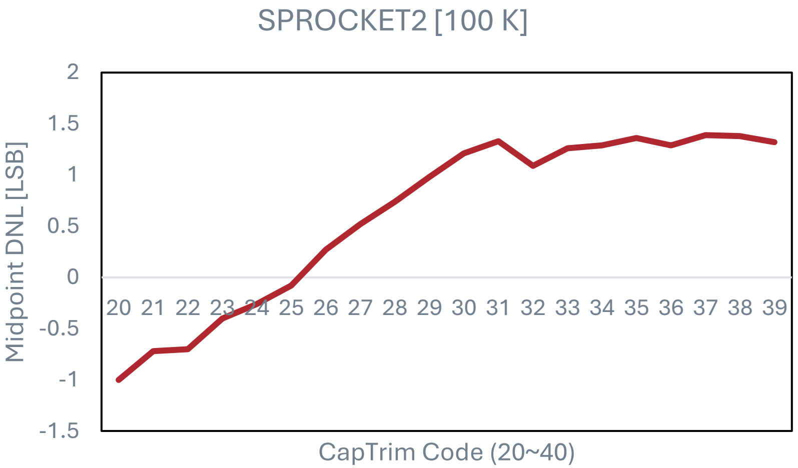
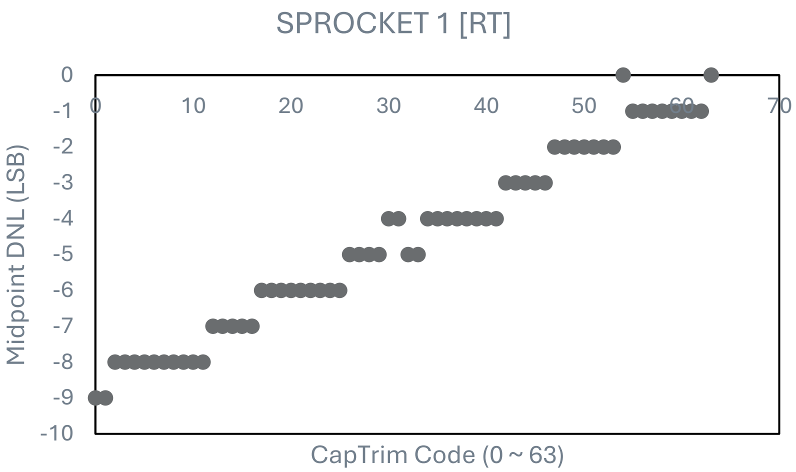
Results: ADC Linearity

Midpoint DNL versus CapTrim Code (Comparison of v1 and v2 ASICs)

CapTrim Value	0 (Min)	**25 (Opt)**	63 (Max)
Worst DNL [LSB]	5.95	**0.44**	-1 (missing codes)
Worst INL [LSB]	3.30	**0.58**	1.38



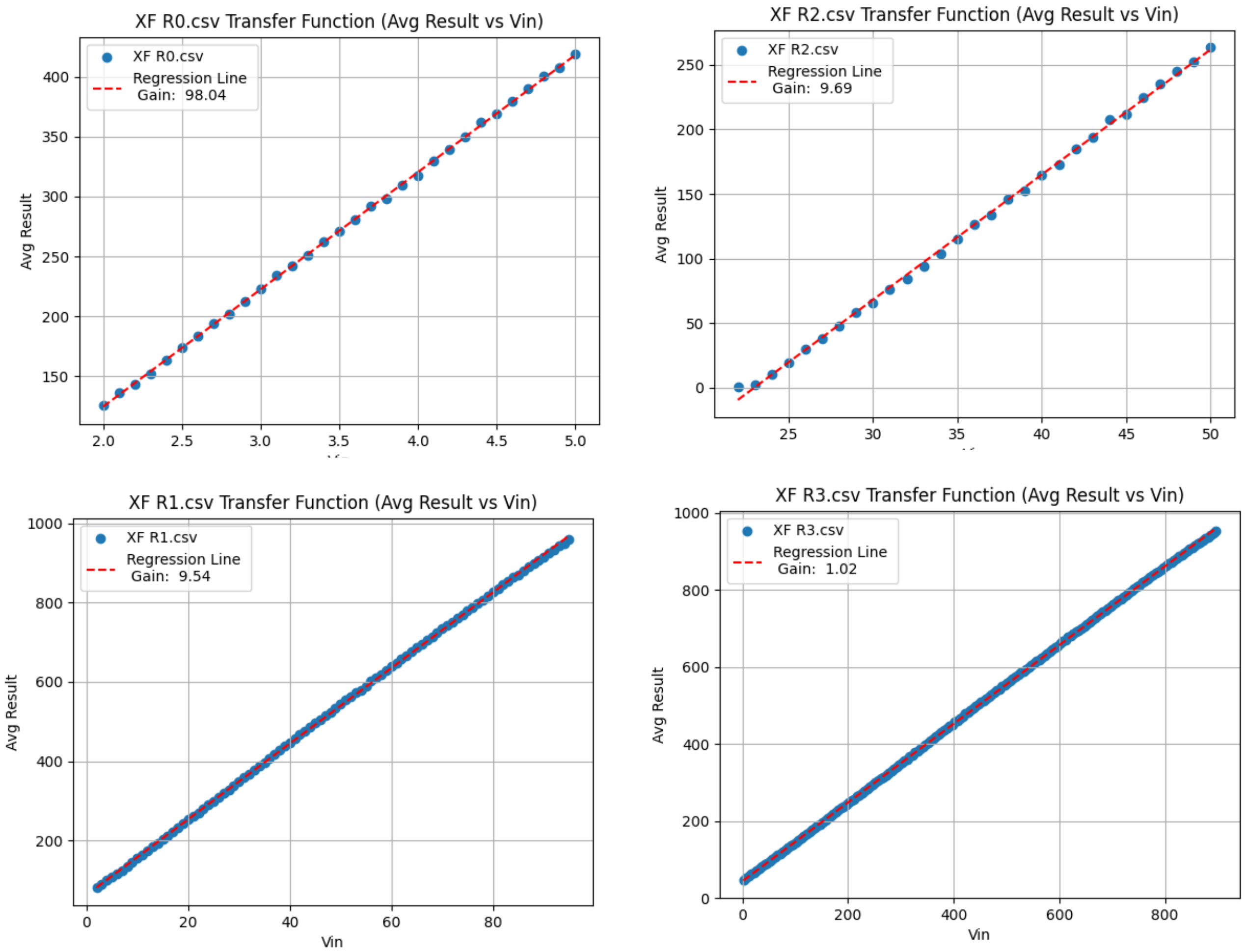


FoM: Gain

R	Design	Meas (Warm)	Meas (100K)
0	100	98.04	96.00
1	10	9.54	9.88
2	10	9.69	10.05
3	1	1.02	1.03

- Within expected variation.

Average Result [Digital Code] vs Vin [mV] per Gain Region



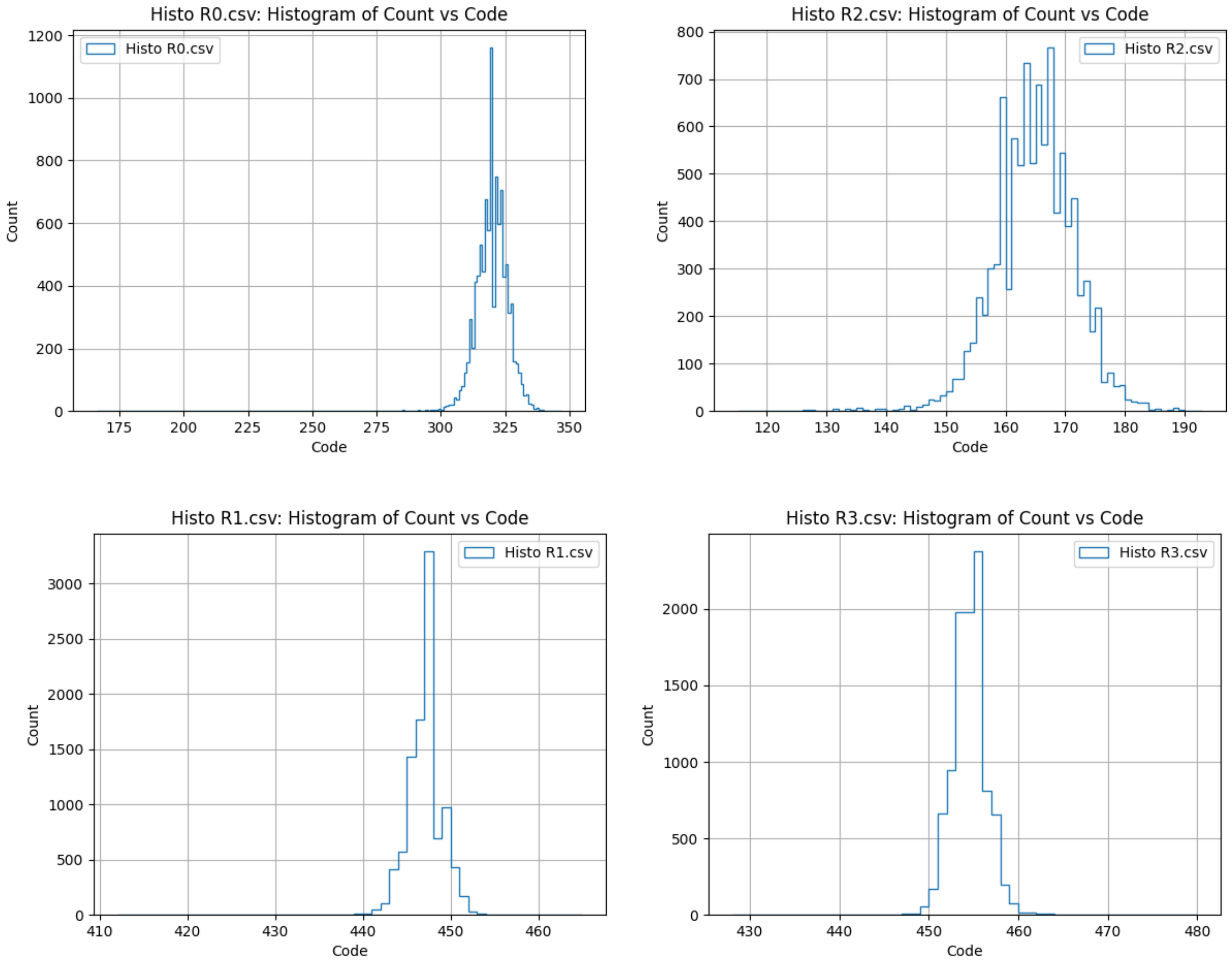
Region 0	Range2=1 (**high gain**) and the input is small, so autorange integrates **10 samples**.
Region 1	Range2=1 (**high gain**) and the input is large, so autorange integrates **1 sample**.
Region 2	Range2=0 (**low gain**) and the input is small, so autorange integrates **10 samples**.
Region 3	Range2=0 (**low gain**) and the input is large, so autorange integrates **1 sample**.

FoM: Noise (rms, input-referred)

R	Design	Meas (Warm)	Meas (Cryo)
0	20 uV	63.2 uV (6.2 codes)	111 uV (10.75 codes)
1	--	216 uV (2.07 codes)	990 uV (9.78 codes)
2	--	690 uV (6.69 codes)	1.07 mV (10.71 codes)
3	--	1.98 mV (2.02 codes)	3.71 mV (3.82 codes)

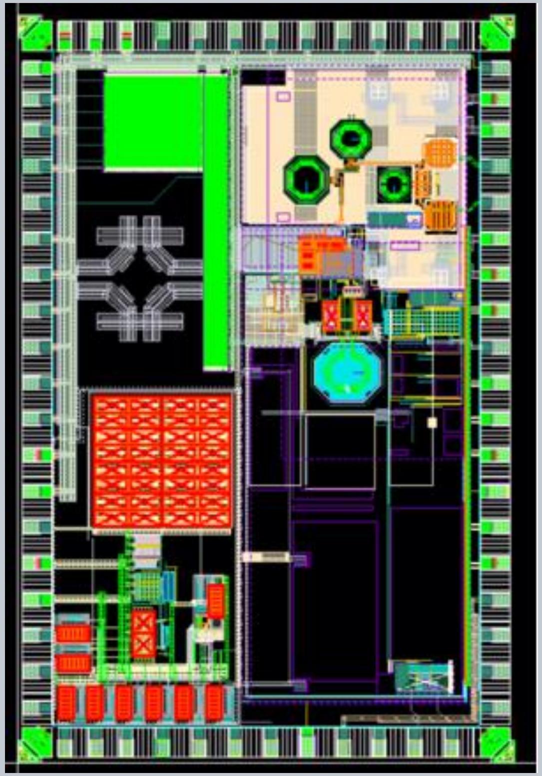
- 10-sample modes (R0 and R2) show the expected $\sqrt{N}$ improvement in noise.
- R0 value >3x off from design spec.
- Some reason to believe there are errors due to Arbitrary Waveform Generator or test pixel parasitics.

Histogram of Results [Digital Code] vs Vin [mV] per Gain Region

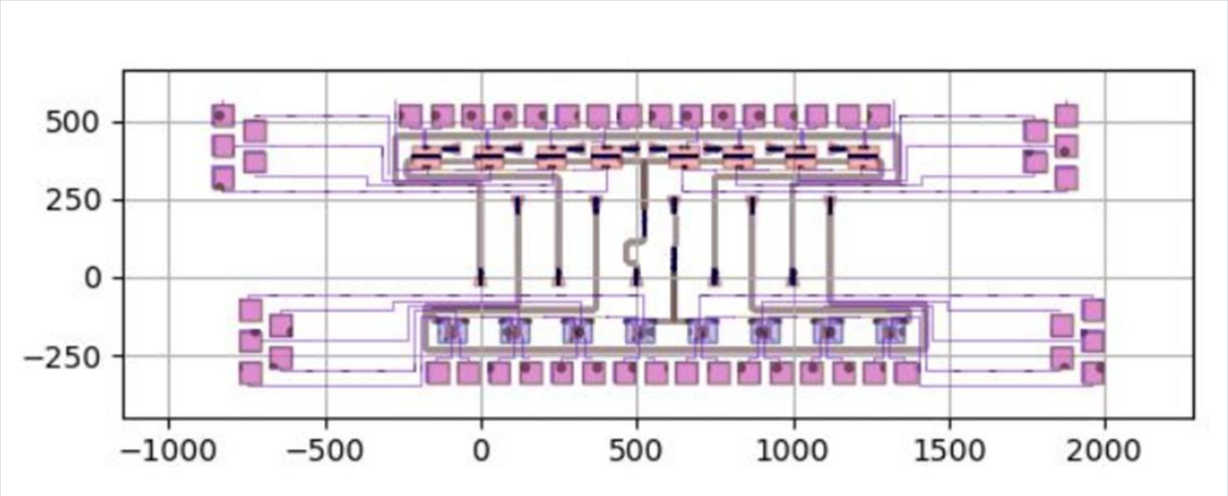


SPROCKET By the Numbers

	SP1	SP2	SP3A	SP3	SP3-FR
Tapeout	Sep 2022	Dec 2022	May 2023	Nov 2023	Early 2026 (TBD)
ASIC Dimensions	5 x 3 mm	5 x 3 mm	2 x 3 mm	24 x 5 mm	~ 21 x 28 mm
ADC Pixels	32 x 64 = 2,048	32 x 64 = 2,048	N/A	64 x 320 = 20,480	320 x 384 = 122,880
Equivalent CIS Pixels (1:16)	128 x 256 = 32,768	128 x 256 = 32,768	N/A	256 x 1,280 = 327,680	1,280 x 1,536 = 1.97 M
Data Volume	2 GB / s	2 GB / s	N/A	13.6 GB / s	~ 80 GB / s
Readout Strategy	LVDS	LVDS	10.24 Gb/s Optical	1 x 20.48 Gb/s SiPh Link	5 x 20.48 Gb/s SiPh Links



Collaboration
Fermilab: ASIC transmitter (some IP from CERN lpGBT); System assembly and Testing
University of Washington: Photonic Integrated Circuit (PIC) Design
TSMC 65 nm ; AMF Photonics

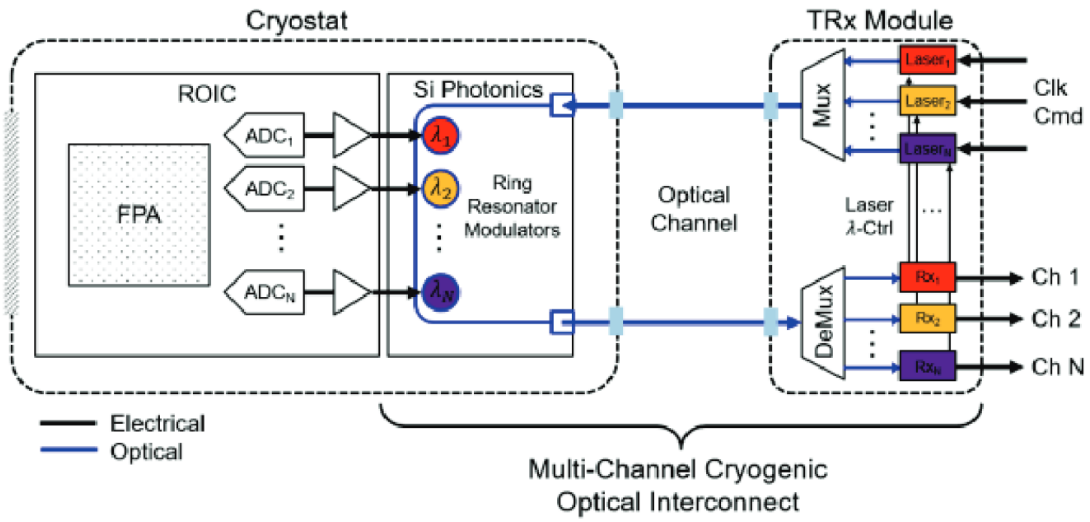


SparkDream
Scaling Bandwidth through Integrated Silicon Photonics

The SParkDream Project

High bandwidth links for data transfer

- SiPh is a must-have technology for future detectors:
- **100x** bandwidth, **100~1000x** lower heat load, **10~100x** channel density, EMI/crosstalk immunity



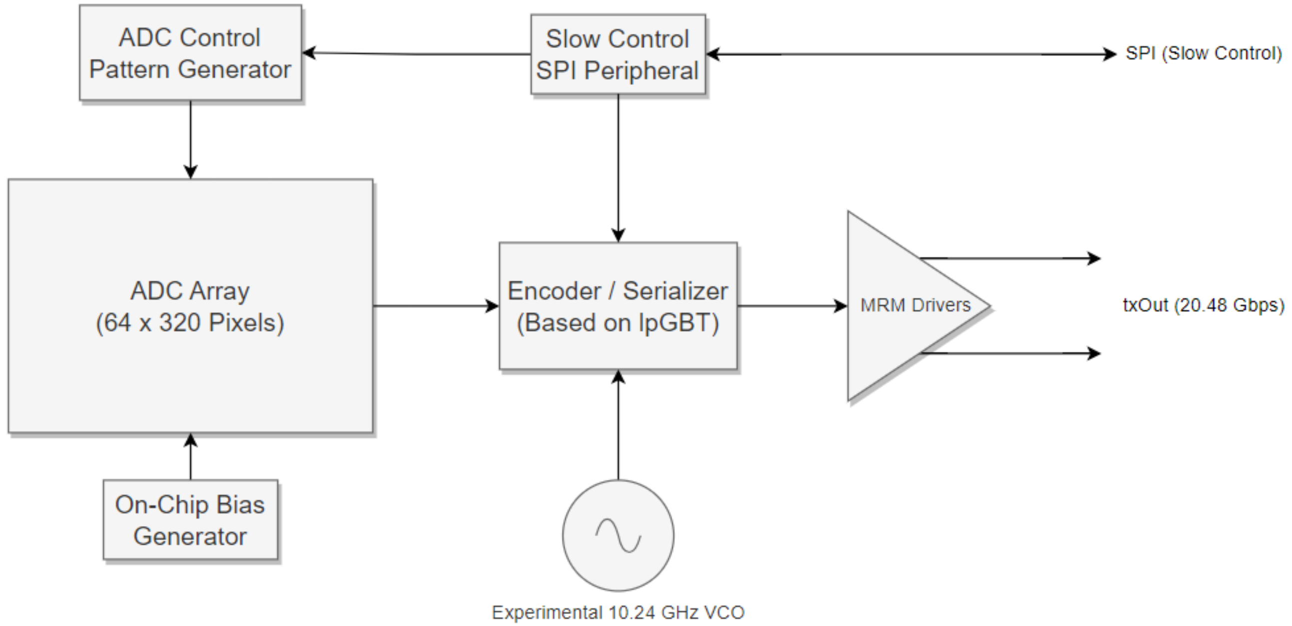
Key Milestones / Scope:

- Single-Channel SiPh Link
- Multi-Channel (Wavelength Division Multiplexed) SiPh Link
- Single/Multi-Channel SiPh Link at 100 K
- *Reach Goal:*
  - Fermilab PIC with performance to 4 K (AMF Photonics)
  - Co-integrated electronics and Photonics (GF 45 SP CLO)

SParkDream: The PIC (Micro-Ring Modulators)

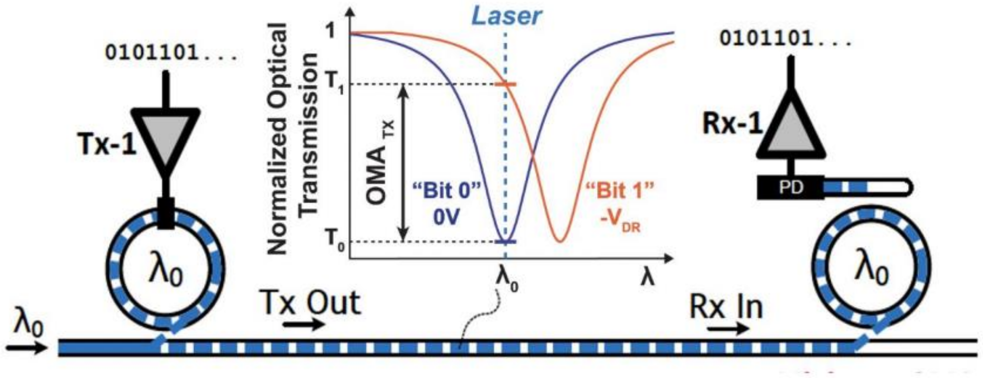
The Potential:

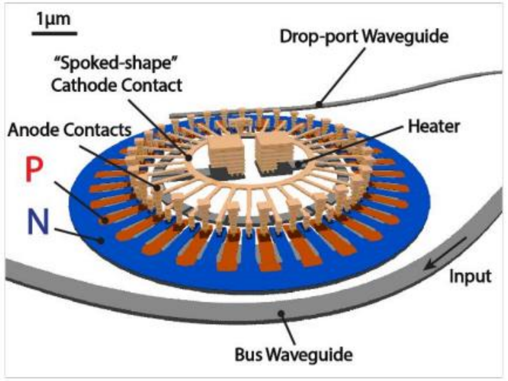
- Extremely high bandwidth through WDM
- Low power (signaling mirror analogy)



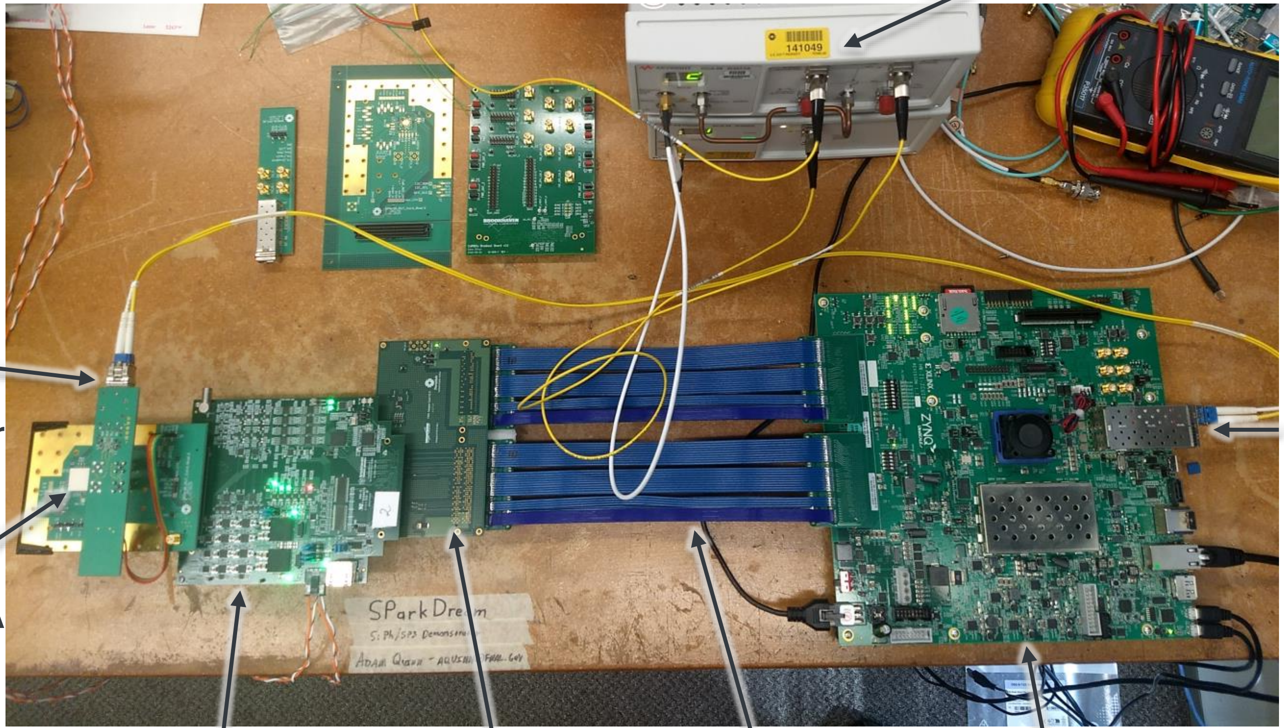
The Challenges:

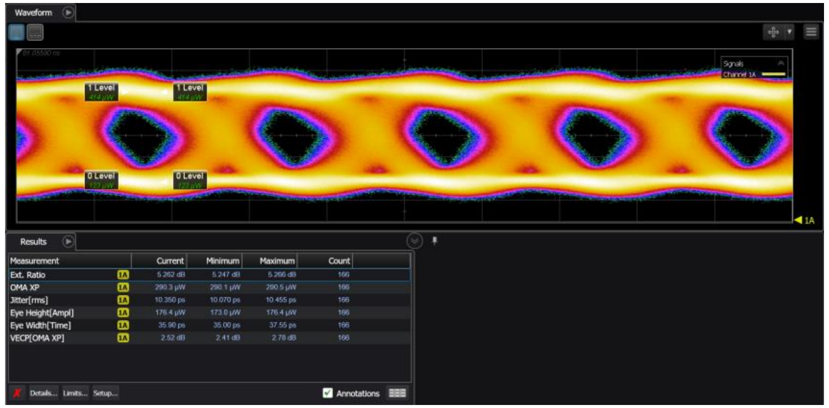
- Improving cryogenic bandwidth
- Tuning cryogenic MRMs
- **Electronic/Photonic Co-design**



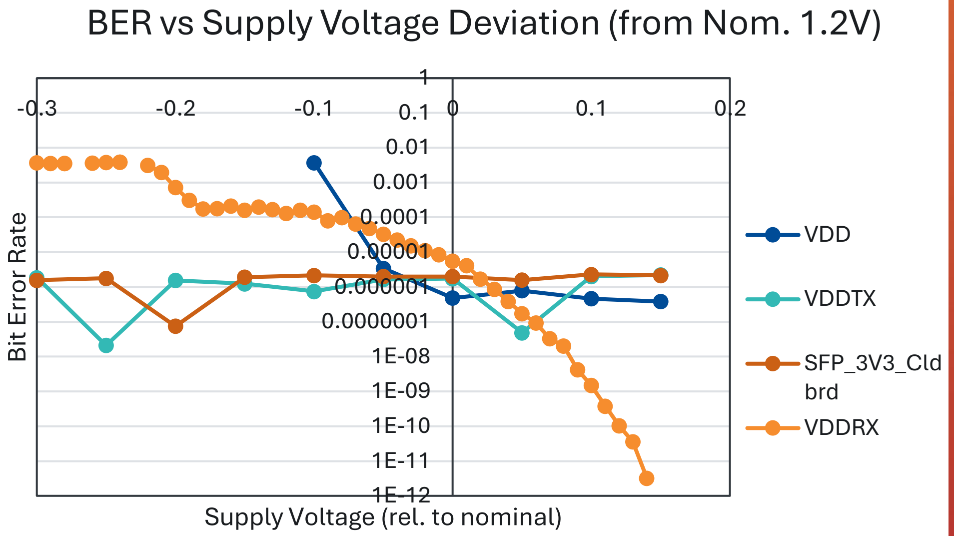


FY25: Discrete Optics Demo ("SParkDream v0")





SFP+ Optical Receiver



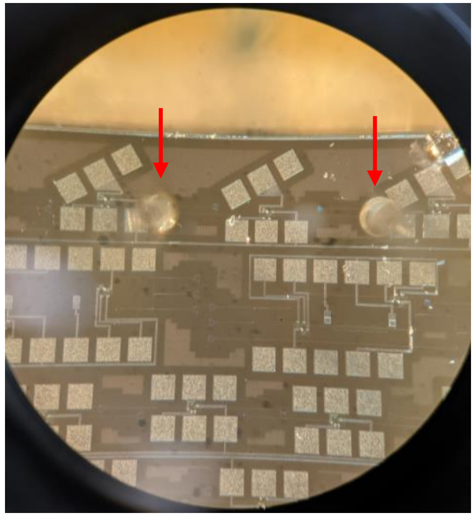
- **Goal:** Use discrete optics to prototype a readout chain for 10.24 Gbps data stream.
  - First time a custom optical readout system has been built in our lab.
- **Difference vs ultimate SParkDream objective:** Integrated vs discrete; orders of magnitude of power.

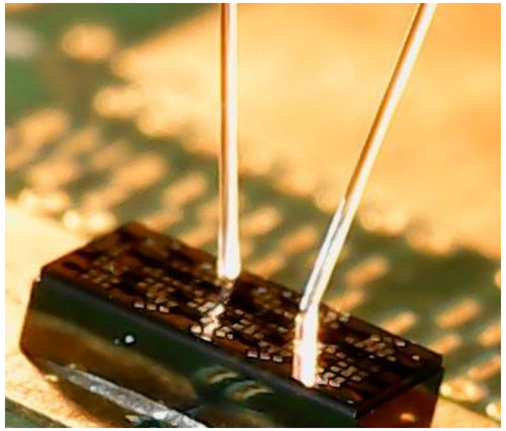
Results: Link fully functional.

Demonstrated BER << 3.2×10^{-15}

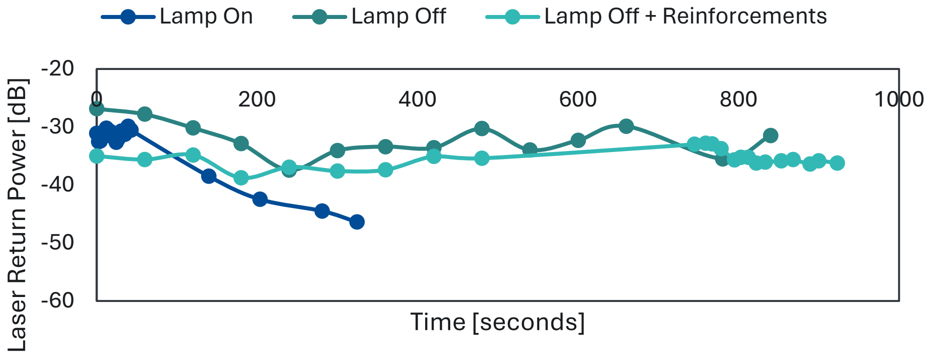
FY25: Silicon Photonics Development

- Using UW-PIC1 chip, built an optical loopback demonstrator.
- Prototyped micro-positioners and demonstrated successful alignment to photonic IC grating couplers.
- Stripped, cleaned, and aligned fibers → Observed light!

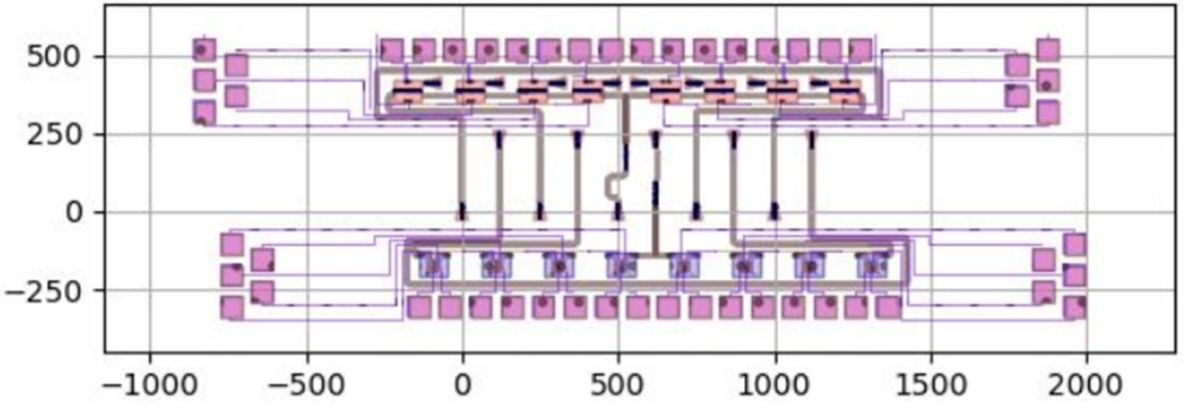




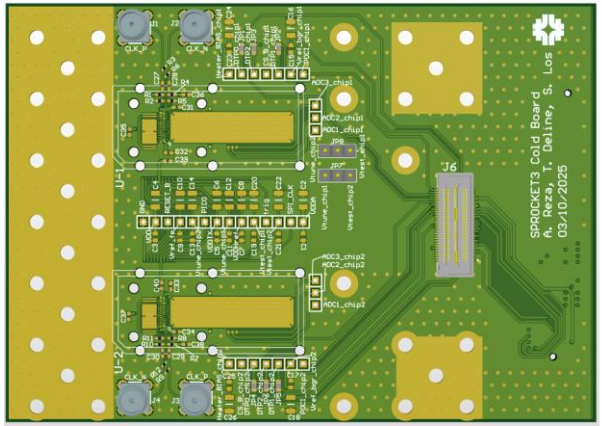
Laser Return Power Drift Over Time [dB vs sec]



- U. Washington completed design and taped out UW-PIC2, which is designed for higher performance + more robust integration.



- We designed PCBs and procured test stand equipment to enable a full-scale demonstrator with this chip.



Next Steps in technology maturation

Next Steps

Skipper-in-CMOS

- Complete testing all split options (High throughput test setup and data evaluation complete)
- Backside Illumination prototype
- Full reticule Sensor fabrication

Readout Electronics

- Test SPROCKET 3 – (next few months)
- Design and fabricate SPROCKET 3 FR (full reticule)

Photonics Integrated Circuit

- Test PIC2 (Expected in Aug)

System

Integrate and test the module

  - Bump bonding and 3D hybrid bonding planned for sensor + electronics;
  - Wire bonding and 2.5D interposer options will be explored for photonic integration

Project Team

Skipper-in-CMOS

- Claudio R. Chavez Blanco,
- Agustin J. Lapi,
- Miguel Sofo-Haro (CNEA),
- Benjamin C. Parpillon,
- Adi Birman (Tower),
- Guillermo Fernandez-Moroni,
- Lorenzo Rota (SLAC),
- Fabricio Alcalde Bessia (CNEA),
- Aseem Gupta (SLAC),
- Fernando Chierchie,
- Julie Segal (SLAC),
- Christopher J. Kenney (SLAC),
- Angelo Dragone (SLAC),
- Shaorui Li,
- Amos Fenigstein (Tower),
- Juan Estrada,
- Farah Fahim,
- Davide Braga

SPROCKET

- Adam Quinn;
- Manuel B. Valentin (NU),
- Thomas Zimmerman,
- Davide Braga,
- Seda Memik (NU),
- Farah Fahim

SparkDream

- Adam Quinn
- Xiaoran Wang,
- Alan Prosser,
- Sajjad Moazeni (UW)

SLAC NATIONAL ACCELERATOR LABORATORY

CNEA

Tower Semiconductor

NORTHWESTERN UNIVERSITY

UNIVERSITY of WASHINGTON

Fermilab is hiring!

Senior & Junior Analog ASIC design engineer positions are available