SRS Scalable Readout System

concepts and status

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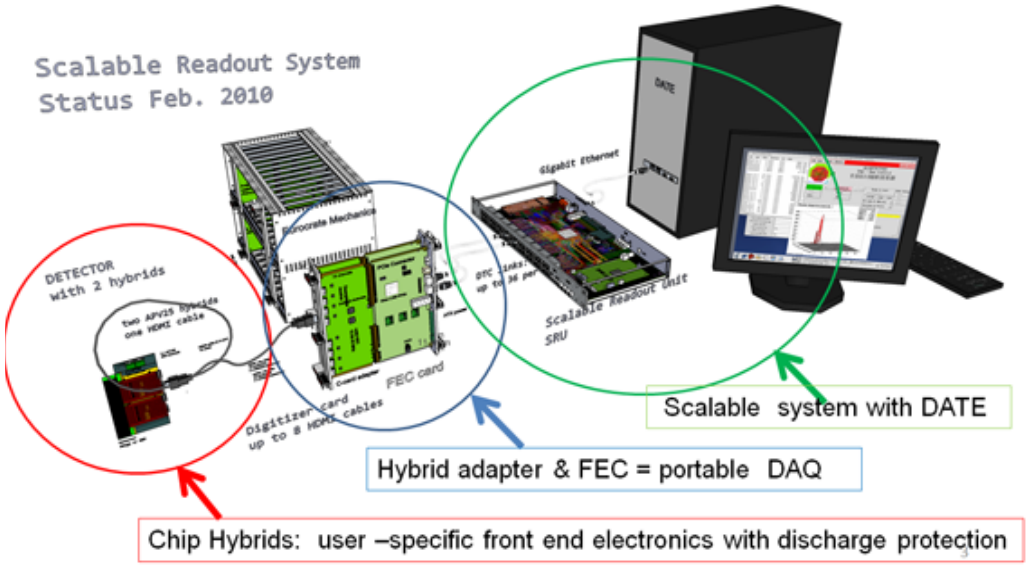
more details on SRS frontend and chip-link
=> see presentation by
S. Martoiu DT-TP

ITS Miniweek meeting, June 12, 2011

What is SRS

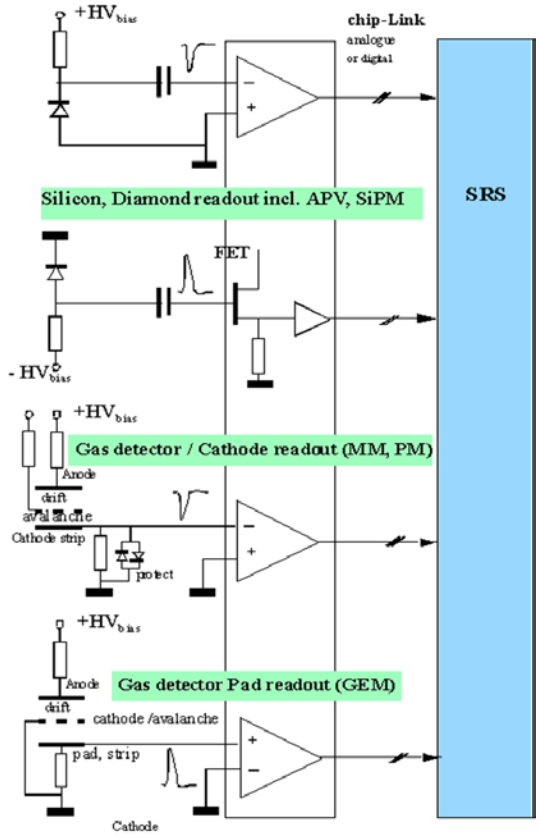
Proposed by RD51* in 2009 as a scalable readout architecture, SRS has a general-purpose chip link interface for a common, portable readout backend allowing to connect a variety of frontend chips connected to the same readout backend. Today SRS is reality for ATLAS, ALICE, CMS upgrades and proposed MPGD applications (homeland security, water quality, medical etc.).



* http://rd51-public.web.cern.ch/RD51-Public/Welcome.html

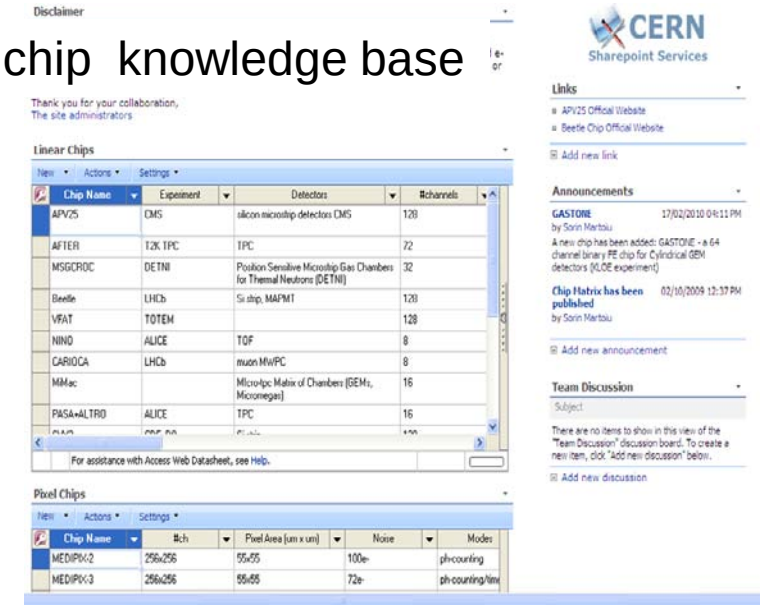
One common R.O. system

for different types of detectors



-> choose the best-suited chip for application
-> connect via a "chip-link" to the SRS backbone
-> chooses preferred Online system
-> eventually become part of developer community

RD51 chip knowledge base

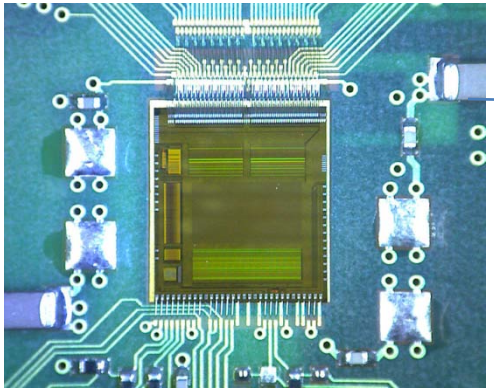


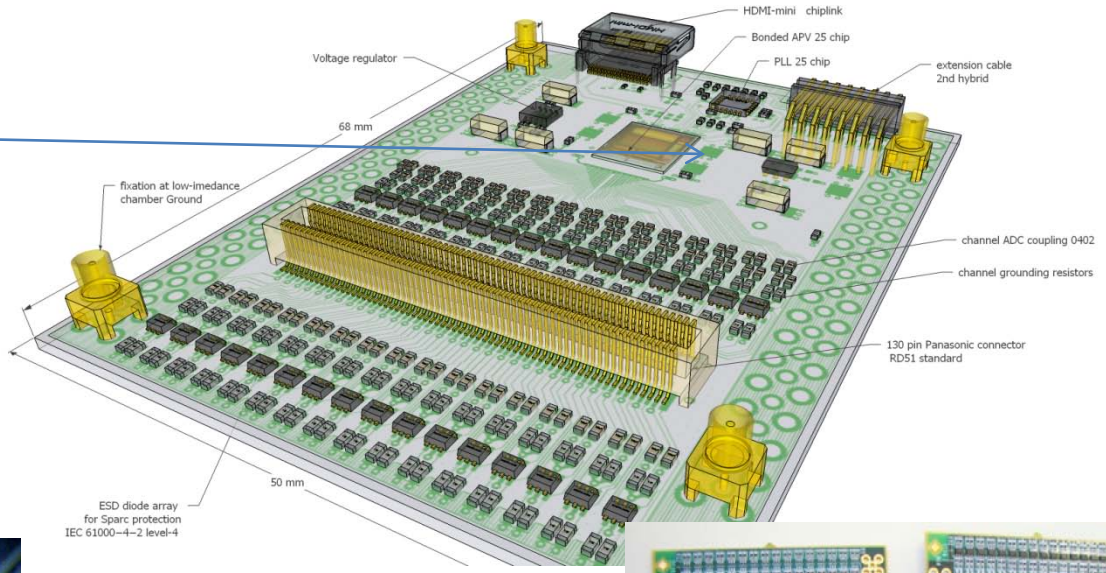
SRS chips on hybrids so far:

- **APV25**, 128 ch. analogue, hybrid in production, 300 already in use
- **Beetle**, 128 ch. analogue / digital,Lo trigger (design started at WIS)
- **VFAT** 128 channels digital (hybrid design started for CMS and Totem)
- **VMM1**, BNL-ATLAS, on-chip ADC, derand.-buffer, 64 ch, trigger (started)

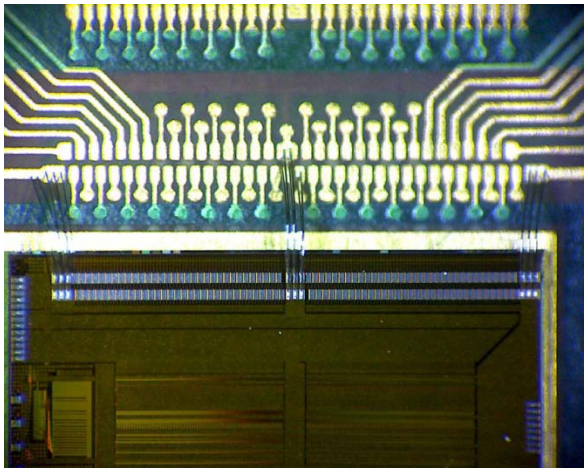
APV-25 hybrid

Photo of wire-bonded APV chip





closeup wire bonding

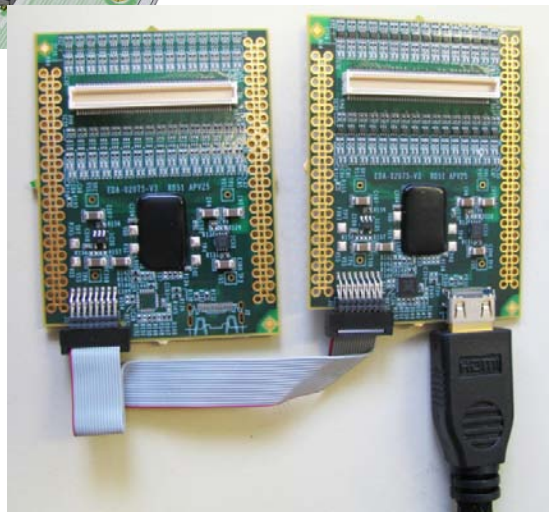


Revision 3:

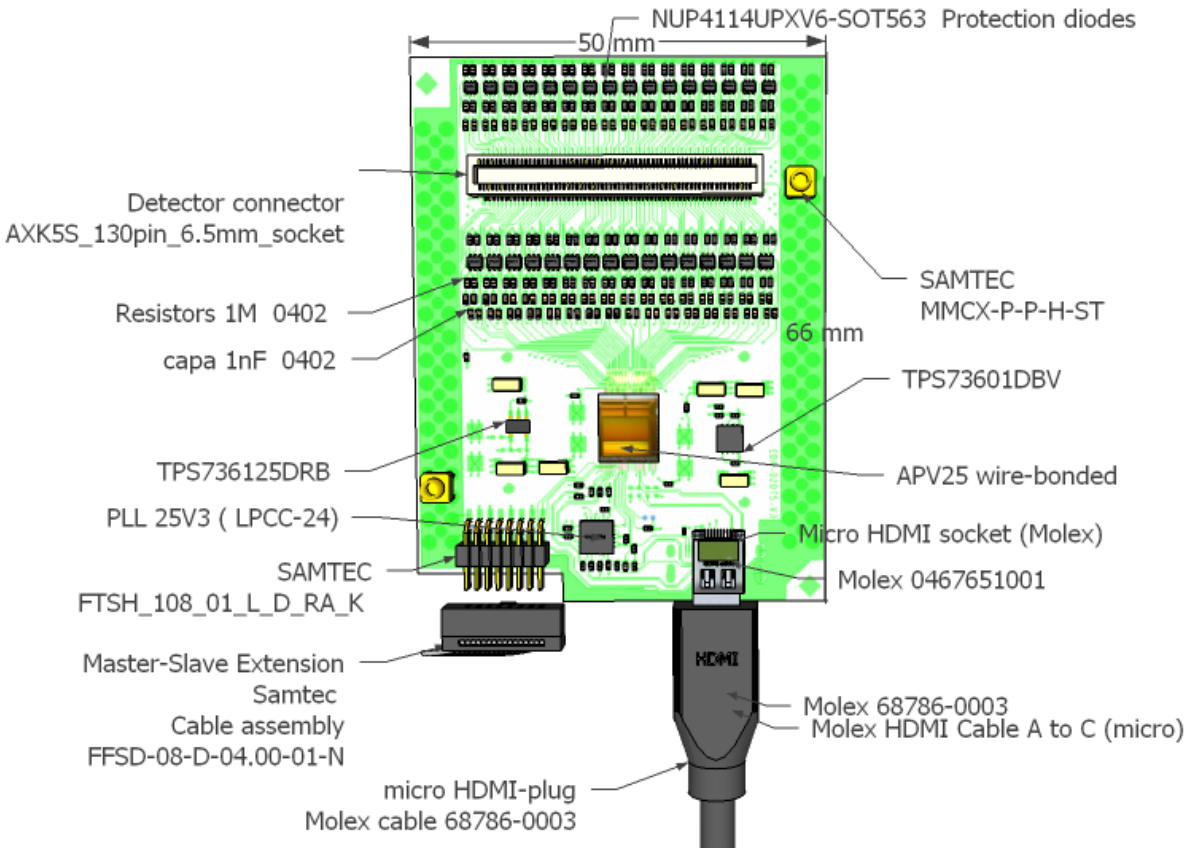
topglobbed hybrids
Slave (L) and Master (R)

Revision 4:

same but
Micro HDMI connector



Final version V4 : APV25



Powered via HMDI cable

SRS formfactor

3U and 6 U Adapters (220 deep)

PCIe connectors used as interface to A B or C cards

-PCIx1: GND, LV Power and HV (optional)
-PCIx8: GND, I2C, 3Gigabit Rx-Tx-Clk, 8 bit diff. Or 16 bit Control
-PCIx16:GND, JTAG chain,3Gigabit Rx-Tx-Clk, 16 bit diff. Or 32 bit Data

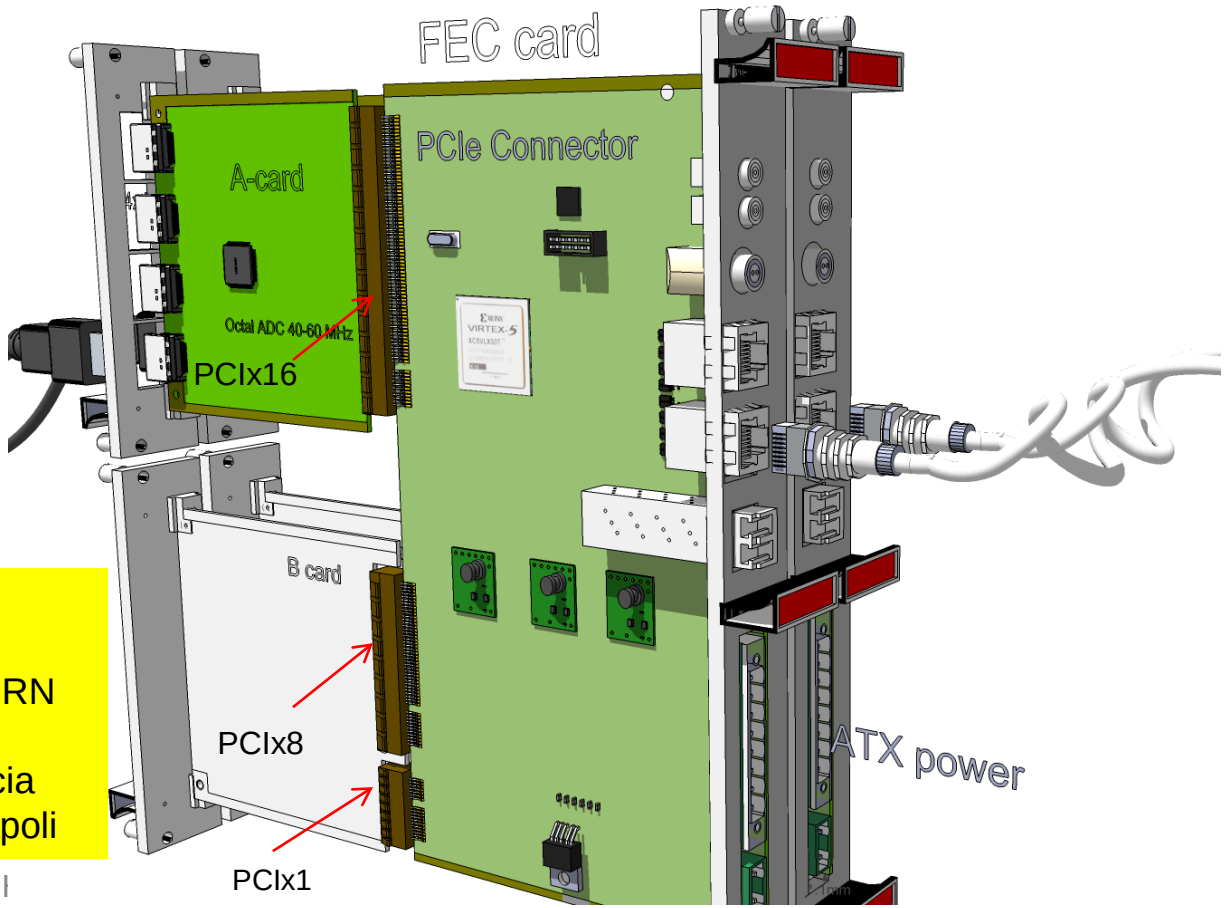
A –Cards: 3U for small detector interface logic

B –Cards: 3 U for miscellaneous extensions and LV-HV control

C – Cards: 6U for detectors

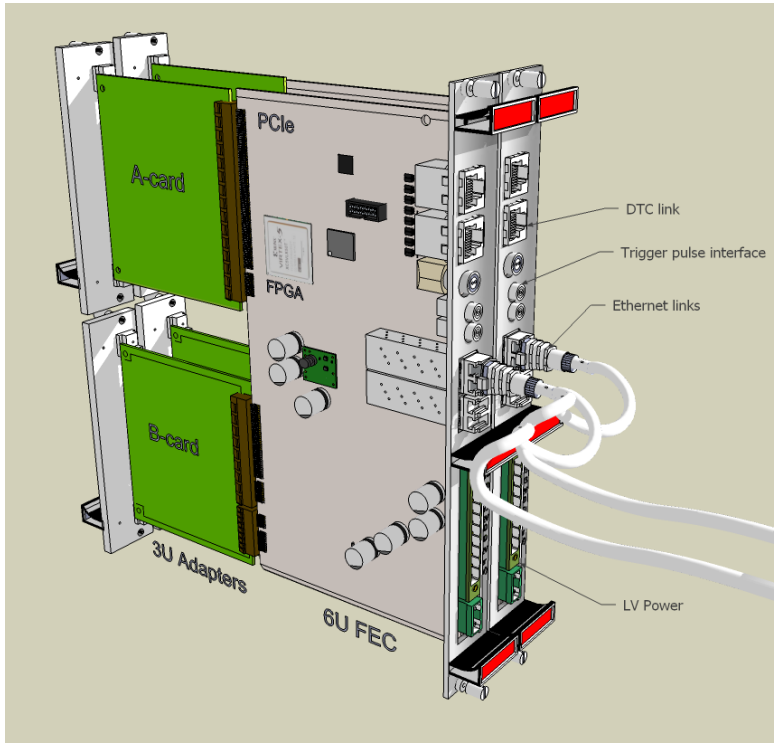
C-cards so far:

- ADC-HDMI adapter, RD51 CERN
- BNL chip adapter Arizona Univ
- LVDS card , NEXT, UVP Valencia
- Clock –Trigger splitter INFN Napoli

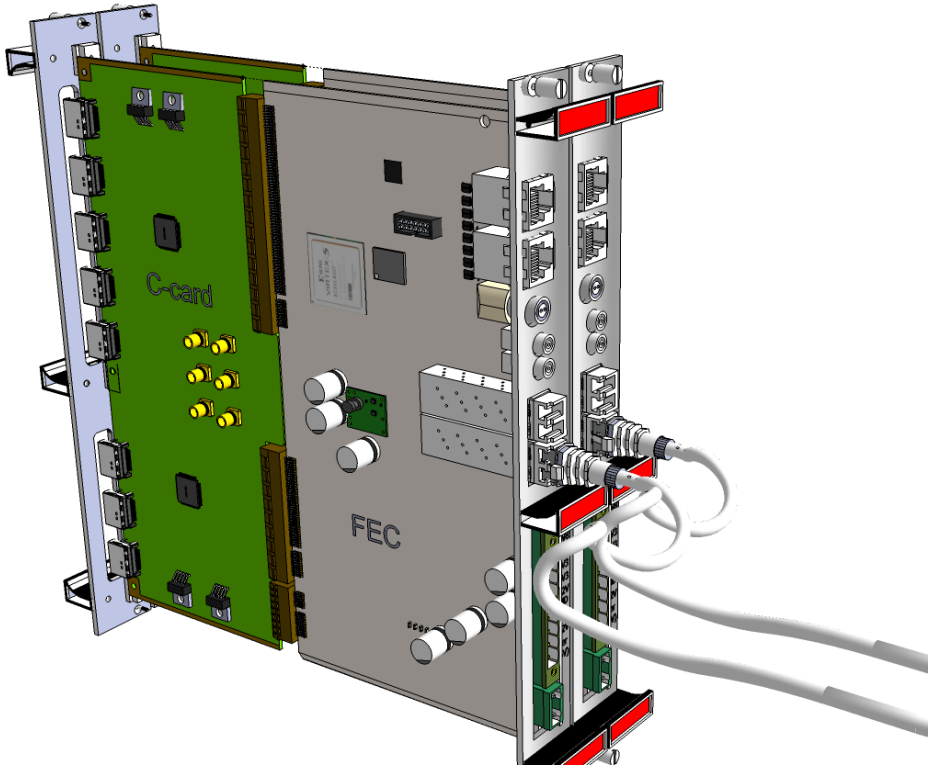


FEC and adapter cards

up to 14 units in 6U x220 Europa Chassis



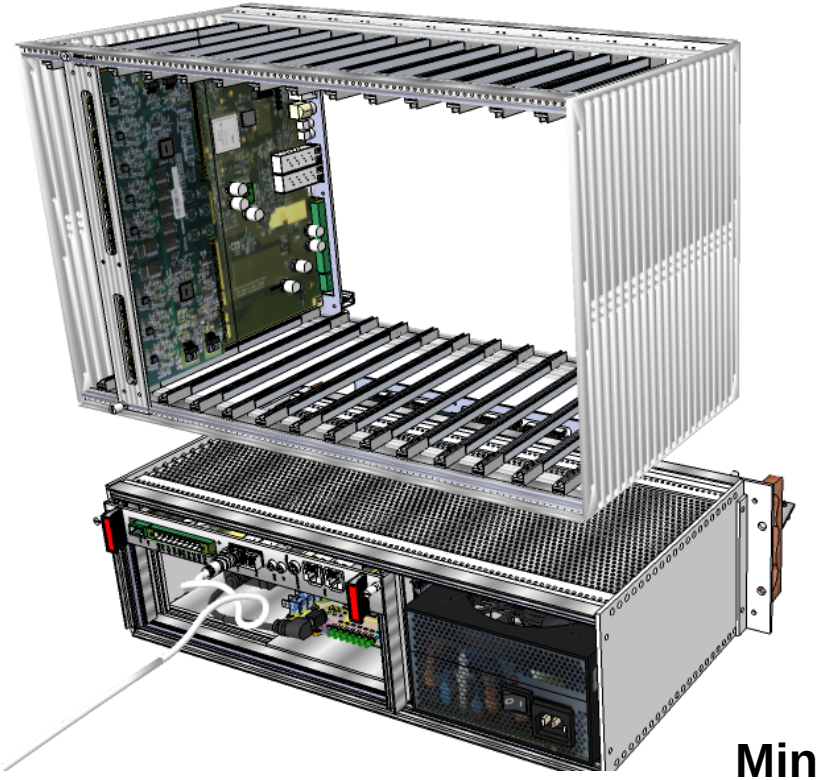
3U adapter cards (A+B)

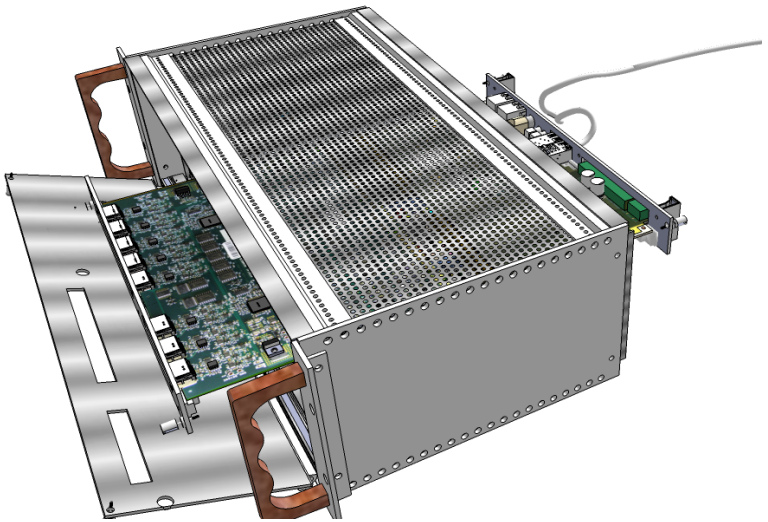


6U adapter cards (C)

Eurocrate vs Minicrate

Eurocrate 6U: up to 14 positions, separate power





Minicrate 3U , max 2 positions, power included

SRS cards

8 x HDMI chip link

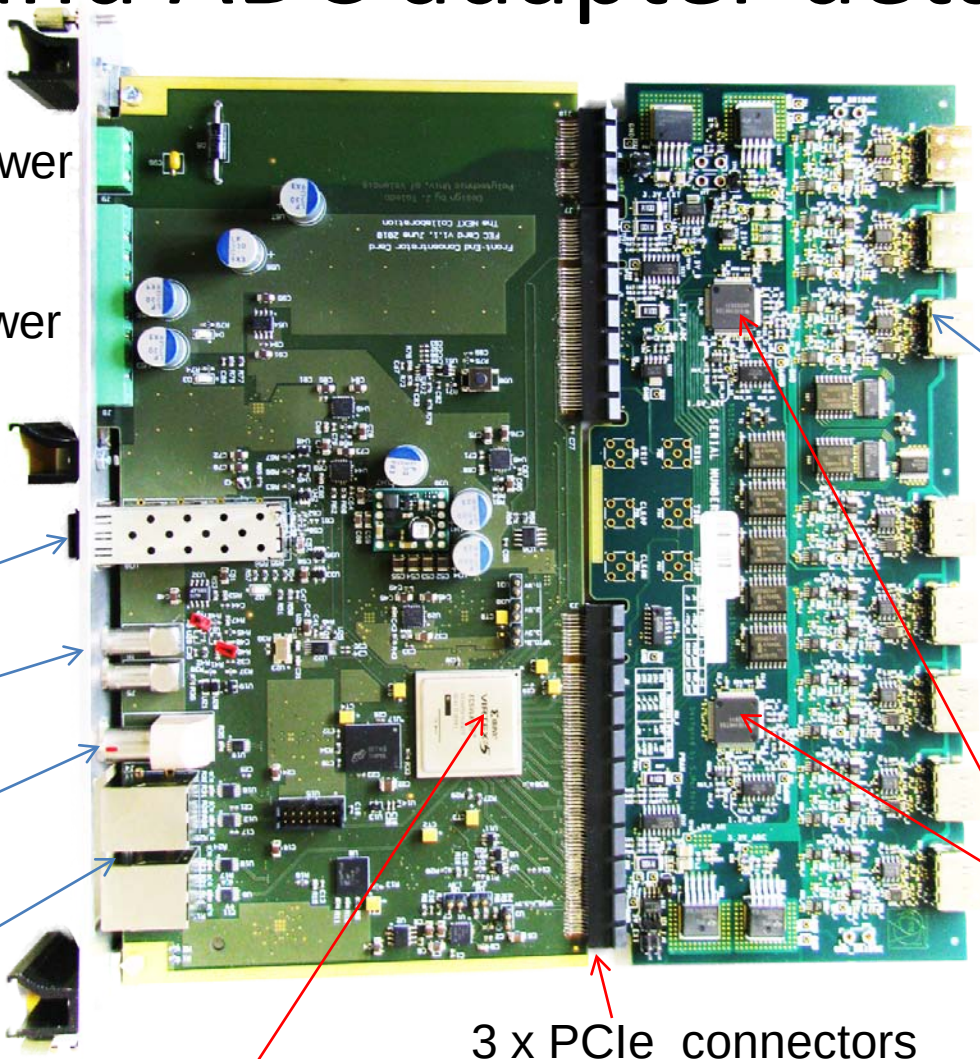
HDMI- ADC adapter V1.1

PCIe connectors

FEC V3

- Power
- Trigger
- DAQ-link
- DTC link
- User I/O
- User Power

FEC and ADC adapter details



FEC card V1.2

ADC card V1.0

HV power

LV power

HDMI chip links
8x

GbEthernet
(2x on new V6)

NIM I/O (Trigger)

LVDS I/O (BUSY)

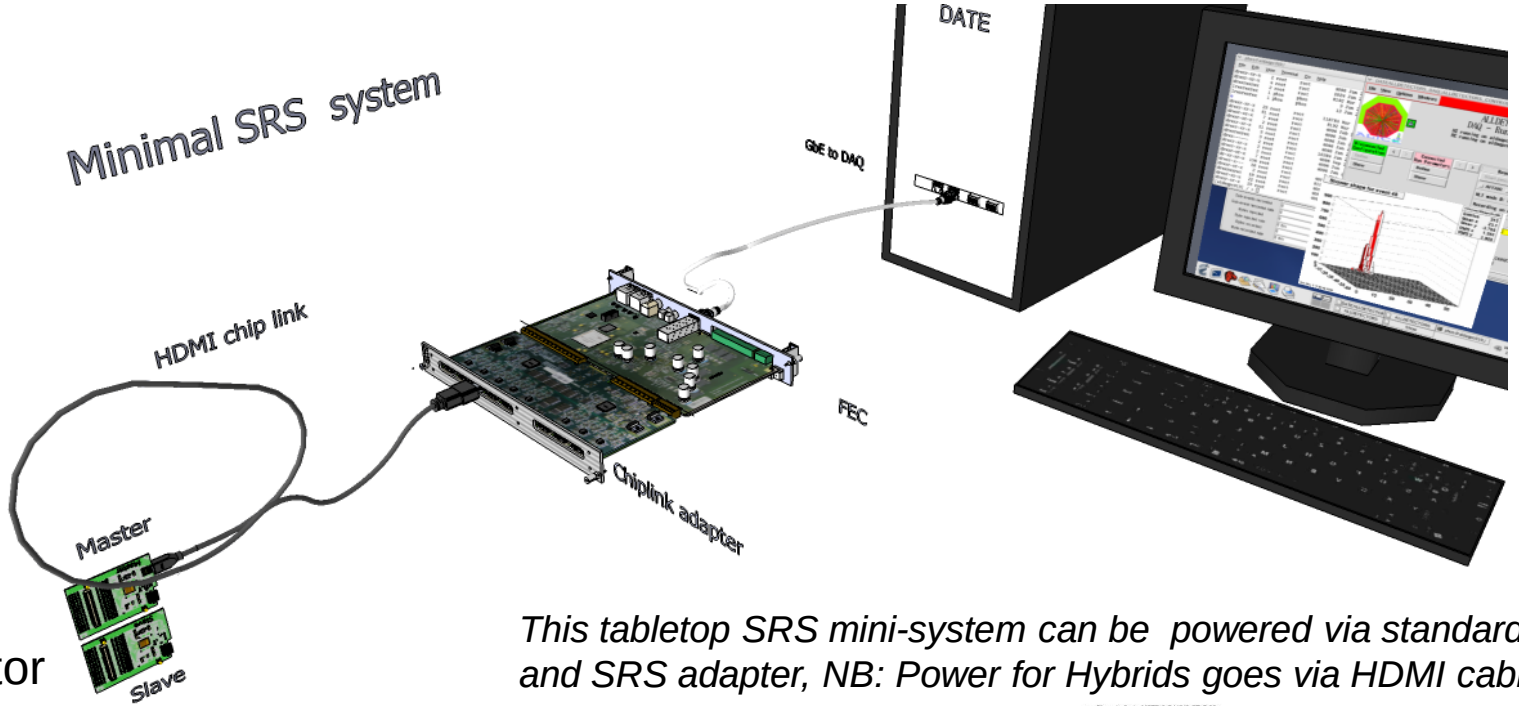
2x RJ45
DTC link to SRU

Octal ADCs
12 bit 40 MHz
(65 MHz in new version)

3 x PCIe connectors

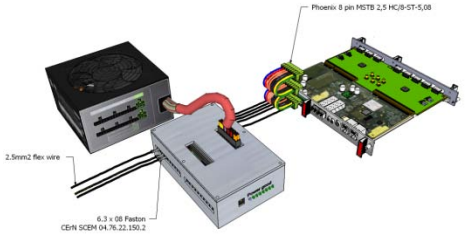
Virtex 5 FPGA (Virtex 6 in new version)

minimal SRS system



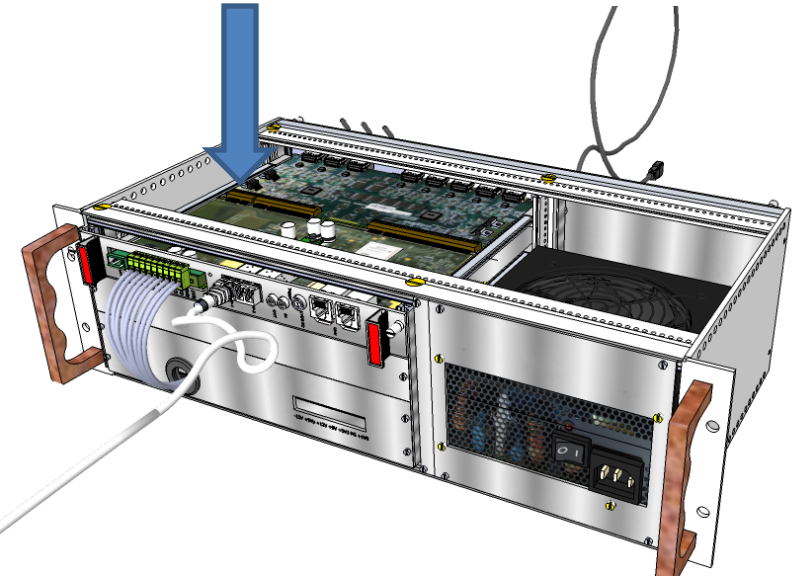
This tabletop SRS mini-system can be powered via standard ATX power and SRS adapter, NB: Power for Hybrids goes via HDMI cables !

Hybrid units of 128 channels



Minicrate

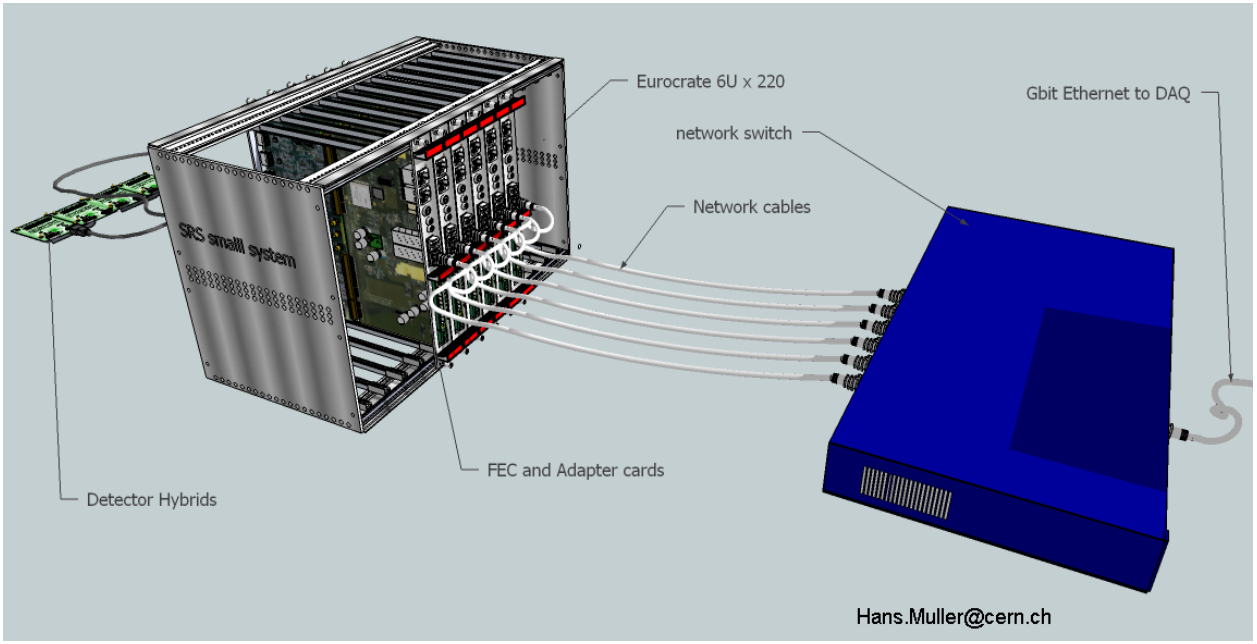
FEC and ADC card



Compact, powered SRS system (5 kg) up to 2 FEC cards (4096 ch)

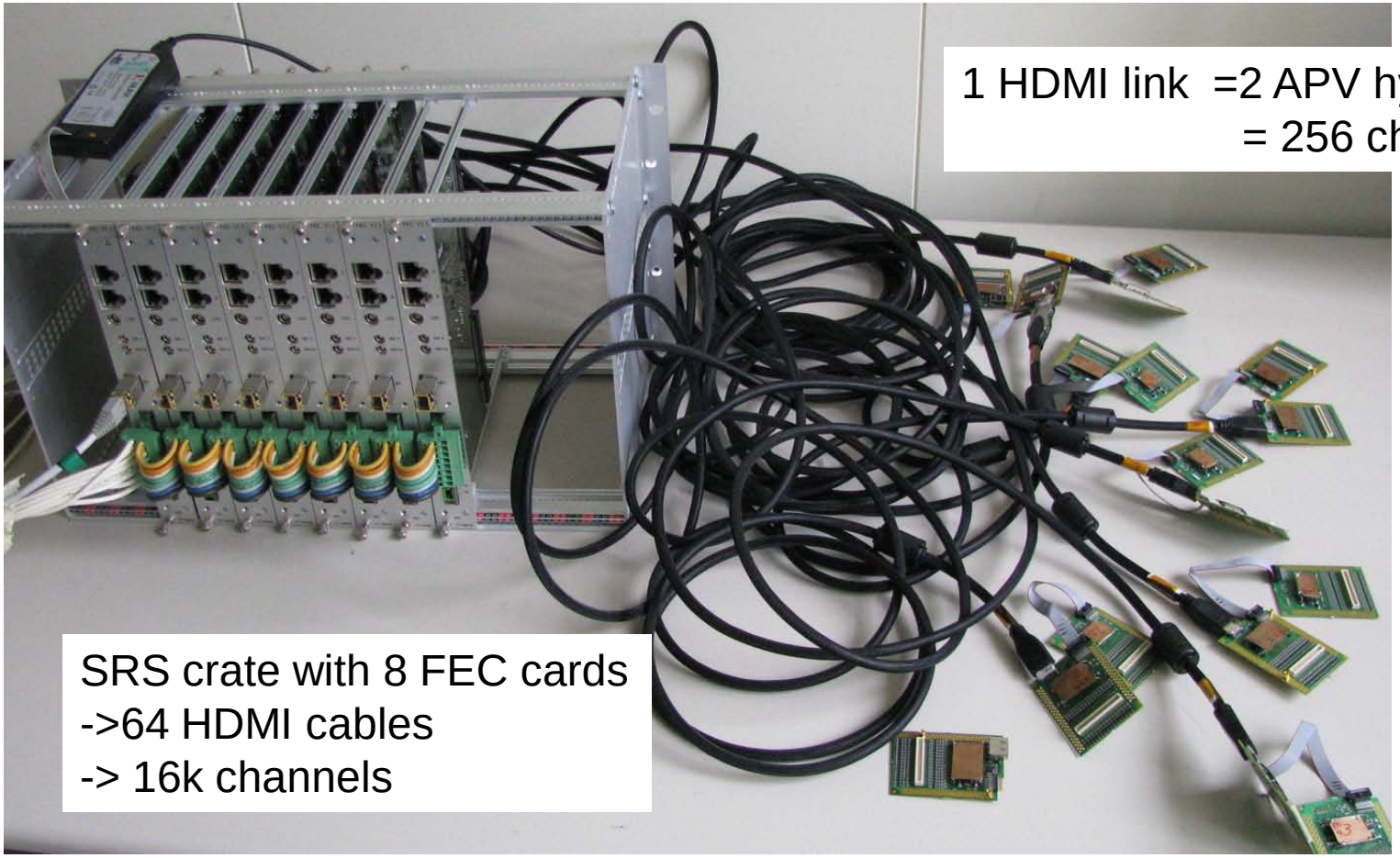
Medium-sized SRS systems

6U x220 crate for up to 14 FEC cards

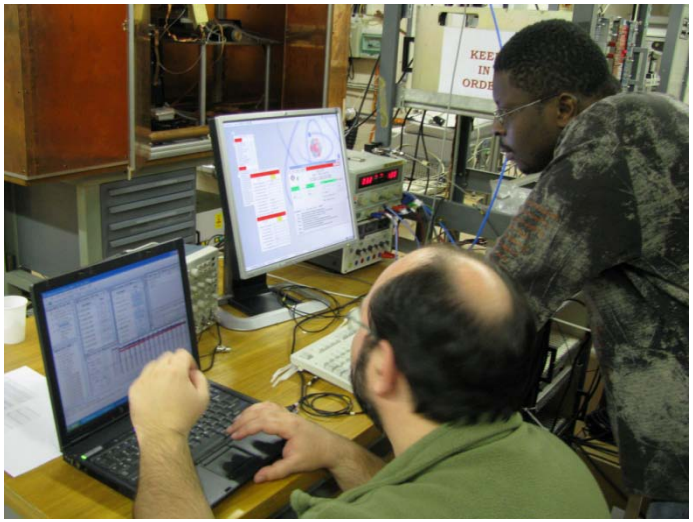


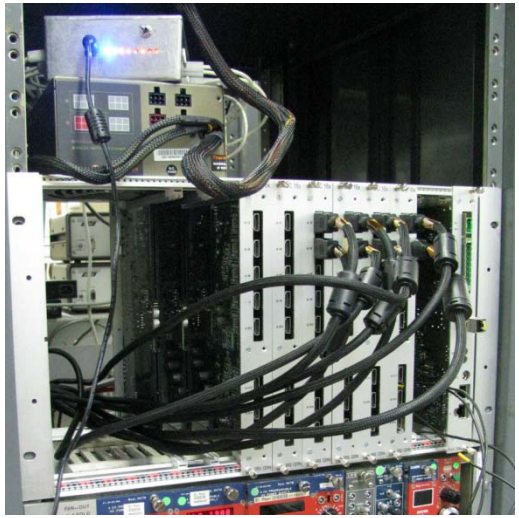
DAQ is connected via a GbE switch

16 k channel crate with HDMI chiplink



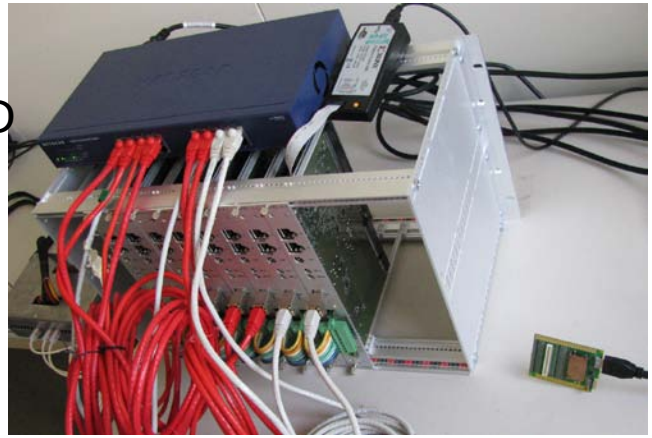
Default SRS Online system: DATE & AMORE





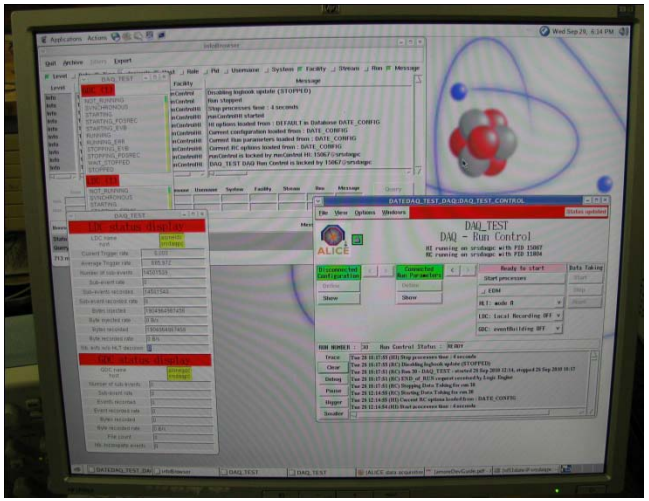
GDD lab
RD51

SRS lab
ALICE AID

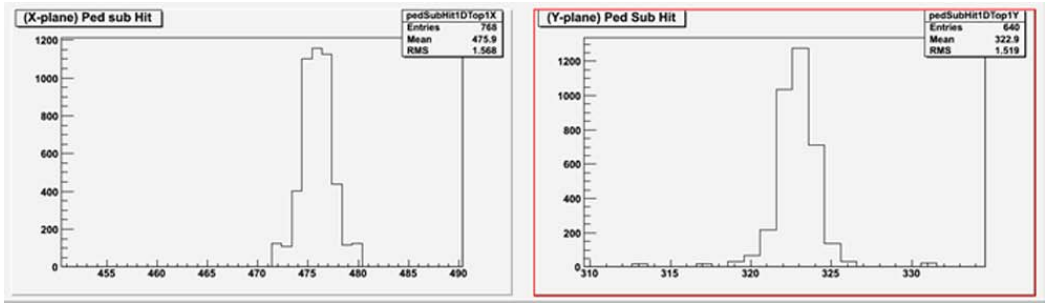


SRS online screens

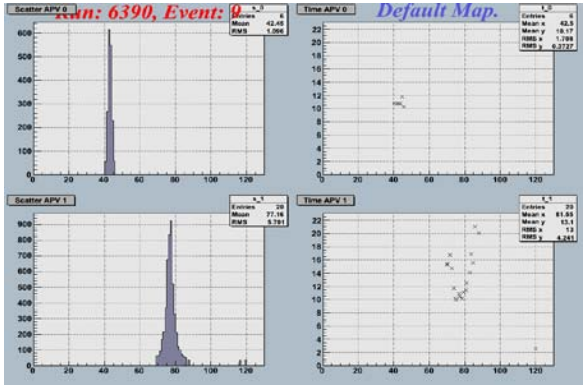
DATE = default Online system



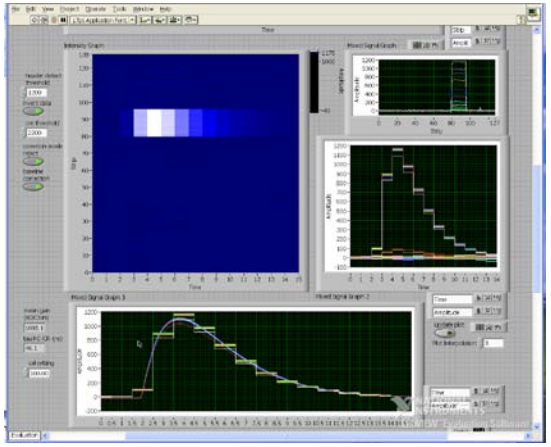
Root & AMORE



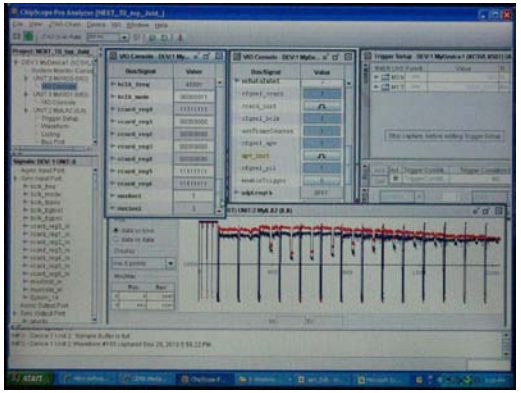
MMDAQ (Atlas MM)



Labview

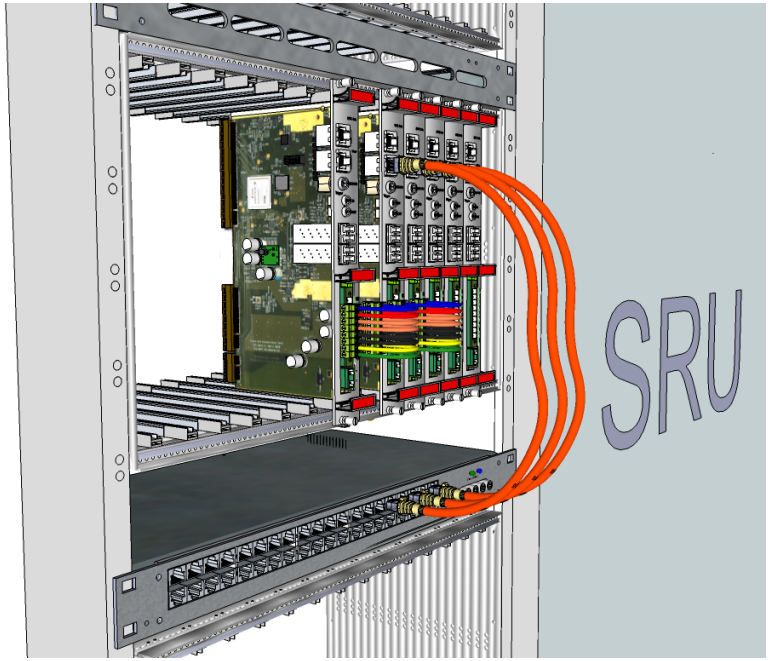


Xilinx ISE chip-scope



Large SRS system

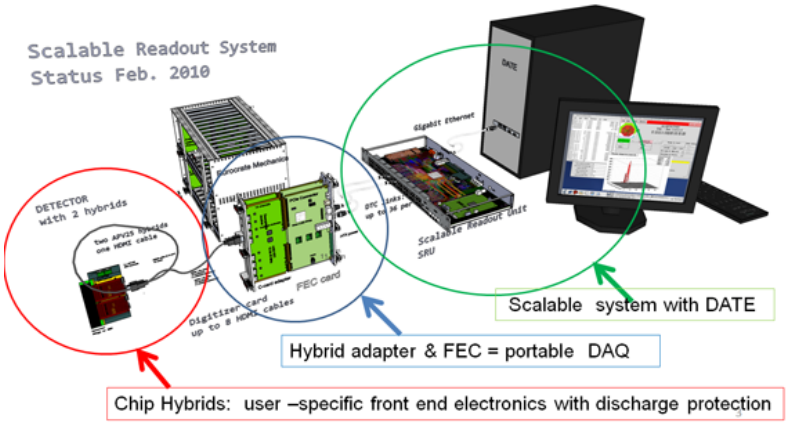
-> SRU-based readout Clusters



1 SRU concentrates event and trigger data from 40 FECs into 10 Gigabit Ethernet link to DAQ

1 SRU: up to 84k channels

physical overview SRS of RD51



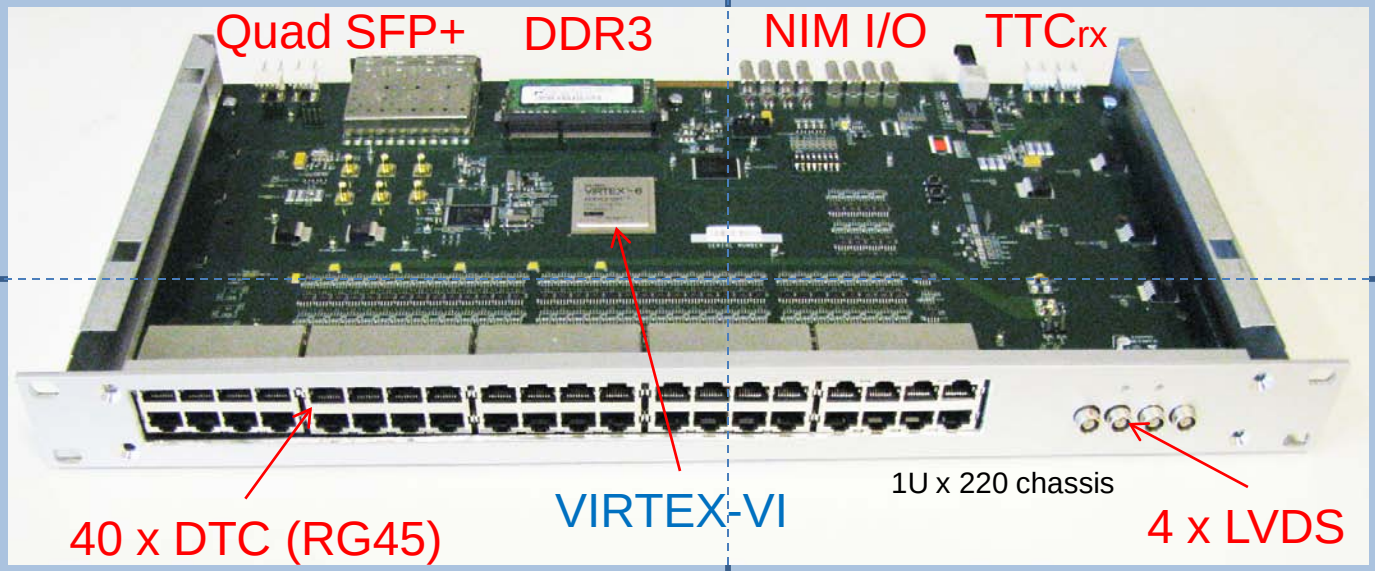
Scalable Readout Unit (SRU)

10 GbE DAQ and DCS link

Event buffer

USER

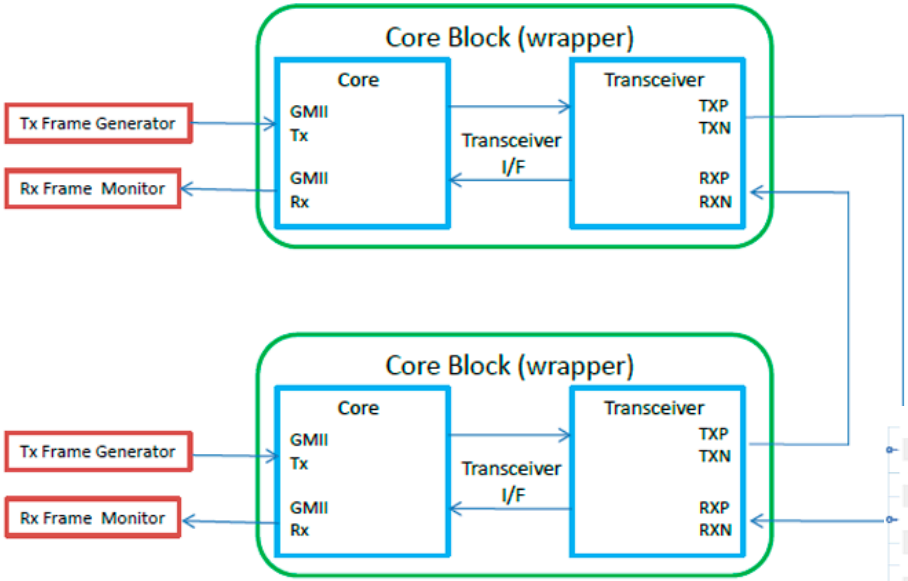
TRIGGER

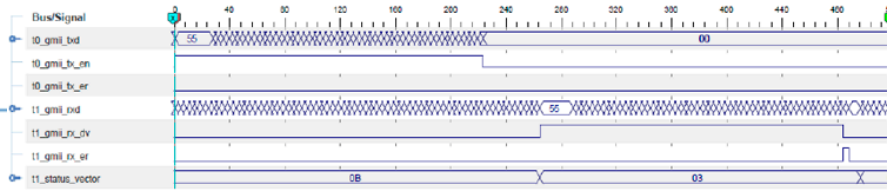


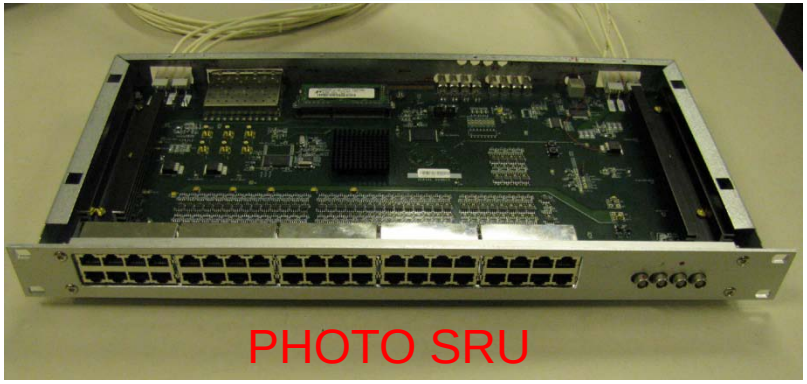
DATA Trigger Control
for 40 FECs

CLOCK & BUSY

SFP+ link on SRU







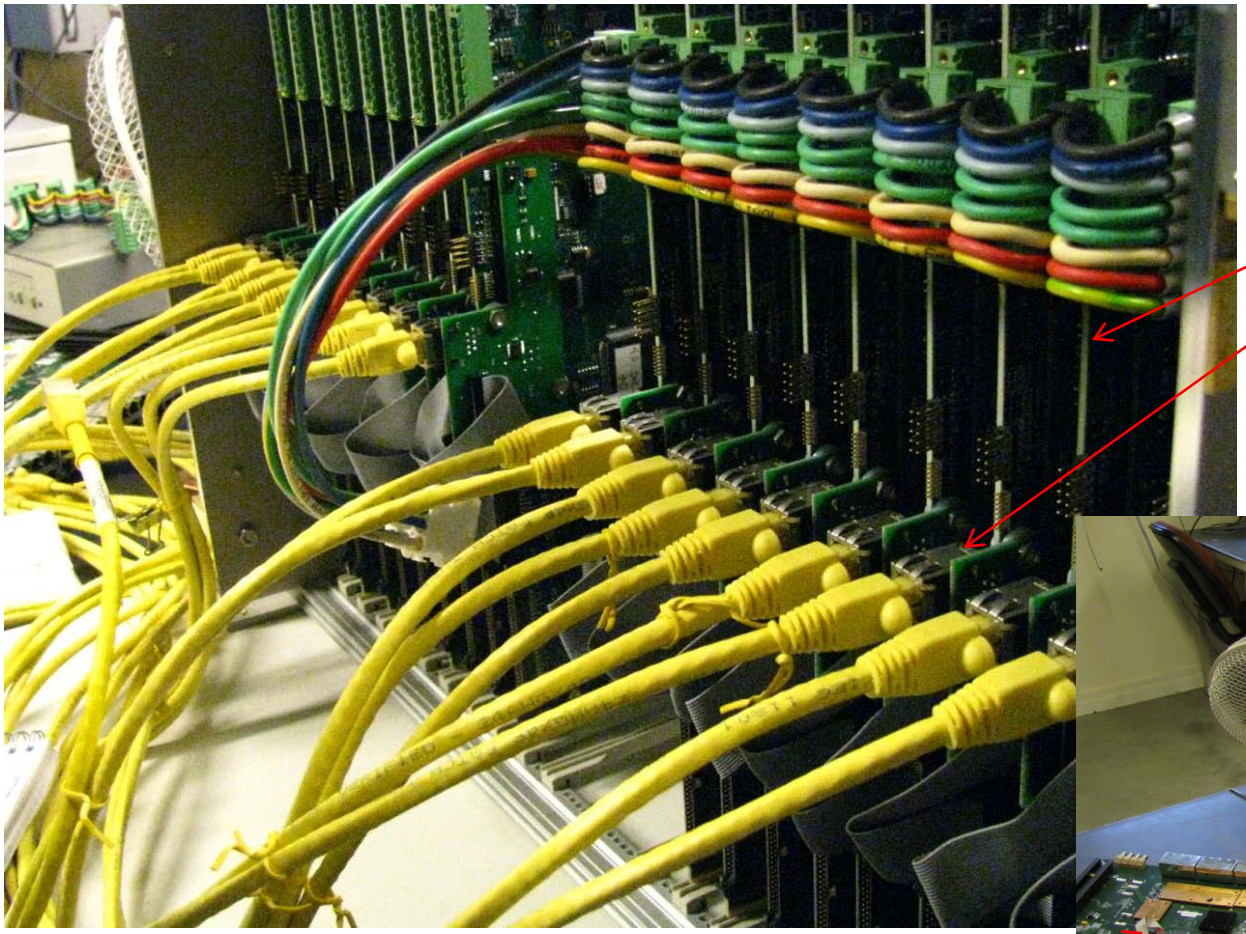
SFP+ hardware on SRU works!

- t0_gmii_txd is the data send out the transceiver T0 (one SFP+ transceiver)
- t1_gmii_rxd is the data received by the transceiver T1 (another SFP+ transceiver)
- T0 and T1 is connected via a direct SFP+ cable.
- There is some transmission delay between T0 and T1.

EMCal ALICE

ALTRO bus readout replaced via “DTC links*” to SRU

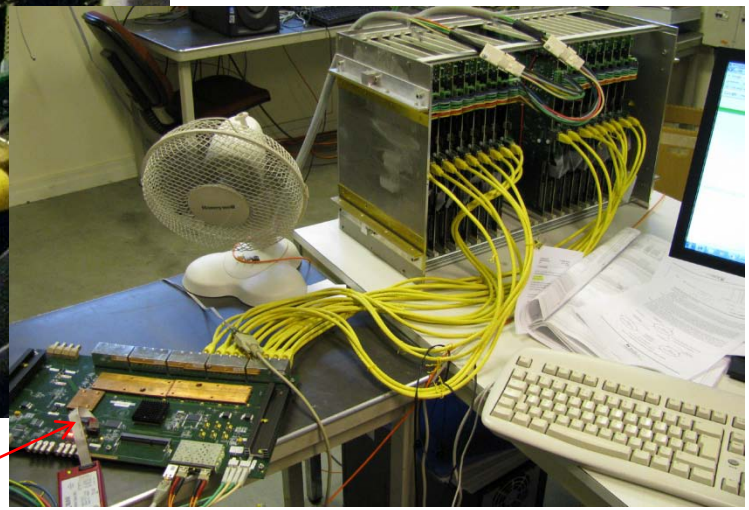
* DTC = Data/Trigger/Contol across CAT6 cables



legacy FEE cards (PHOS, EMCal, DCaL)

DTC adapter plugin for FEE

FEE crate EMCaL/DCaL



SRU

SRS status 2011

- 1st medium-sized (16 k ch) SRS system commissioned (FIT Florida)
- 1st SRS in ATLAS LHC cavern (MAMMA-Atlas)
- 1st SRU under test for readout of legacy FEE cards (EMCal-Alice)
- 1st experience with small SRS system (HIP, WIS & Univ.Aveiro,Coimbra)
- APV hybrid micro-via technology in production (ELTOS & HYBRID-SA)
- SRS hybrid with Beetle chip under design (WIS)
- SRS Mini-crates being prepared for shipment (NA62, UNAM, BNL)
- Scalable Detector Controls (SDC) via Ethernet (NTU Athens, RD51 CERN)
- Labview based DAQ and Monitoring system (INFN Napoli)
- DATE Online (32/64 bit, SLC5) across Network switch (Alice DATE)
- Online Zero-suppression & Feature extraction started (INFN Napoli)
- Clock and Trigger Fanout card for small systems, awaited (INFN Napoli)
- Commercialization discussions with 4 European companies
- SRS items to become available via CERN store in 2011

SRS developer activities

- Gigabit Ethernet in Virtex5 -FEC (done, UPV Valencia)
- DATE equipment port : SRS via UDP (done CERN ALICE)
- APV online monitoring with AMORE (done FIT)
- ADC de-serializer in Virtex5 (done UPV)
- APV data packing in UDP (done CERN RD51)
- APV configuration via Labview (done CERN)
- MMDAQ , Online system MAMMA (done CERN ATLAS)
- Scalable Detector Controls, SDC (done CERN + NTU Athens)
- Zero Supression, feature extraction in Virtex-5 (ongoing INFN Napoli)
- FEC upgrade, Virtex-6, quad SFP+, remote config. etc (ongoing UPV + CERN)
- DTC link between SRU and FEC (ongoing CCNU Wuhan)
- GbE on SRU via SFP+ on Virtex6 (finalizing CCNU)
- BNL chip SRS adapter (ongoing, Univ. o Arizona)
- Labview DAQ via GbE (finalizing INFN Napoli)
- Beetle chip hybrid (progressing WIS, Israel)
- Timepix SRS adapter (preparing, Phys Inst Bonn)
- Porting of PHENIX DAQ system to SRS (starting, BNL)
- Clock and Trigger fanout, proto board expected (INFN Napoli)

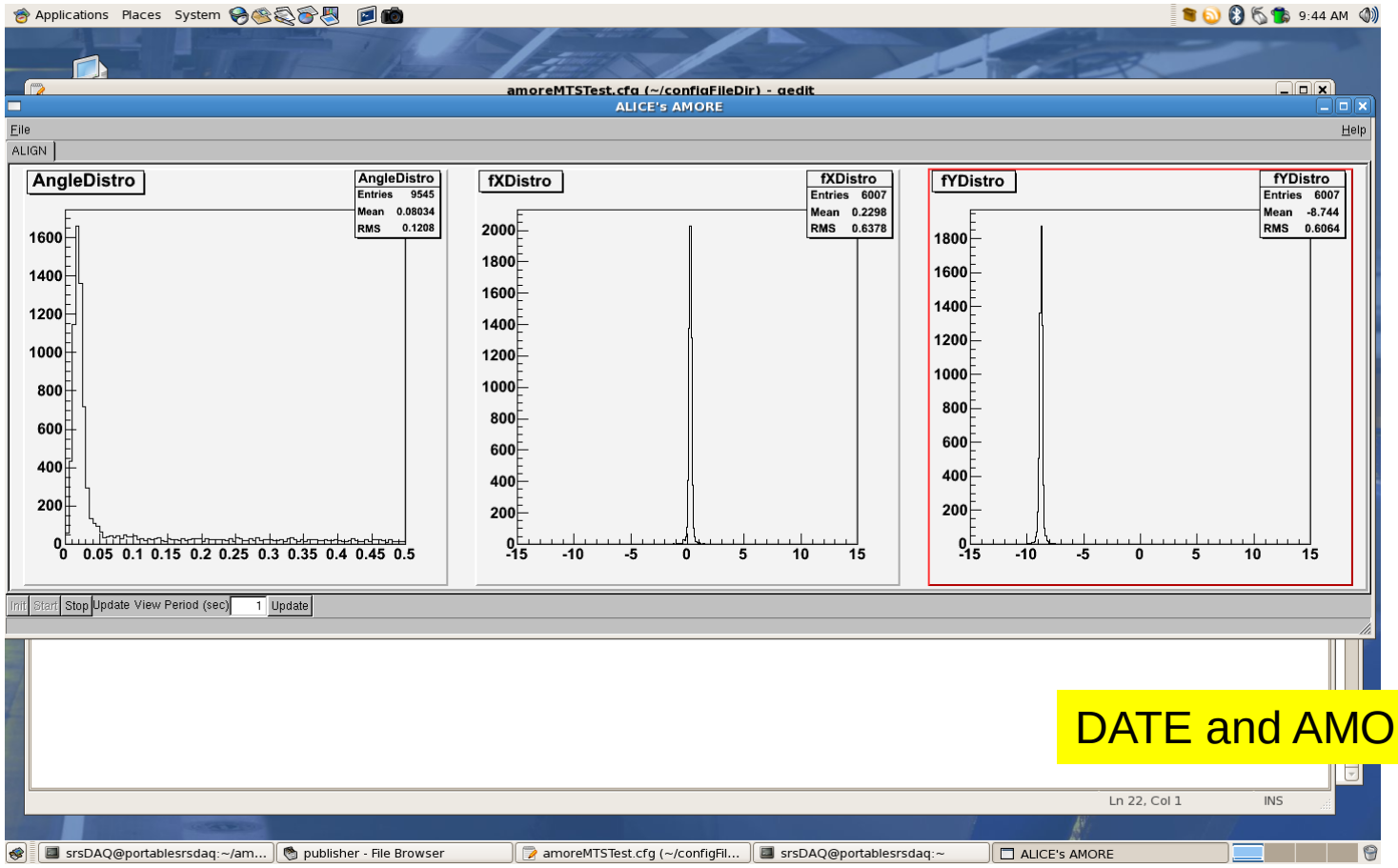
Message to ALICE / ITS

- SRS became a defacto standard for a large international community
- Main concepts originate from ALICE, with contributions from UPV Valencia
- Significant work going on for new SRU-based ALICE EMCal readout
- UPD equipment port of DATE was developed by ALICE Online with SRS teams
- Slow controls: via Ethernet and generic IP ports
- HDMI chiplink was an excellent choice !
- More SRS features being worked on by SRS developers
- SRS open standard allows for new paradigms (links, trigger, data formats)
- Basic SRS hardware components will become available though CERN store
- More work needed on SRU and L0/L1 trigger generation in SRU
- Progress is driven by convinced users and developers

ITS team is welcome to join the SRS community !

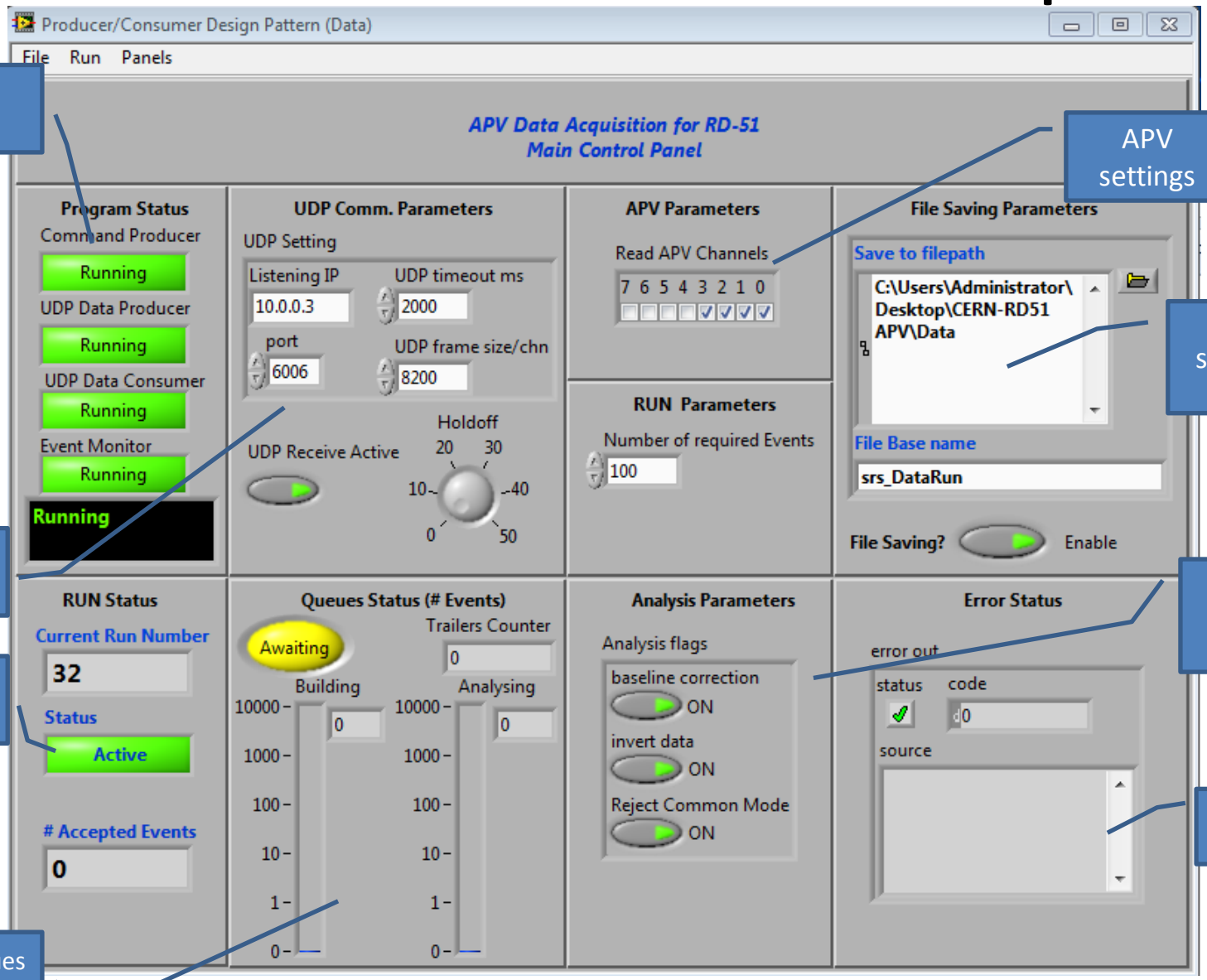
Backup slides

Offline with SRS
muon track distribution from GEM x-y



DATE and AMORE

SRS- Labview Main control panel



Running Processes control

APV settings

Data Files saving paths & Naming

UDP Parameters

Online analysis parameters

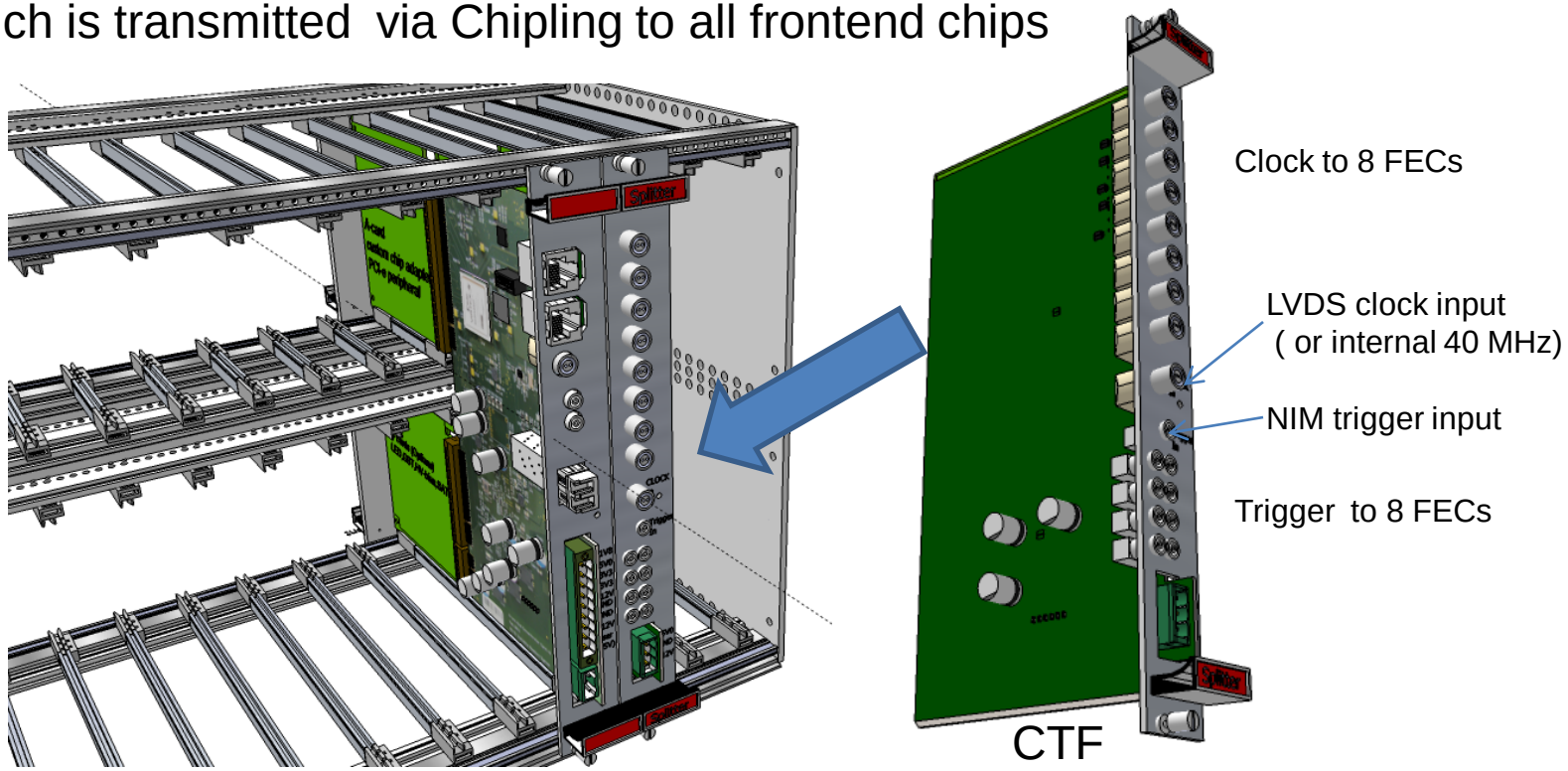
RUN status control

Error status

Internal queues occupacy

Common trigger/Clock

Small systems without SRS need to synchronize clock and trigger which is transmitted via Chipling to all frontend chips



The new CTF card distributes a common SRS clock and trigger signal to all SRS FECs within a small system

Note: Large, SRU based systems receive clock and trigger via DTC links from SRU