

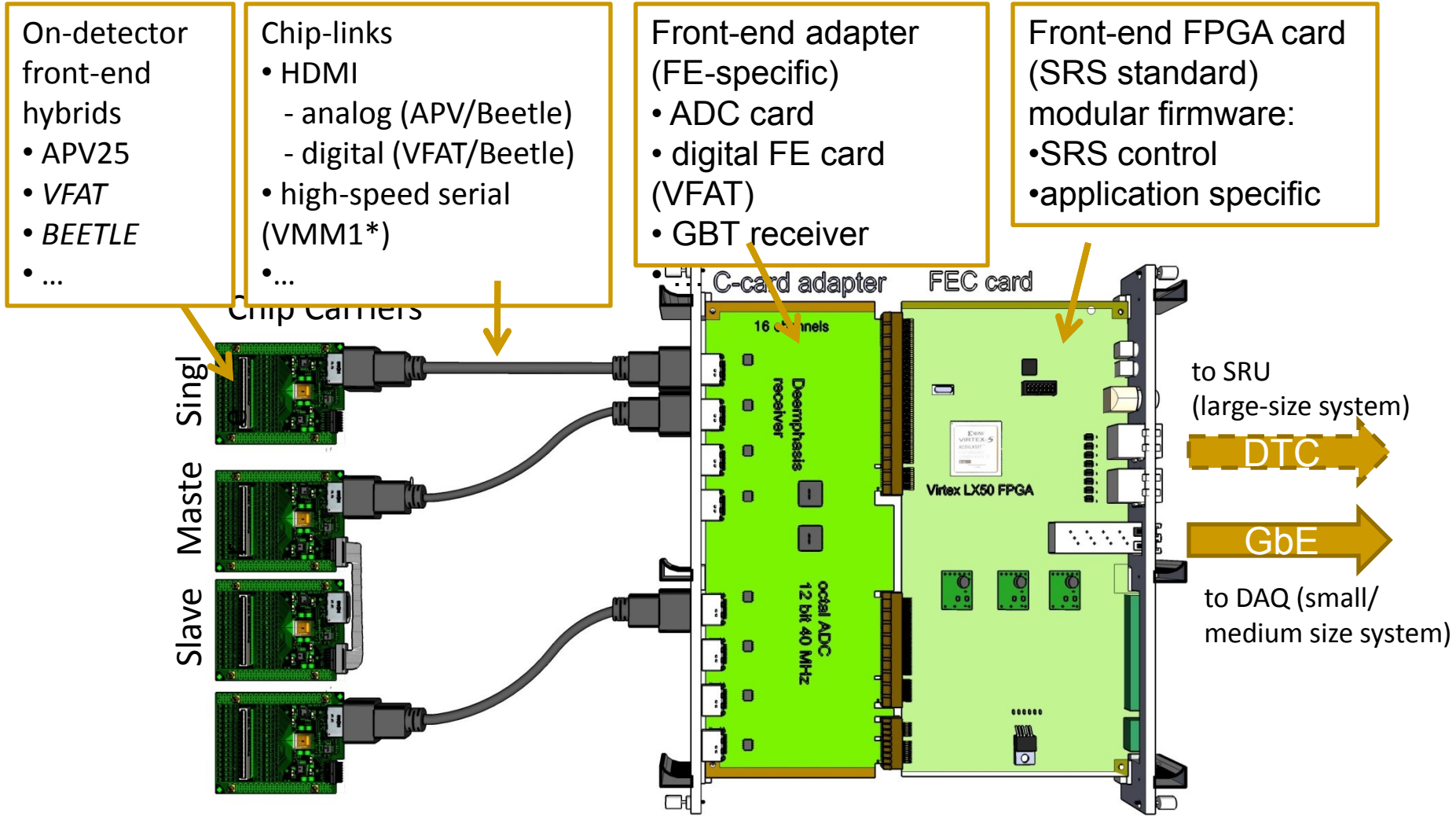
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# SRS Front-End Components

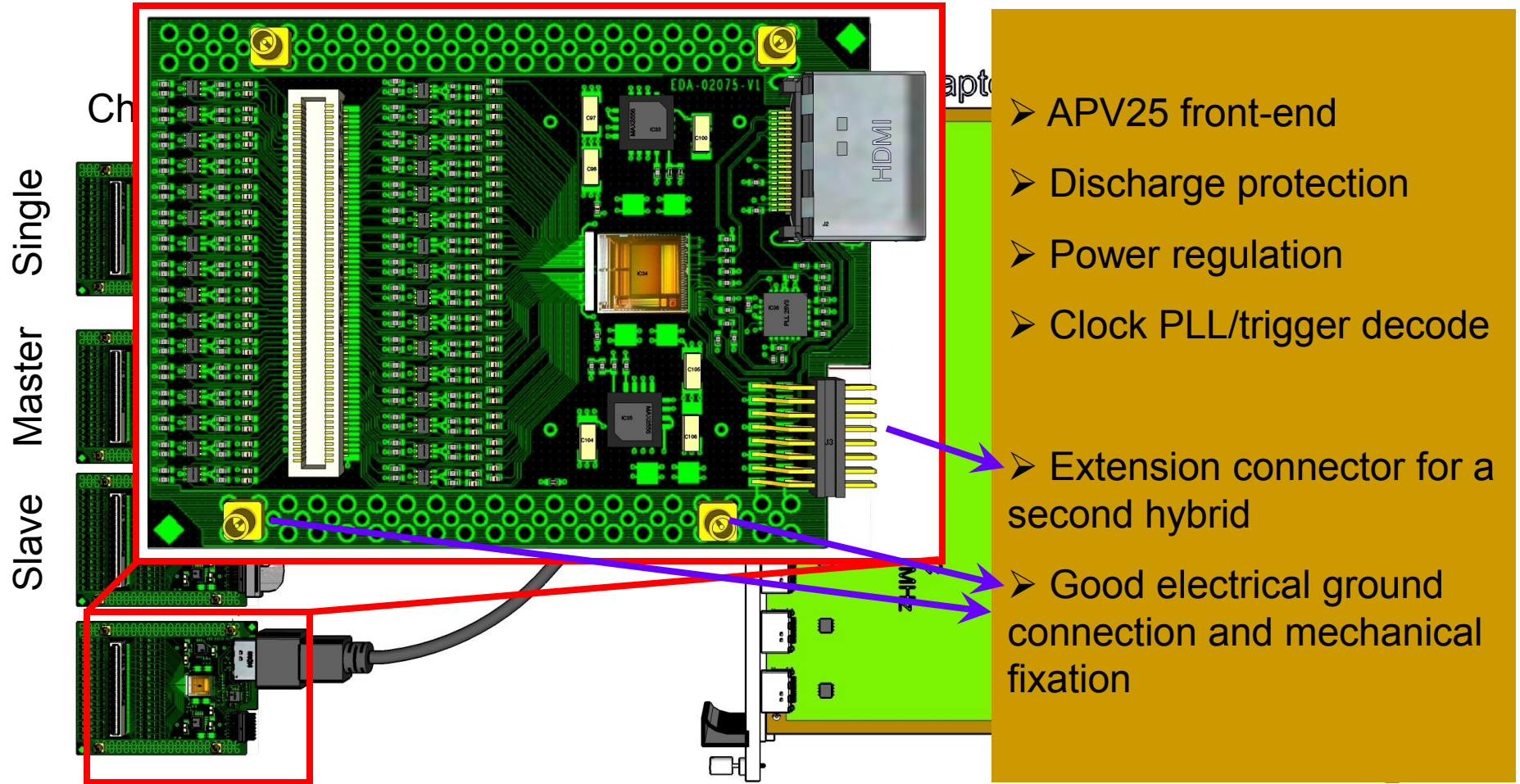
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Sorin Martoiu, CERN

# Overview

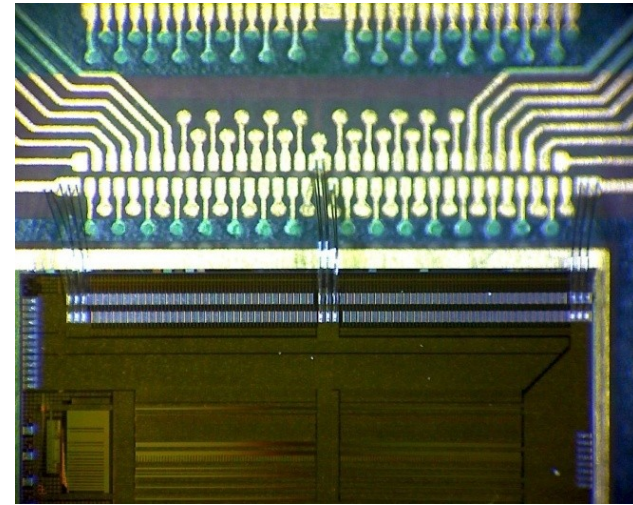
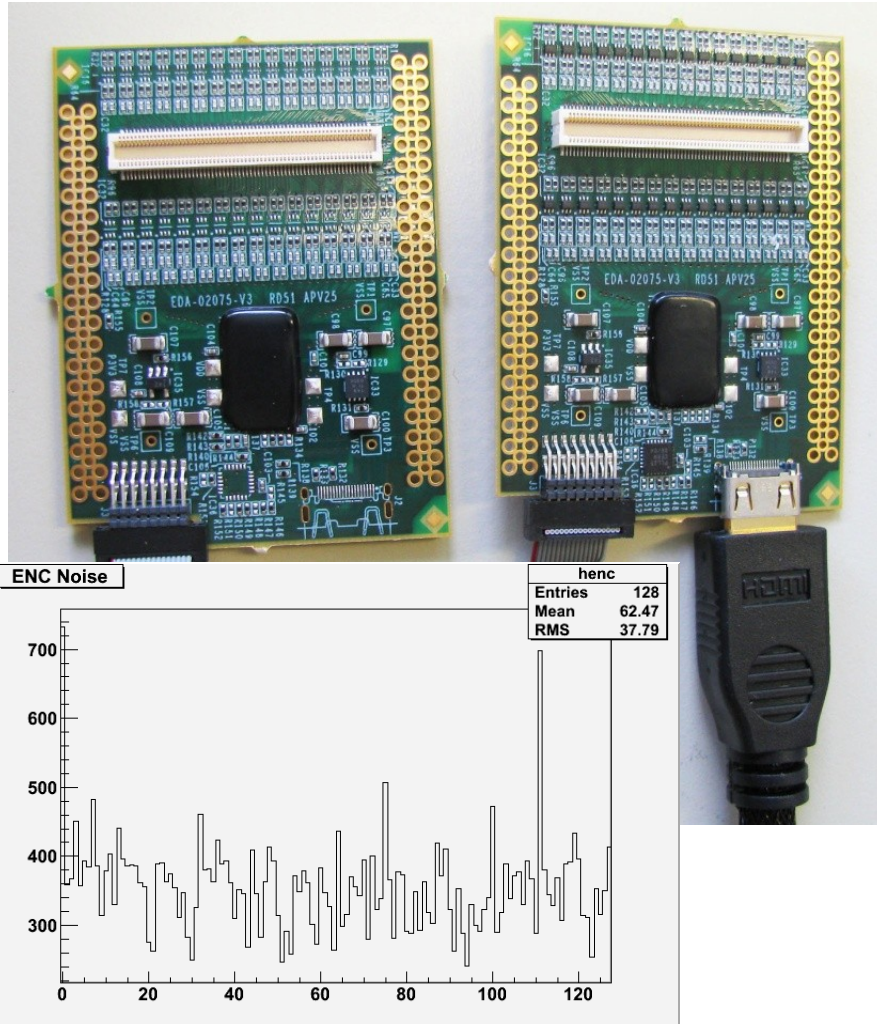


# APV25 Hybrid



- APV25 front-end
- Discharge protection
- Power regulation
- Clock PLL/trigger decode
- Extension connector for a second hybrid
- Good electrical ground connection and mechanical fixation

# APV25 Hybrid



- Printed circuit pitch adapter using microvias
- Front-end chip glob-topped
- PCBs produced in industry.
- Good production and assembly yield

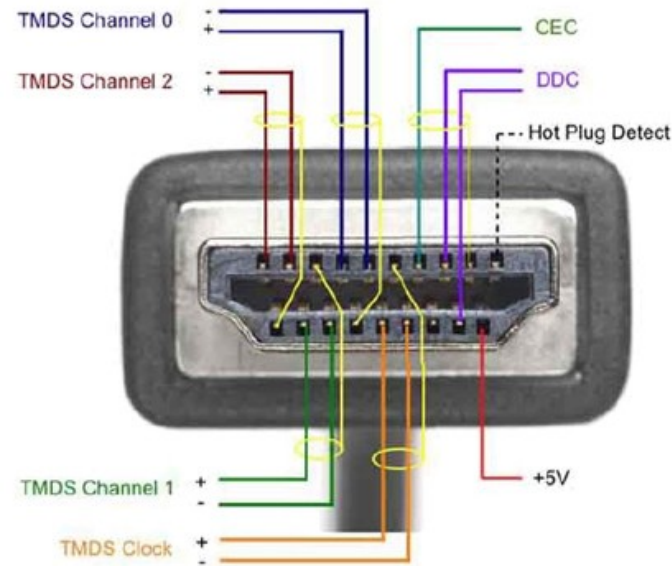
# HDMI

## Features:

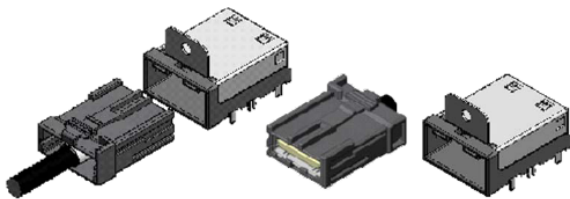
- 4(8) **high-speed individually shielded twisted-pair** cables
- 5 additional lines: I<sup>2</sup>C, power,.. (Ethernet - additional individually shielded twisted-pair for rev 1.4)
- 19/29 pins in total
- Low cost. Widely available.

## Electrical Characteristics:

- 100 ohm  $\pm$  10% characteristic differential impedance
- **340 MHz** bandwidth (analog)
- **10.2Gbps** (TMDS – 3 data lines + 1 clock) @ 15m length
- 1.78ns Maximum Cable Assembly Inter-Pair Skew
- 0.5A/pin current rating for both cable and connectors



### 1) Automotive HDMI Type E Connector



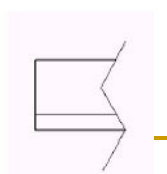
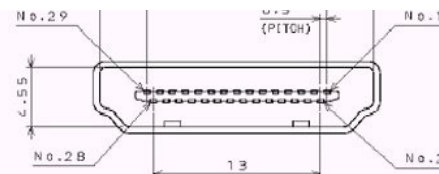
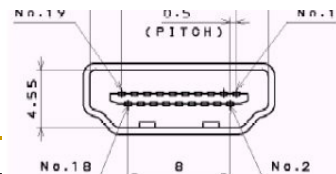
Standard



Mini



Micro

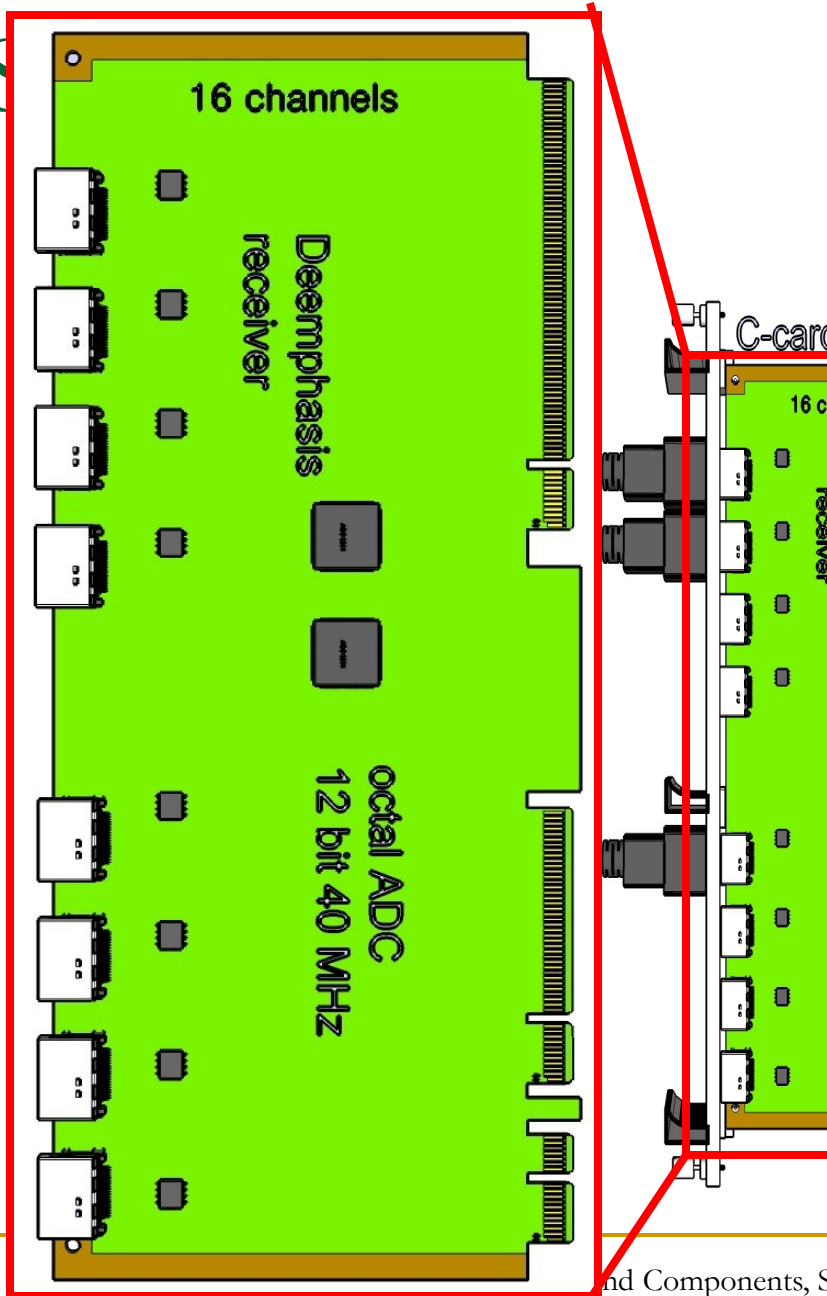


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# HDMI Pinout

Pin Number	HDMI Signal	APV25 (2x)	Beetle Analog – 2x Digital – 1x	VFAT2
1,3	TMDS 2	AOUT0 (analog)	OUT0 (analog/digital)	DOUT (digital)
4,6	TMDS 1	AOUT1 (analog)	OUT1 (analog/digital)	S1 (digital)
7,9	TMDS 0		COMPOUT (dig)	T1 (digital)
10,12	TMDS CLK	BCLK	BCLK	CLK
13	CEC	RST*	RST*	RST*
14	Reserved			IMON
15	SCL	I2C	I2C	I2C
16	SDA	I2C	I2C	I2C
18	Power	3.3V	3.3V	3.3V
19	HotPlug			VMON

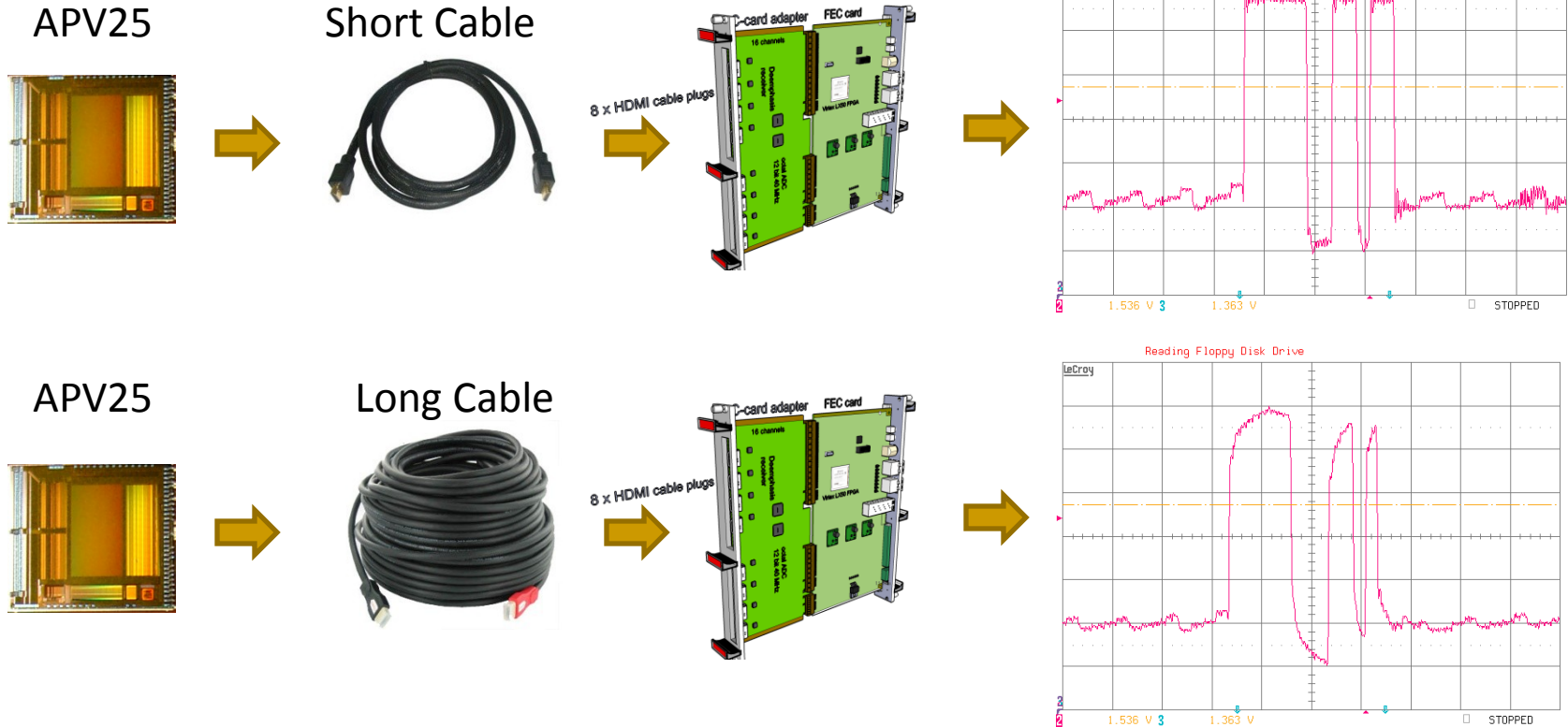


- 16 ADC channels (12 bit, up to 70 Msp/s)
- Equalization for long cables
- Clock distribution
- Slow control distribution
- Monitoring

### Firmware (FPGA):

- Optional signal processing (equalization, pedestal and common-mode correction, etc.)
- Event building and buffering
- GbE data transport and slow-control

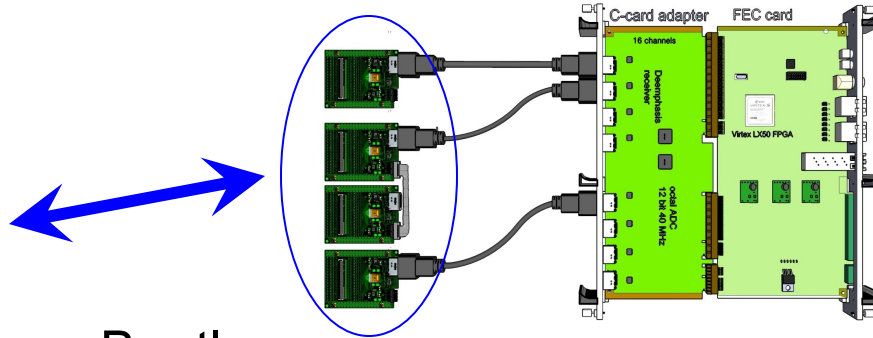
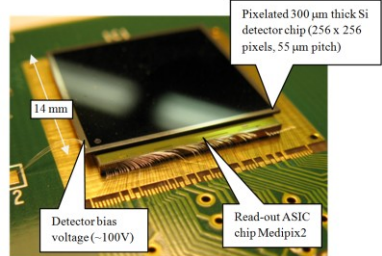
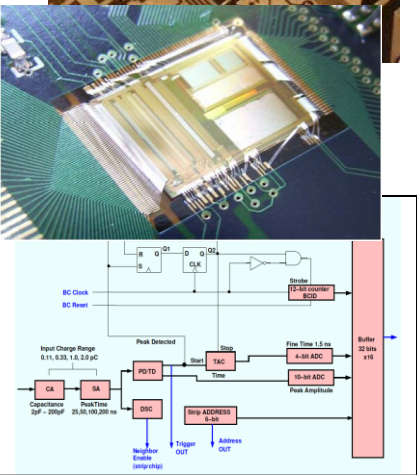
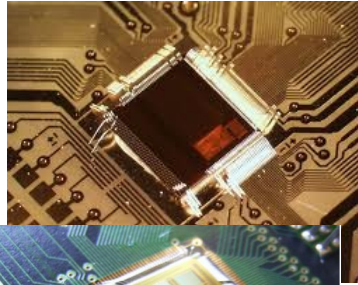
# Input Equalization



- 4 analog equalization steps to accommodate cables up to 30 meters
- Optional fine-tune digital correction in FPGA

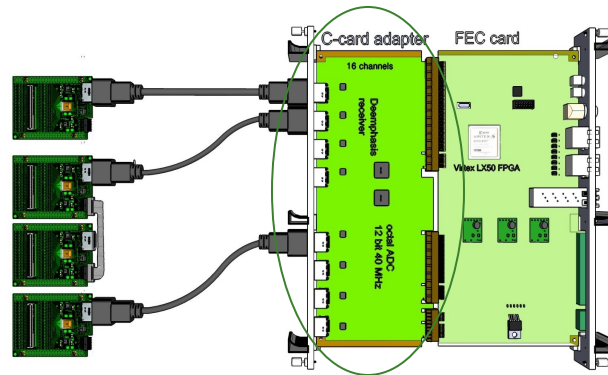


# New SRS Front-Ends



- Beetle
  - Digital and analog mode (HDMI)
  - Hybrid under design (Weizmann Institute of Science, Israel)
- VFAT2
  - Digital (HDMI)
  - Hybrid under definition (CERN)
- VMM1
  - Chip under design (BNL – ATLAS Muon Phase 1 Upgrade)
- Timepix
  - Under definition (University Bonn)

# New SRS Front-Ends



- Digital Adapter Card
  - Beetle – 960Mbps
  - VFAT2 – 640Mbps
- High-speed serial card
  - 8 channels
  - Up to 5Gbps
  - Copper or optical
  - GBT, VMM1(final), general purpose data concentrator card