The development of Si detector in ALICE: from ITS2 to ITS3

Alessandra Fantoni (INFN Frascati)

on behalf of the ALICE Collaboration

Workshop on Advances, Innovations, and Future Perspectives in High Energy Nuclear Physics

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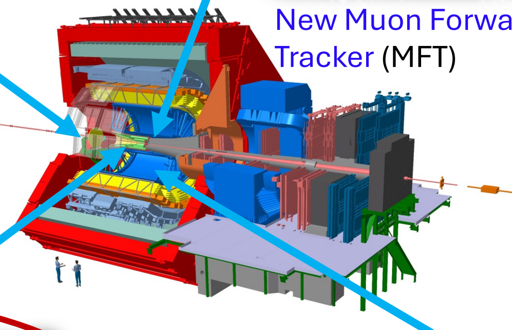
ALICE upgrades in Long Shutdown 2 (LS2)

- Major upgrades completed for ALICE during LHC LS2 (2019 - 2021)
- Motivation
  - High-precision measurements of rare probes at low p_T
    - Cannot be selected by hardware trigger
    - Need to record large minimum-bias data sample
    → read out all Pb-Pb interactions up to the maximum collision rate of 50 kHz
- Goal
  - Pb-Pb integrated luminosity > 10 nb^{-1} (plus pp, pA and O-O data) → gain factor 100 in statistics for minimum-bias sample with respect to Run 1 and 2
  - Improved vertex reconstruction and tracking capabilities
- Strategy
  - New ITS, MFT, FIT and TPC readout chambers
  - New readout of most detectors and new trigger system
  - New integrated Online-Offline system (O^2)

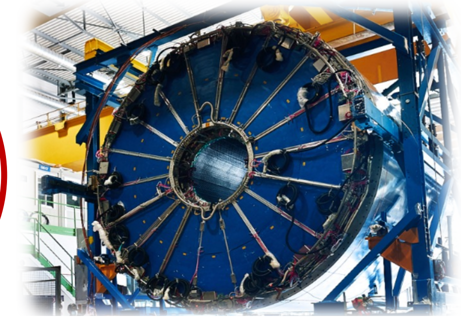
ALICE upgrades during the LHC Long Shutdown 2, JINST 19 (2024) P05062

New Fast Interaction Trigger (FIT)

New Muon Forward Tracker (MFT)



New Inner Tracking System (ITS2)



New GEM-based Time Projection Chamber (TPC) readout

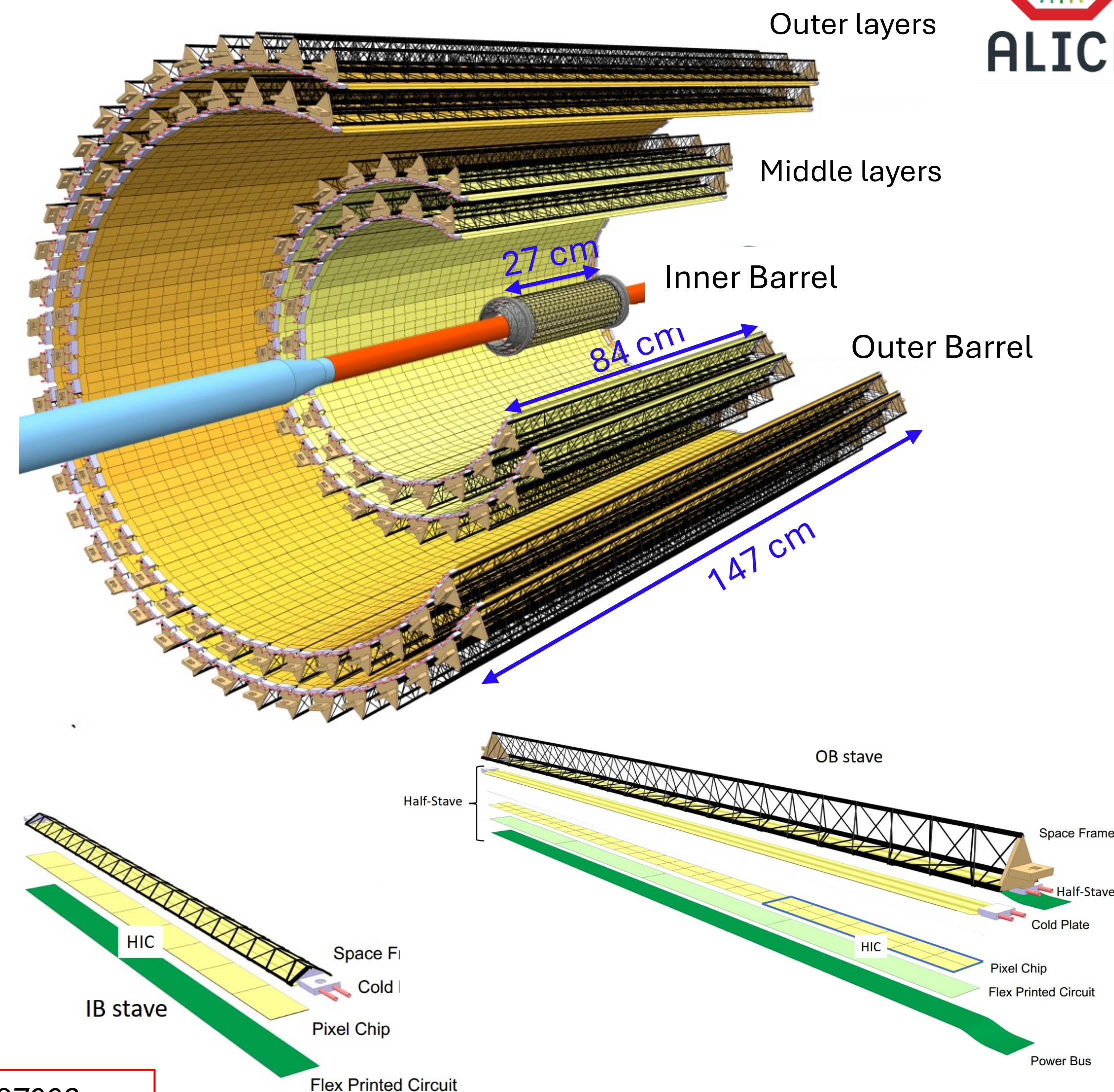
New trigger and readout systems

New Online/Offline (O^2) system

ALICE 2

ITS2 objectives and layout

- Improve impact parameter resolution by factor ~3 in rϕ and factor ~5 in z at p_T = 500 MeV/c
  - Get closer to IP: 39 mm → 23 mm
  - Reduce material budget:
    - 1.14% X_0 → 0.36% X_0 per layer (inner layers)
  - Reduce pixel size: 50 x 425 μm^2 → 29 x 27 μm^2
- Improve tracking efficiency and p_T resolution at low p_T
  - Increase number of track points: 6 → 7 layers
- Fast readout
  - Detector readout rates up to 100 kHz (Pb-Pb, was 1 kHz for ITS1) and 400 kHz (pp)
- 7 cylinders covering ~10 m^2 area with 12.5 billion pixels
  - Inner Barrel (IB)
    - 3 Inner Layers (48 staves)
  - Outer Barrel (OB)
    - 2 Middle Layers (54 staves) + 2 Outer Layers (90 staves)

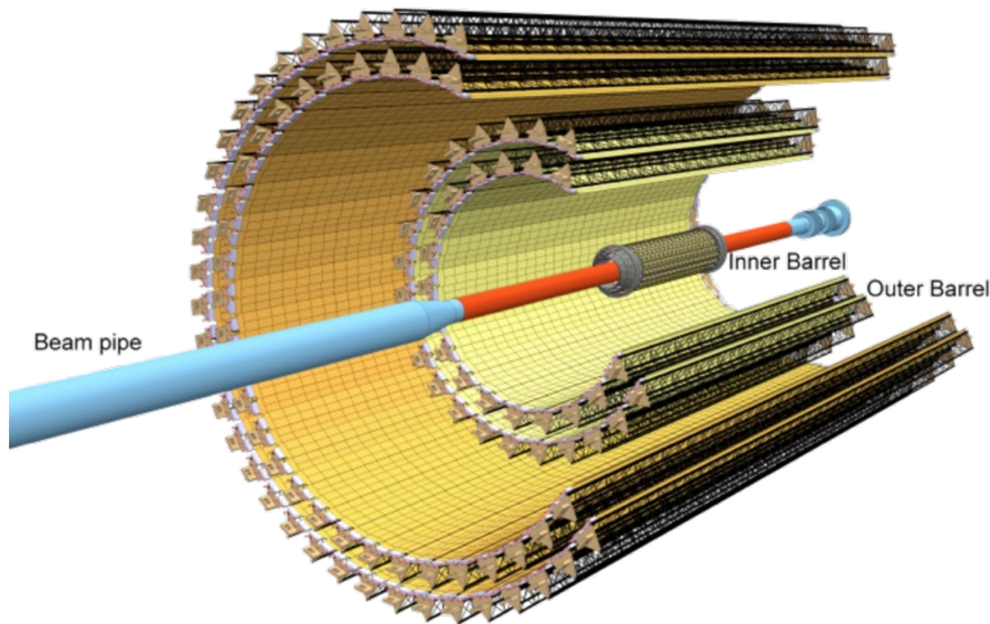


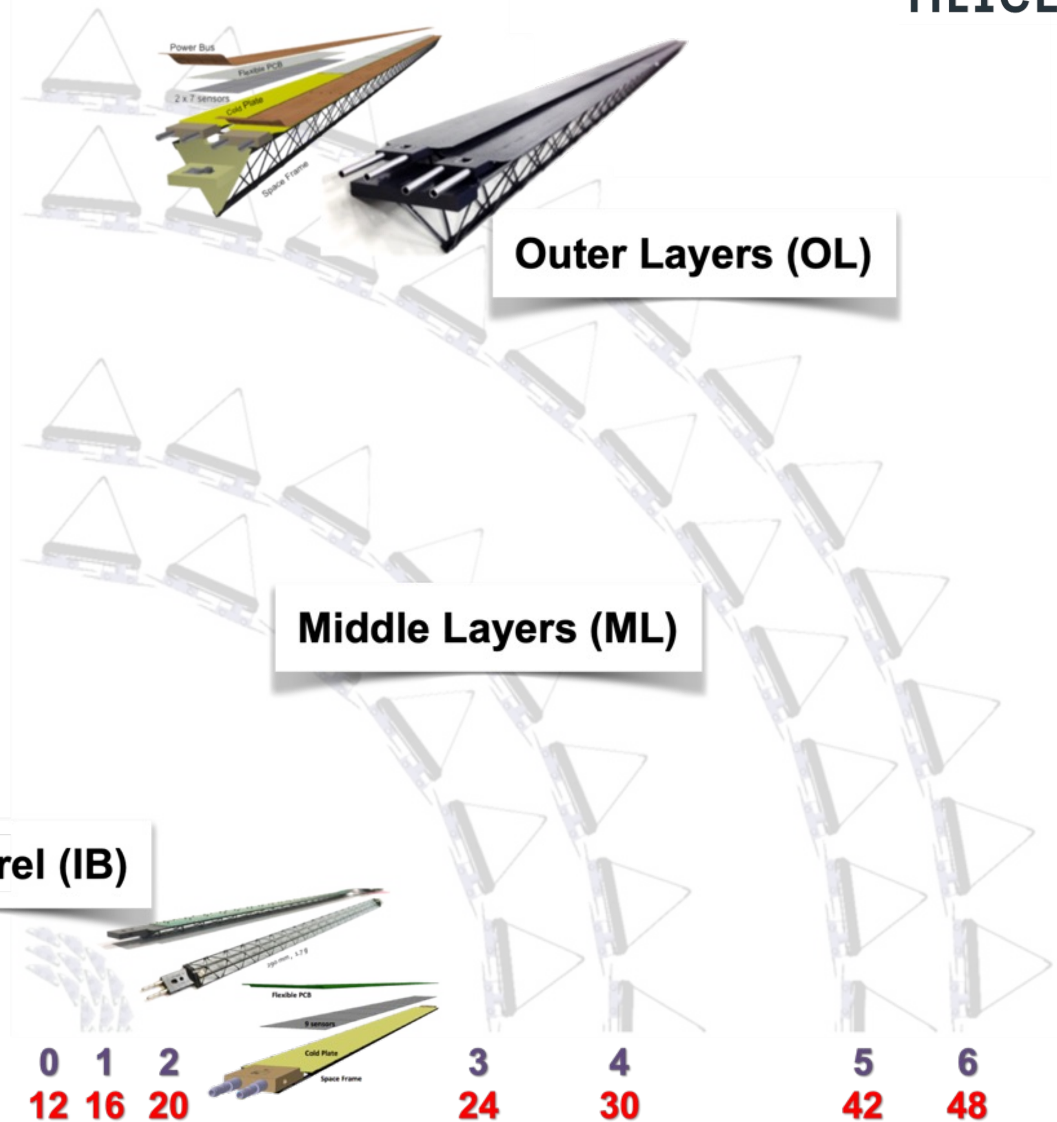
Technical Design Report for the Upgrade of the ALICE Inner Tracking System, J. Phys. G 41 (2014) 087002

ALICE upgrades during the LHC Long Shutdown 2, JINST 19 (2024) P05062

The largest MAPS detector (so far)

- 7 Layers (3 inner / 2 middle / 2 outer) from R = 22 mm to R = 400 mm
- 192 Staves (48 IL / 54 ML / 90 OL)
- Ultra-lightweight support structure and cooling
- 10 m^2 active silicon area, 12.5 x 10^9 pixels



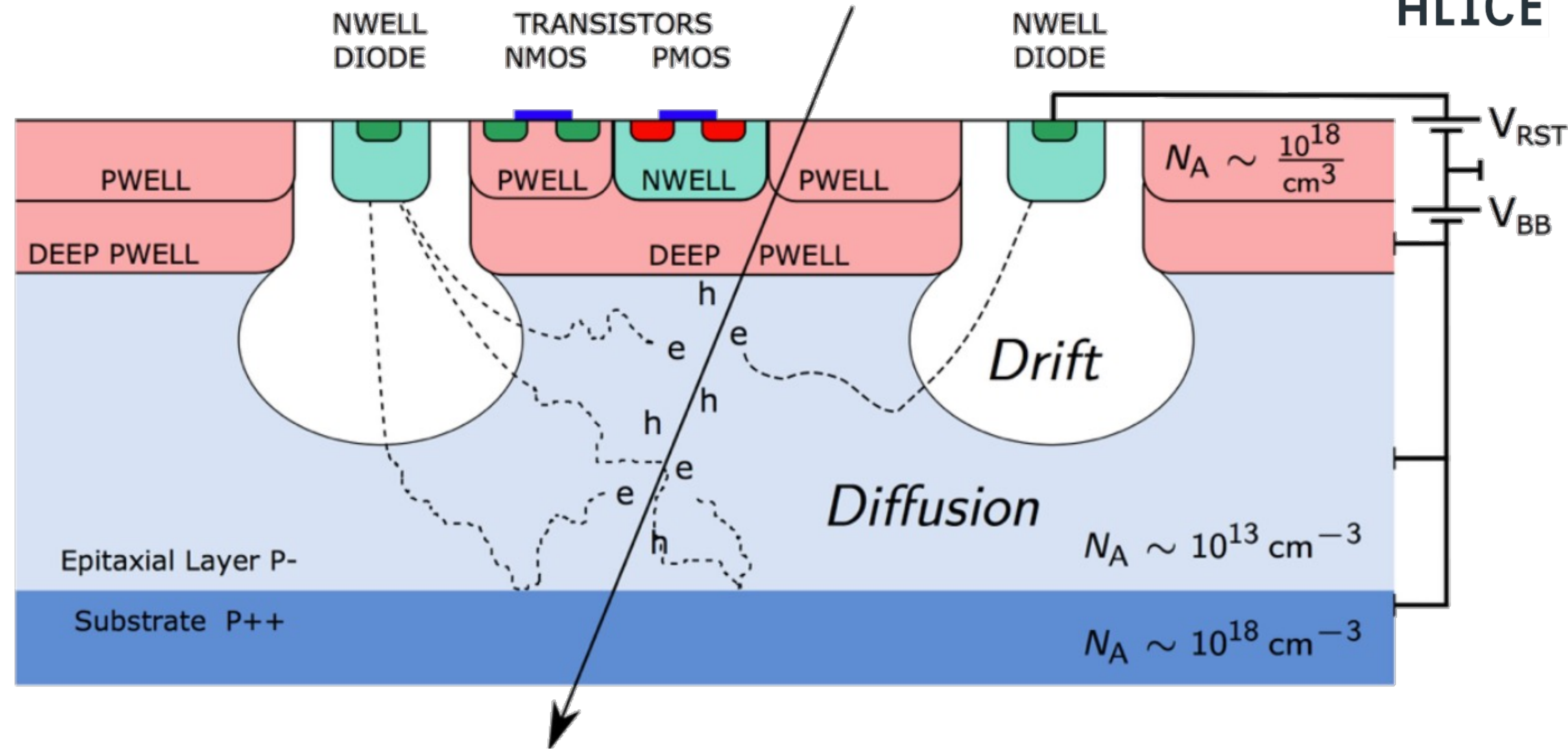


MAPS: CMOS Monolitic Active Pixel Sensor

MAPS: sensor and electronics on the same substrate

Exploits commercial CMOS imaging sensor (CIS) process to detect charge particles

First processed used to MAPS that featured a DEEP P-WELL allowing to shield CMOS circuitry and avoid loss of efficiency

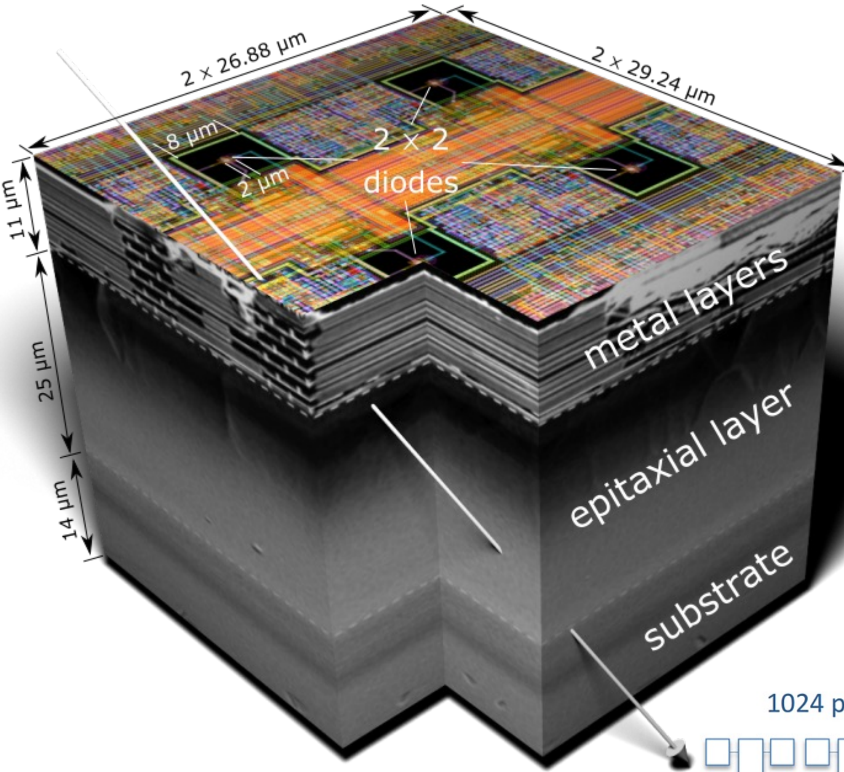


characteristics:

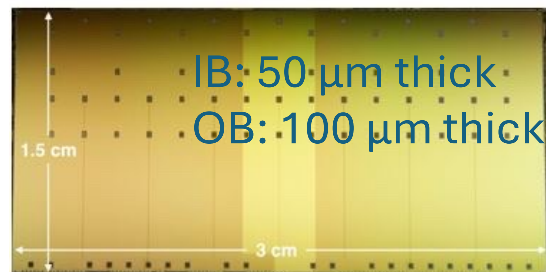
- thin sensor (all in 1 layer, thinned down to <50μm)
- easy integration
- low noise
- low power consumption

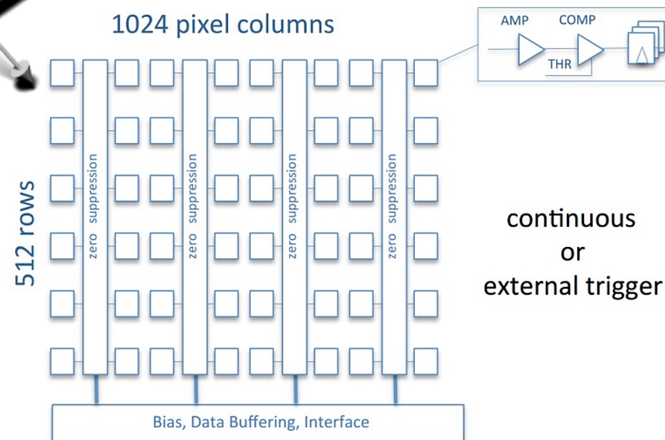
- good detection efficiency with careful adjustment of the amount of diffusion, optimizing the pixel geometry and the epitaxial layer thickness
- position resolution improved profiting from charge sharing
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification.

ALPIDE: ALICE Pixel DEtector



- Thin: O(50 μm)
- Very granular: O(30 μm)
- Small diodes: capacitances of O(5 fF)
- Highly integrated: O(100) transistors in-pixel





ALPIDE technology features:

- TowerJazz 180 nm CiS (CMOS Imaging Sensor) Process
- Deep p-well implementation available → full CMOS
- High resistivity (>1 kΩ·cm), 25 μm thick, p-type epi-layer
- Possibility of reverse biasing
- Smaller charge collection diode → lower capacitance → higher S/N
- Epitaxial layer serves as active volume → substrate can be thinned down

Sensor specification:

- Pixel pitch: 27 μm x 29 μm → spatial resolution: ~5 μm
- Priority Encoder Readout
- Power consumption: 47.5 mW/cm^2 (IB) and 35 mW/cm^2 (OB)
- Integration time: < 10 μs
- Fake-hit rate: << 10^{-6} /pixel/event
- Readout bandwidth up to 1.2 Gbit/s (IB) and 400 Mbit/s (OB)
- Continuous or triggered readout

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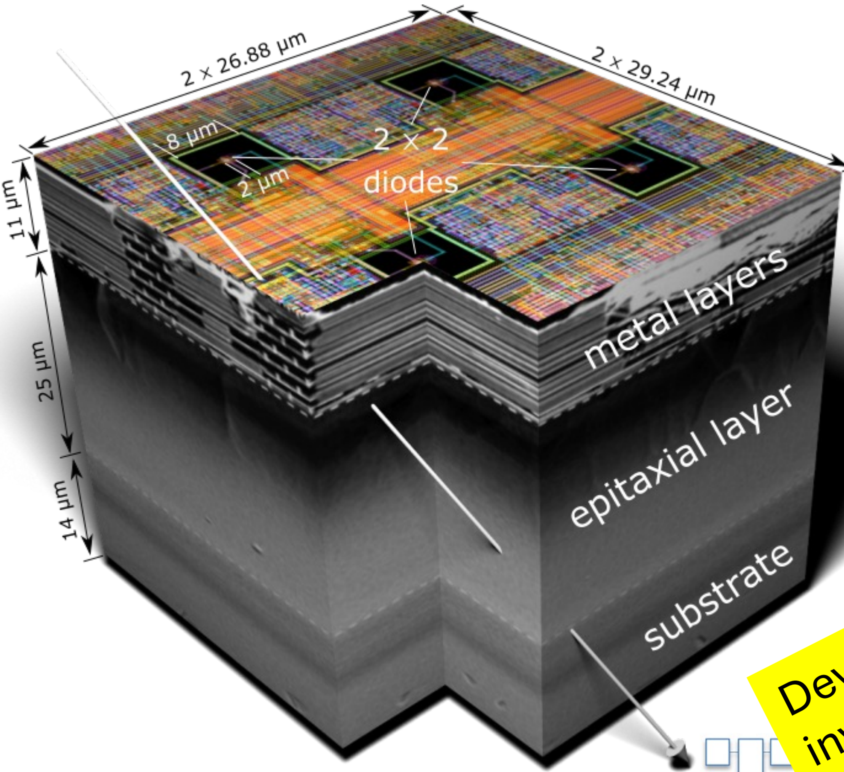

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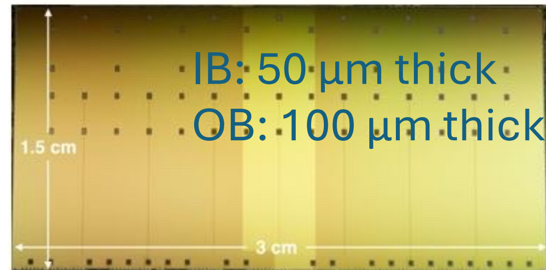
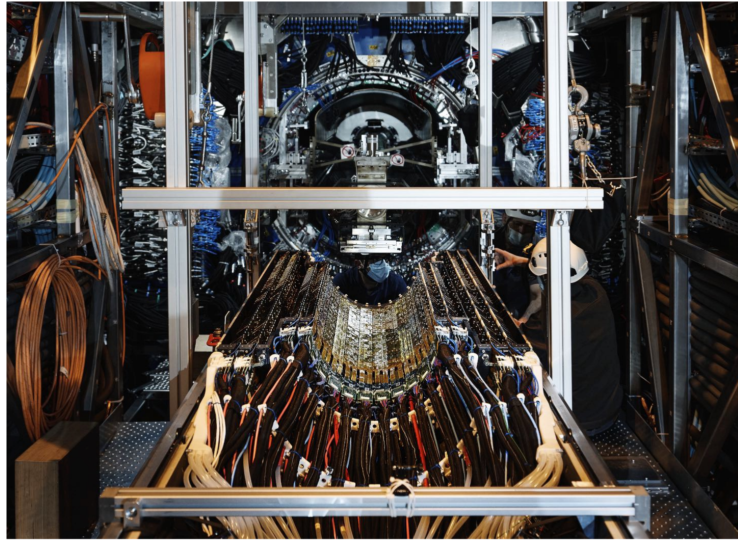


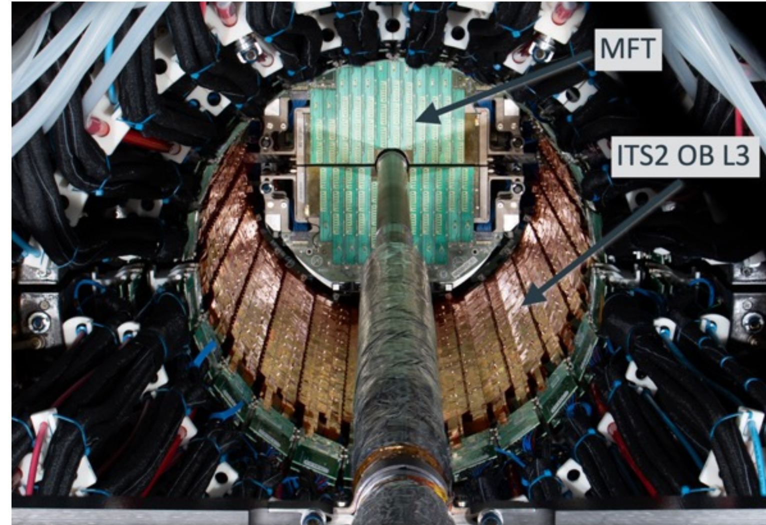
IB: 50 µm thick
OB: 100 µm thick

Development effort of 5y involving many institutions: CERN, INFN, Irfu, IPHC, Yonsei, **CCNU**

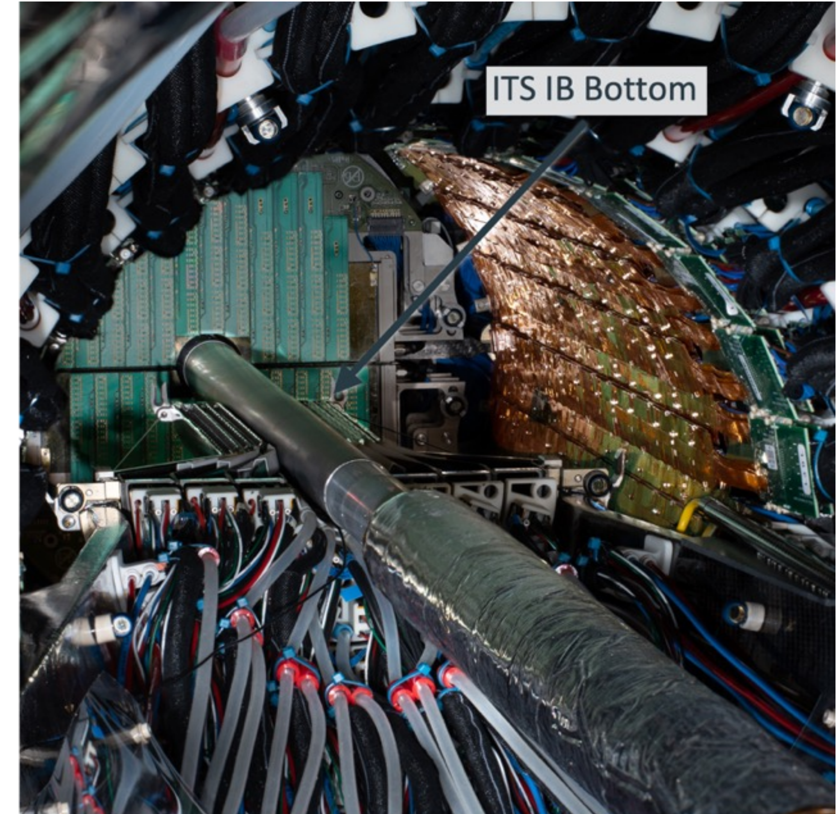
Talk by Xiangming Sin 21/10 16:50

ITS2 installation


ITS Bottom half barrel insertion



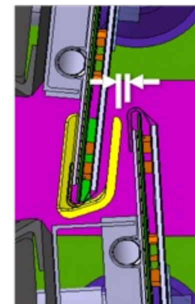
ITS Outer Barrel surrounding the beam pipe, MFT in the back



ITS Inner Barrel Bottom and Outer Barrel

- Installation challenges
  - Precise positioning around the beam pipe (nominal clearance ~ 2 mm)
  - Manipulating from 4 m distance
  - Difficult to see actual position by eye
  - precise matching of top and bottom barrel halves (clearance between adjacent staves ~ 1.2 mm)
- Dry-installation tests on the surface to test and exercise procedures
- Use of 3D scans, surveys and cameras

1.2 mm nominal clearance


OB stave edge clearance when fully mated

ITS2 calibration

The Challenge:

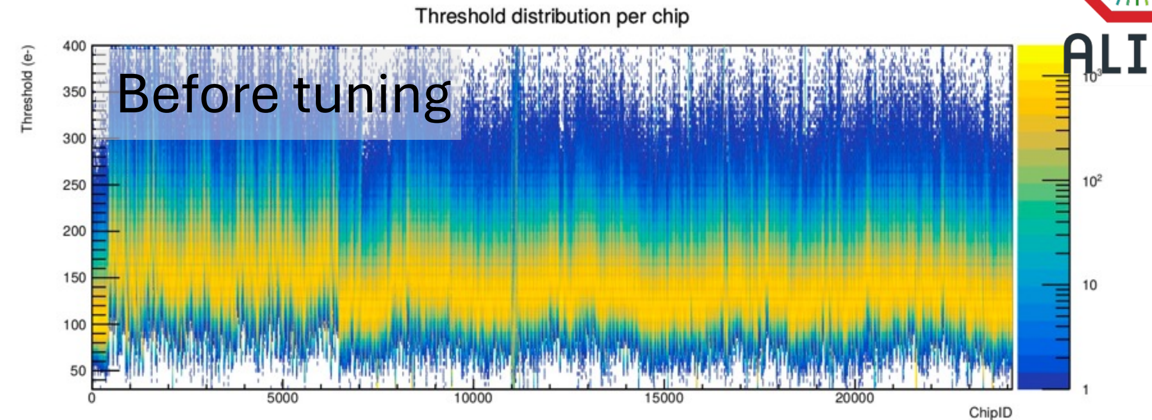
- Online calibration of 12.5 billion channels
- Threshold scan of full detector: > 50 TB of event data
- Several scans to be run sequentially
    - Threshold tuning (adjust thresholds to target)
    - Threshold scan (measure actual thresholds)

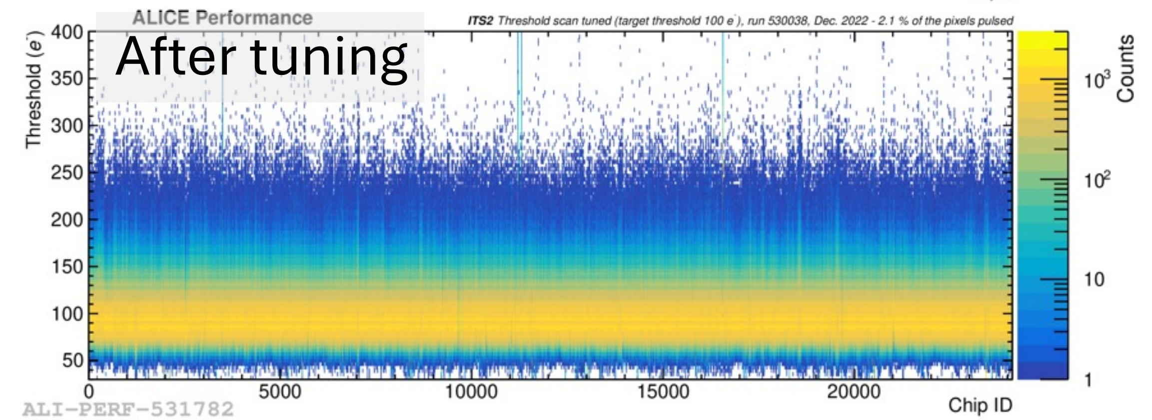
Procedure:

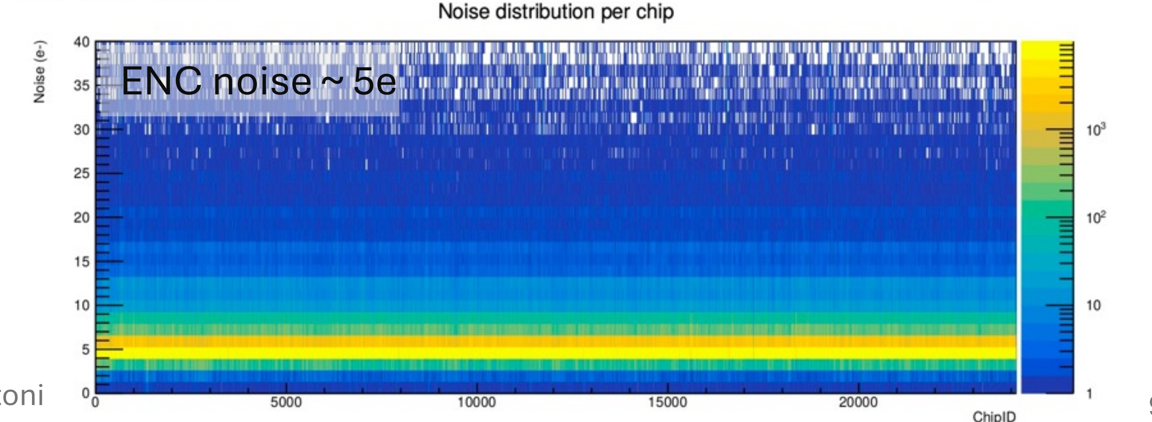
- DCS performs actual scans: configure and trigger test injections
- Scan runs in parallel but independently on all staves
- Distributed analysis on event processing nodes
- full procedure takes **less than 30 minutes**

Results:

- Scan with online analysis successfully run on full detector
- before tuning: settings used in surface commissioning, detector already fully efficient
- After tuning: Thresholds very stable on all the chips: RMS of threshold distribution compatible with what we had during production
- ENC noise ~ $5e^-$



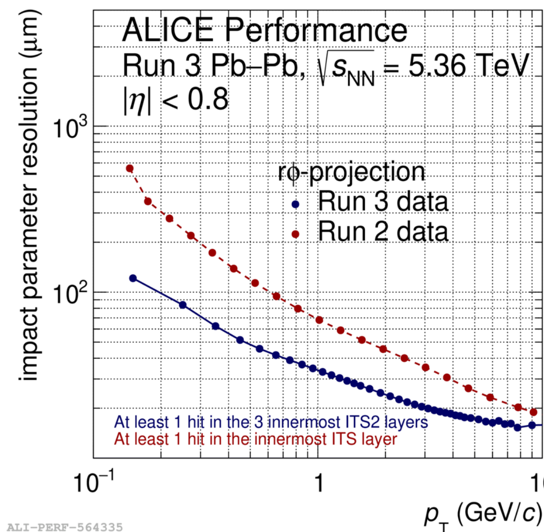




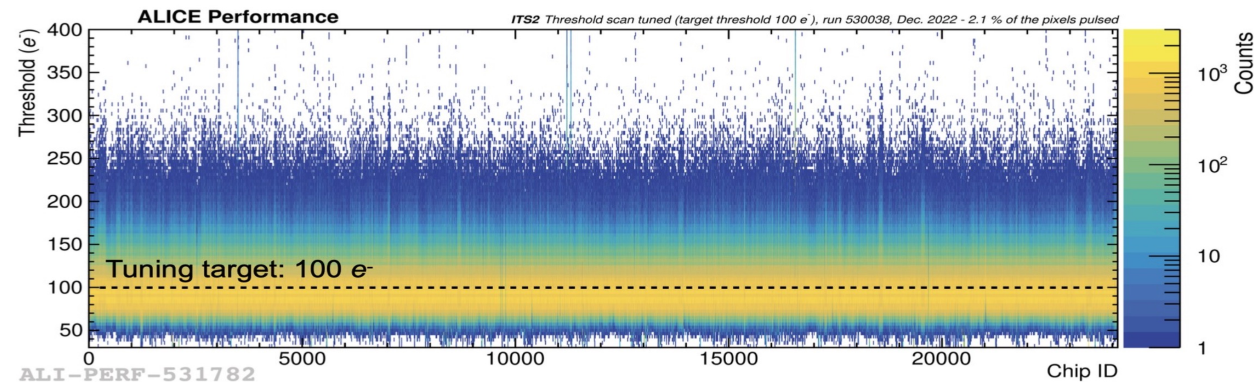
ITS2 performance

- Stable operation of 24k chips
- >99% functional pixels
- Tuned and stable thresholds
- Well controlled fake hit rate: $< 10^{-6}$/pixel/event
- 2 x better impact parameter resolution at 1 GeV/c

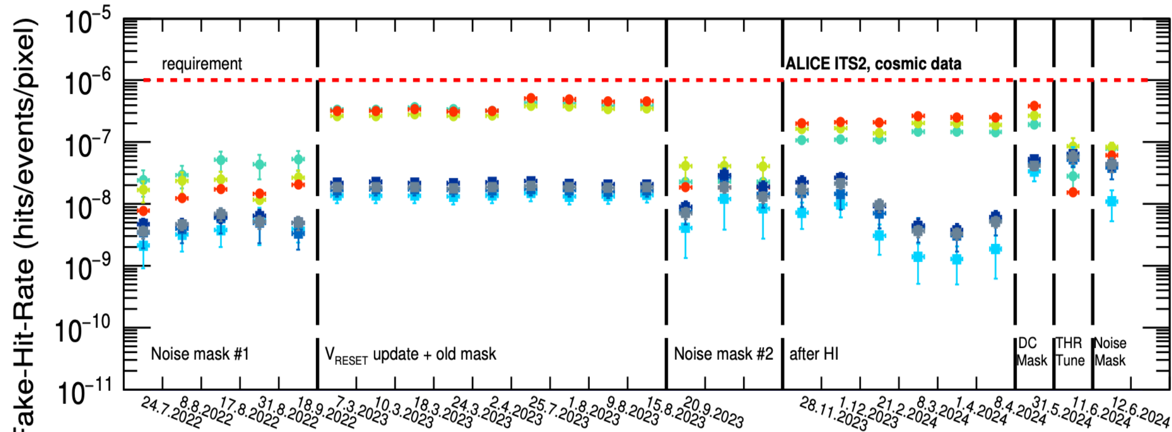
Impact parameter resolution

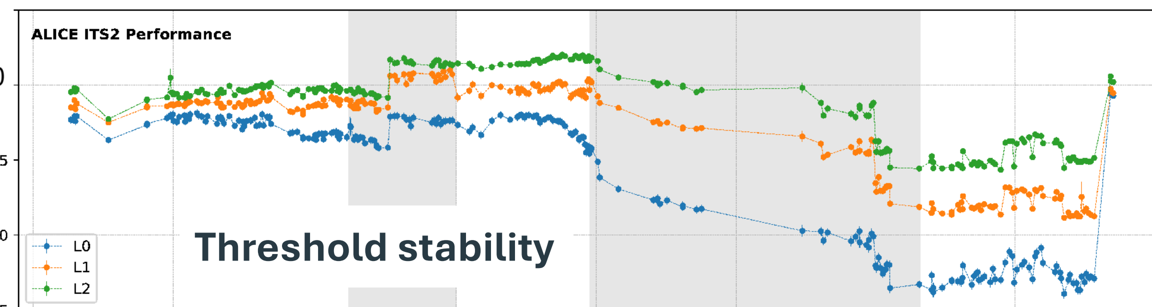


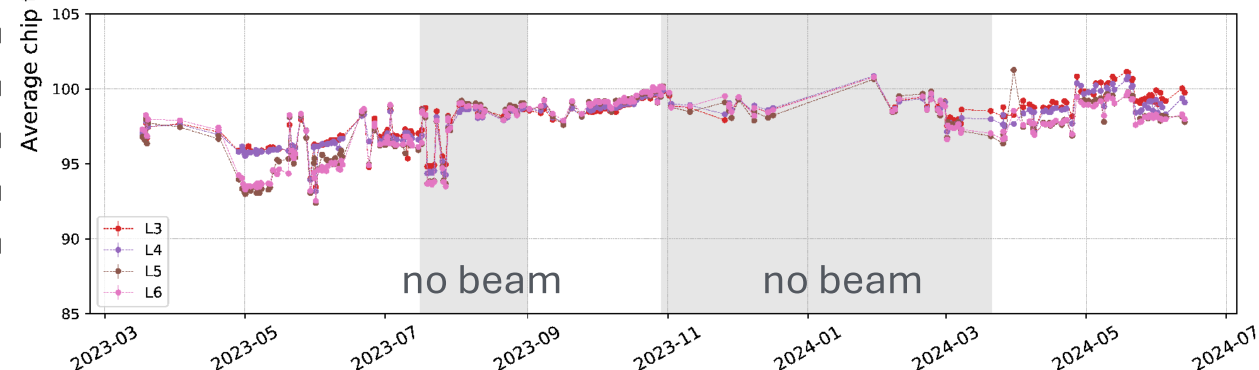
Threshold uniformity



Fake-hit rate







ITS2 Data Quality Control (QC)

7 QC online tasks to monitor data and MC simulation quality:

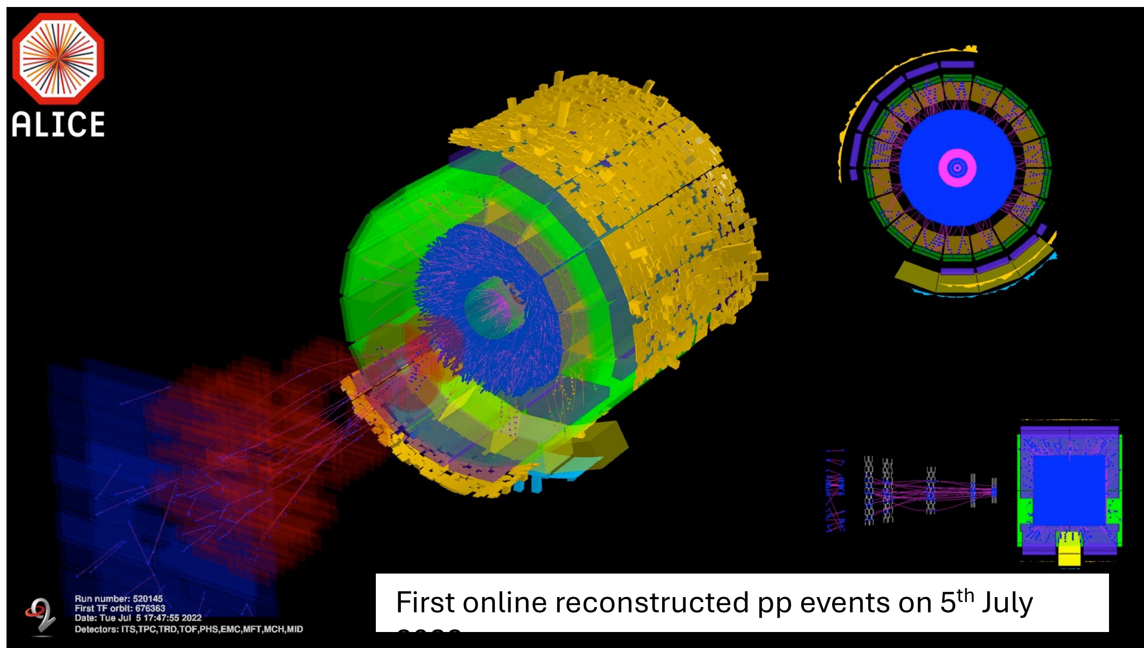
- Front-end electronics: data integrity check using diagnostic information in headers / dedicated packets
- Occupancy: monitoring of detector occupancy
- Cluster: monitoring cluster size, topology etc.

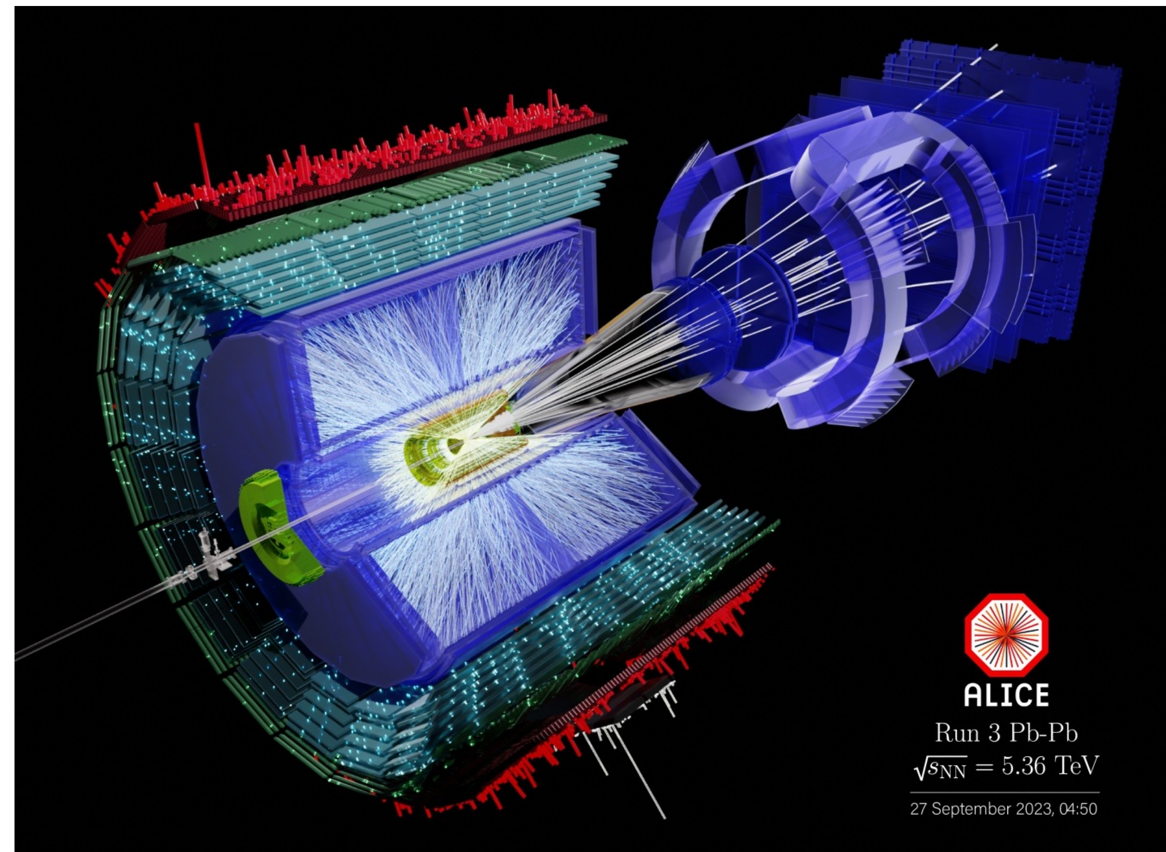
QC post-processing online and offline: analysis and trending of QC online plots (run by run)

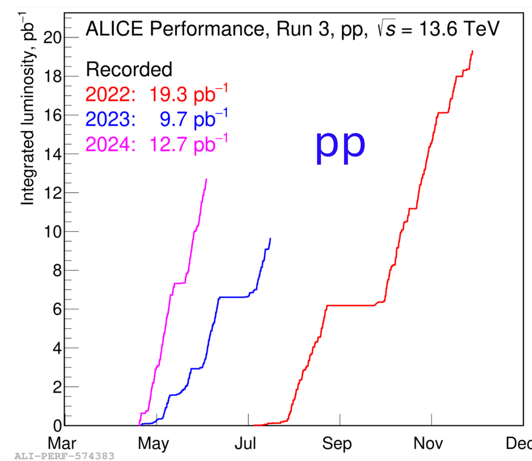
- *Tracks:* monitoring of track multiplicity, angular distribution, clusters etc.
- *Noisy pixels:* extraction of noisy pixels for offline noise masks
- *Threshold:* monitoring during calibration scans (threshold, noise, dead pixels)
- *Chip status: availability of data from a given chip per time frame*

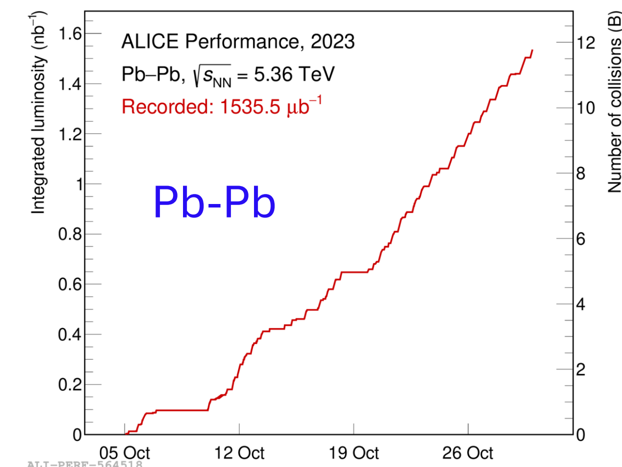
ITS2 in Run3

- Integrated luminosity so far (pp collisions): ~42 pb^{-1}
- Integrated luminosity for Pb-Pb in 2023 Oct.: ~1.5 nb^{-1}
  - Recorded Minimum Bias sample of ~12 billion collisions, ~40 times larger than Run 1+2
- ALICE standard interaction rate: 500 kHz (pp) – peaking at 47 kHz in Oct. 2023 (Pb-Pb)
  - Instantaneous luminosity: ~10^{31} (pp) – 10^{27} (Pb-Pb) $cm^{-2}s^{-1}$









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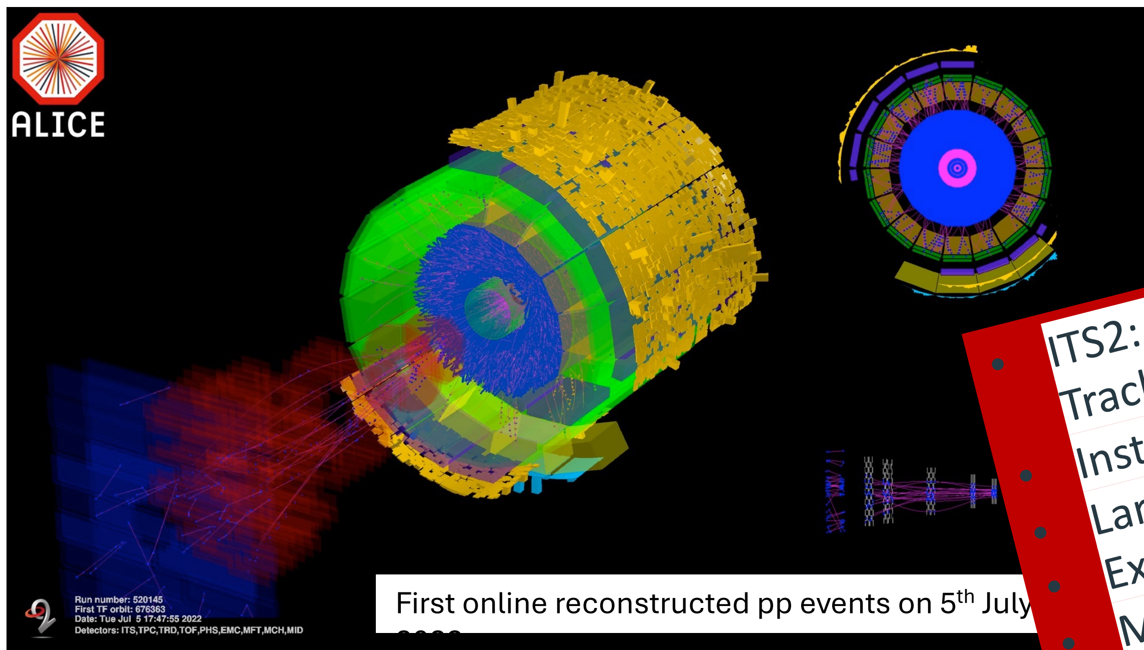
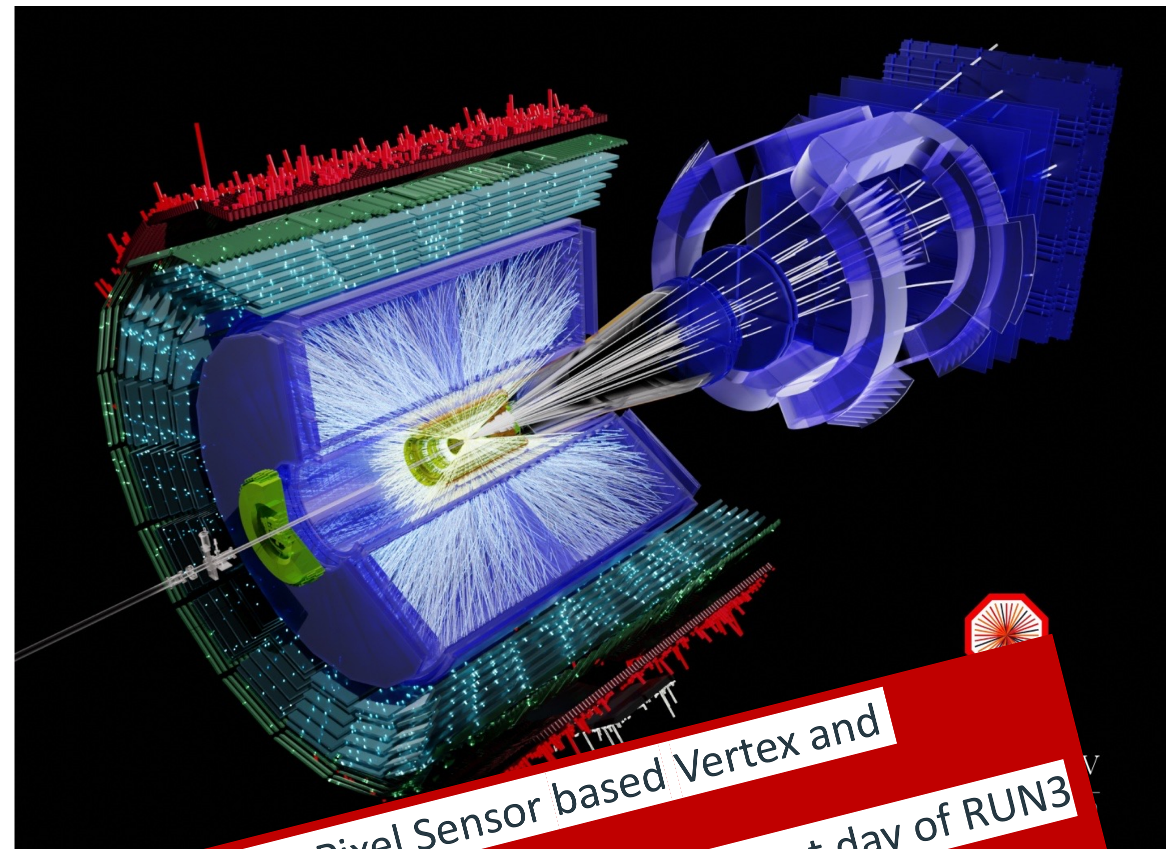
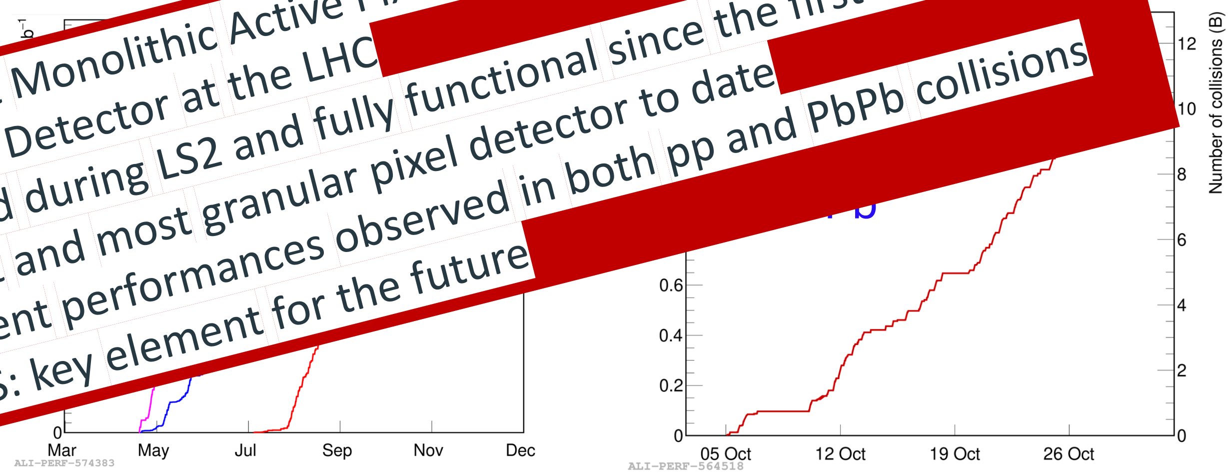


First online reconstructed pp events on 5th July 2022





- ITS2: first Monolithic Active Pixel Sensor based Vertex and Tracking Detector at the LHC
- Installed during LS2 and fully functional since the first day of RUN3
- Largest and most granular pixel detector to date
- Excellent performances observed in both pp and PbPb collisions
- MAPS: key element for the future

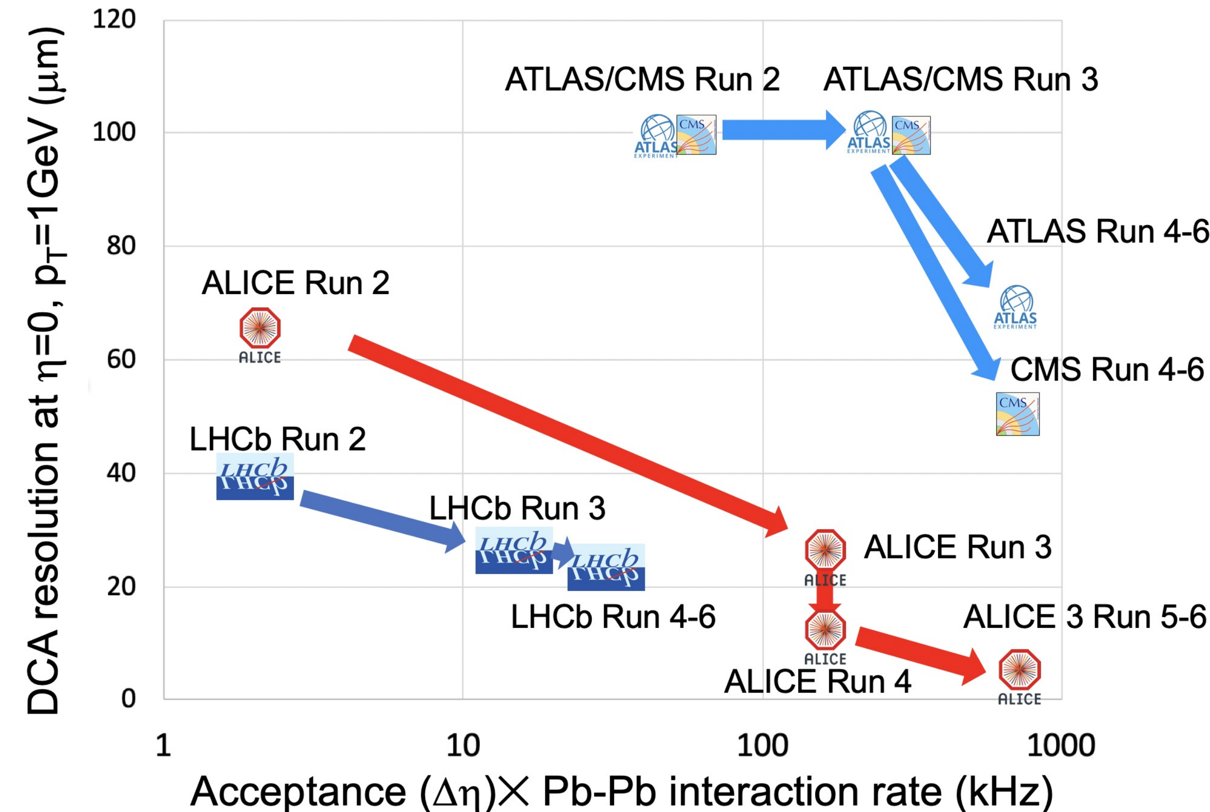
Further Si detector development: ALICE 2.1

ALICE 2 → ALICE 2.1 (for RUN 4)

- Impact parameter resolution reduced by a factor of ~2 in low p_T region
- Tracking efficiency up to more than 30% higher, in low p_T region

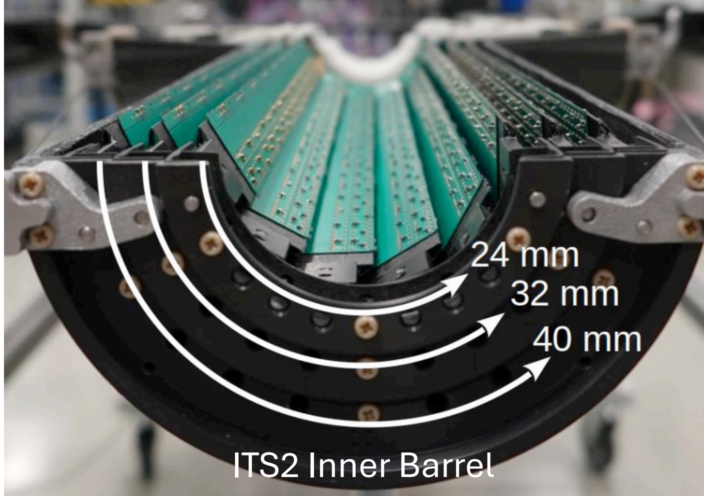
Most striking improvements in the study of:

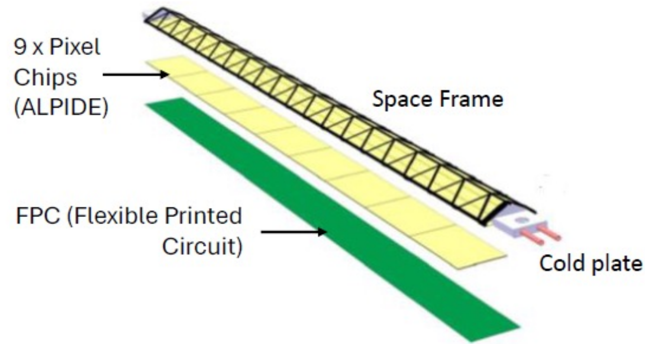
- Low momentum charm and beauty hadrons
- Low-mass dielectrons
- Beauty baryons
- Beauty-stange mesons
- Charm strange and multi-strange baryons
- Light charm hypernuclei

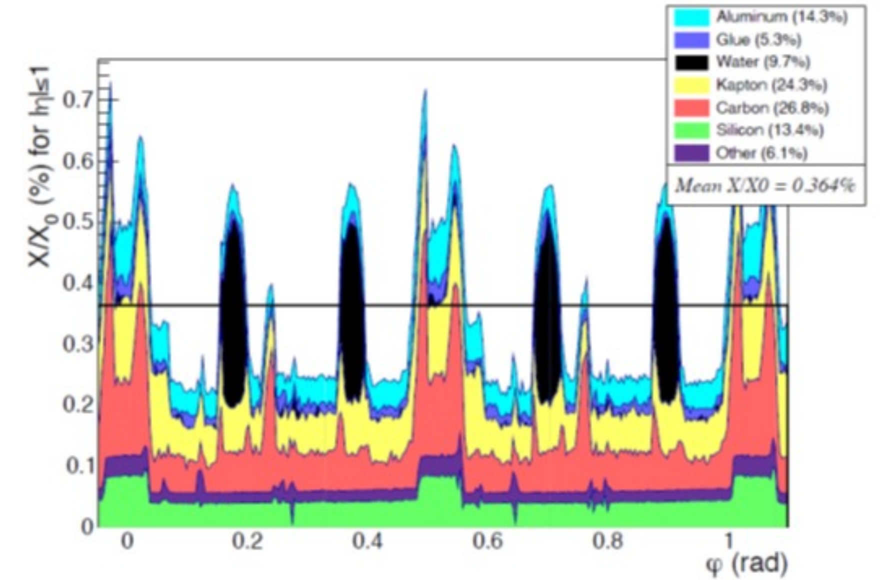


How to improve: ITS2 → ITS3

ALICE





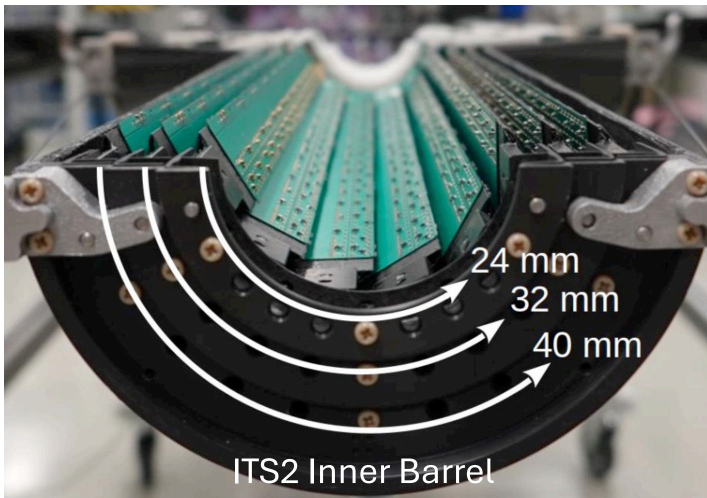


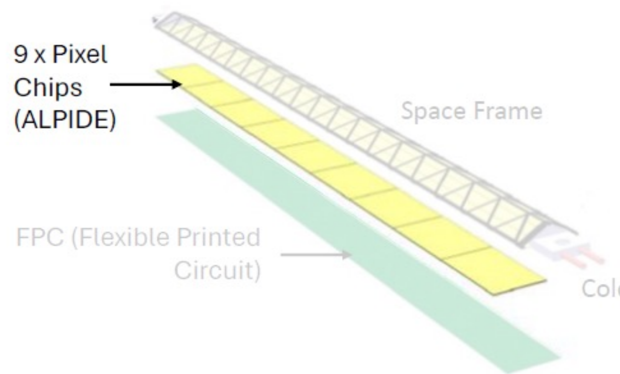
Non-sensitive material:
Silicon has 1/7 of total material budget

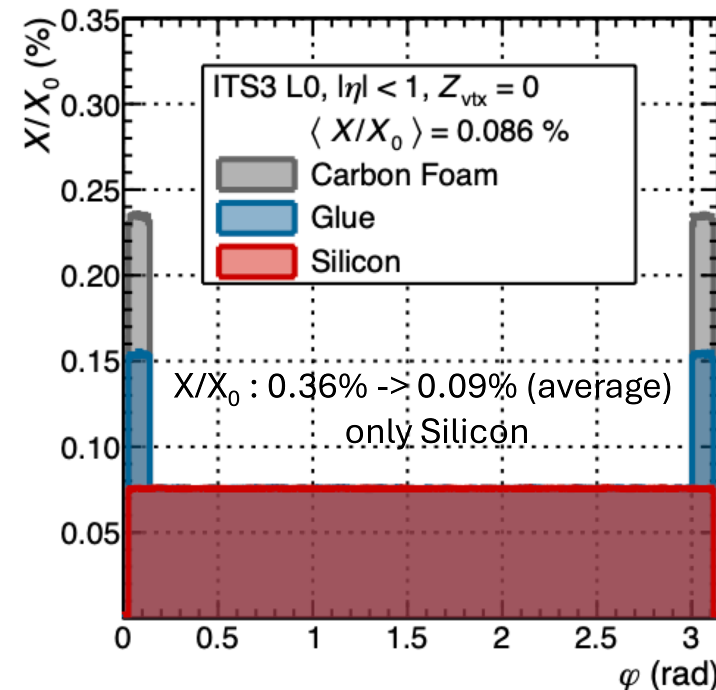
Non-uniformly distributed material & Irregularities:
Stave overlapping, support and water-cooling structure

Unable to be closer to the interaction point:
Mechanical constraints

How to improve: ITS2 → ITS3







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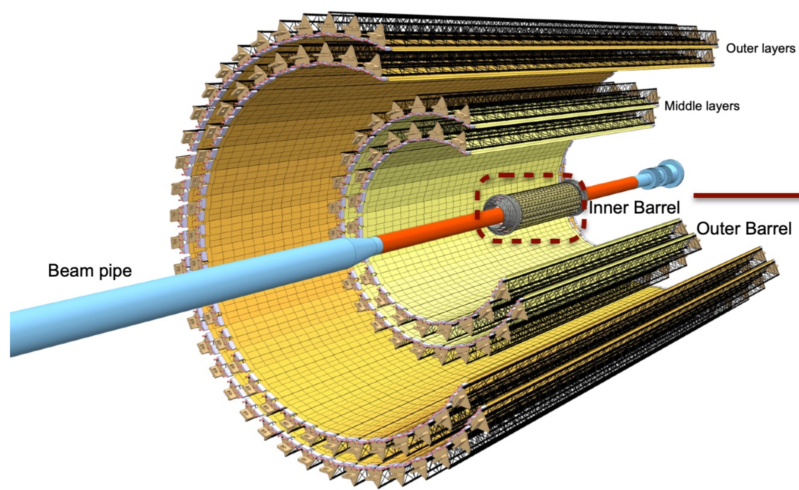
Mechanical constraints

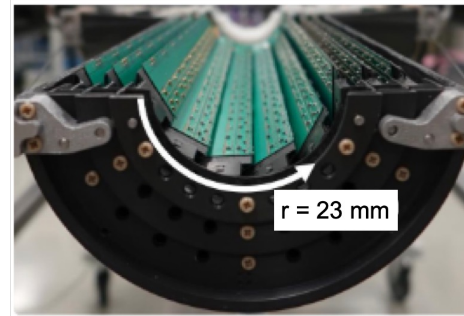
Removal of water cooling
Possible if power consumption stays below 40 mW/cm^2

Removal of circuit boards (power and data)
Possible if integrated on Silicon sensors

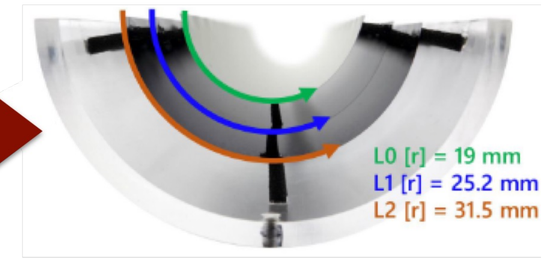
Removal of mechanical structure
Stability due to bent Silicon wafers

From ITS2 to ITS3

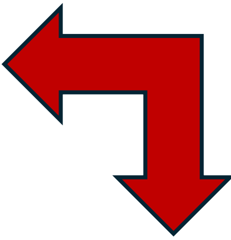




ITS2 Inner Barrel

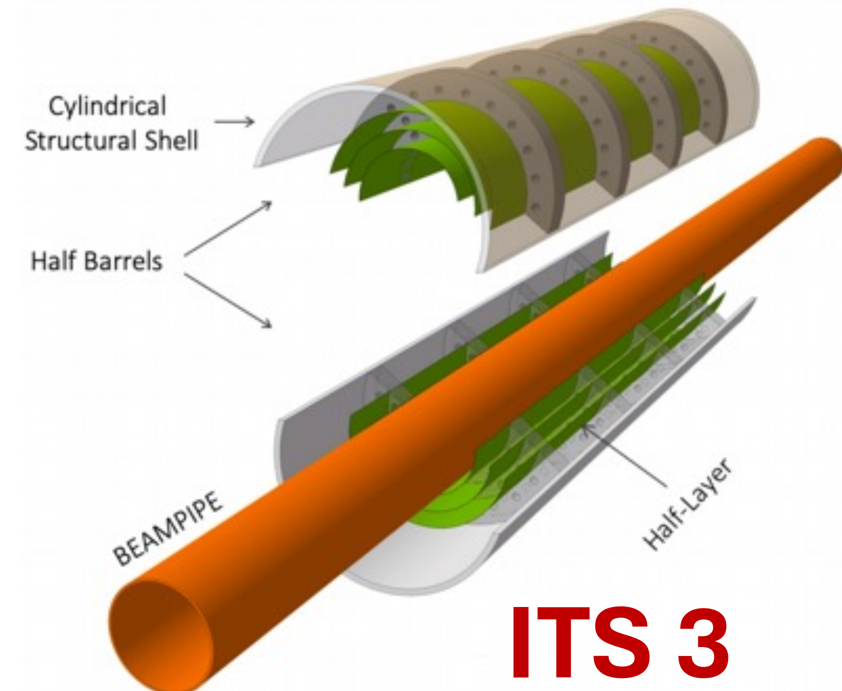


ITS3 Engineering Model 1

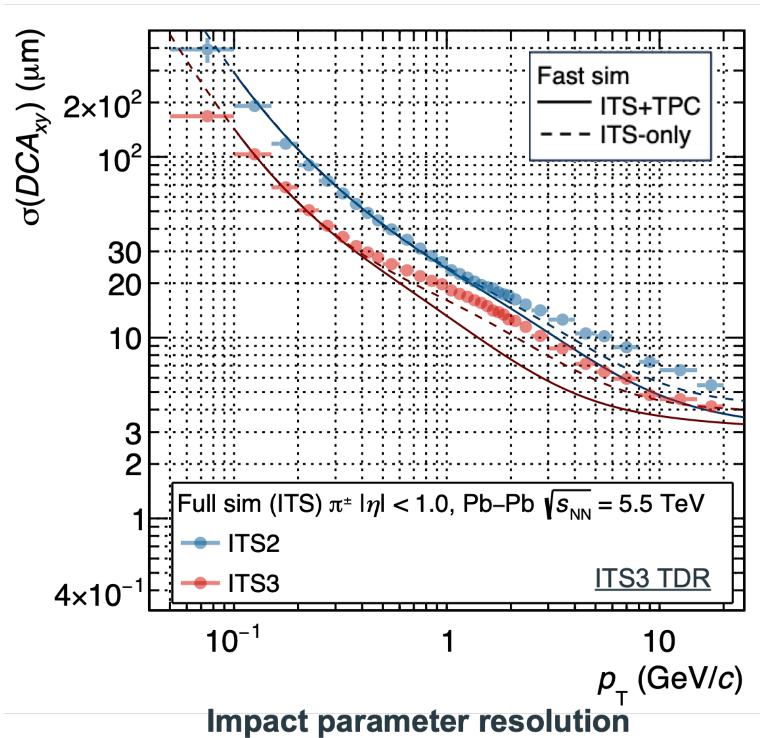


- Replacement of ITS2 Inner Barrel with 3 new ultra-light, truly cylindrical layers of curved 50 μm thick wafer-scale sensors (1 sensor per half-layer) MAPS in 65 nm technology
- Air cooling and ultra-light mechanical supports (carbon foam)
- Reduced material budget: 0.36% X_0 => 0.09% X_0 per layer very homogenous material distribution (water cooling, circuit boards and mechanical support removed)
- Innermost layer radius: 23 mm =>19 mm
- Beam pipe radius: 18 mm => 16.2 mm

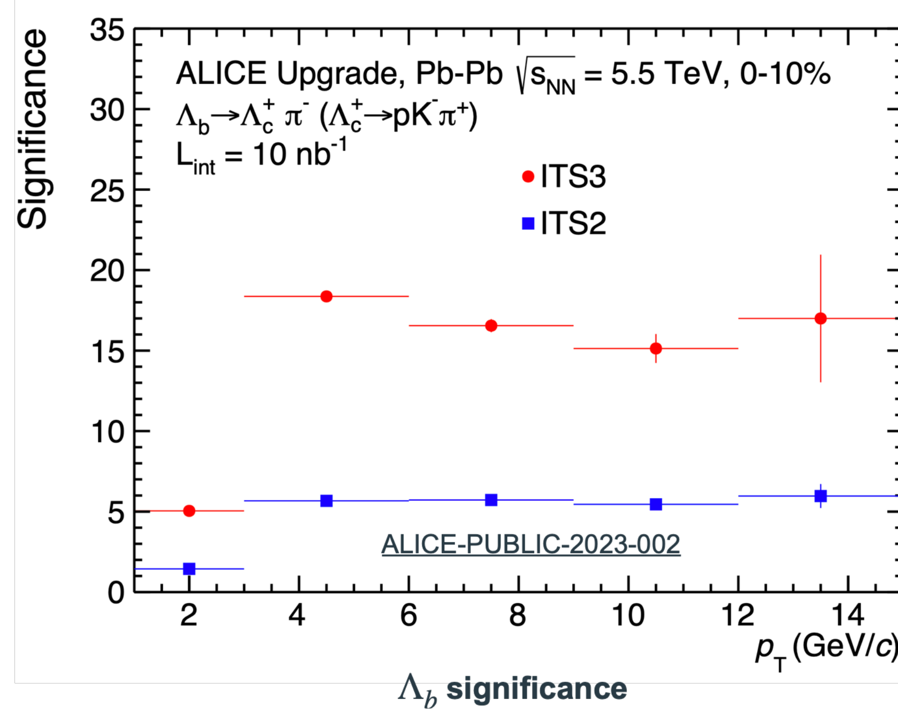
ITS3 TDR — CERN-LHCC-2024-003



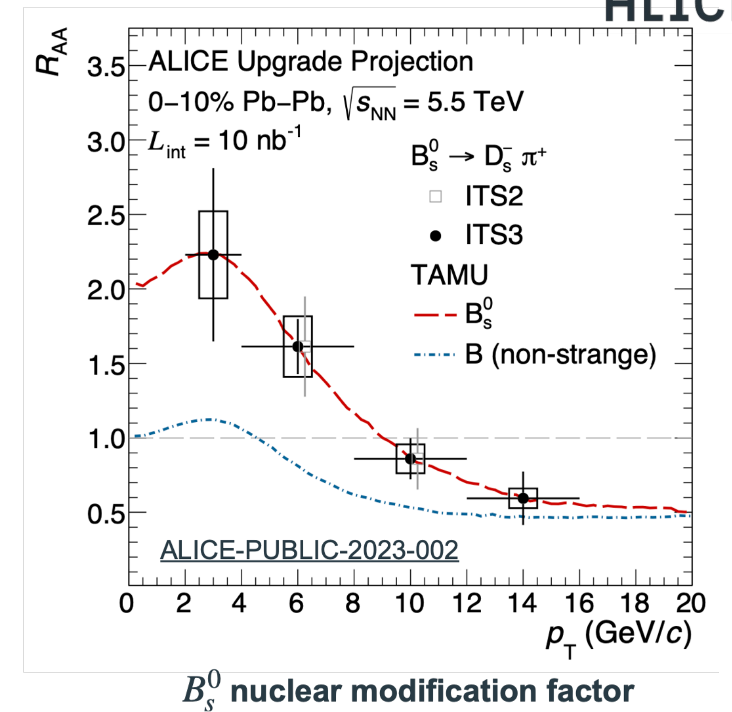
ITS3 Physics Impact



Impact parameter resolution



Λ_b significance



B_s^0 nuclear modification factor

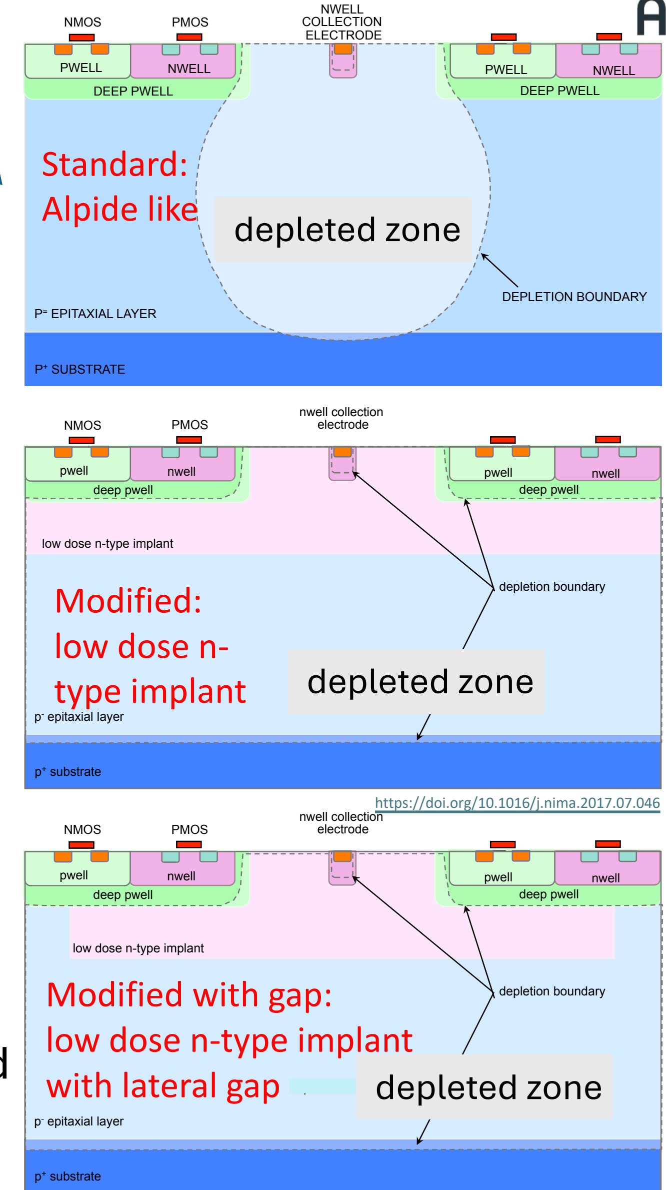
- DCA resolution improved by about a factor of 2 improved separation of secondary vertices
- Many fundamental observables strongly profiting or becoming in reach
  - Charmed and beauty baryons
  - Low-mass di-electrons
  - Full topological reconstruction of B_s

ITS3 physics performance studies: ALICE-PUBLIC-2023-002

Optimization of the sensor

TECHNOLOGY: MAPS in 65 nm CMOS process

- GOAL: create planar junction using deep **low dose n-type implant** and **deplete the epitaxial layer**: same approach as 180nm
- Additional deep p-type implant or **gap in the low dose n-type implant improves lateral field near the pixel** boundary and accelerates the signal charge to the collection electrode.
- Process modification developed in the ALICE ITS2 R&D context
- Further optimised within ATLAS R&D
- Experience with 180 nm => 65 nm CIS process could be modified
- Full depletion => new applications: faster charge collection, higher radiation hardness



3 main pixel designs implemented

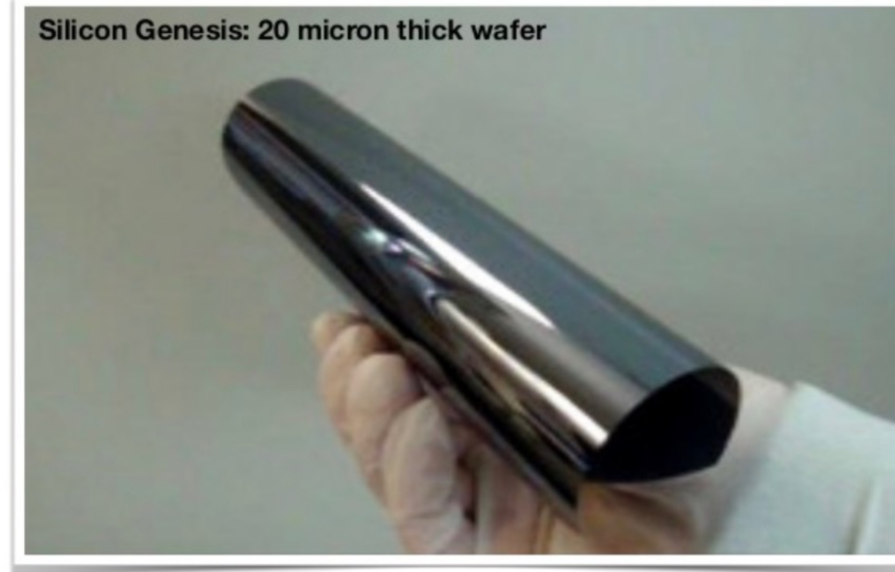
[*A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance, NIM A871 (2017) 90*]

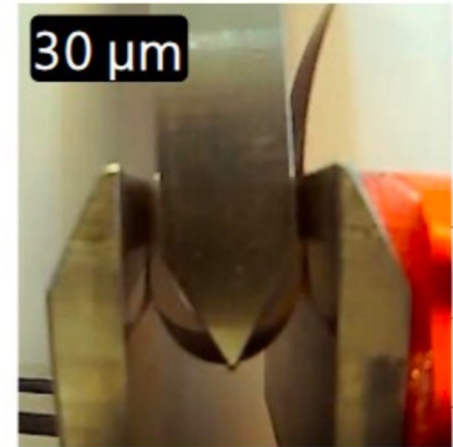
[*https://doi.org/10.22323/1.420.0083*]

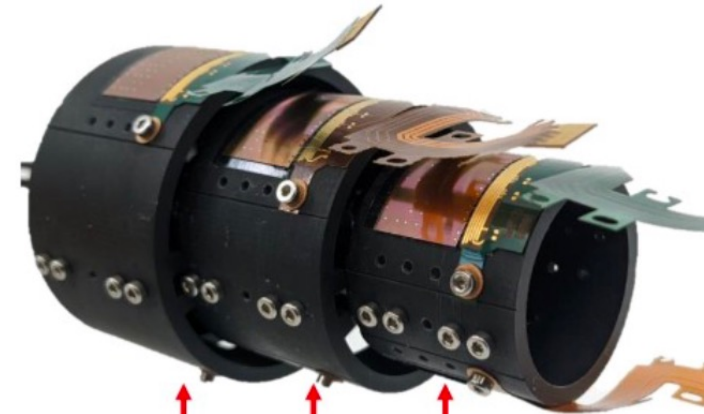
[*https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013*]

ITS3 requirements and R&D

- **MAPS in 65 nm technology** (TPSCo* CMOS)
- 300 mm wafer-scale chips, fabricated using **stitching****
- **Bending of silicon,** thinned to ≤ 50 µm → Flexible (bent to target radii)
- Air cooling and ultra-light mechanical supports (carbon foam)







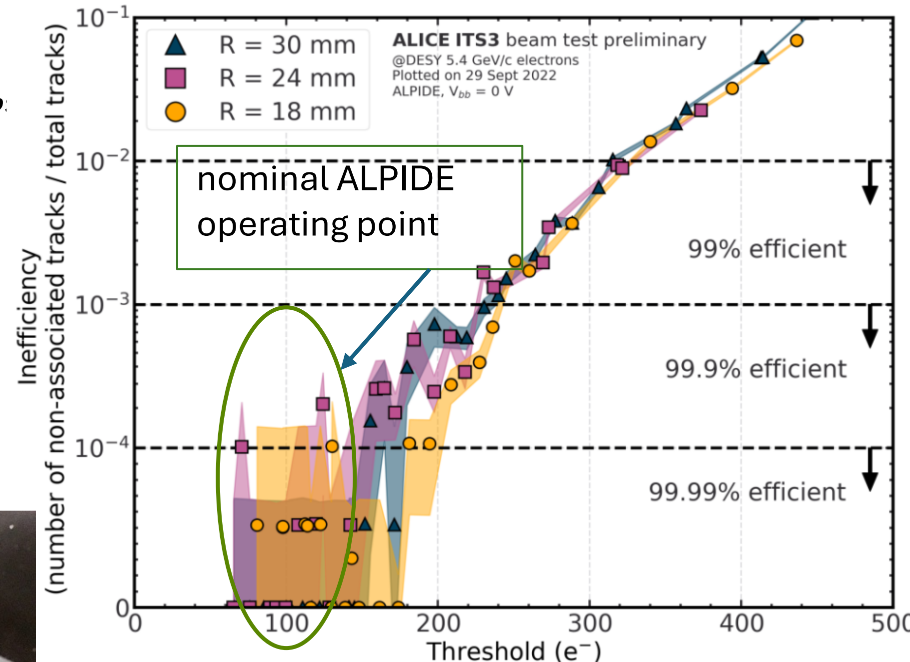
ALPIDEs (180 nm) bent to ITS3 target radii

* Tower Partners Semiconductor Company

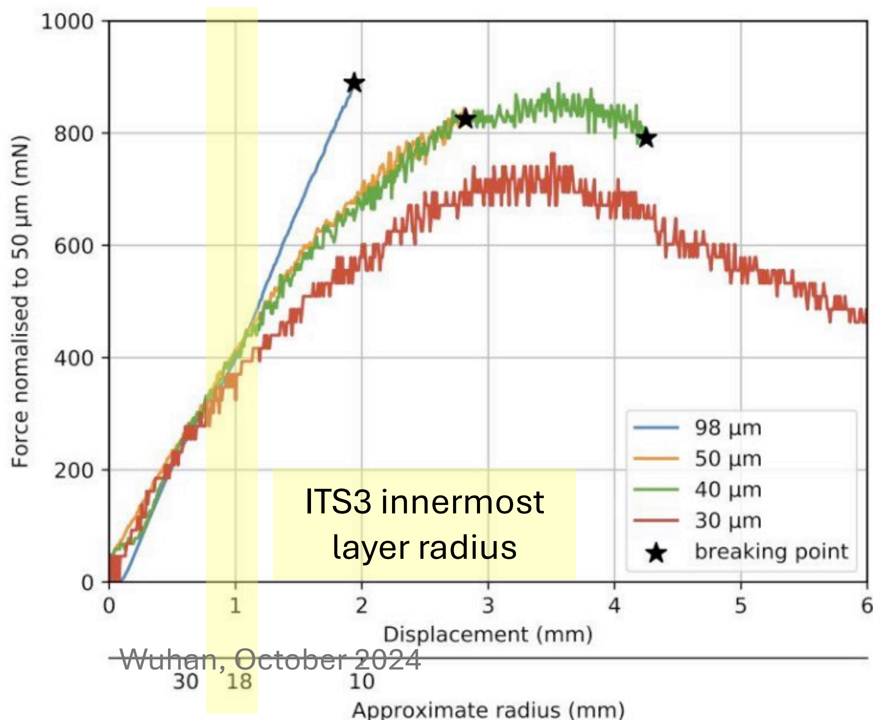
** **Stitching technique:** *Tower Semiconductor Ltd. Stitching design rules for forming interconnect layers, US Patent 6225013B1. 2001.*

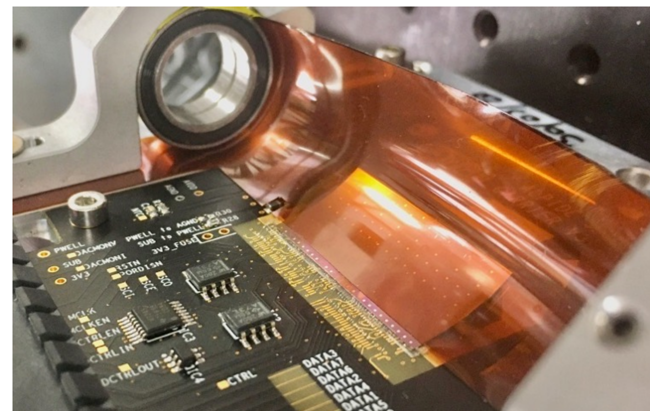
ITS3 ALPIDE chip sensor bending

- Beam tests at DESY TB24 with $E_{e^- beam}$ = 5.4 GeV (testbeam telescope consisting of 6 flat ALPIDE tracking planes)
- Project target for thicknesses and bending radii are in a "not breaking" regime
- Results validated on bent 65 nm pixel test structures
- 50 µm thick ITS2 chip (ALPIDE) bent to 22 mm showed excellent efficiency in TB; no significant variation in the performance
- No degradation of detection efficiency & spatial resolution observed



First results on bent MAPS, NIM A 1028 (2022) 166280





- bent MAPS feasibility demonstrated for the first time
- no sign of any deterioration in operations
- important milestone in the R&D for ALICE ITS3

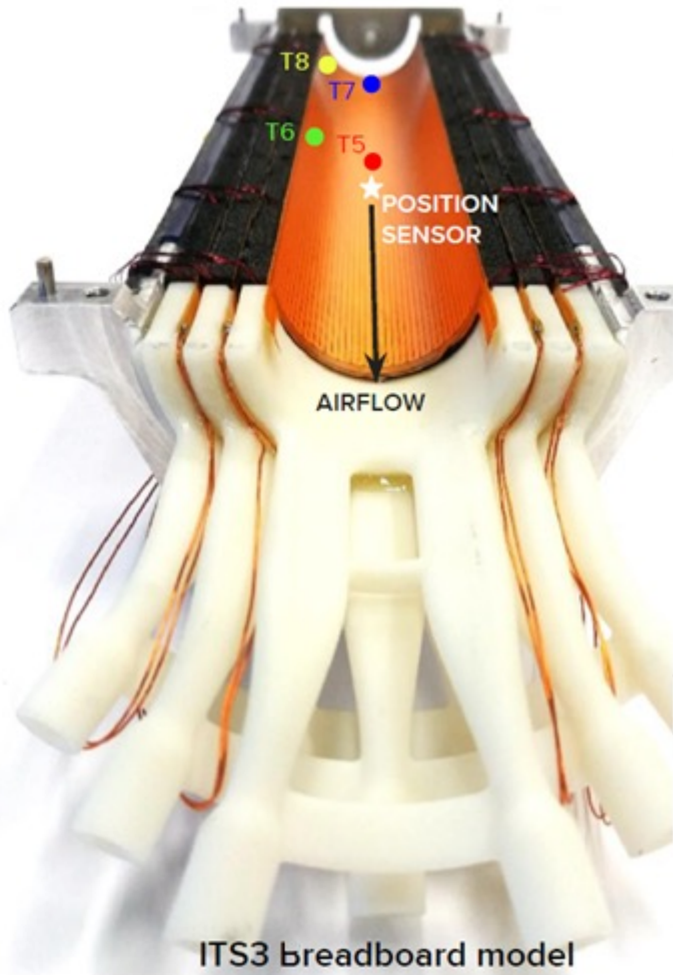
Air cooling: thermo-mechanical performance

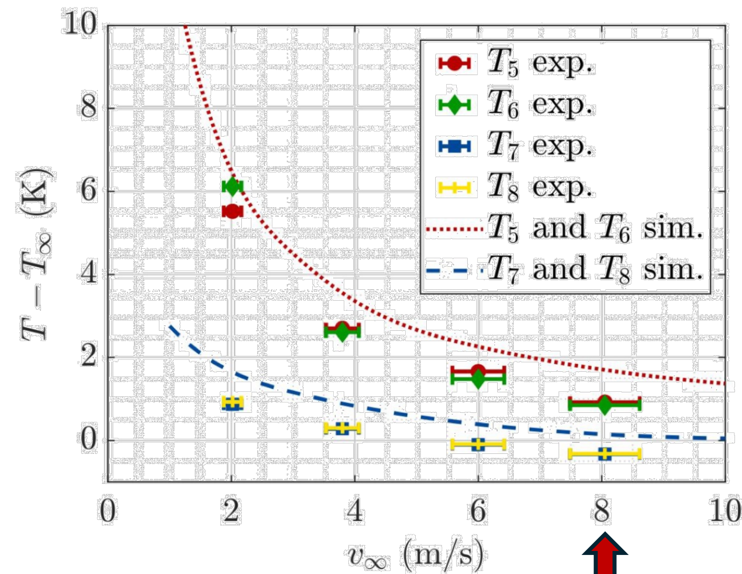
Breadboard model based on silicon with added Kapton heaters

Airducts for precise flow control

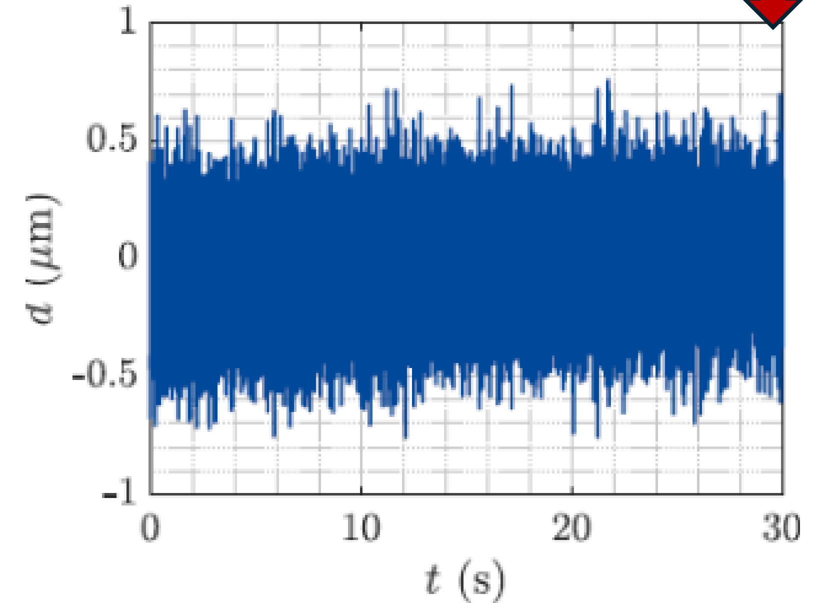
Tests in wind tunnel (with laser measurements system for vibrational analysis) :

- Si and polyimide sandwich with copper serpentines embedded
- exemplary power consumption: 1000 mW /cm^2 in end-caps, 25 mW /cm^2 in matrix
- $\Delta T < 5°C$ and vibrations within ± 0.5 μm with 8 m/s airflow



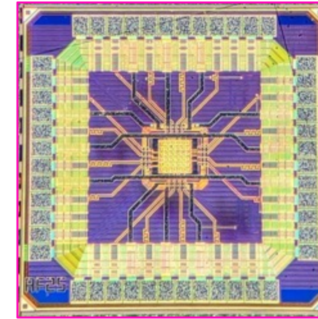


(c) Layer 0 - Matrix

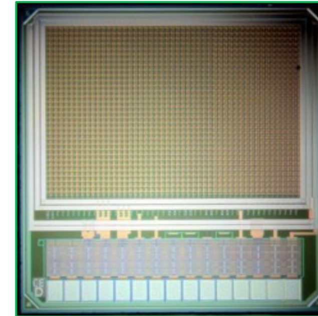


MLR1: 65 nm technology validation

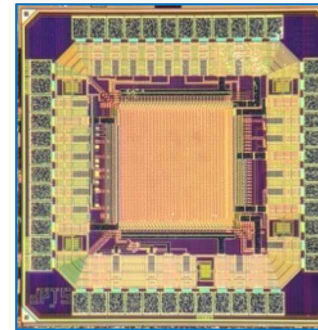
- ALICE ITS3 together with CERN EP R&D
  - leverages on experience with 180 nm (ALPIDE)
  - excellent links to the foundry
- 65 nm chips benefits:
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - larger wafers (200 mm → 300 mm)
- ITS Pixel prototype chips selection: APTS, CE65, DPTS
- Main goals:
  - learn technology features
  - characterize charge collection
  - validate radiation tolerance
- Testing since September 2021:
  - huge effort shared among many institutes
  - laboratory tests with ^{55}Fe source
  - beam tests @ PS, SPS, Desy, MAMI
- Extensive qualification strategy: validation in terms of charge collection efficiency, detection efficiency and radiation hardness



APTS: Analogue Pixel Test Structure
- matrix: 6×6 pixels
- readout: direct analogue of central 4×4 submatrix
- pitch: 10, 15, 20, 25 μm



CE65: Circuit Exploratoire 65 nm
- matrix: 64x32, 48x32 pixels
- readout: rolling shutter analogue
- pitch:15, 25 μm



DPTS: Digital Pixel Test Structure
- matrix: 32×32 pixels
- readout: asynchronous digital with ToT
- pitch: 15 μm

AREA: 1.5×1.5 mm^2

DPTS radiation hardness

T = 20°C

Detection efficiency (%) — 70, 75, 80, 85, 90, 95, 99, 100

Fake-hit rate ($pixel^{-1}\ s^{-1}$) — 10^{-3}, 10^{-2}, 10^{-1}, 10^{0}, 10^{1}, 10^{2}, 10^{3}

Threshold (via V_{casb}) (e^-) — 75, 100, 125, 150, 175, 200, 225, 250, 275, 300, 325, 350

FHR measurement sensitivity limit

DPTS (15 µm pixel pitch)

- Detection efficiency
- Fake-hit rate
- Non-irradiated
- 10^{13} 1MeV n_{eq} cm^{-2}
- 10^{14} 1MeV n_{eq} cm^{-2}
- 10^{15} 1MeV n_{eq} cm^{-2}
- 10 kGy
- 100 kGy
- 10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}

requirements for ITS3 satisfied

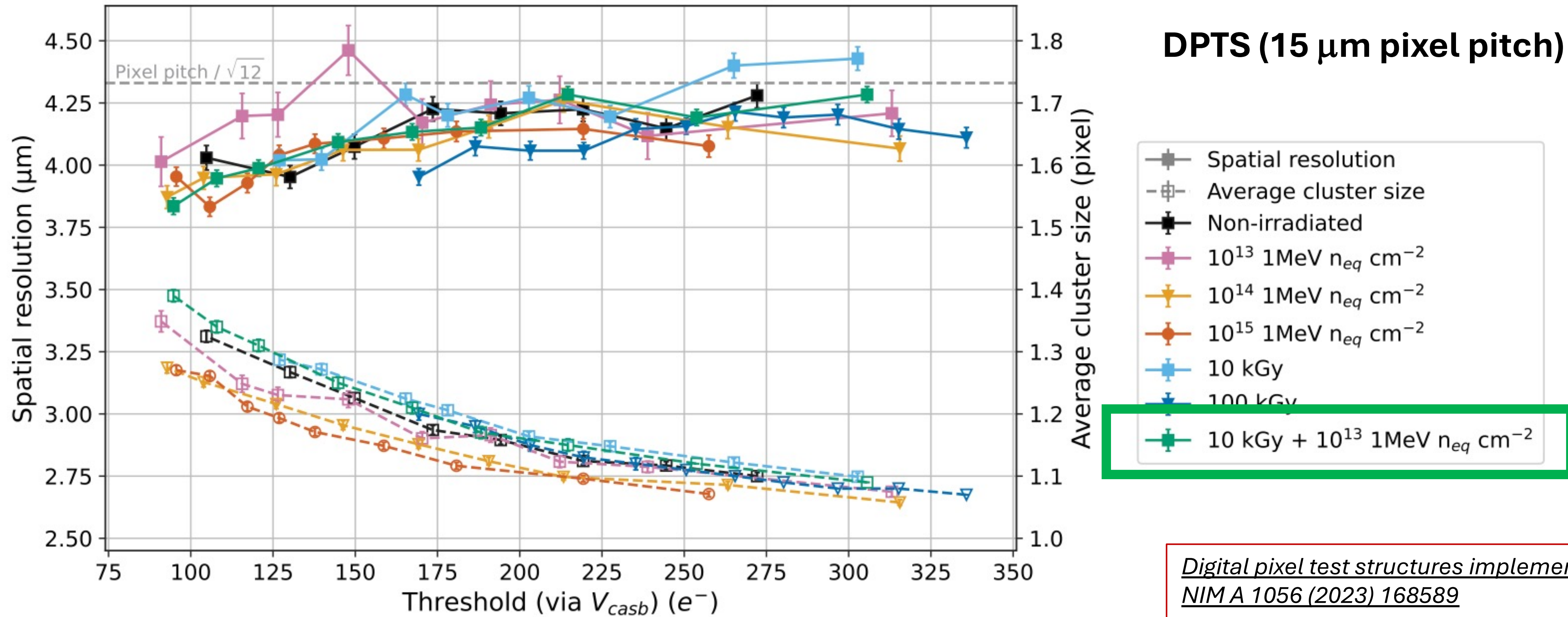
Digital pixel test structures implemented in a 65 nm CMOS process, NIM A 1056 (2023) 168589

Detection Efficiency and Fake Hit Rate vs Average Threshold (V_{sub} = -2.4 V)

Irradiation dose indicated by different colors

Efficiency > 99% and FHR < 2×10^{-3} pix^{-1} s^{-1} after irradiation at ITS3 requirements

DPTS spatial resolution



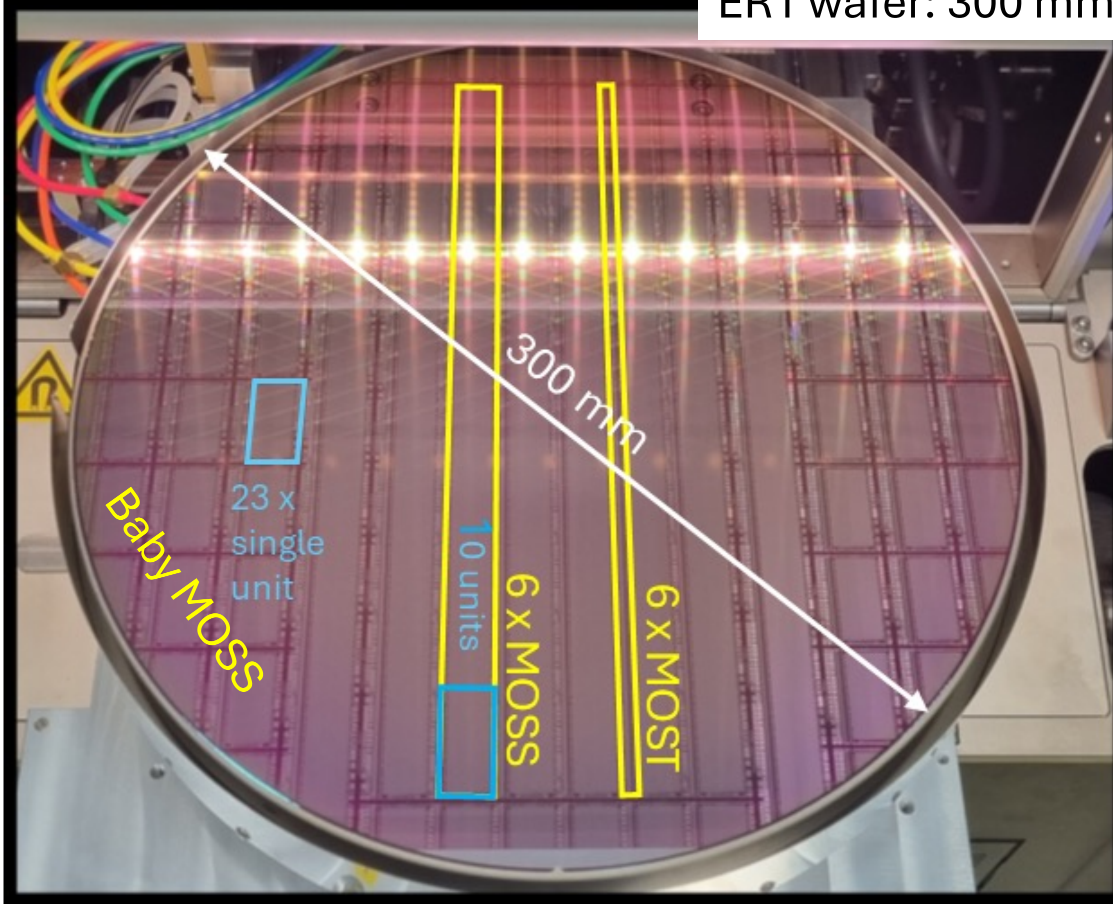
Digital pixel test structures implemented in a 65 nm CMOS process, NIM A 1056 (2023) 168589

Spatial Resolution (solid lines) and Average Cluster Size (dashed lines) vs Threshold

spatial resolution measured slightly better than pixel pitch / √12 (no degradation with received dose)

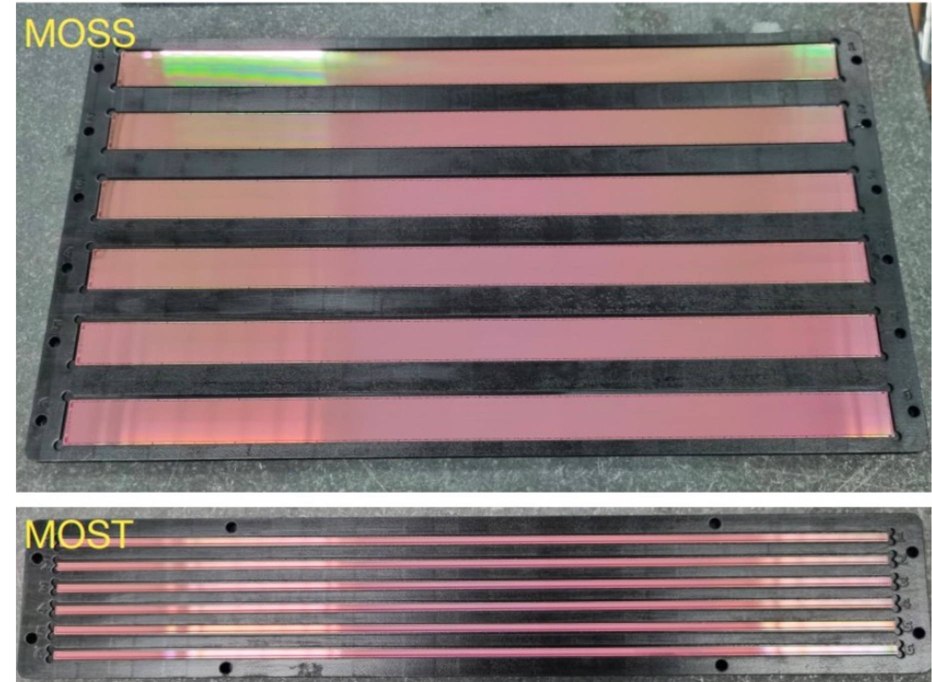
light systematic decrease of average cluster size with the increasing non-ionising radiation dose

Stitched MAPS in Engineering Run1 (ER1, 65 nm)

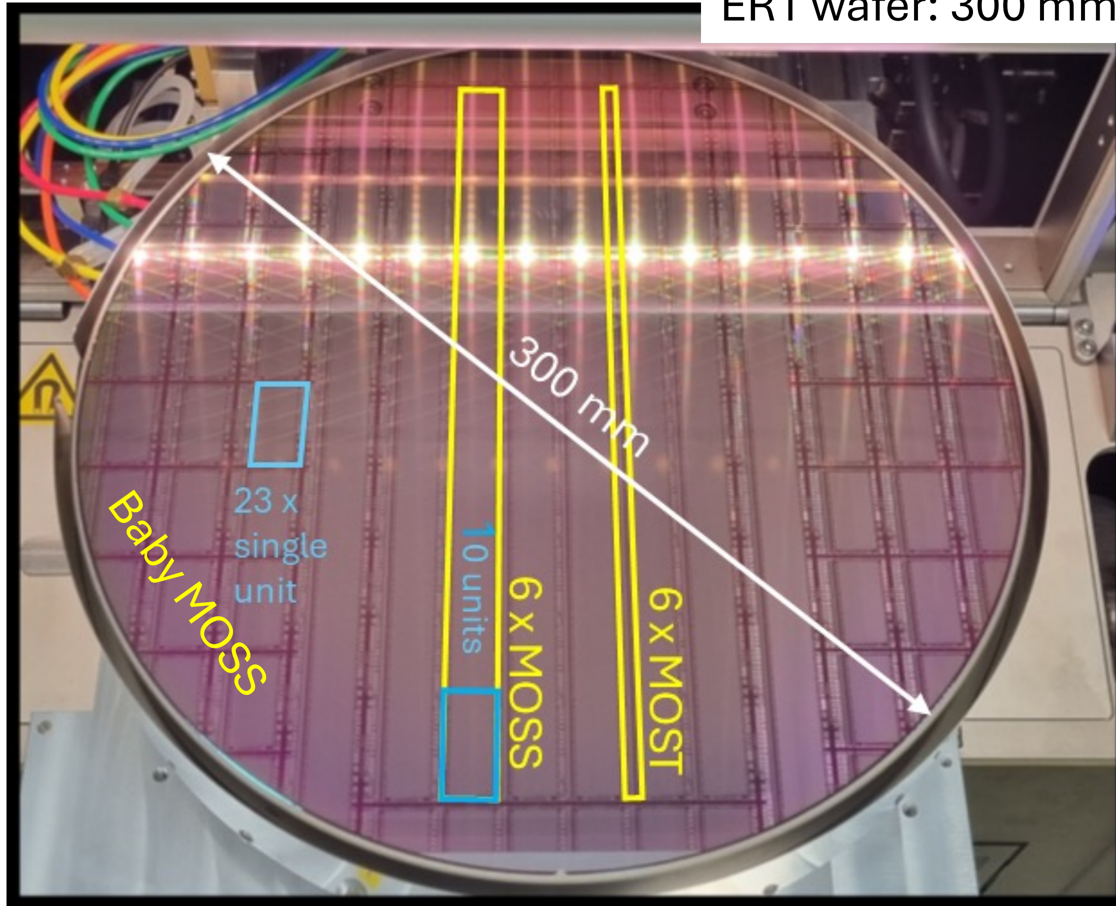


ER 1 first stiched MAPS, large design exercise (300 mm)

2 stitched prototypes produced in summer 2023,
24 wafer, 6 of each sensor per wafer



Stitched MAPS in Engineering Run1 (ER1, 65 nm)



ER 1 first stiched MAPS, large design exercise (300 mm)

MOSS - MOnolithic **S**titched **S**ensor (14 x 259 mm^2)
- 6.72 Mpixel, different pitches (18 and 22.5 μm)
- conservative design

MOST - Timing (2.5 x 259 mm^2)
- 0.9 Mpixel , 18 μm pixels
- more dense design

First subset thinned down to 50 μm

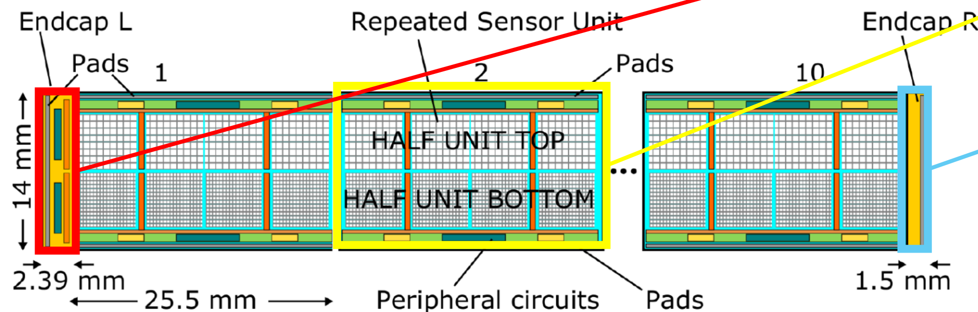
Goals:
- show feasibility of stitching process:
  - manufacturing yield (power segmentation granularity)
  - power distribution and readout over 27 cm length
  - study uniformity, noise, spread, leakage
  - pixel architecture characterization
- understand stitching 'rules', redundancy, fault tolerance

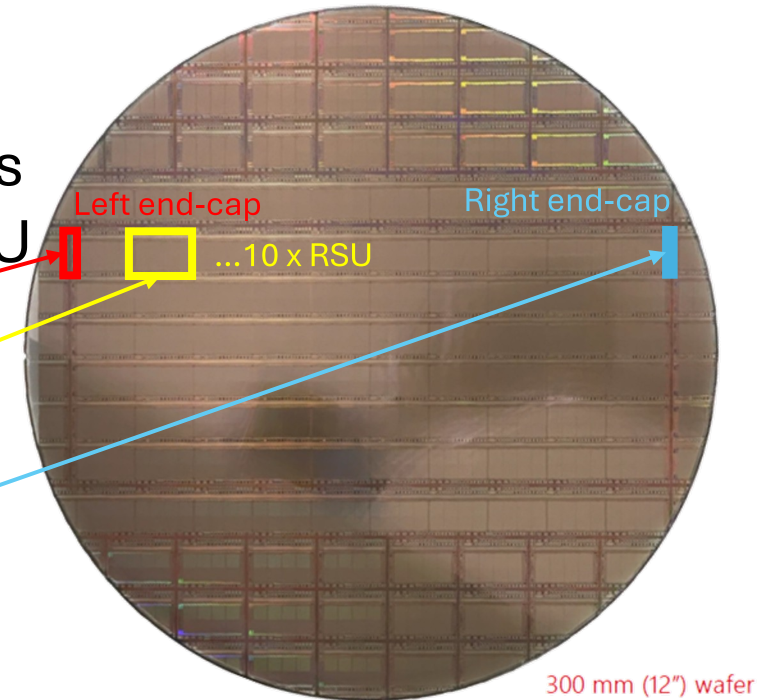
MOSS

MOnolithic Stitched Sensor (MOSS) segmented into:

- 10 Repeated Sensor Units (RSU) & 2 end-caps regions (powering and readout)
- 2 independent Half Units (HU) per RSU
  - Top HU: 4 matrices of 256 x 256 22.5 µm pixels
  - Bottom HU: 4 matrices of 320 x 320 18 µm pixels

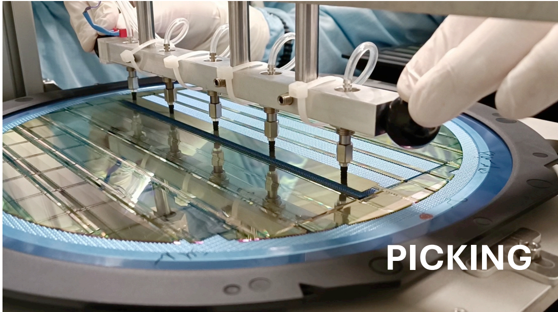
Readout either through left endcap or for every half RSU separately

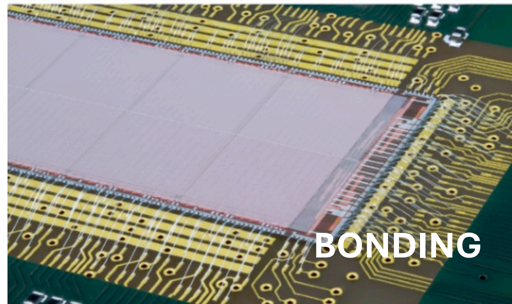


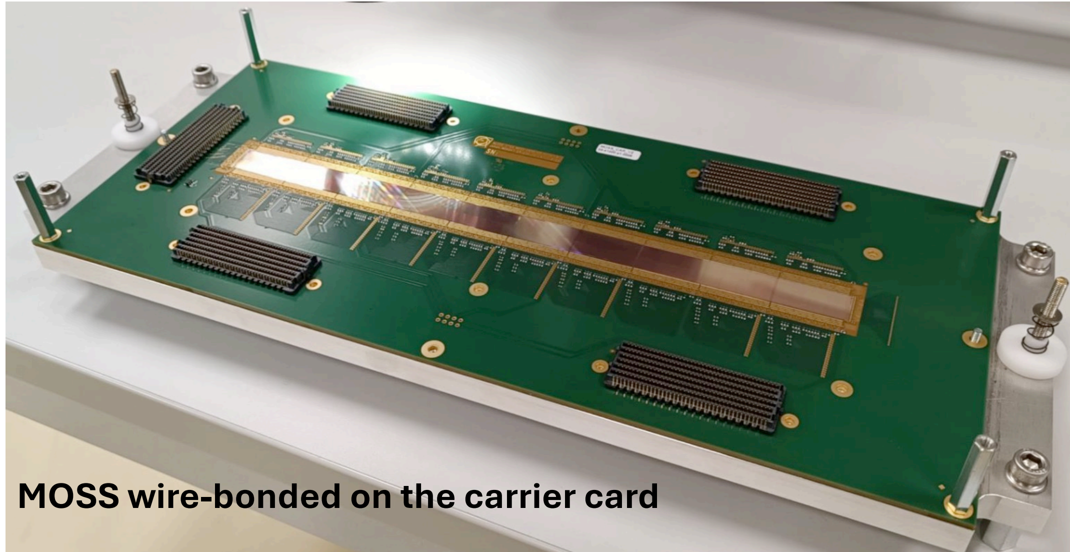


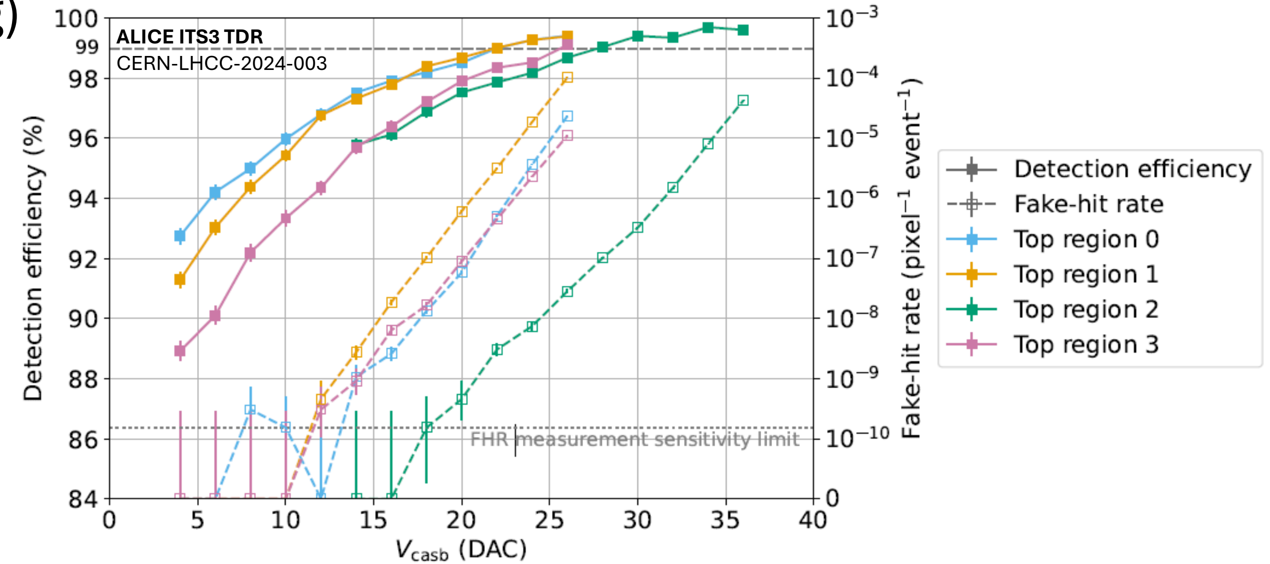
MOSS first testing results

Not trivial to handle a large & thin chip => development of tools and procedures (picking, bonding, mounting)



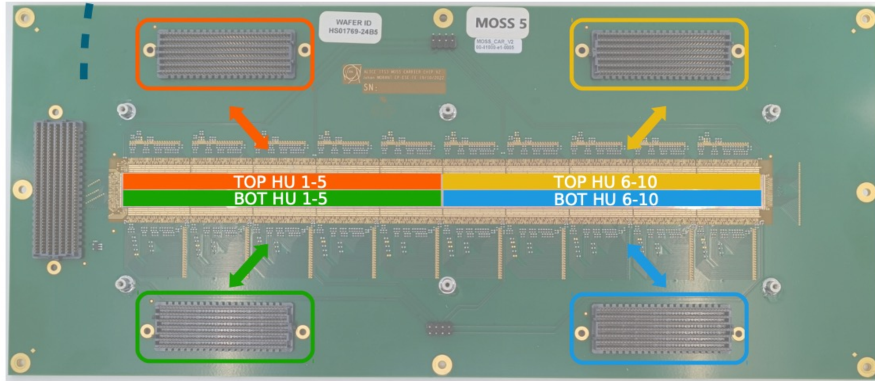






- Beam test at CERN PS
- Chip is operational
- Efficiency and spatial resolutions expected from MLR1 chips ➔confirmed
- Yield: currently under study with extensive characterization campaign with wafer prober. Target < 2% dead pixels per layer

MOSS tests



We operate the MOSS over the long edge for the series testing

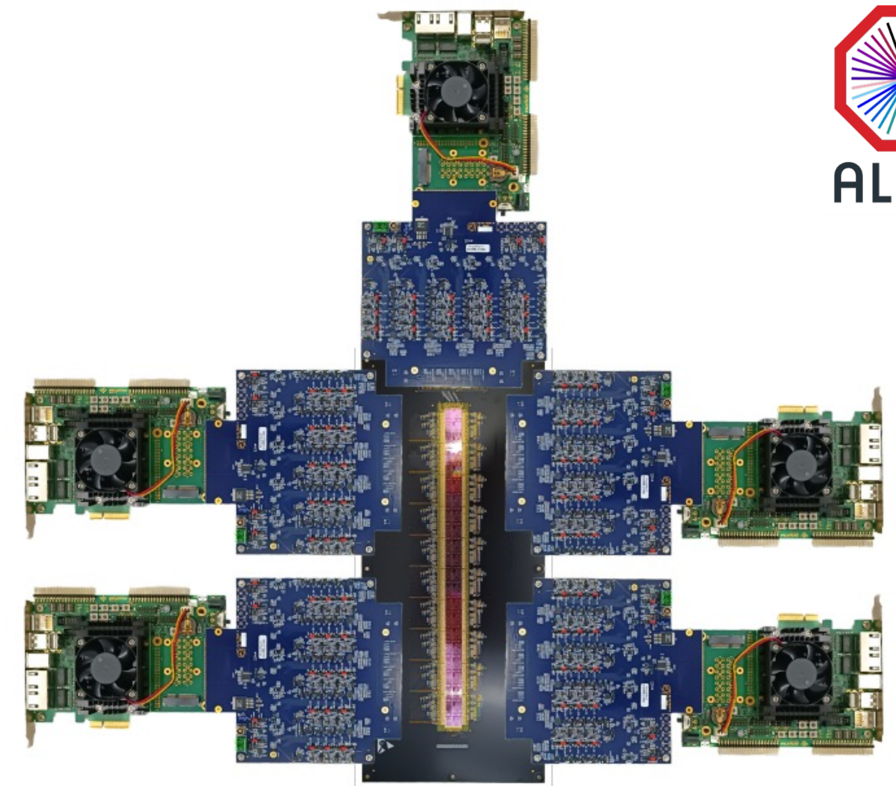
MOSS bonded on carrier

Impedance measurement

Power ramps

Impedance measurement

Full powering and functional test



Power On scan - HU: 100% success
(Shift)Register scan – regions: 98.85% success
DAC scan - DAC units: 99.60% success
Digital scan – regions: 98.85% success
Analogue scan – regions: 98.70% success
THR scan – regions: 98.00% success
FHR scan – regions: 94.70% success
=> Total 99.38% OK

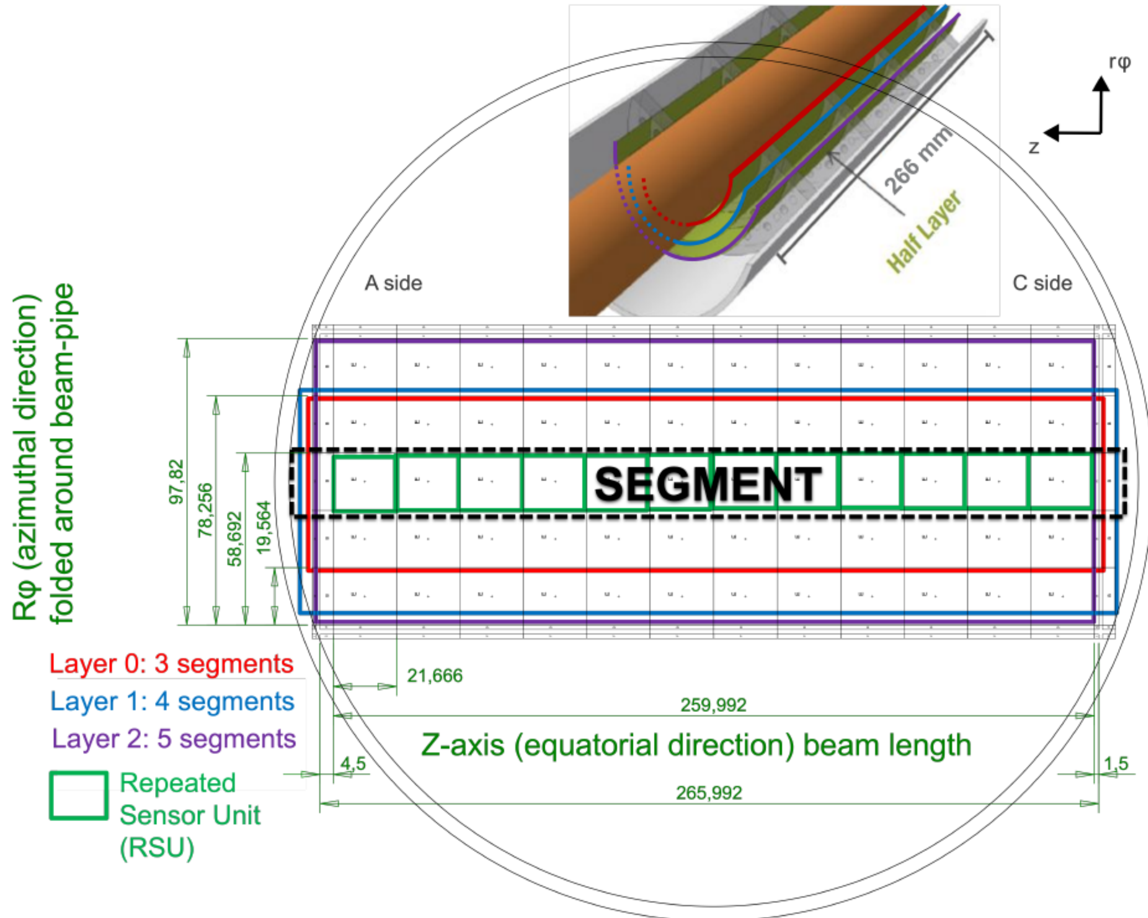
82 MOSS chips bonded on the carrier card
(6 MOSS/wafer * 14 wafer)

Yield & pixel performance: massive check of functionality,
=> no significant lossess

ITS3 milestones

- **ER2 - full size prototype sensor**

Design according to final ITS3 specs and finalised incorporating learnings from MLR1 and MOSS testing:



- modular design: each sensor is divided into 3, 4 or 5 segments with 12 RSUs
- powering and readout only from end-caps
- end-caps acting as a separate readout circuit on the same silicon wafer
- submission to the foundry in fall 2024

- **ER3 – final sensor production**
- **optimization of assembly sequence and detector integration → qualification model (QM) half barrels**
- **final assembly and commissioning**

TDR for ALICE ITS3: CERN-LHCC-2024-003/ALICE-TDR-021

Summary

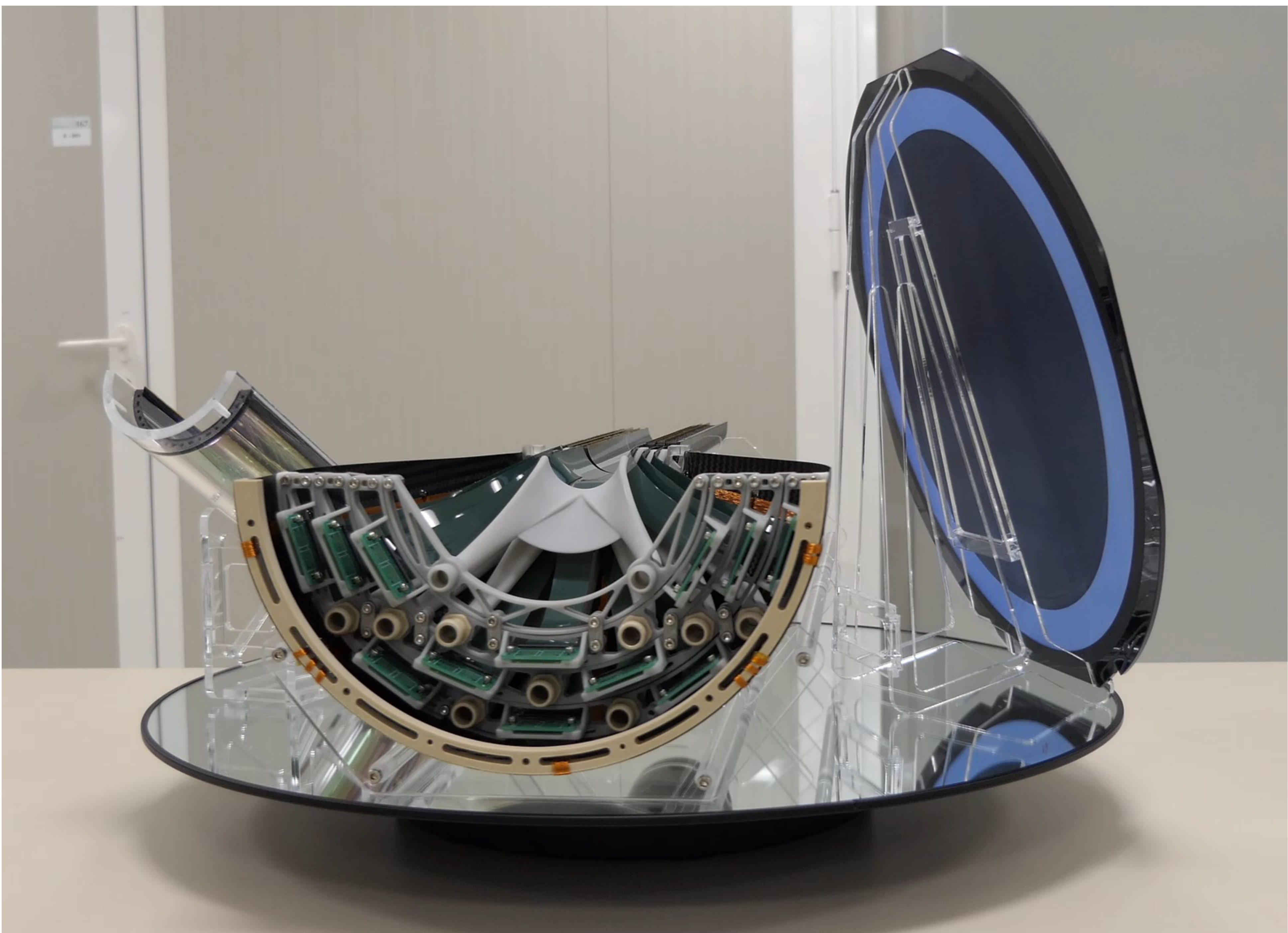
ITS2

- important step forward for the technology of MAPS
- first Monolithic Active Pixel Sensor based Vertex and Tracking Detector at the LHC
- largest and most granular pixel detector to date
- successfully operated in pp and Pb-Pb collisions in RUN3
- many learnings during the actual operations => important inputs for ITS3

ITS3

- further development of silicon detector with a truly cylindrical wafer-scale MAPS:
    - bent MAPS performance demonstrated in TB
    - air cooling tested
    - MAPS based on the TPSCo 65 nm process qualified (MLR1) beyond the needs of ITS3
    - stitching MOSS qualified
    - massive check of MOSS functionality
    - TDR approved, project in production phase, MoU is prepared for signatures

ALICE silicon detectors are at frontier of technology
ALICE ITS3 on track for installation in LS3



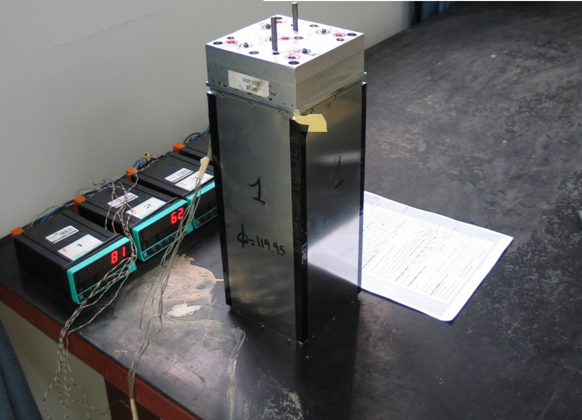
ALICE ITS3
for CERN 70’s

Thanks to
Magnus Mager
shown at the
ALICE Upgrade
Week
7-11/10/2024
Kracow

Wuhan – DCAL 2011

bundle preparation

fibers preparation


first DCAL module

module assembly

Wuhan assembly station

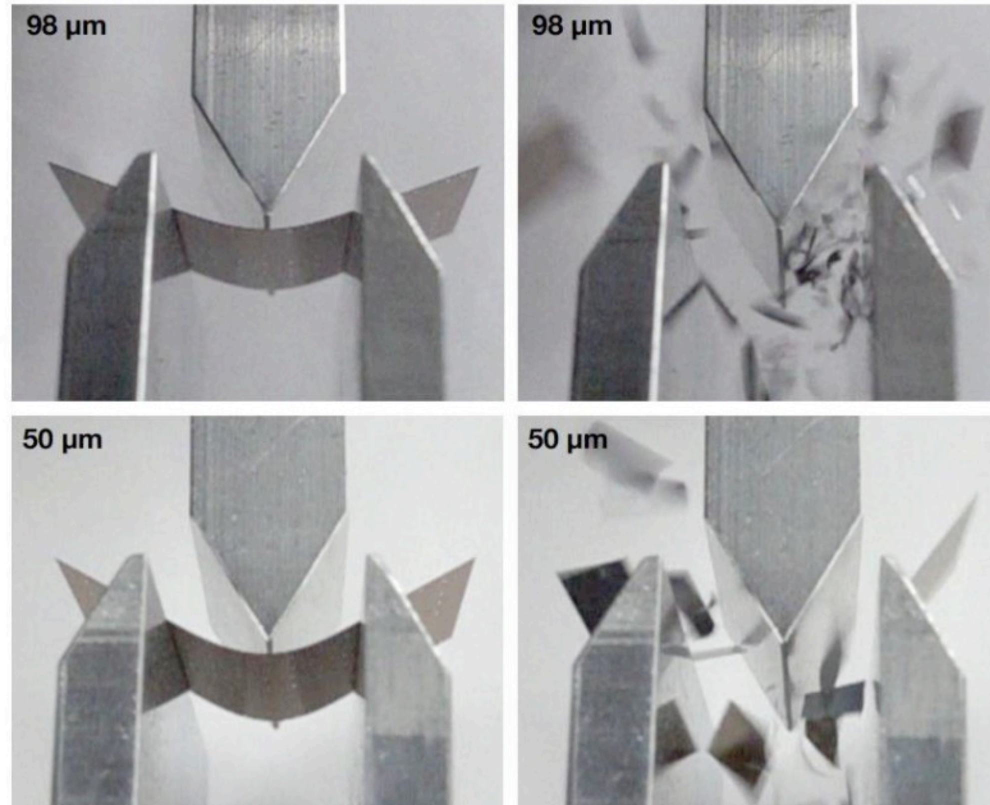
Thank you

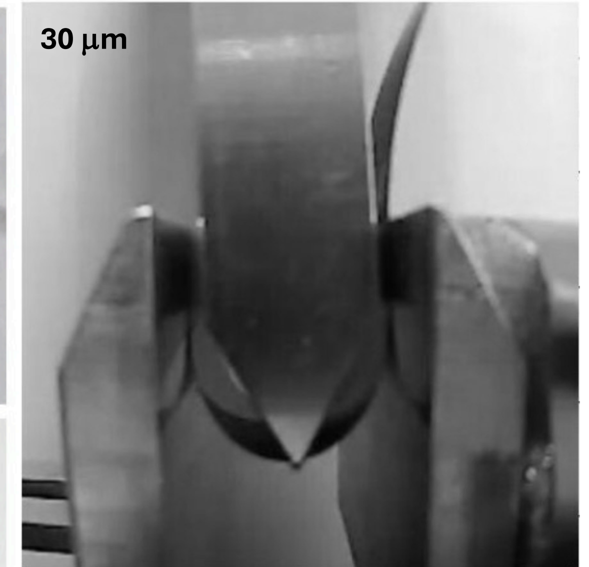
BACKUP

ITS3 sensor bending

ALICE

- MAPS of ~50 μm thickness are quite flexible
- The bending force scales with thickness to the third power → large benefit from going even a bit thinner
- The breaking point moves to smaller bending radii when going thinner

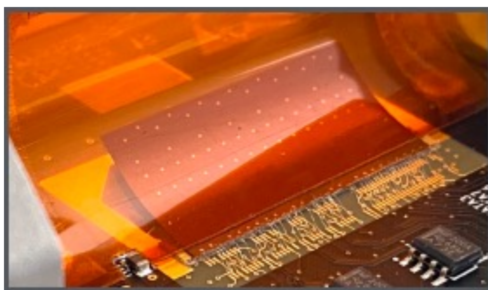




ITS3 sensor bending

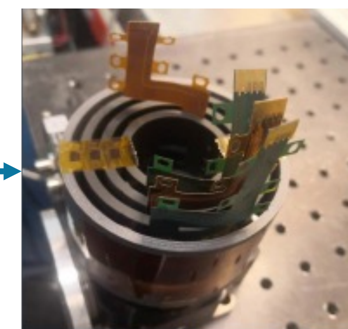
Beam test campaigns on bent ALPIDEs:

1. First bent chip (DESY, Jun 2020)



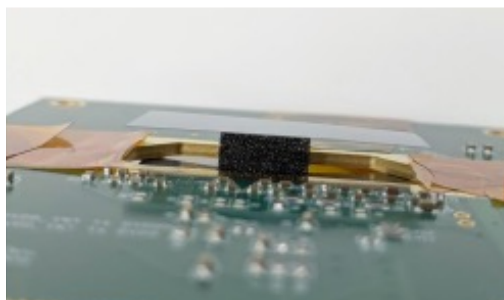
2. Bent chip on cylinder (DESY, Aug/Dec 2020)

3. Bent chips at all radii, carbon foam (DESY, Apr 2021)



4. μITS3 with 6 ALPIDE + target (SPS, Jul 2021)

5. Carbon foam (DESY, Sep 2021)



Air cooling

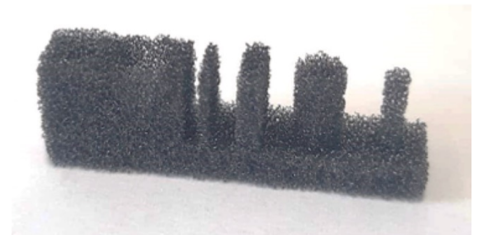
CARBON FOAM SUPPORT STRUCTURE

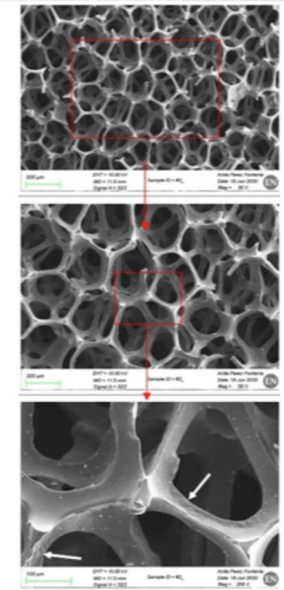
- Different foams were characterized for machinability and thermal properties
- Baseline is ERG DUOCEL_AR, which also features the largest radiation length

ERG DUOCEL_AR

0.06 kg/dm^3

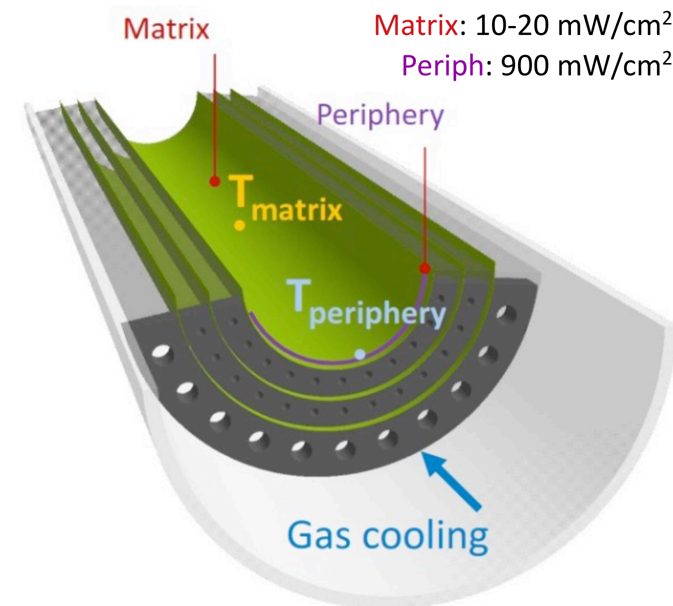
0.033 W/m·K





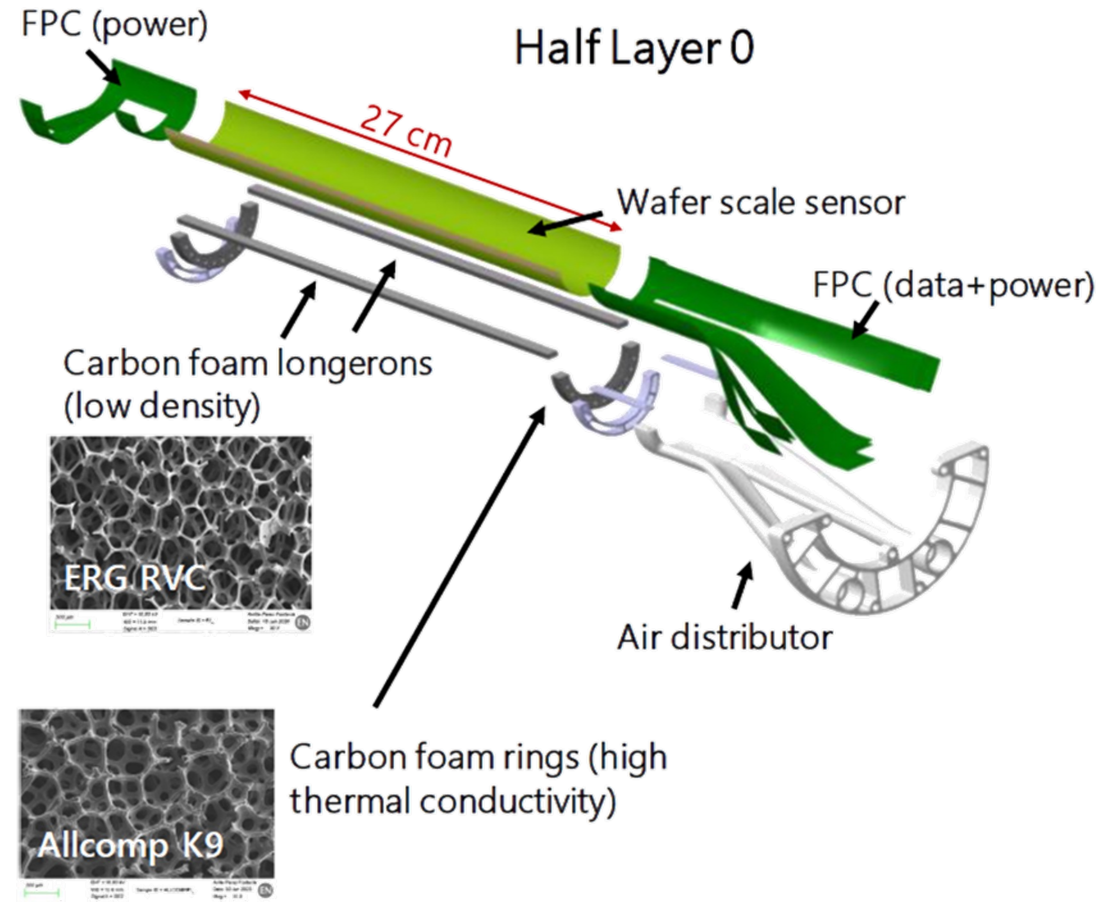
COOLING STUDIES: wind tunnel

- Tests with model and heaters
- Different power & air speed (between 2 and 8 m/s)
- Thermal and mechanical properties are studied on estimated power consumption
- Carbon foam radiator are key for heat removal at periphery
- Air cooling is feasible with margin

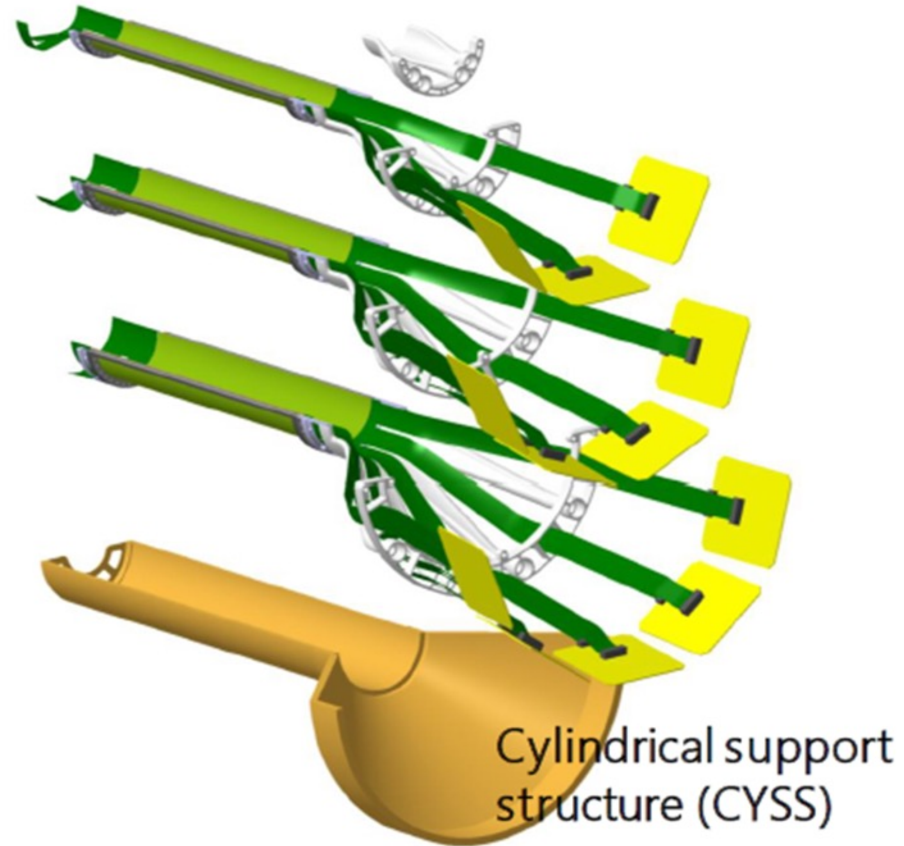


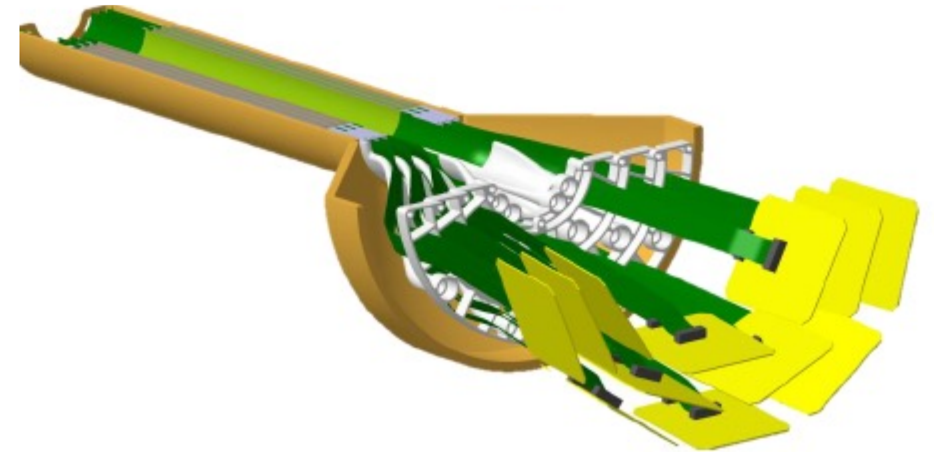
ITS3 layout

ALICE

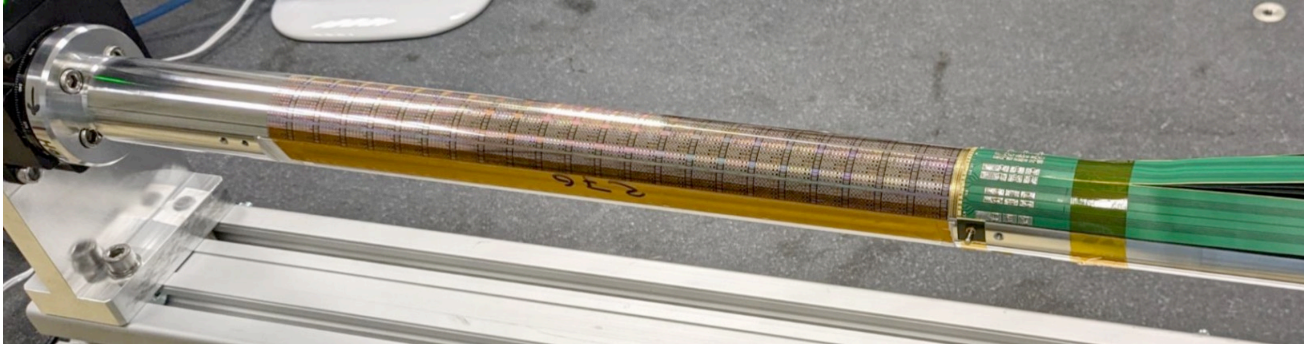


ITS3 layout

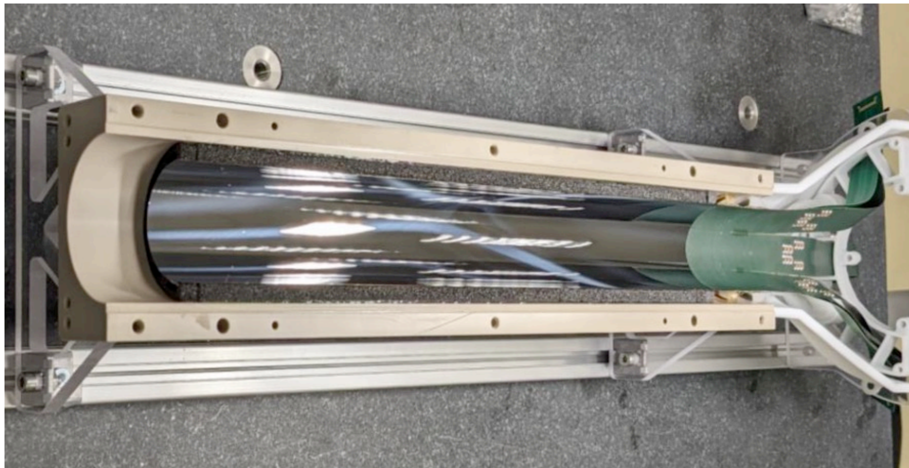




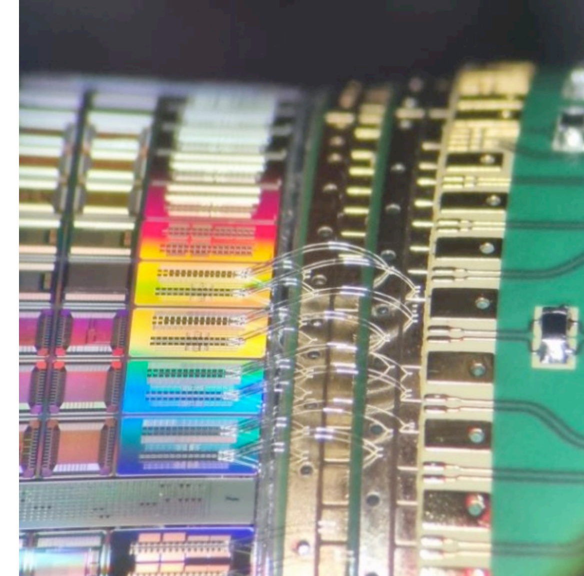
ITS3 assembly tests



FPC and Sensor on jig



First layer assembled



Wire bondings

ALICE

Chip development roadmap

2021
MLR1: First 65nm process MAPS

2022
Successfully qualified the 65 nm process for ITS3

2023
ER1 - first stitched MAPS.
Two large stitched prototypes.
Goal: assess yield and stitching.
Tests ongoing.

2024
ER2 - ITS3 sensor prototype.
Specifications frozen.
Design ongoing

2025
ER3 ITS3 sensor production

MOST

ALICE

- Power is distributed globally - yield is addressed by a highly granular set of switches that allow to turn off faulty parts locally
- Readout is purely asynchronous and hit-driven - low power consumption + timing information