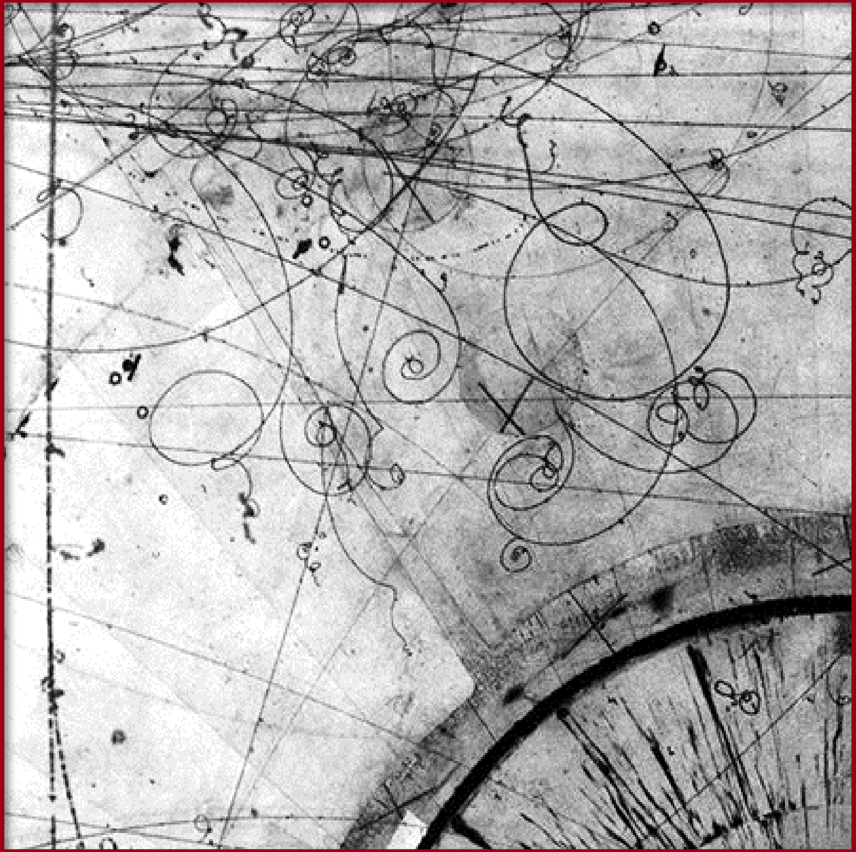
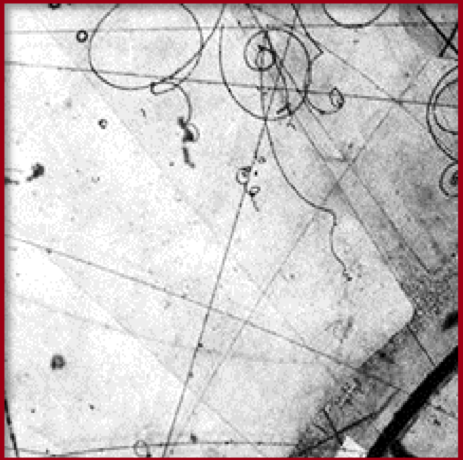


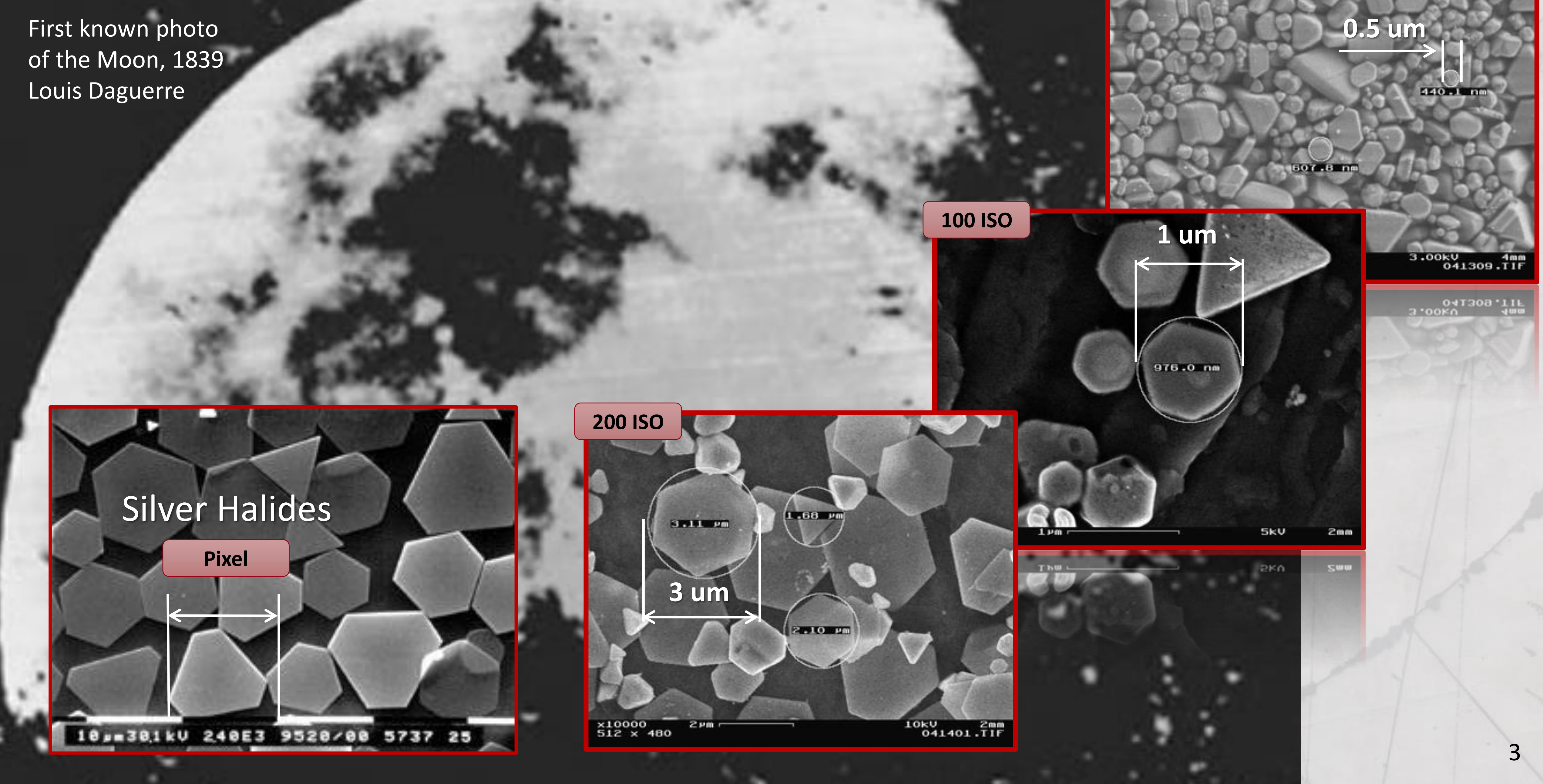
Sensors & trackers R&D

P. Giubilato – 27 June 2024 – FNAL



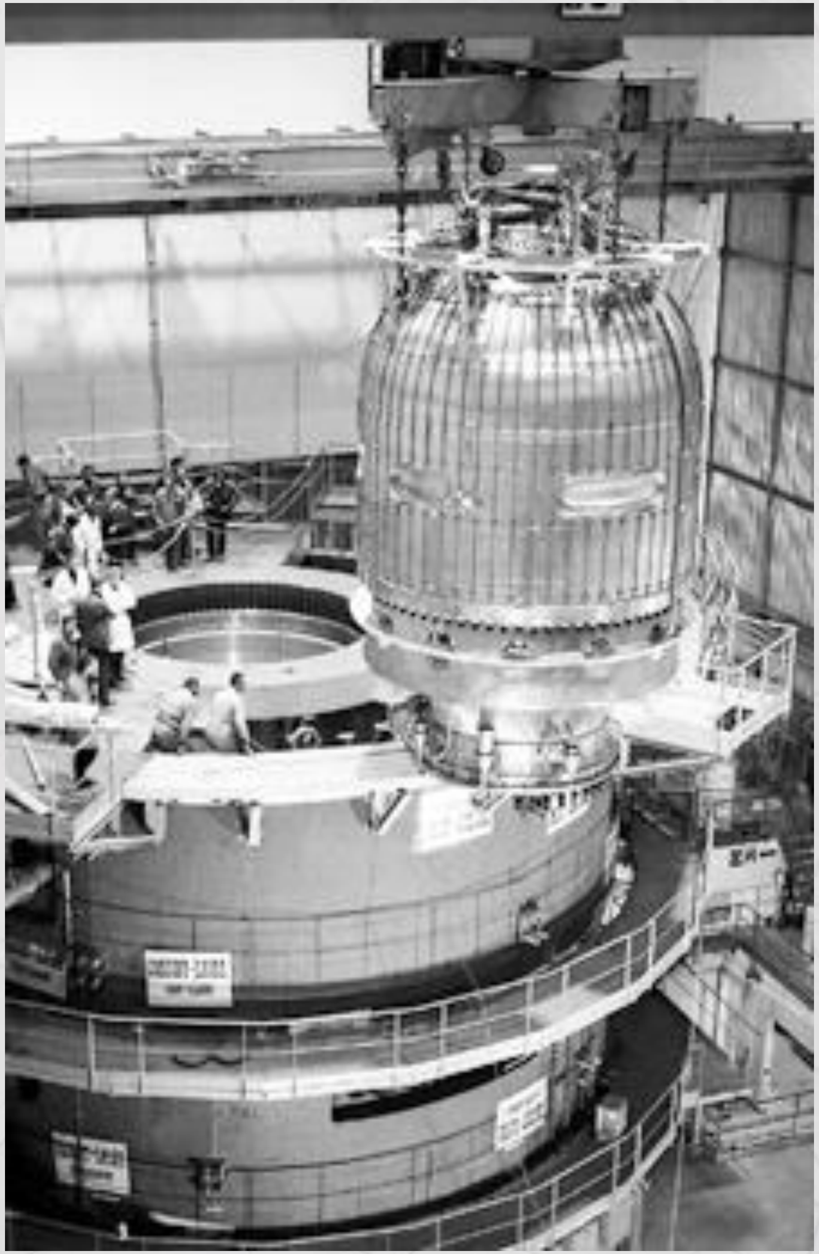
Background

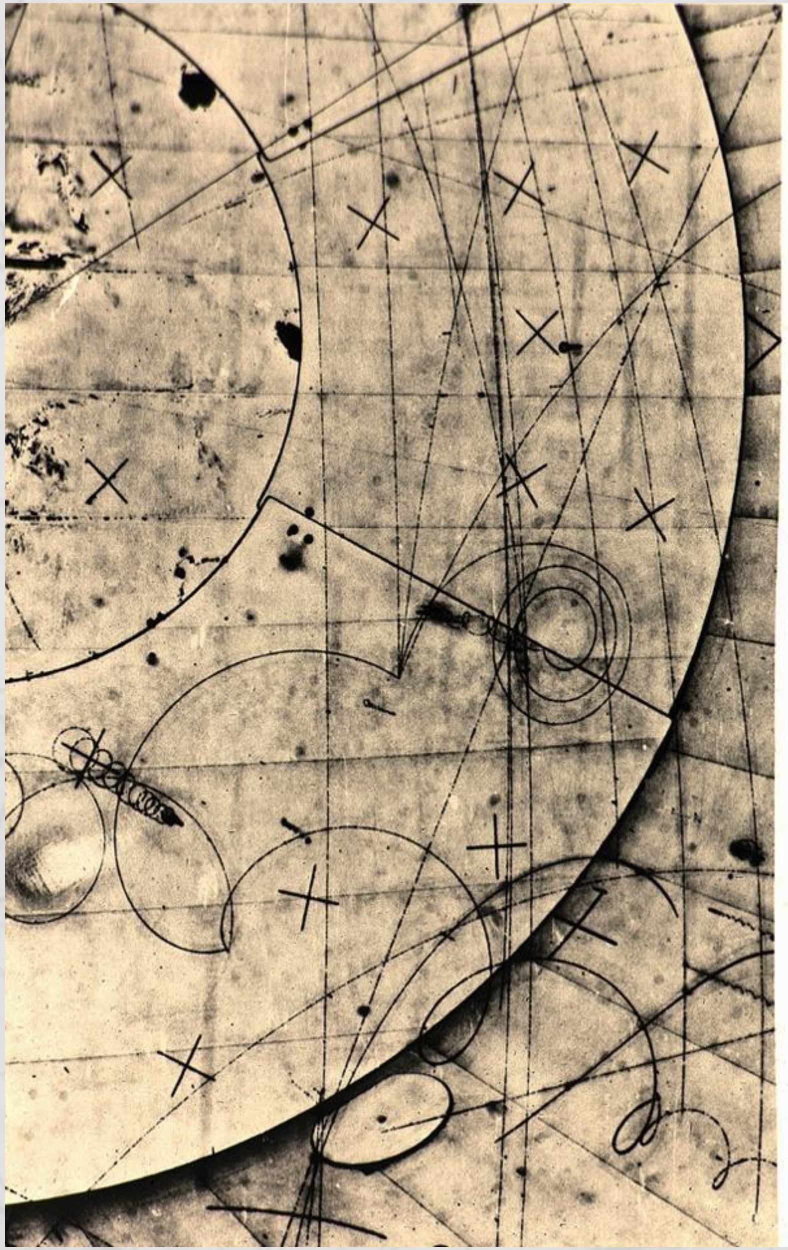
Chemistry had a head-start

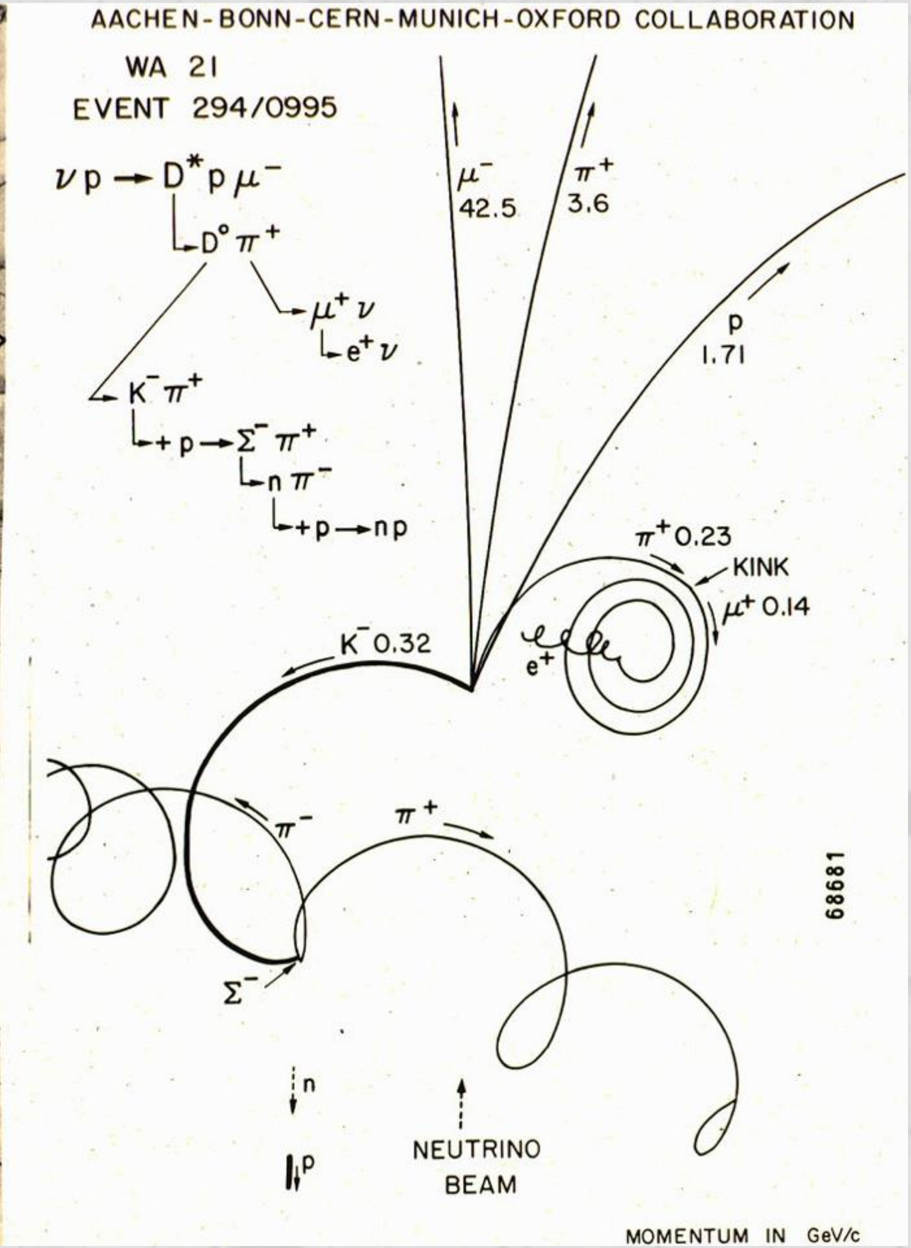


First known photo
of the Moon, 1839
Louis Daguerre

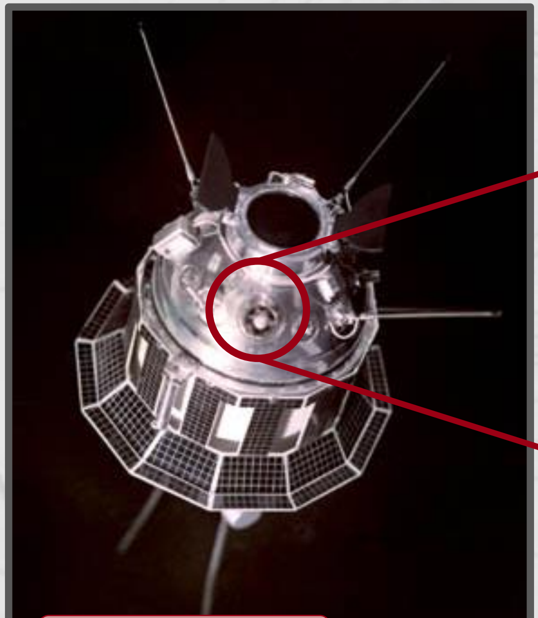
Chemistry did not rule in the space only!



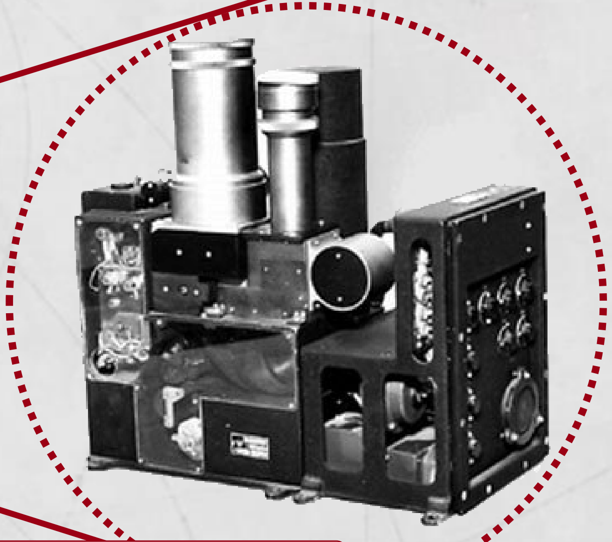




Chemistry has limitations

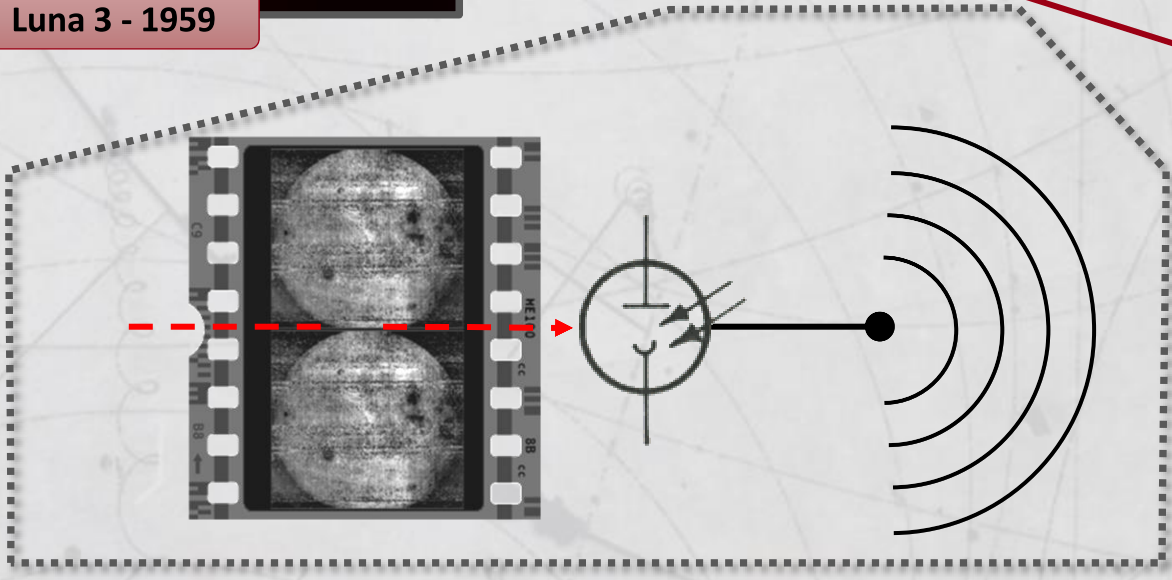


Luna 3 - 1959



Yenisey camera system

The dark side of the Moon, first shot



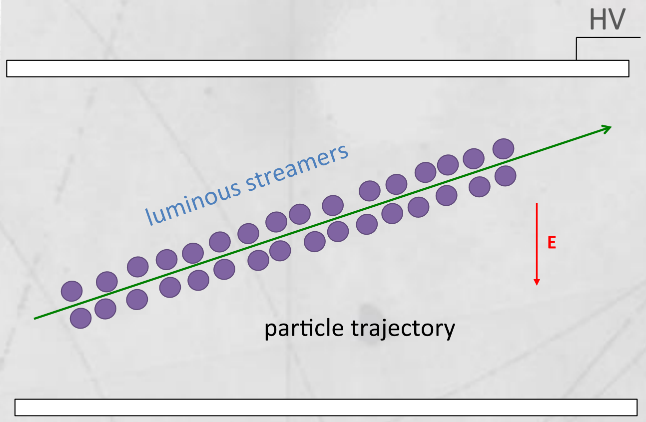
Film limits:

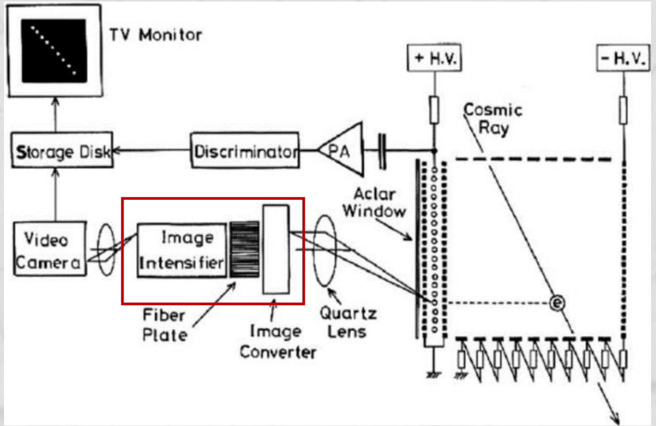
- Doesn’t generate an electric signal
- It is single use, you need a lot of it!
- Needs running mechanics.
- Get fogged by radiation.
- You have to retrieve it!

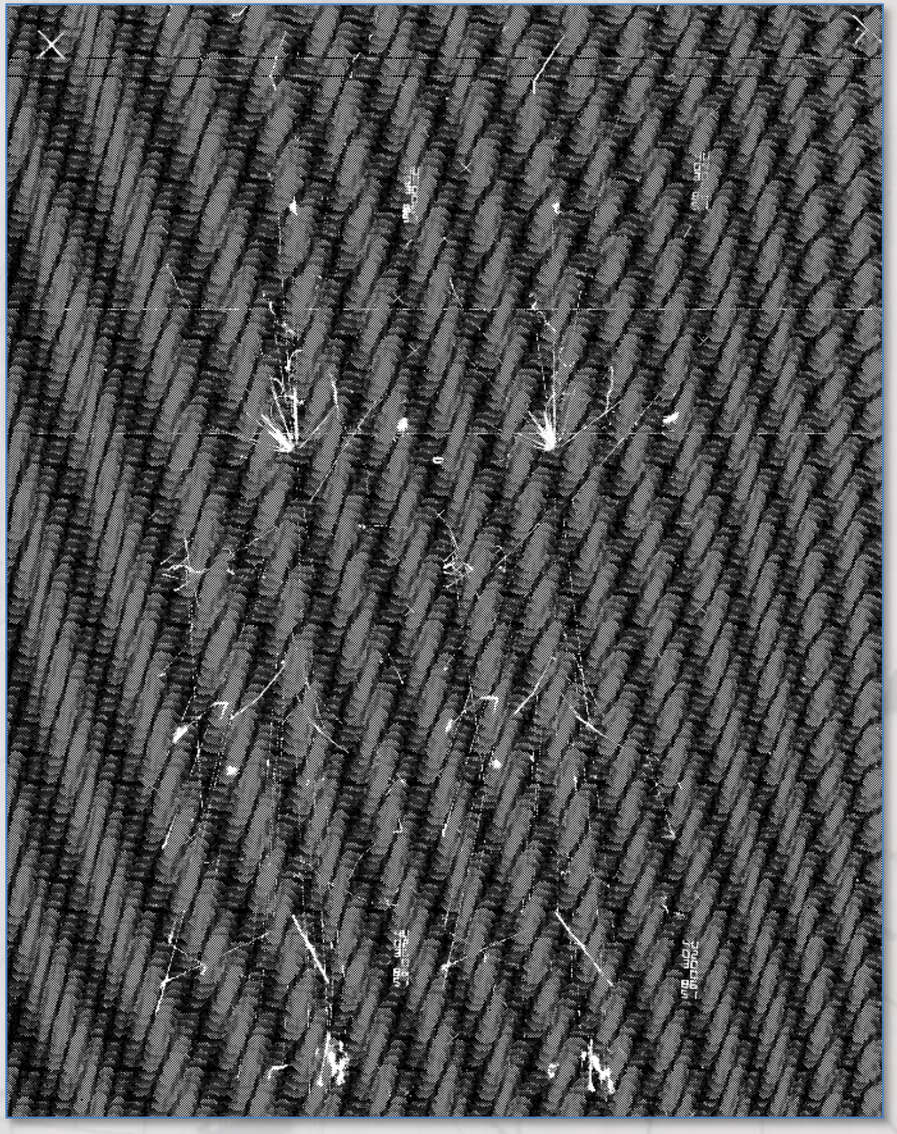
Electro-optics dominates the ‘80s

Large area Image Intensifiers allows to improve Streamer Chamber in the **‘80s** → Avalanche Chamber

LBL Bevelac (1983)
“streamer mode”

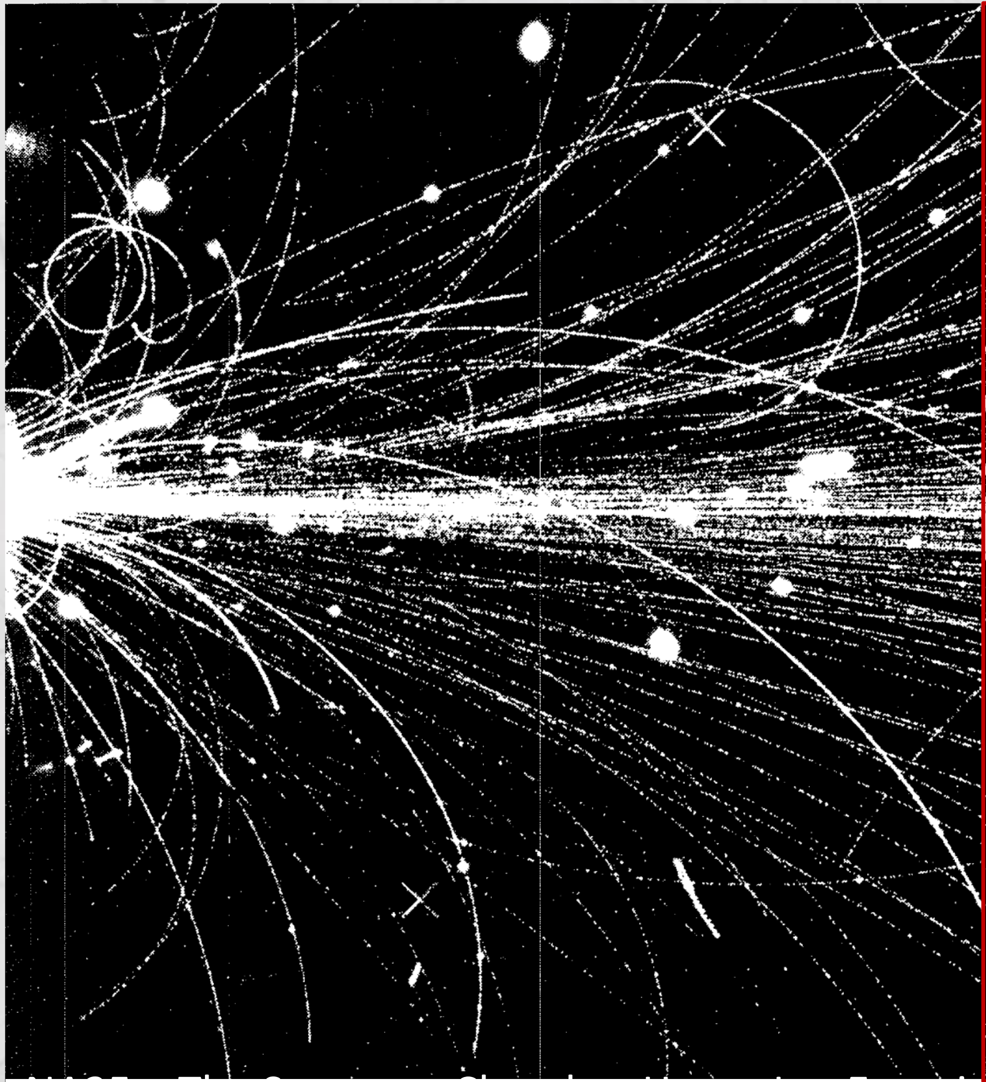


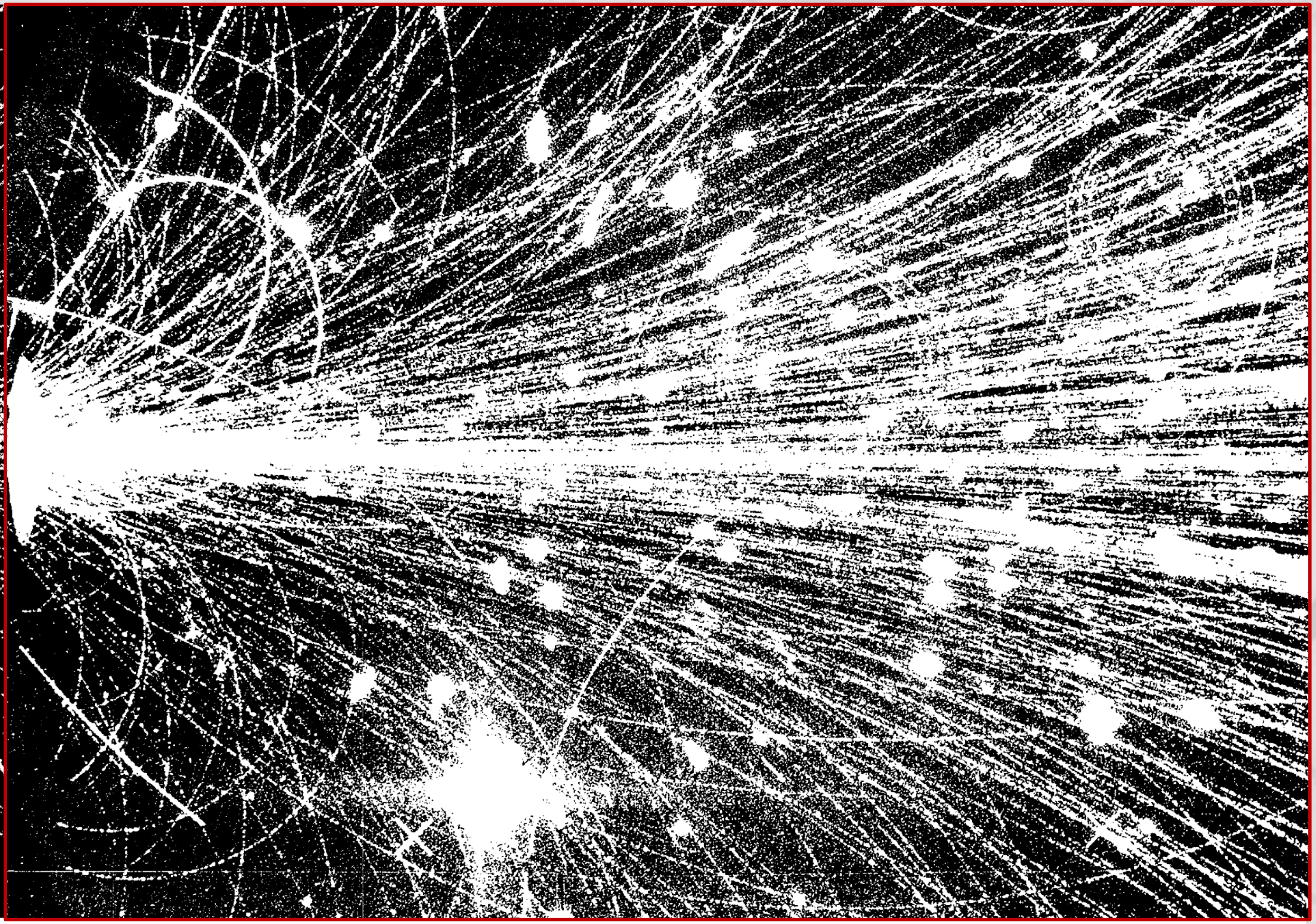




Electro-optics hits the limit

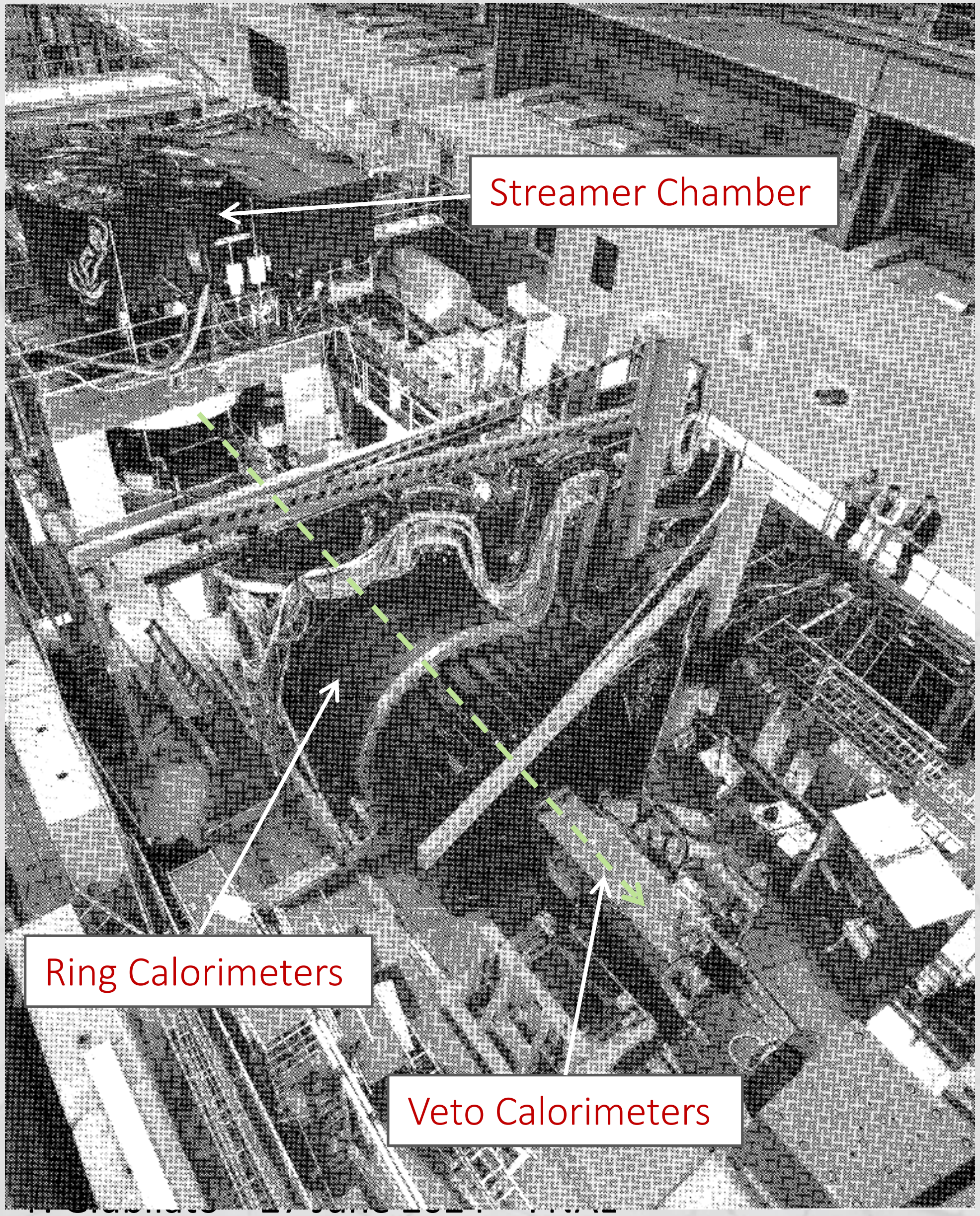
3.2 TeV ^{16}O + Pb interaction, NA35 Streamer Chamber in avalanche mode

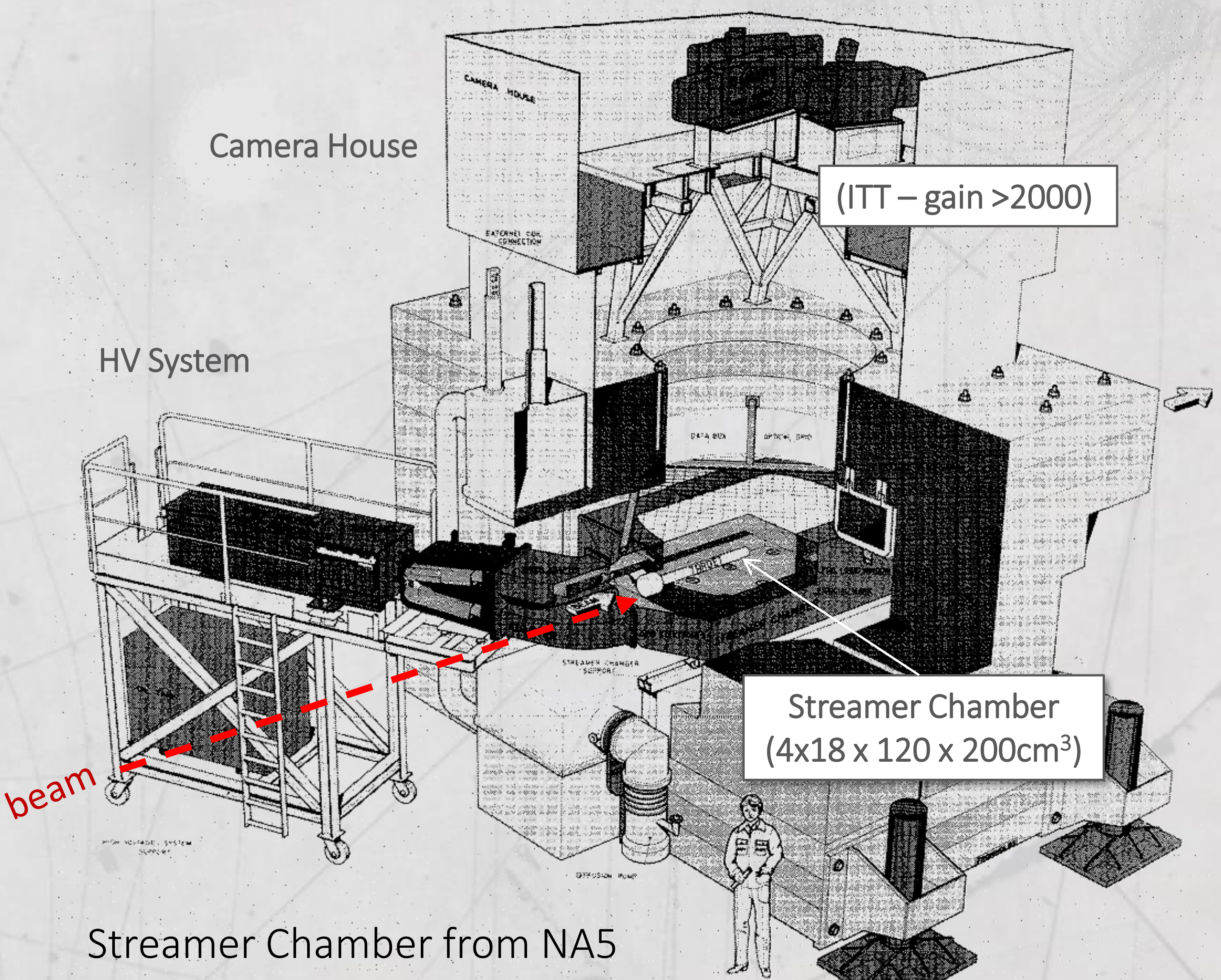




6.4 TeV ^{22}S + ^{197}Au, NA35: **analysis of the charged particles in the central core of the collision becomes impossible**

Streamer chamber heavy Ion experiment 1985

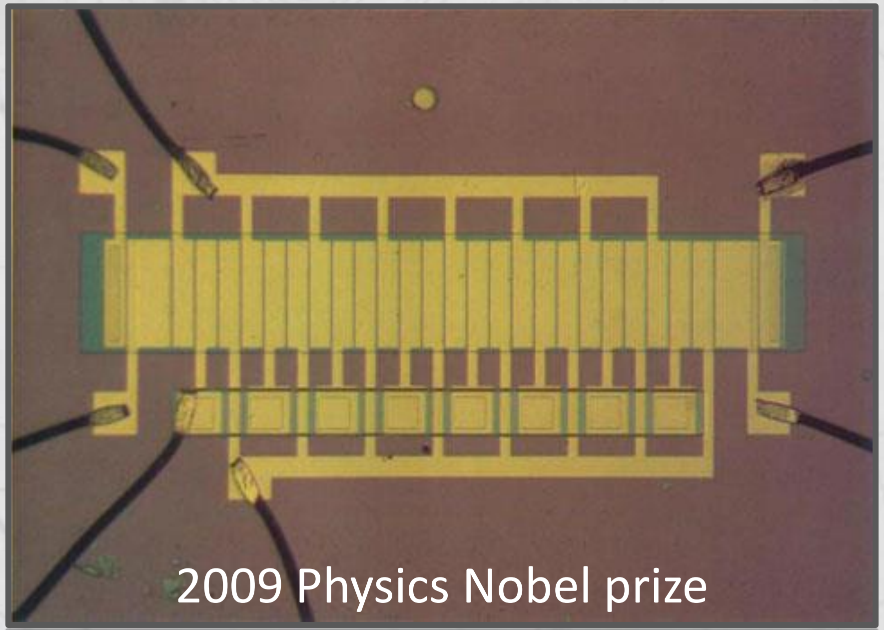




Streamer Chamber from NA5
Optics from UA5

Game-changer: the “electronic film”

1969 at AT&T Bell Labs by **Willard Boyle** and **George E. Smith**. They were working on a semiconductor bubble **memory and** called their design '**Charge "Bubble" Devices**’, later known as Charge Coupled Device.

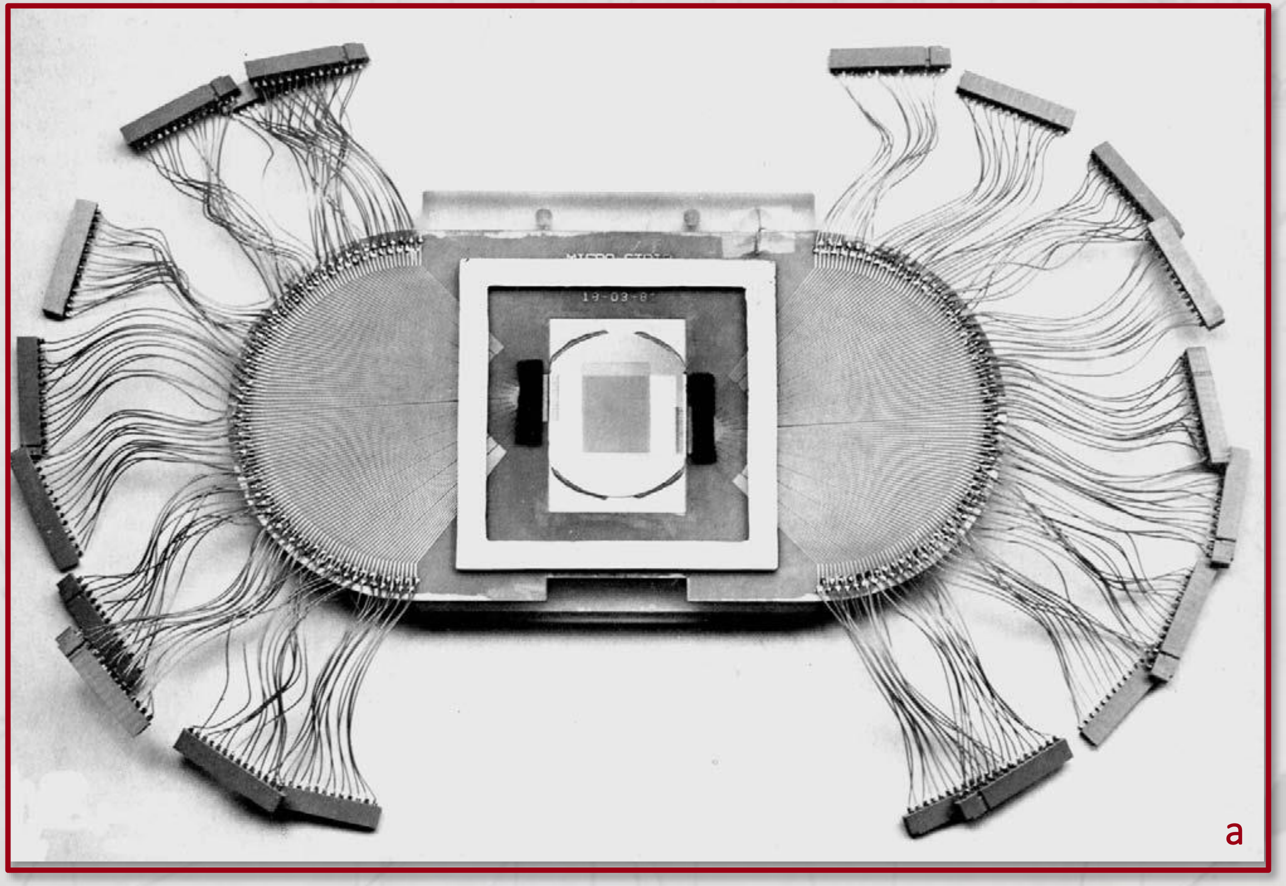

2009 Physics Nobel prize

The possibility to use the same technology at the base of computers and other digital or analogue processing systems (microchip) to build the sensor itself, did open the way to **unprecedented measuring possibilities.**

Silicon arrives in the physics community

End of 70s: R&D at CERN (*Heijne et al., NIM 78, **1980***) and Pisa (*Amendolia et al., NIM 78, 1980*) **to measure short-lived particles** (10^{-12} - 10^{-13} s) leads to micro-strips of 100-200 µm pitch:

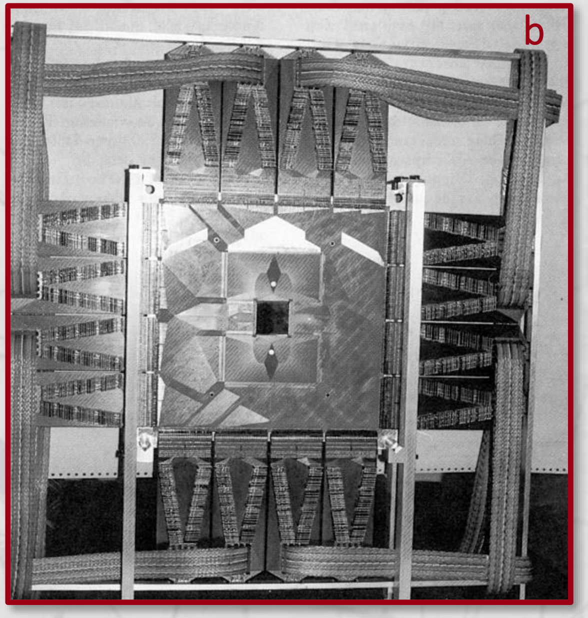
- high detection efficiency (>99%), good spatial resolution (~20mm) and good stability
- Precise vertex reconstruction
- Complex technology (**1980**) → limited availability
- Fabrication of silicon detectors using standardIC planar process (PIN diode → micro-strip detector)



First use of silicon strips detectors by NA11(CERN SPS) and **E706 (FNAL)**

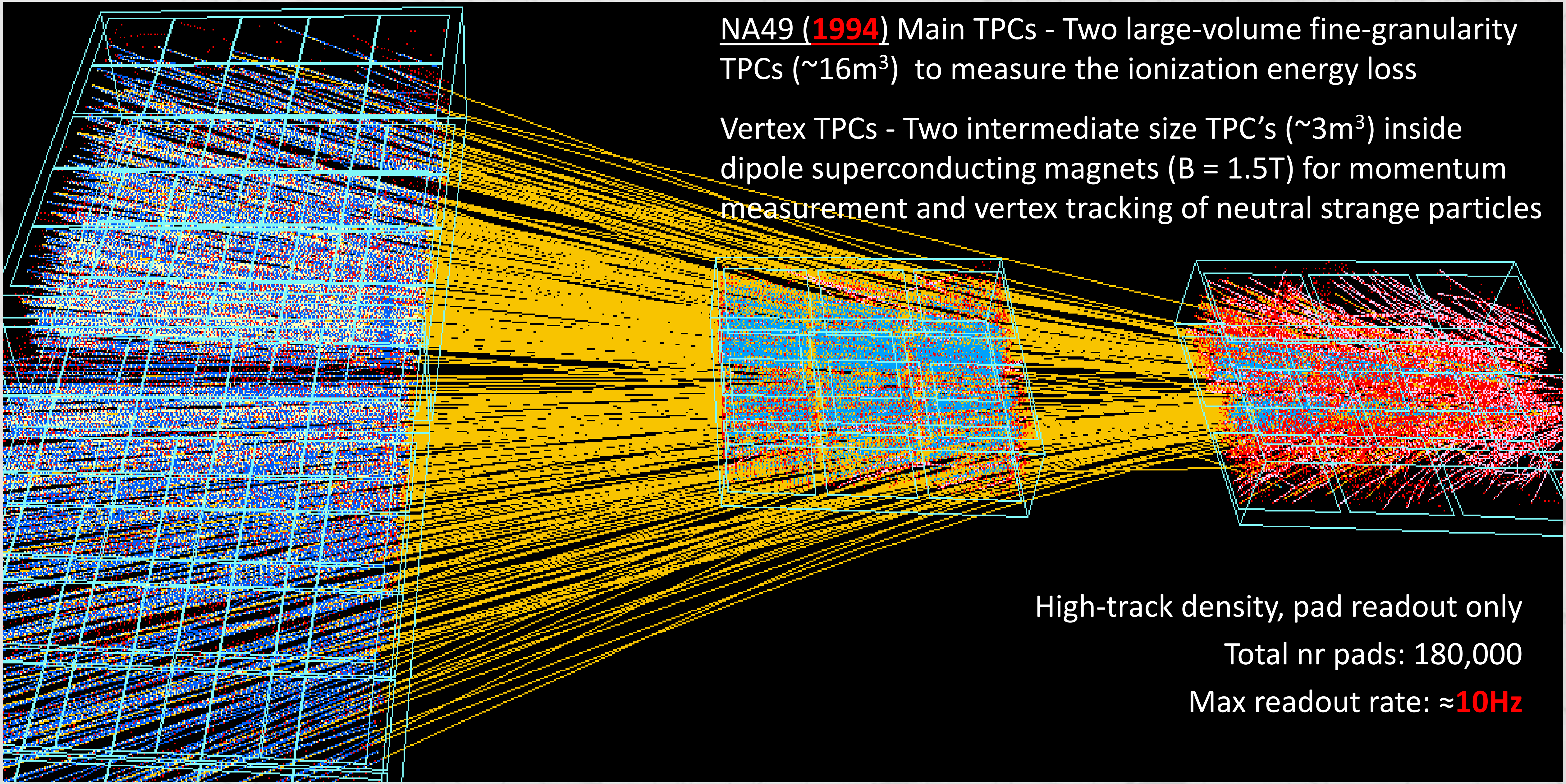
a) NA11 (1981): 6 planes (24 x 36mm^2): resistivity 2-3 kWcm, thickness 280mm, pitch 20mm

b) E706 (1982): 4 planes (3x3 cm^2) + 2 planes (5x5cm^2)



J. Kemmer, et al., *"Development of 10-micrometer resolution silicon counters for charm signature observation with the ACCMOR spectrometer", Proceedings of Silicon Detectors for High Energy Physics, Nucl. Instr. and Meth. 169 (1980) 499.*

Full electronics readout



NA49 (1994) Main TPCs - Two large-volume fine-granularity TPCs (~16m^3) to measure the ionization energy loss

Vertex TPCs - Two intermediate size TPC's (~3m^3) inside dipole superconducting magnets (B = 1.5T) for momentum measurement and vertex tracking of neutral strange particles

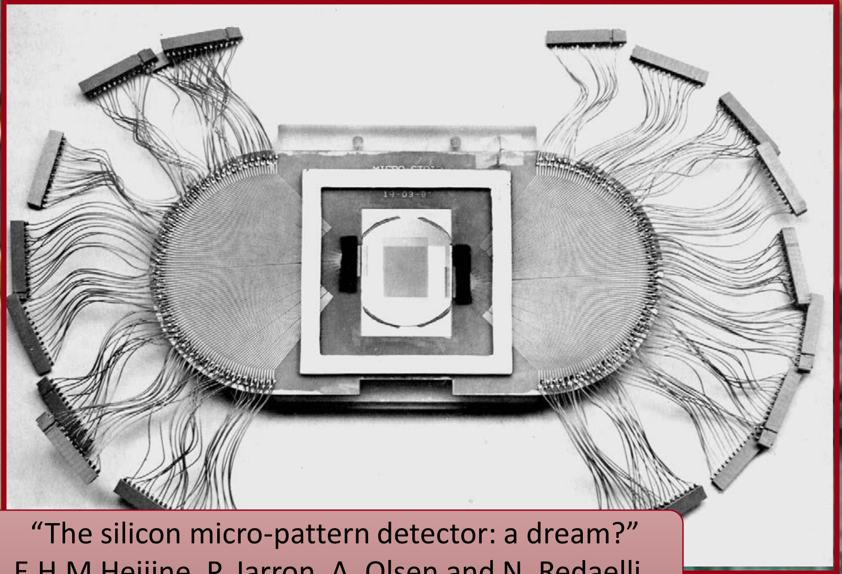
High-track density, pad readout only

Total nr pads: 180,000

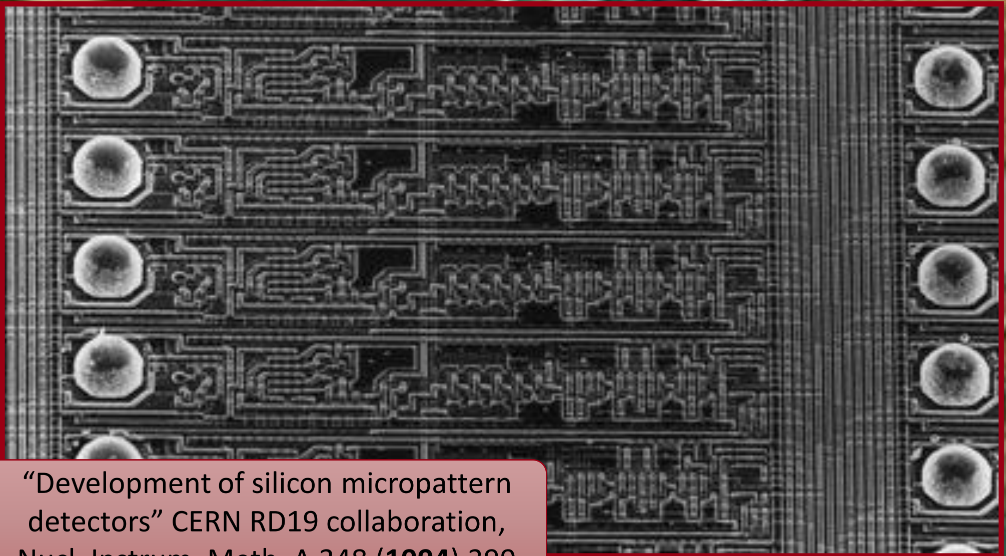
Max readout rate: ≈10Hz

Silicon takes the lead

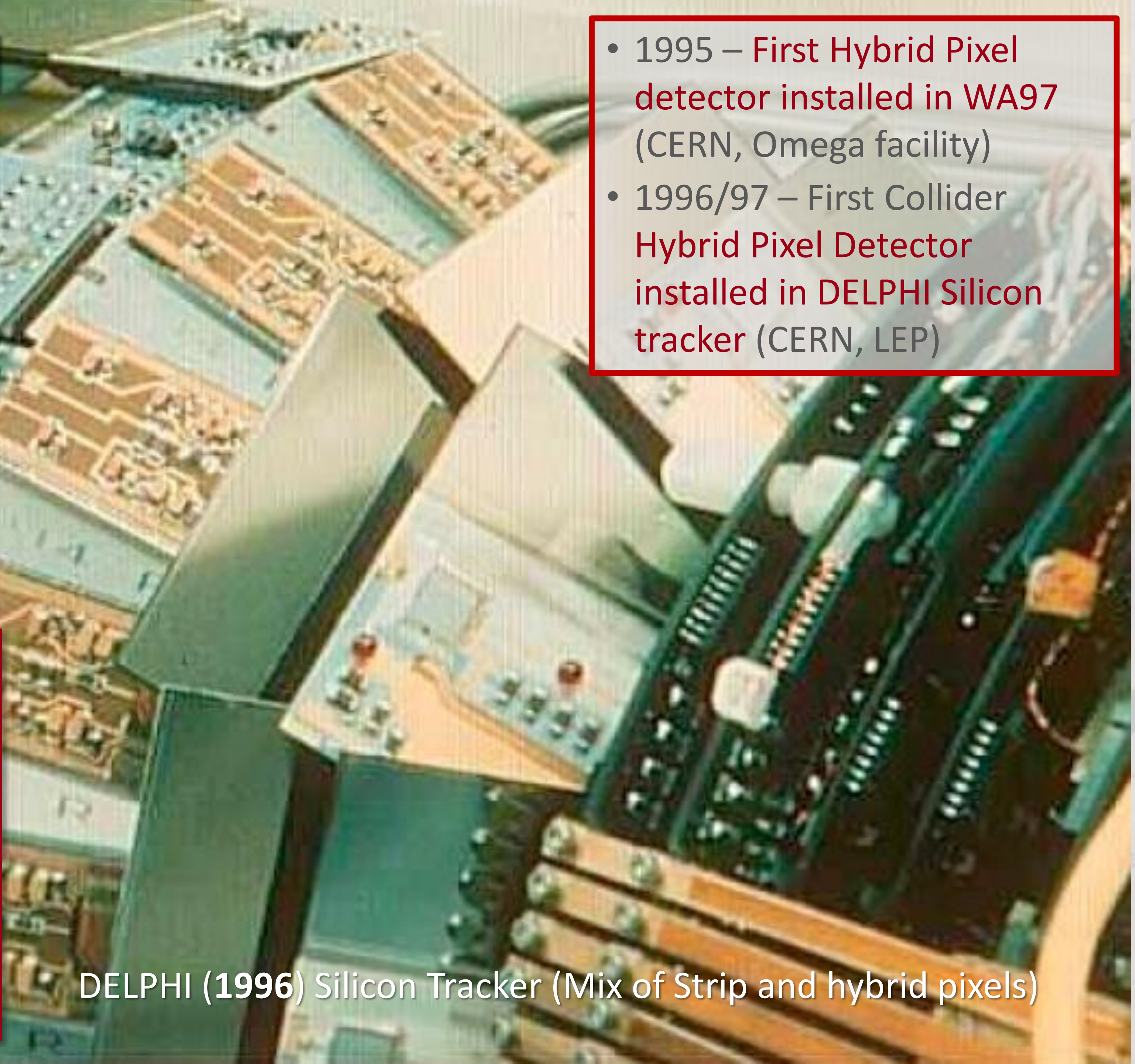
- 1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)
- 1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI Silicon tracker (CERN, LEP)



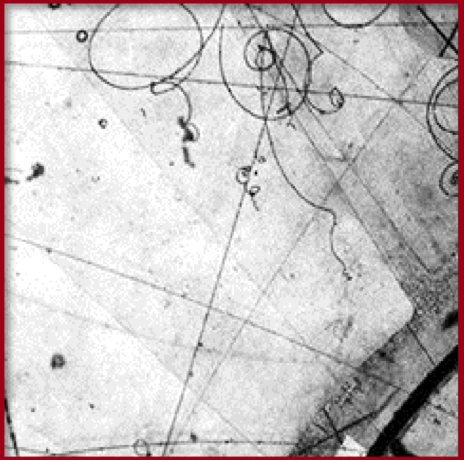
“The silicon micro-pattern detector: a dream?” E.H.M Heijine, P. Jarron, A. Olsen and N. Redaelli , Nucl. Instrum. Meth. A 273 (**1988**) 615



“Development of silicon micropattern detectors” CERN RD19 collaboration, Nucl. Instrum. Meth. A 348 (**1994**) 399

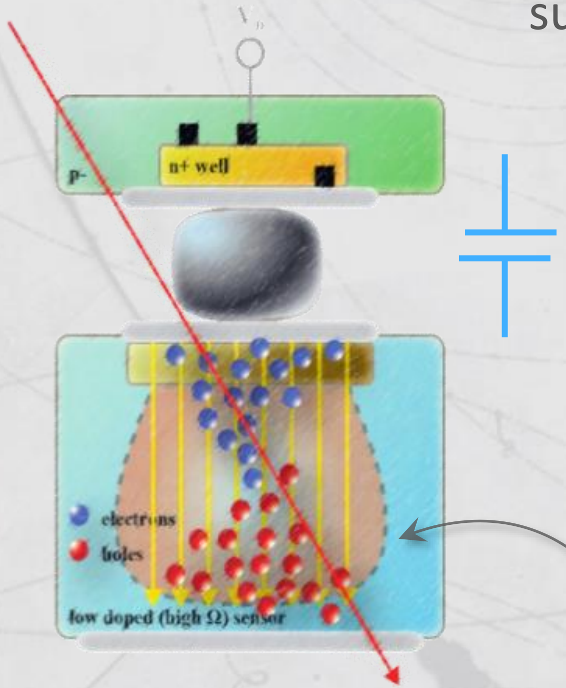


DELPHI (**1996**) Silicon Tracker (Mix of Strip and hybrid pixels)

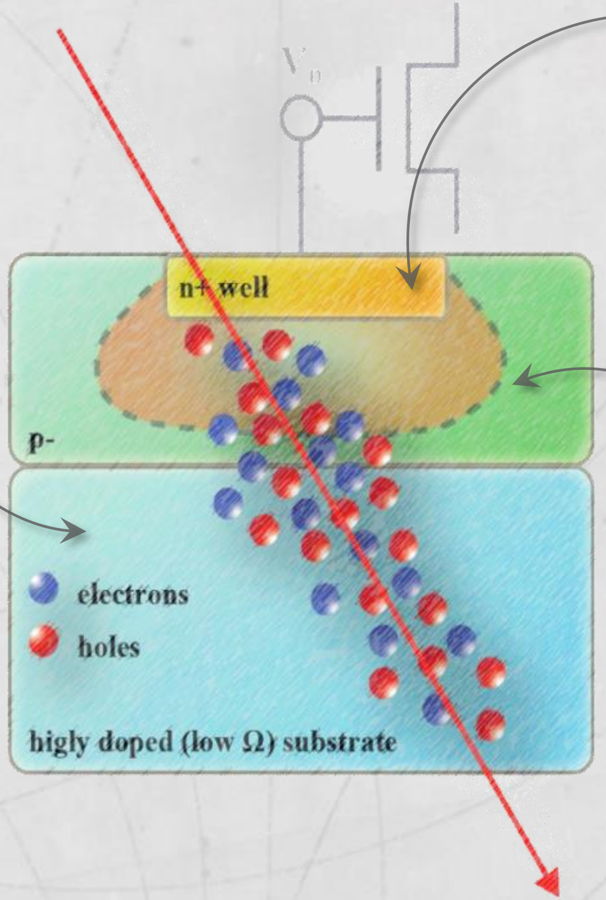


Monolithic Sensors (MAPS)

Monolithic sensor – basic arrangement



Usually a standard (opto) CMOS process, low Ω substrate

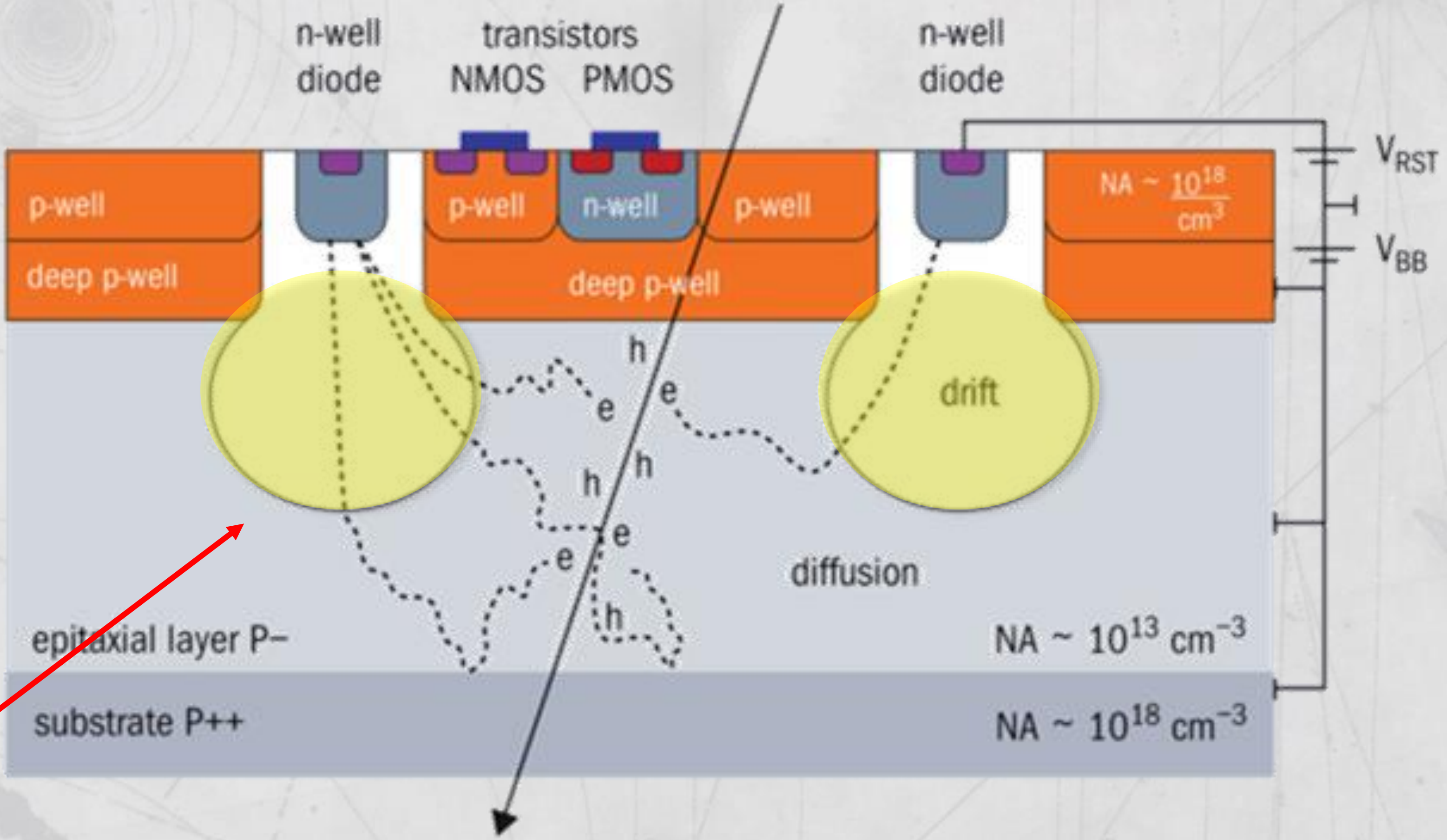


Charge collection by diffusion. Collection time of tens of ns.

Effective collection depth limited to the epitaxial layer (~10µm)

Fast, deep collection volume capacitance, cost, thickness complexity

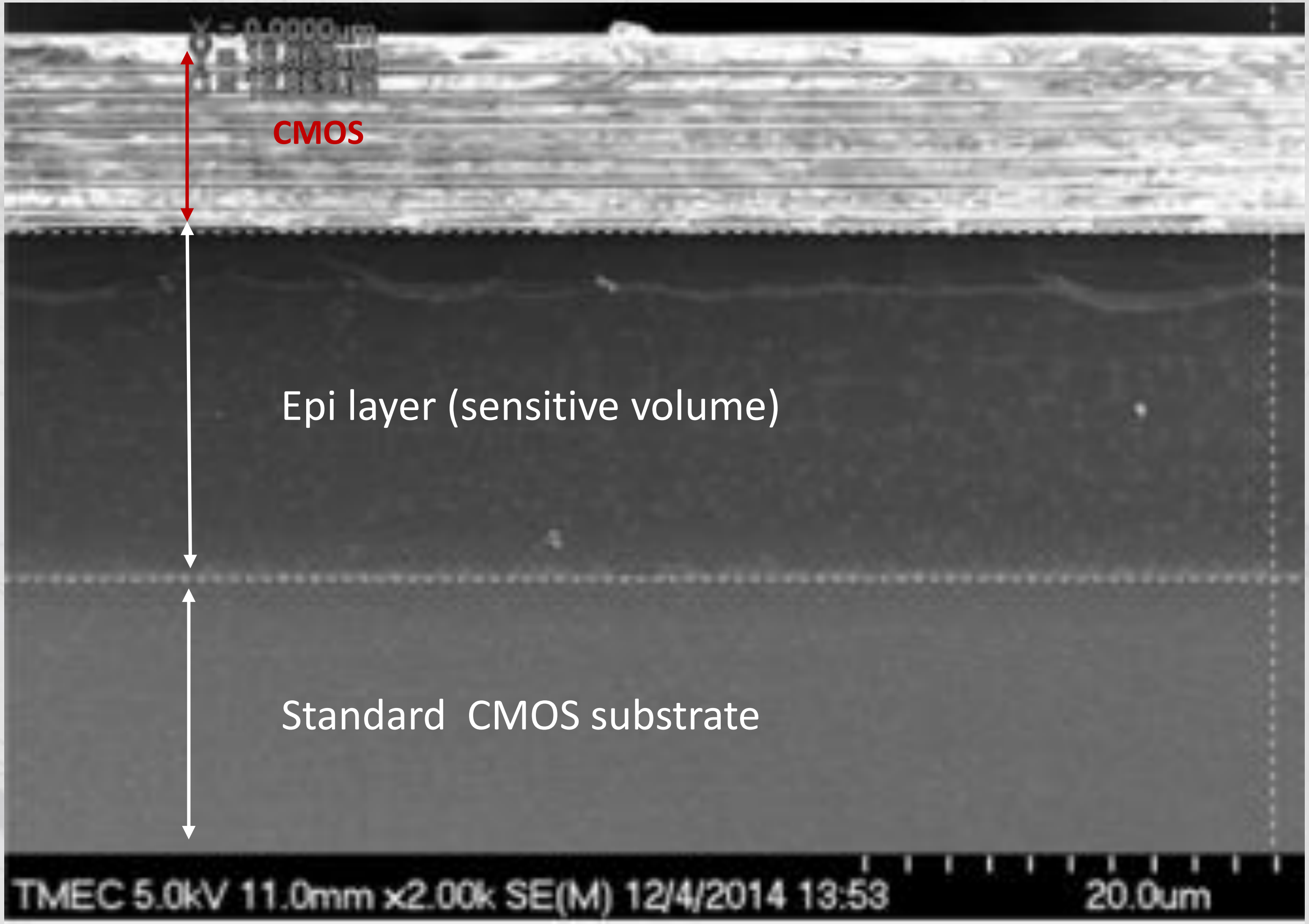
Monolithic sensor – actual implementation



Depleted volume

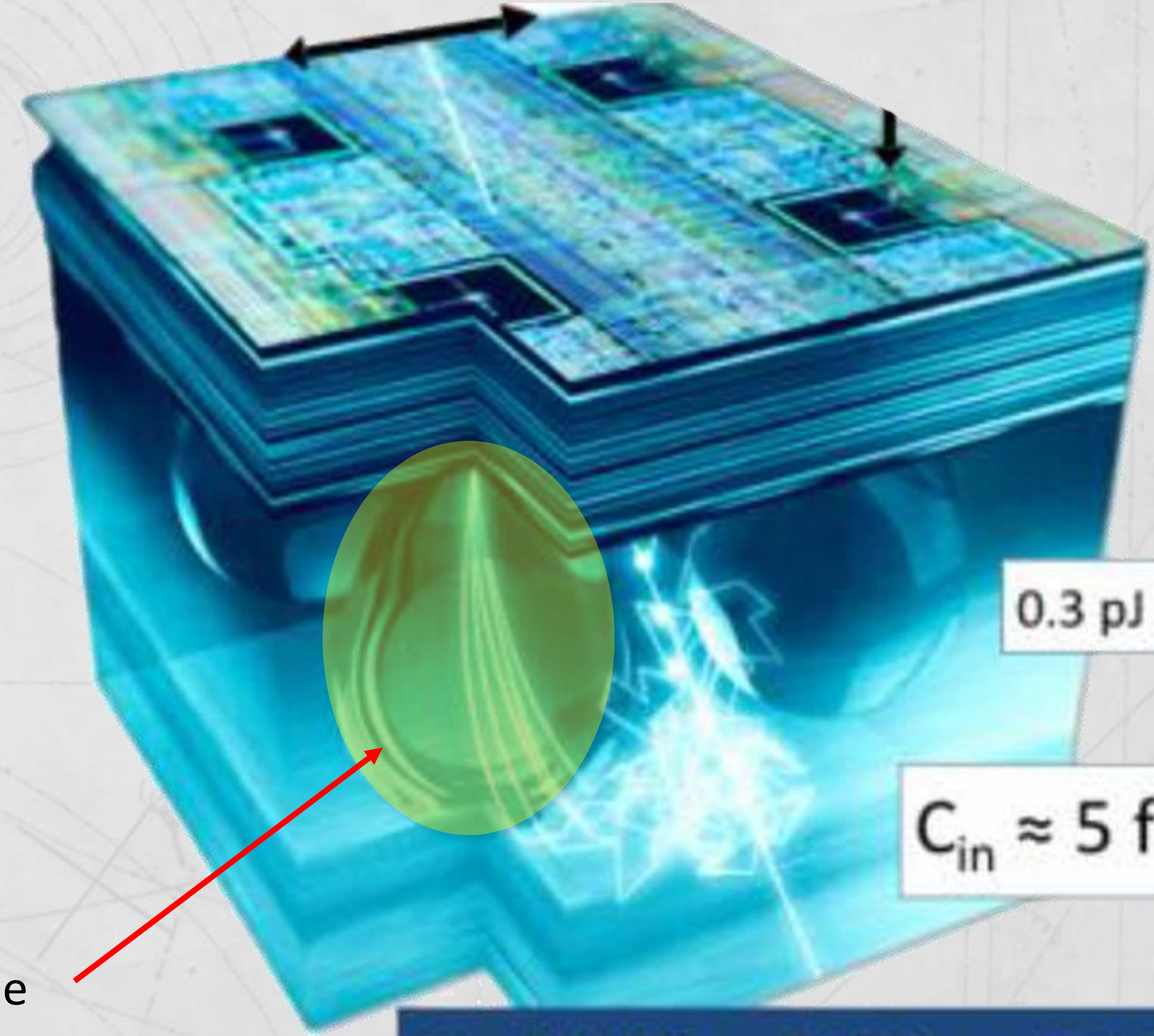
DOI: 10.1016/j.nima.2015.09.057

SEM of a real MAPS



ALICE ITS, SEM picture of prototype chip

MAPS visualized

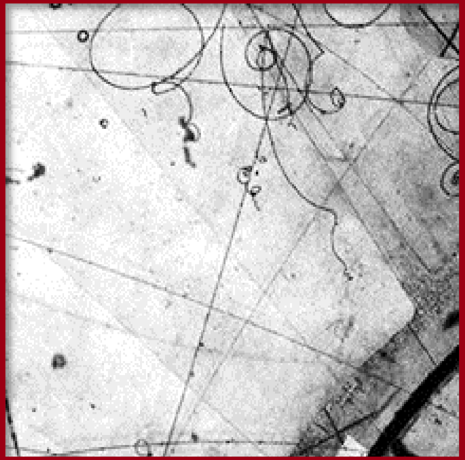


0.3 pJ / bit

$C_{in} \approx 5$ fF

Depleted volume

Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV



Monolithic sensors – few R&D

Monolithic sensor – depletion increases S/N

Assuming input noise $v_{eq} = 0.16\ mV$

(Transistor noise at 40 MHz BW for 1 µA
(1 µA/100x100 µm pixel = 10 mW/cm^2))

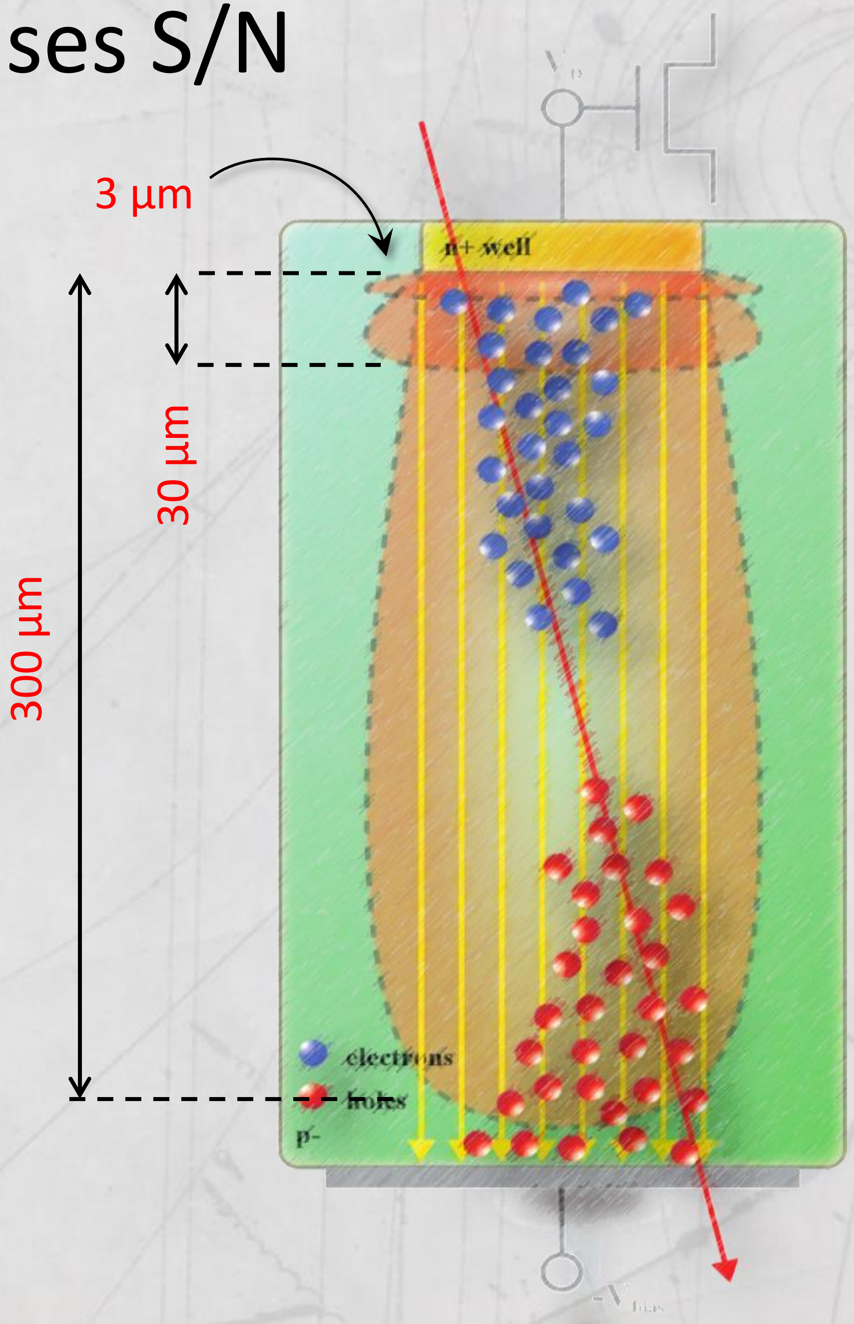
$$\Downarrow$$

$$\frac{S}{N} \geq 25 \rightarrow \frac{Q}{C} \geq 4\ mV$$

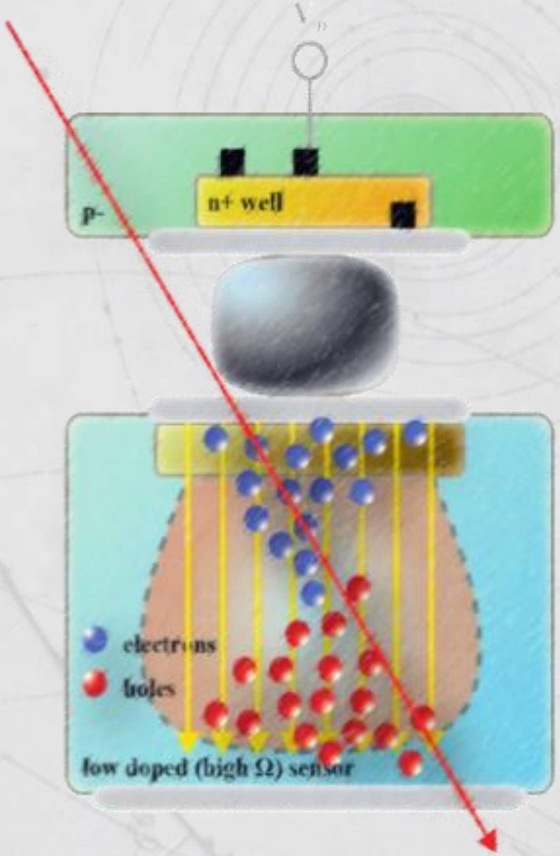
$$\Downarrow$$

25 ke$^-$	2500 e$^-$	250 e$^-$	25 e$^-$
$\frac{4\ fC}{1\ pF} \equiv$	$\frac{0.4\ fC}{100\ fF} \equiv$	$\frac{0.04\ fC}{10\ fF} \equiv$	$\frac{4\ pC}{1\ fF}$
300 µm	30 µm$^-$	3 µm	< 1 µm

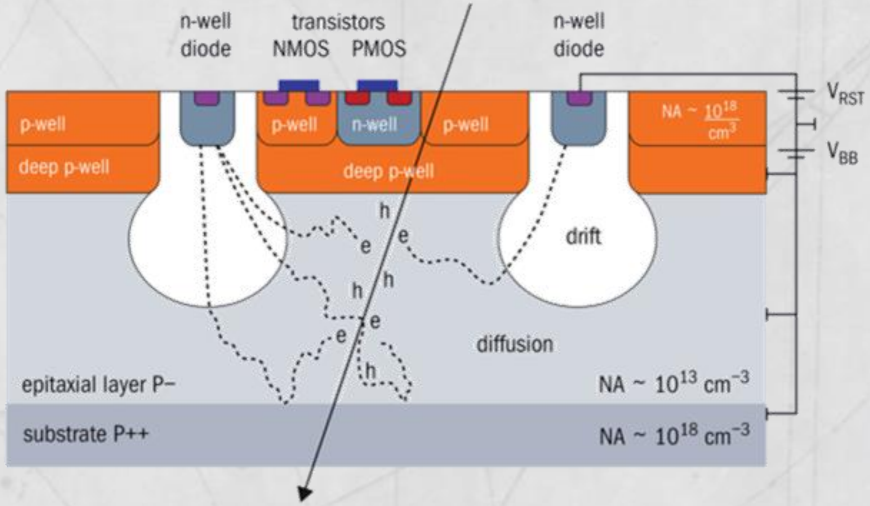
For the same $\frac{S}{N}$ power consumption $\propto \frac{1}{{Q/_{C}}^{2a}}$



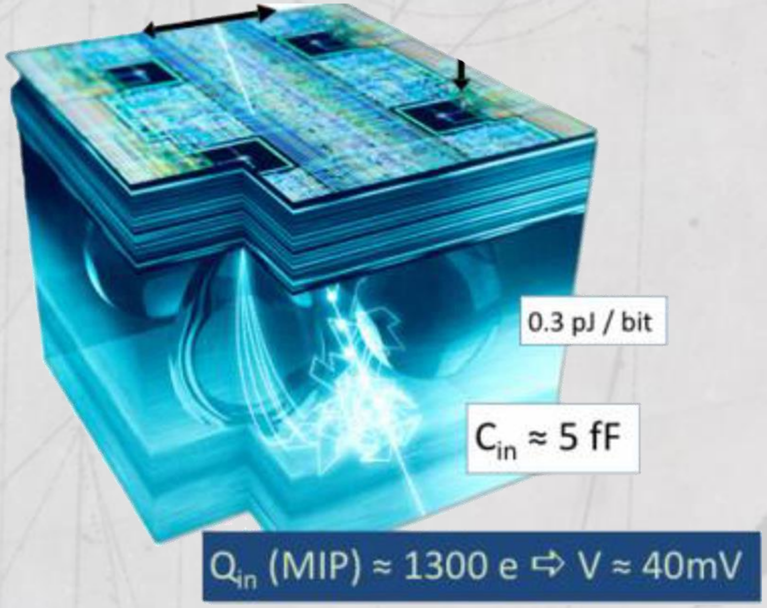
Monolithic sensor – creating a uniform, depleted volume



Easy on hybrid sensors, as the electronics eis decoupled from the sensing volume



More difficult on monolithic, as the field must interact with the surface electronics wells



0.3 pJ / bit

$C_{in} \approx 5$ fF

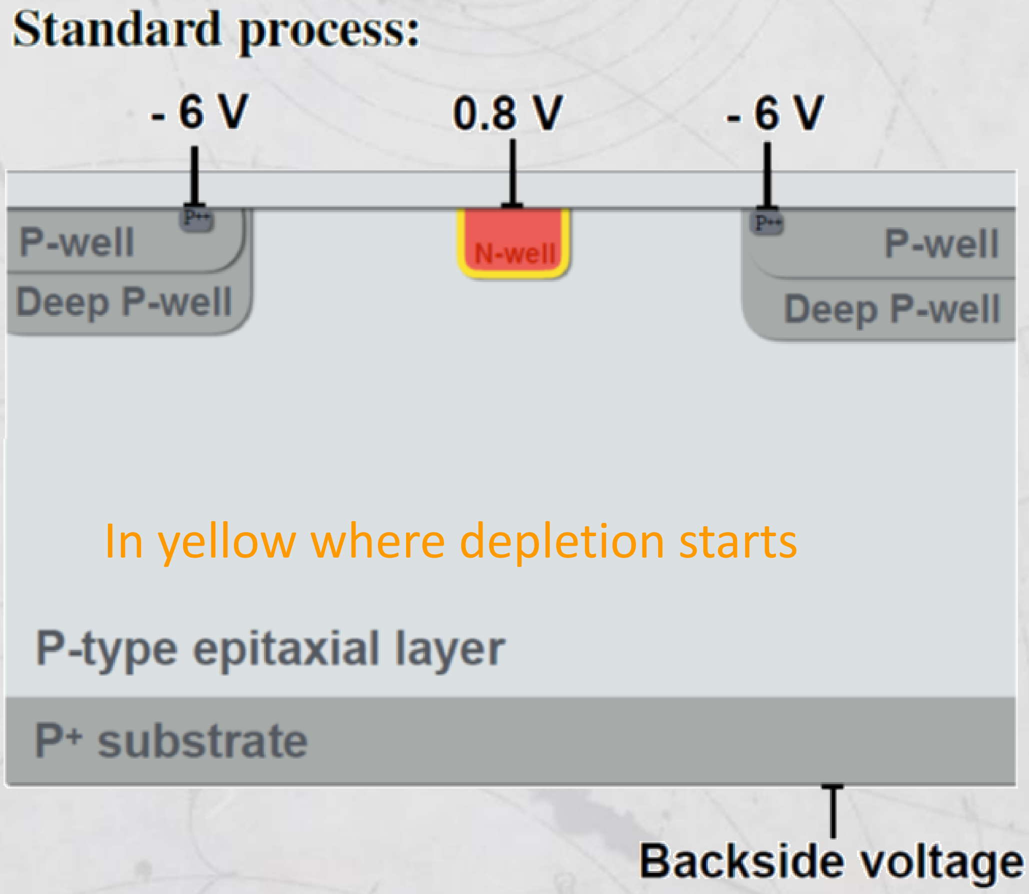
Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

Not the entire volume is actually depleted

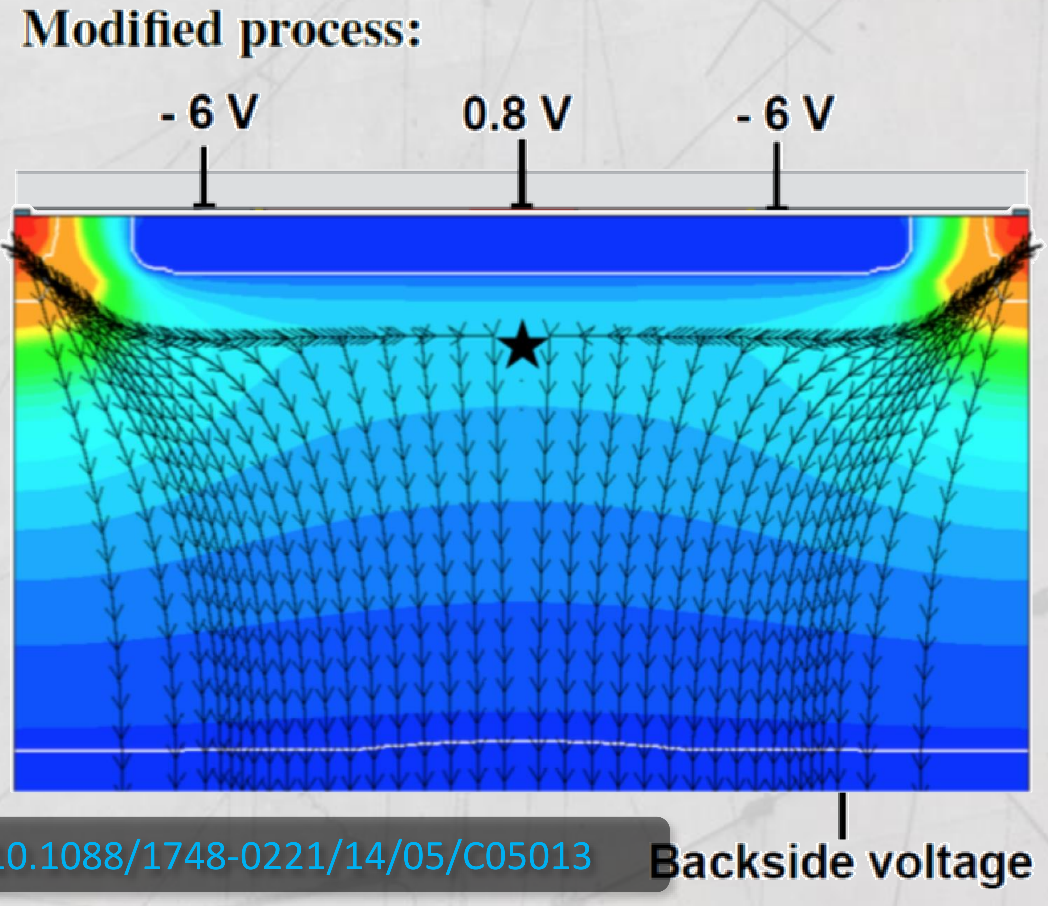
Monolithic sensor – creating a uniform, depleted volume

Standard process (left): difficult to make the depletion layer extend from the junction around the small collection electrode laterally

Modified process: the deep low-dose n-type implant creates a planar junction under the existing implants, so that the depletion starts at the junction, making full depletion easier



In yellow where depletion starts

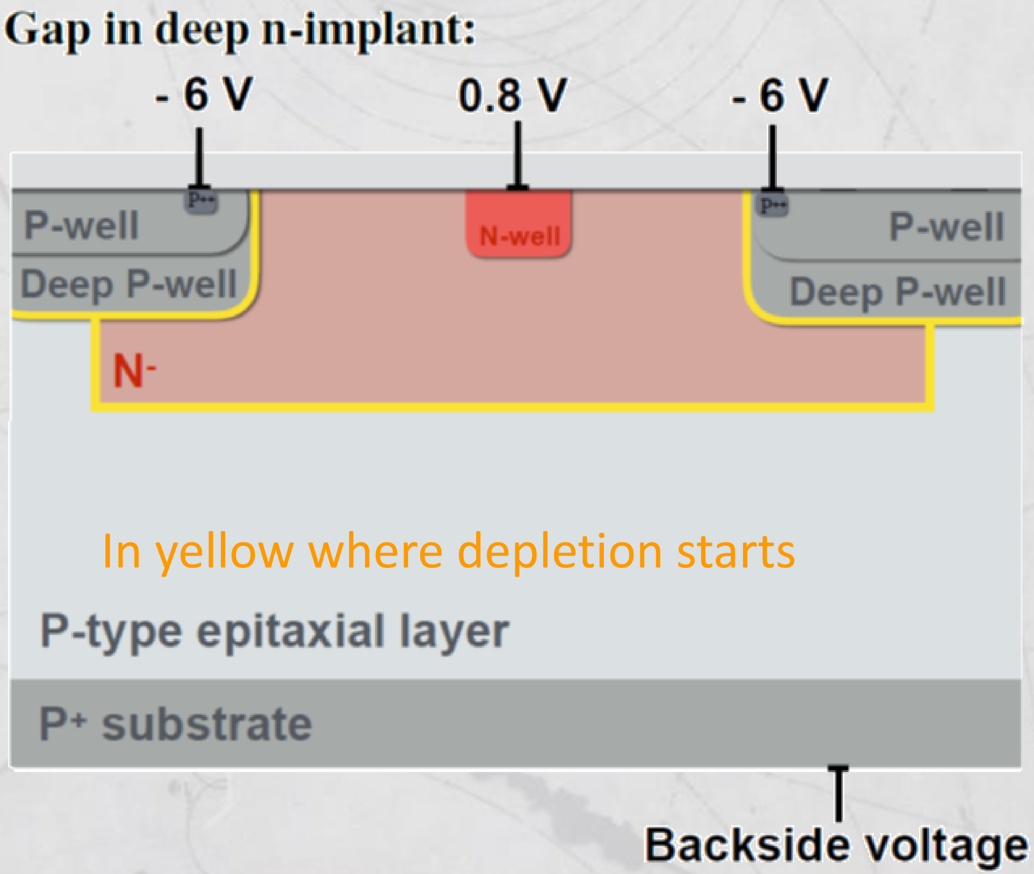


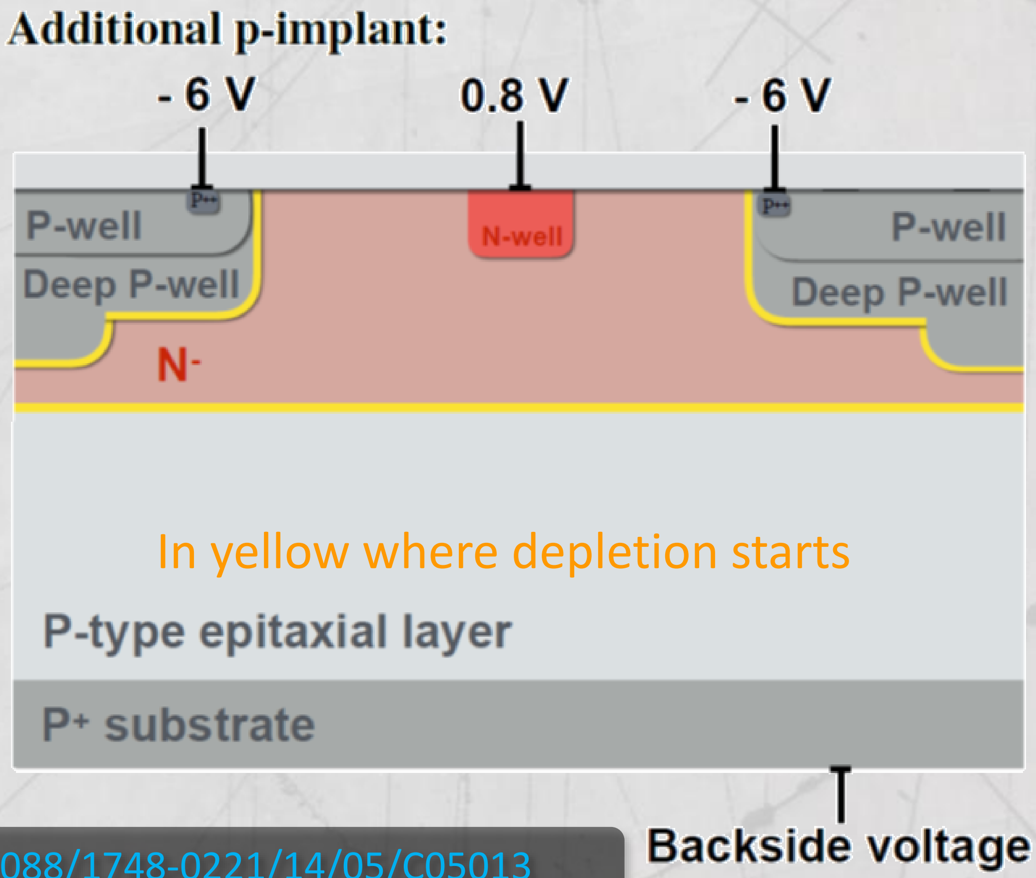
DOI: 10.1088/1748-0221/14/05/C05013

Monolithic sensor – creating a uniform, depleted volume

Additional gap in the deep n-implant helps making the E-field stronger at the sides

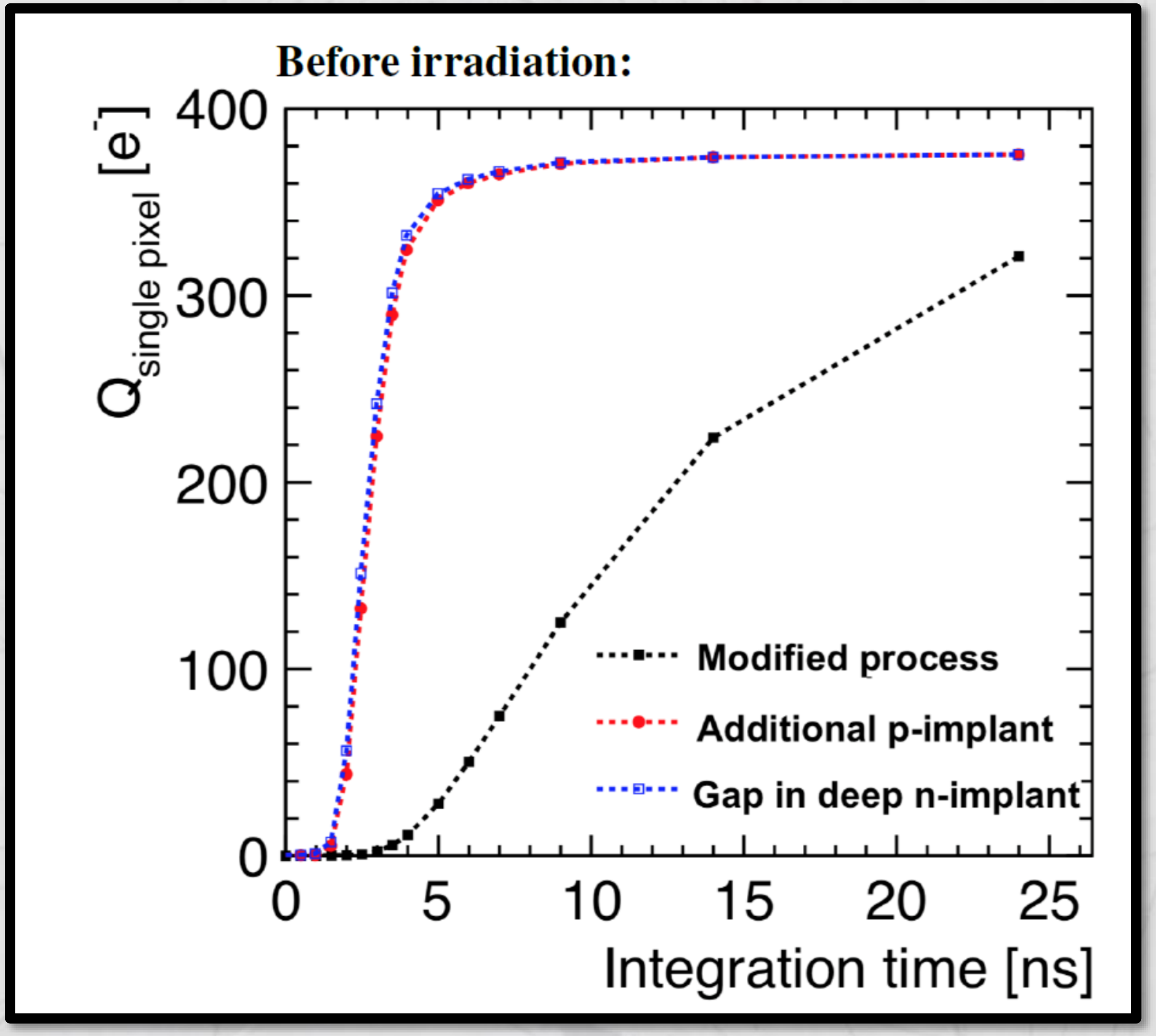
Extra p-implant improves field strength at sides as well

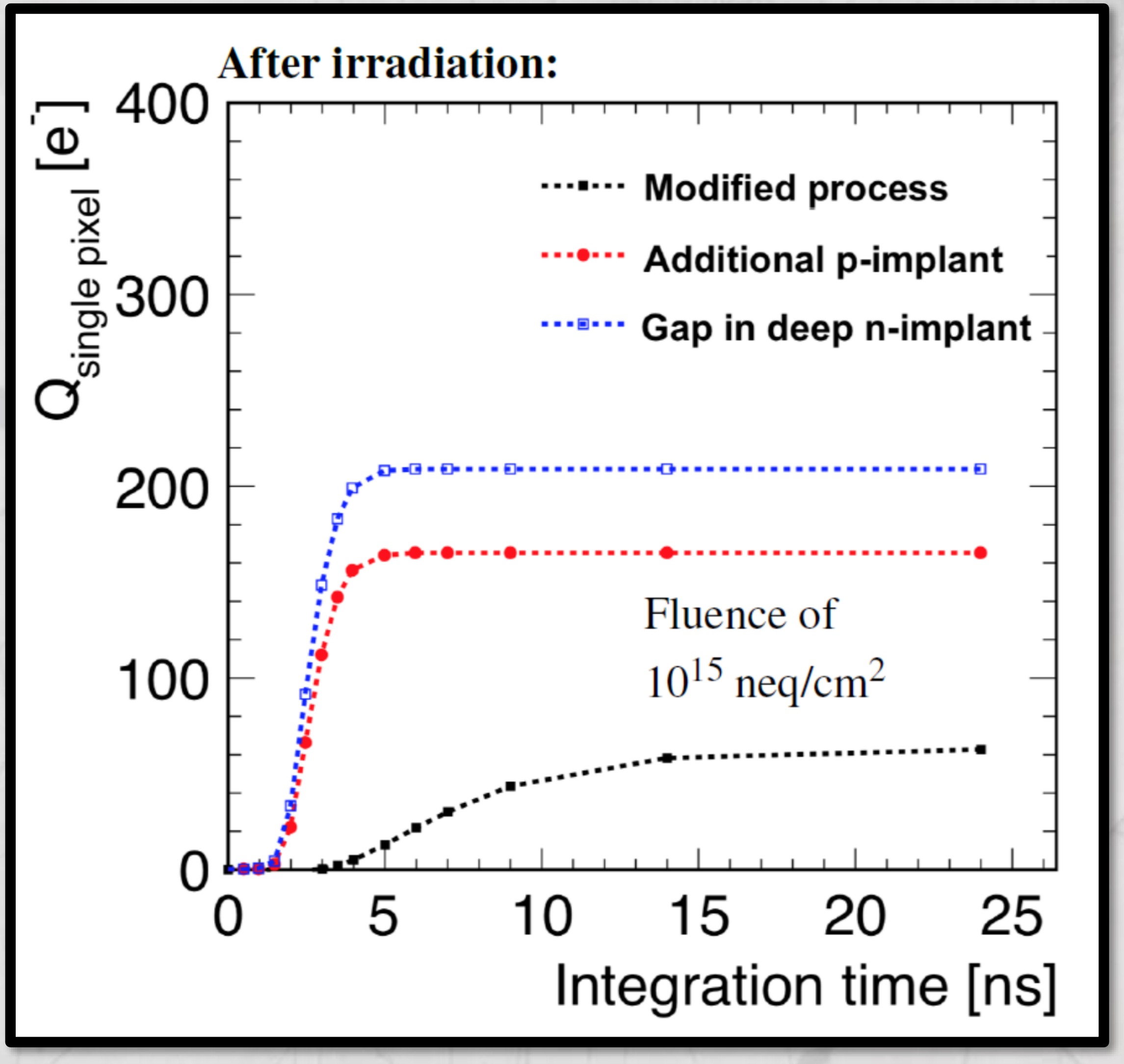




DOI: 10.1088/1748-0221/14/05/C05013

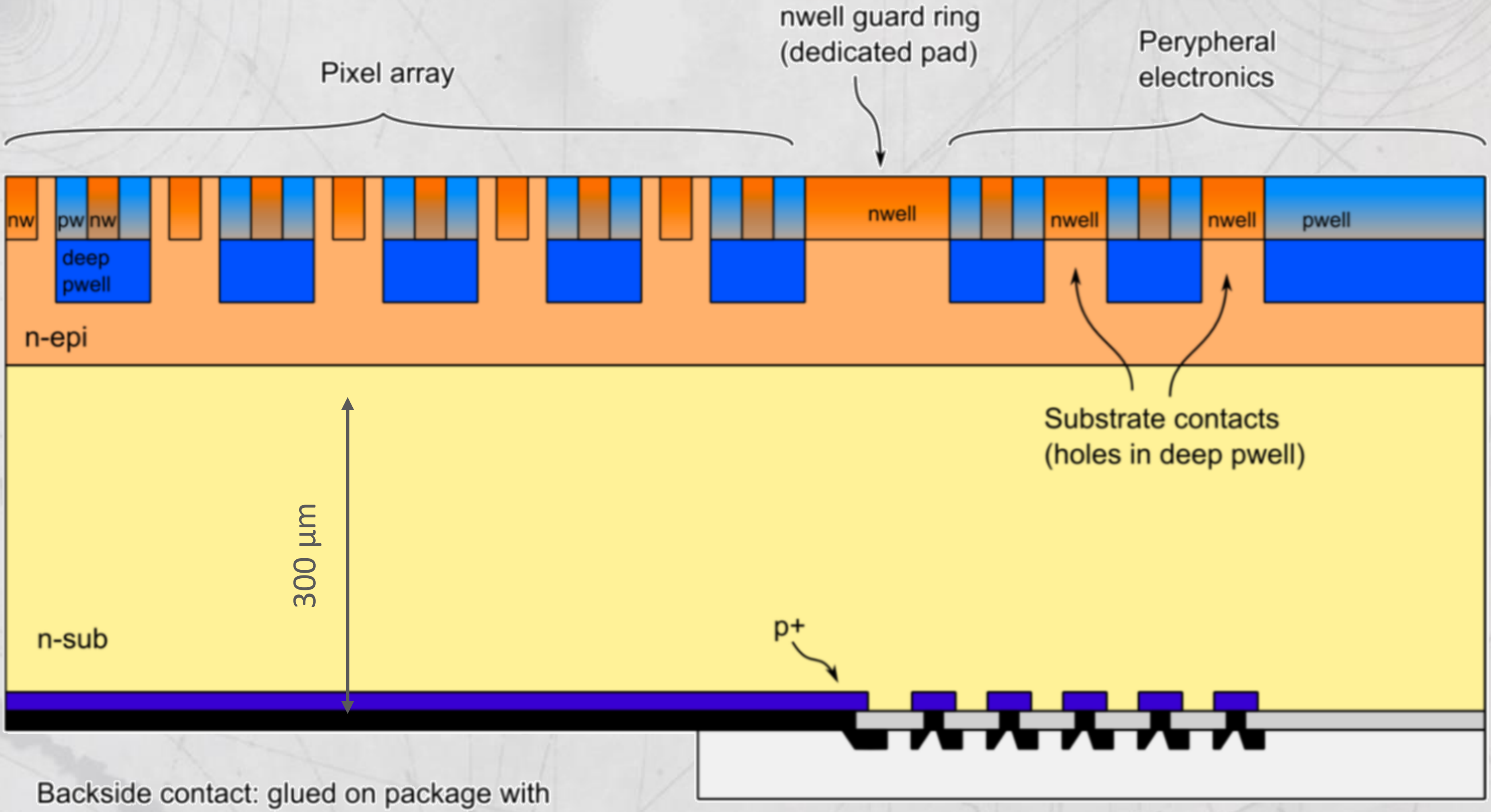
Speed and radiation tolerance are both improved





ARCADIA – fully depleted MAPS – backside processed

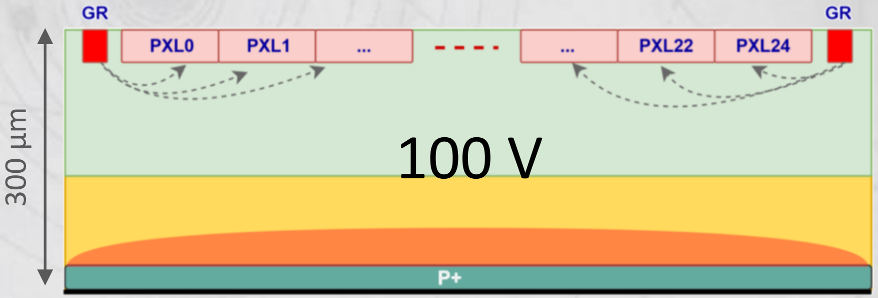
The ARCADIA design uses a sensor solution (SEED) developed in collaboration with LFoundry to achieve uniform, full depletion over thicknesses of few hundreds microns by virtue of a patterned backside (4 mask process).

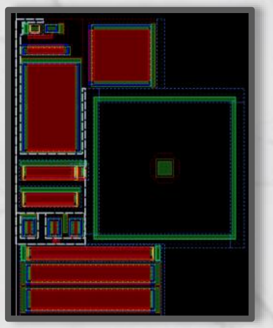


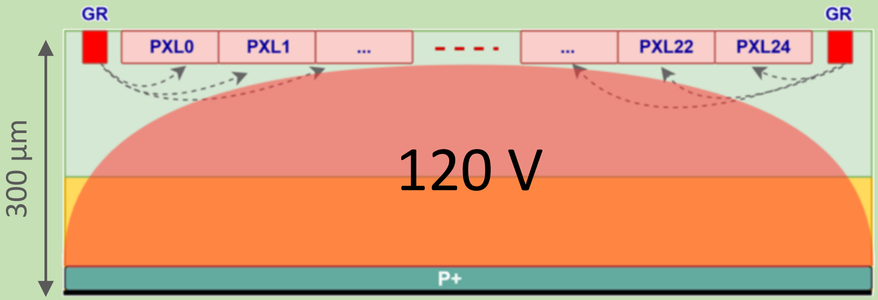
Backside contact: glued on package with conductive epoxy

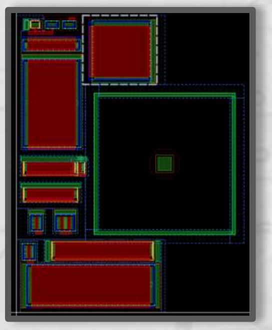
Fully depleted MAPS

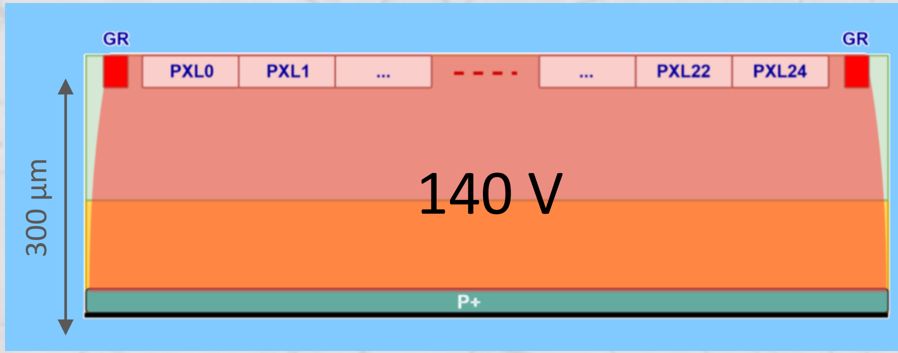
Sensors become fully depleted, with uniform field below the pixel wells, for voltages above 140 V for a 300 µm thick detector. The same happens at lower voltages (60 V) for a thinner version of 100 µm thickness.

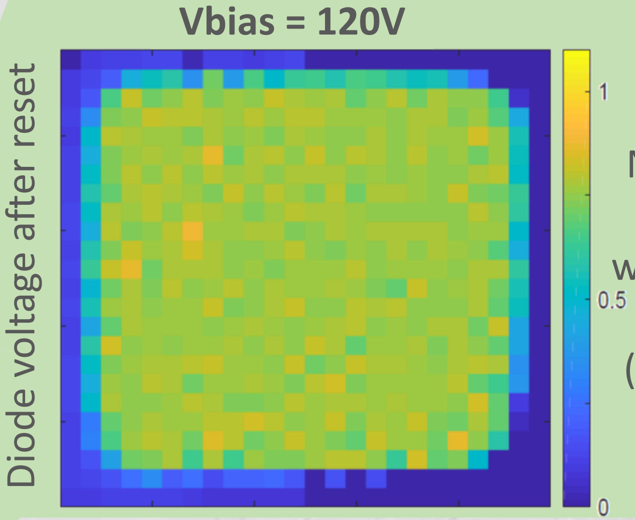




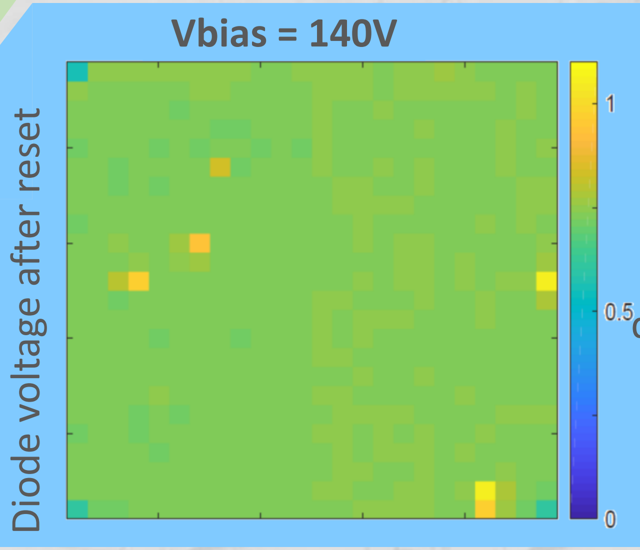








Not yet fully depleted at the sensor periphery, where the diodes remains connected to ground (reset voltage ≈0V at the borders)



Uniform full depletion achieved across the device, even border diodes are insulated from ground (uniform voltage after reset ≈0.6V)

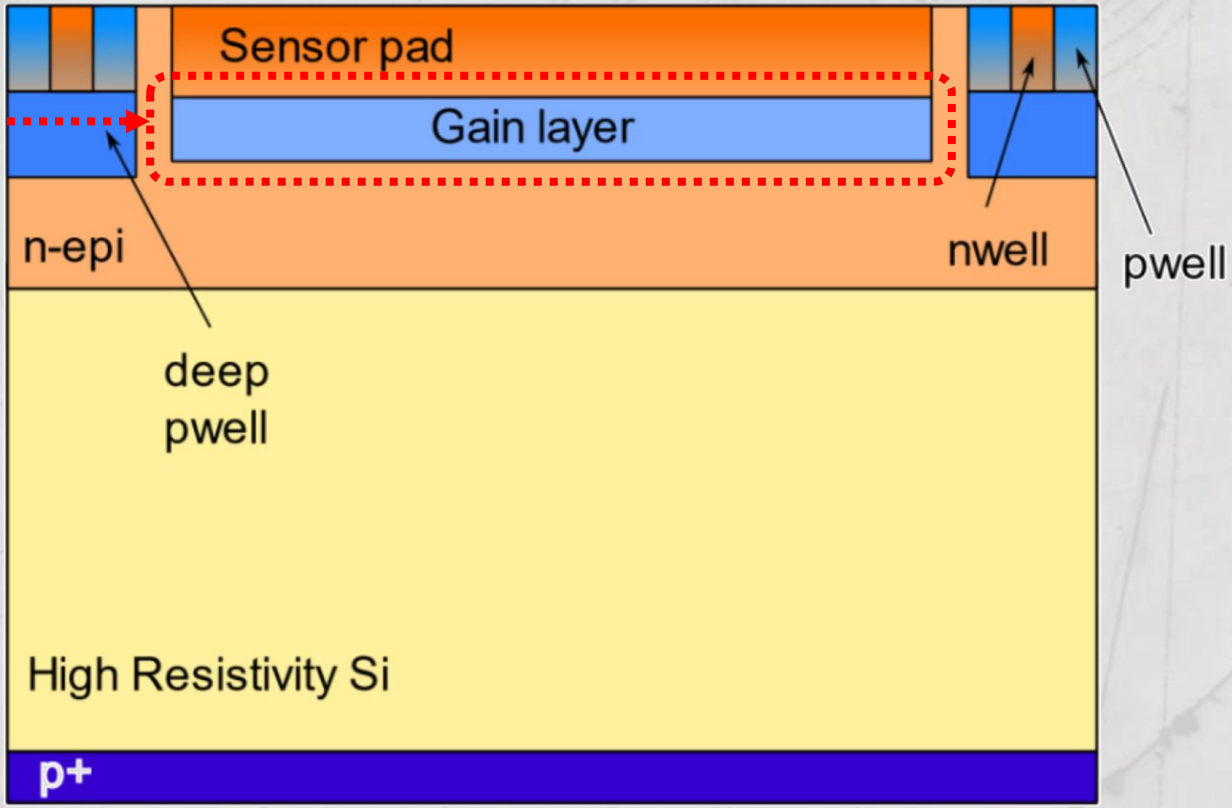
Being tested right now – **here at the FTBF**

ARCADIA sensor for timing – process modification

Stefano Durando

A gain layer can be added with minimal modifications to the process

- With this approach, the sensor should be biased at HV positive bias on the top side of the sensor to increase the gain



Drawbacks:

- Sensor biasing
- AC coupling with the electronics

Simulations :

- Estimation of the dose profile
- Prediction of the impact ionization

ARCADIA sensor for timing – expected performance

Stefano Durando

Sensor simulations:

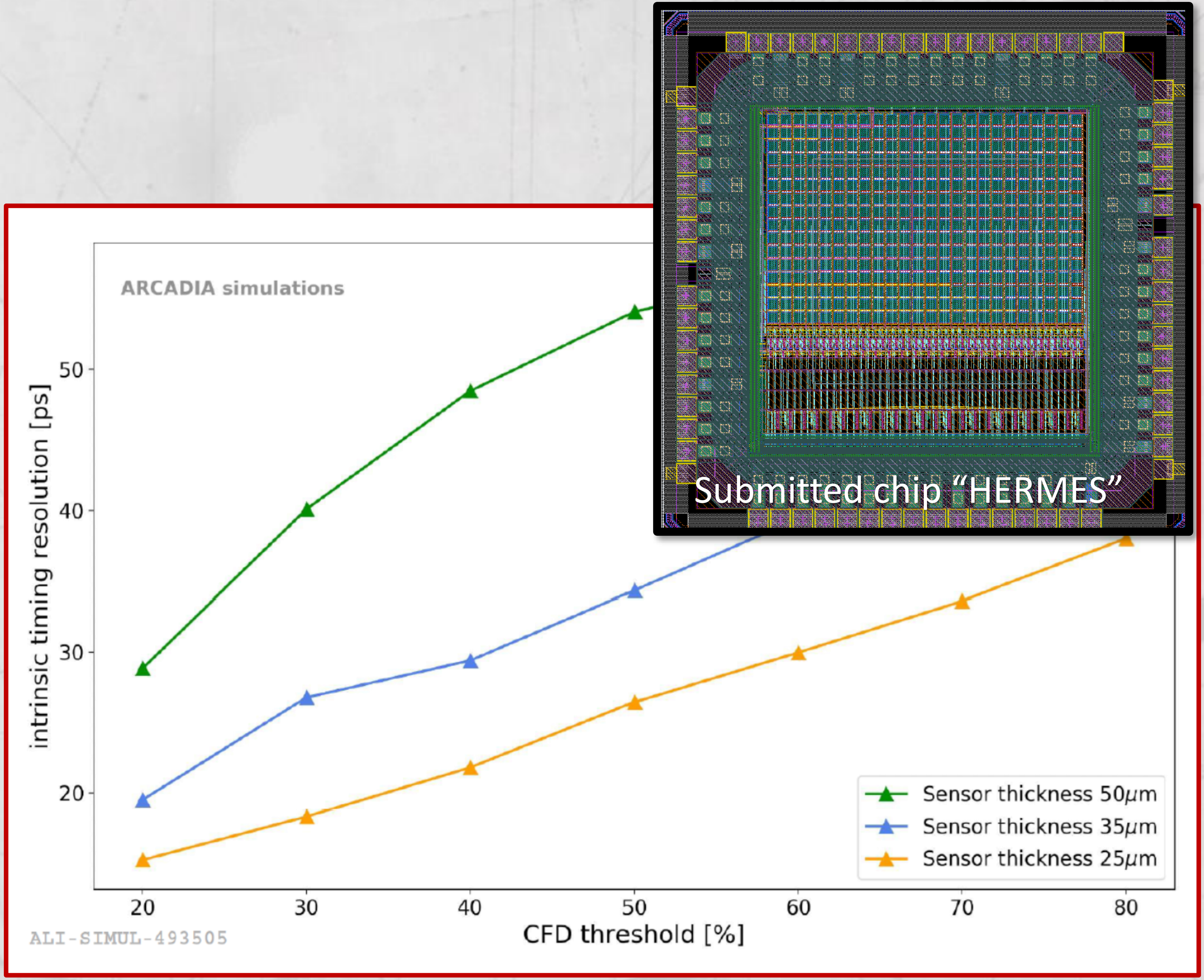
- TCAD, Electric Field & Weighting Potential evaluation, ALLPix2, Pixels

Monte Carlo analysis

- Pitches: 50 - 10 µm
- Thicknesses: 25 - 35 - 50 µm

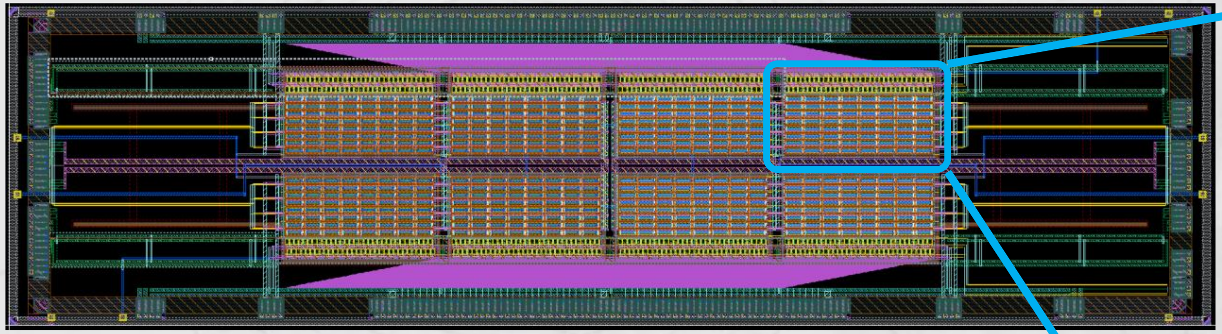
→ Resolution is **20÷30 ps** for the **50 µm pitch**

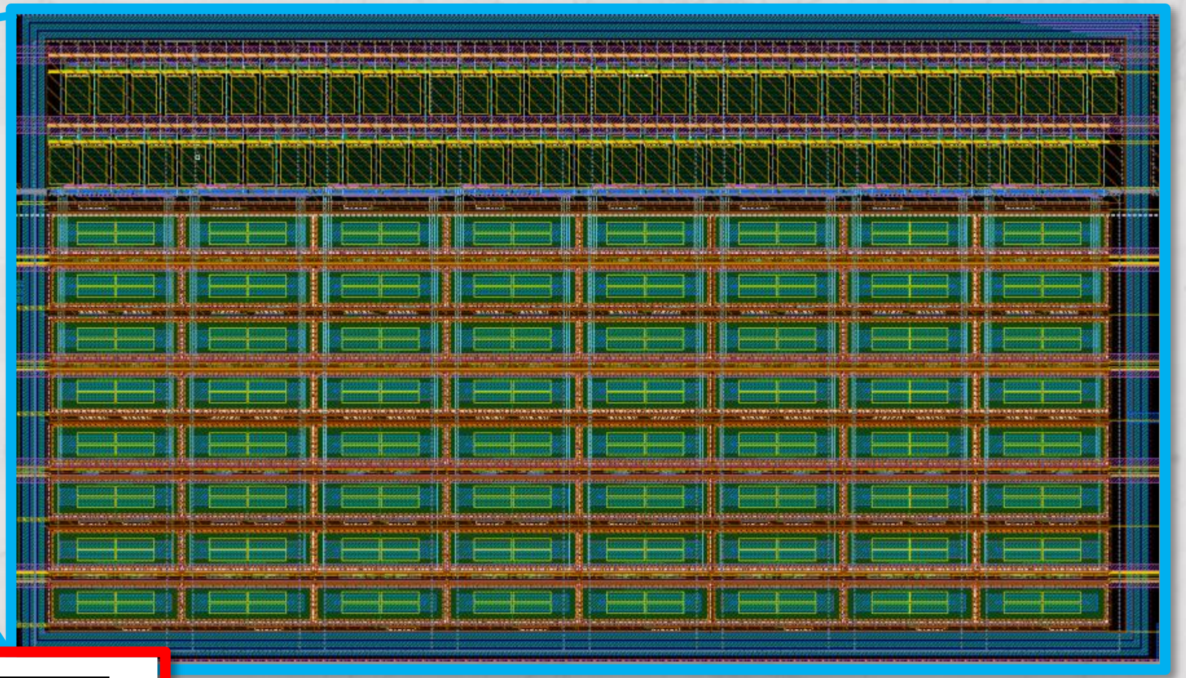
- **Larger PAD sizes** allow for a better field uniformity and better area efficiency
- **Thinner sensors** have a better time resolution
- Still, less charge is generated
- **Increase in the electronics jitter**
- **Gain into the monolithic sensor?**



Submitted chip "HERMES"

ARCADIA sensor for timing – process modification submitted





First demonstrator submitted in July 2022
- 16.4 x 4.4 mm2, 256 x 2 channels
- 110 nm technology node, 6 metal layers
- ARCADIA sensors + additional gain layer
- Silicon just arrived, waiting first measurements

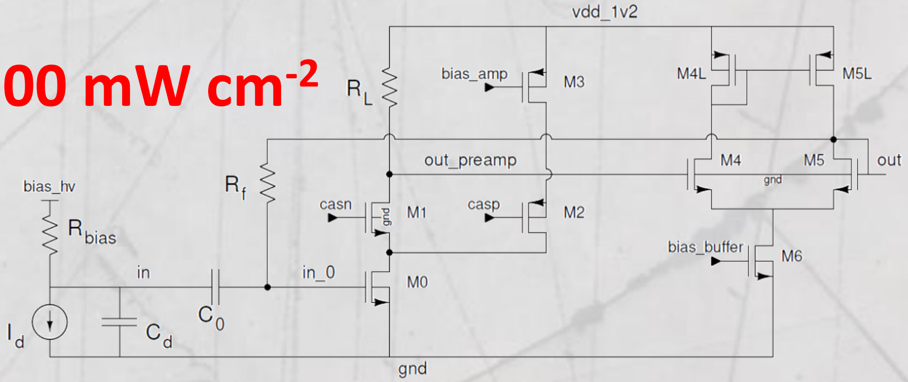
Post layout simulation
- Pixel size = 250 x 100 µm^2
- Diode area ≃ 220 x 70 µm^2
- Sensor cap : Cd ≃ 127 fF
- Electronics area = 250 x 8 µm^2 on the pixel side
- 2 Pixel flavors (different guardrings)
- Minimum active thickness available is 50 µm

Gain	35 mV/fC
BW	460 MHz
rms$_{noise}$	150 e-
PWR	190 uW
jitter$_{10-15-20}$	**10-7-6 ps**

spired by LGADs front-end electronics[1]

300 mW cm^{-2}

I_0	125 µA
I_6	35 µA
Vdd	1.2 V
PWR	190 µW



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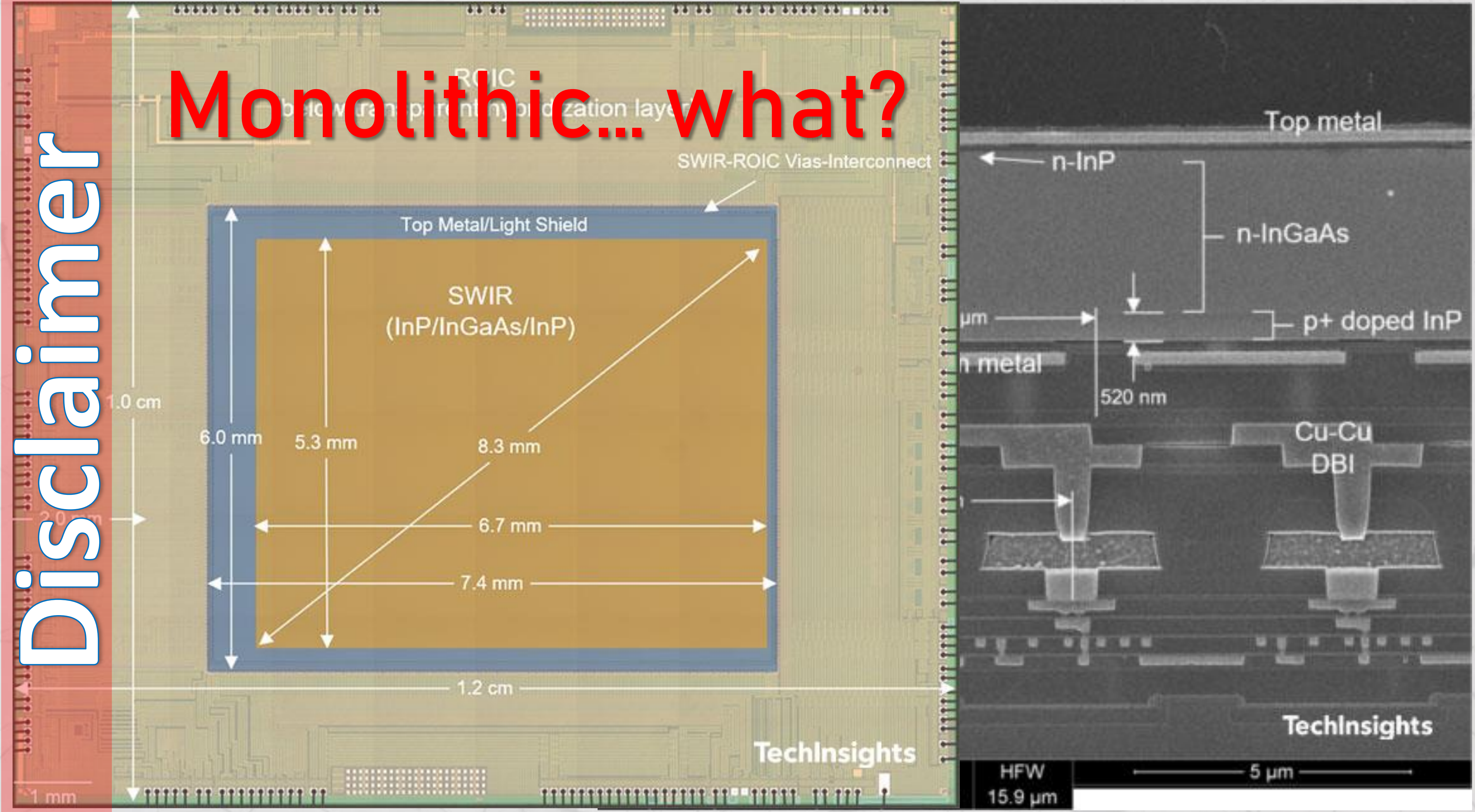
[1] ALCOR, Agapopoulo et al 2020 **JINST 15** P07007

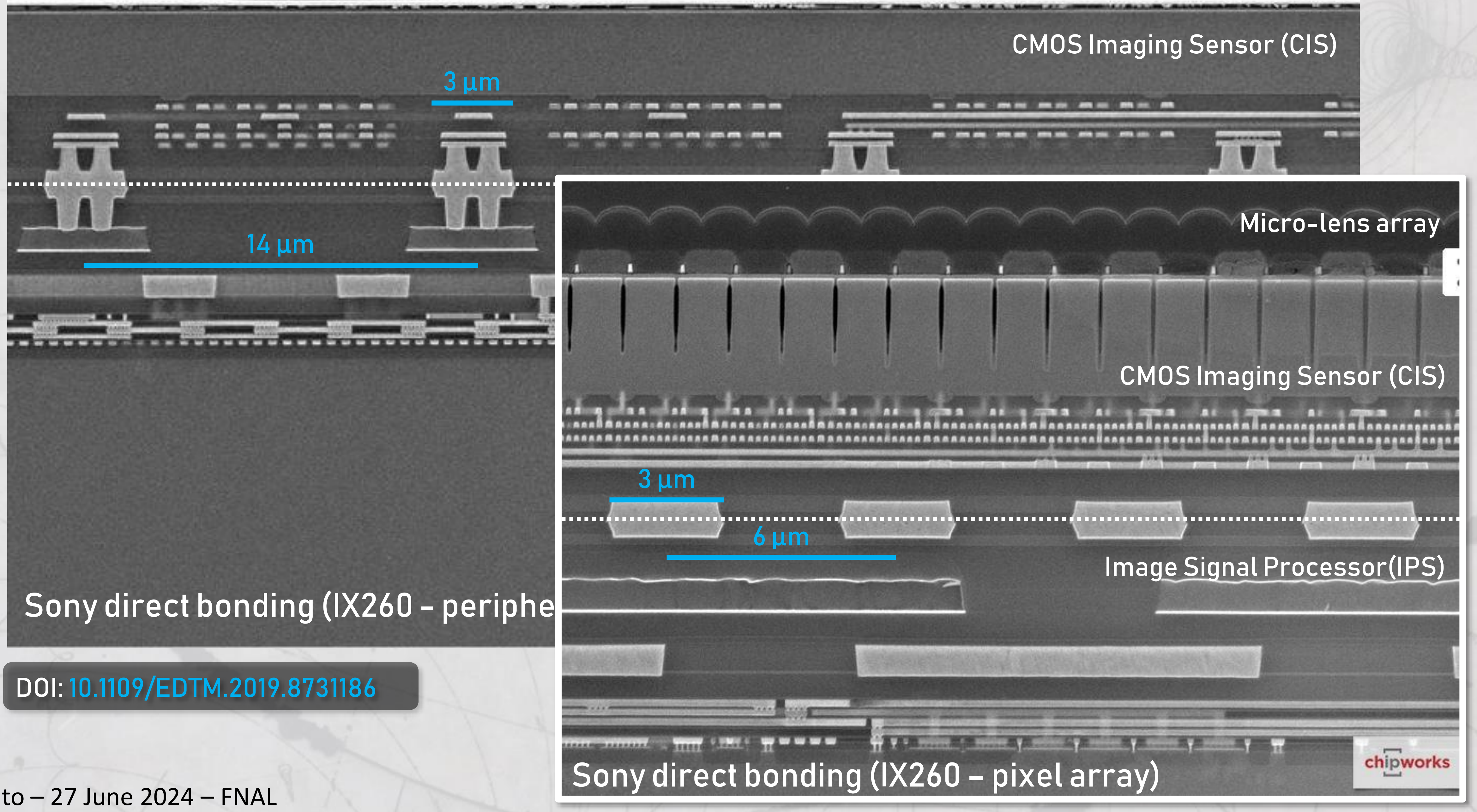
Disclaimer

Monolithic… what?



Disclaimer

Difference is shrinking



Sony direct bonding (IX260 – periphe

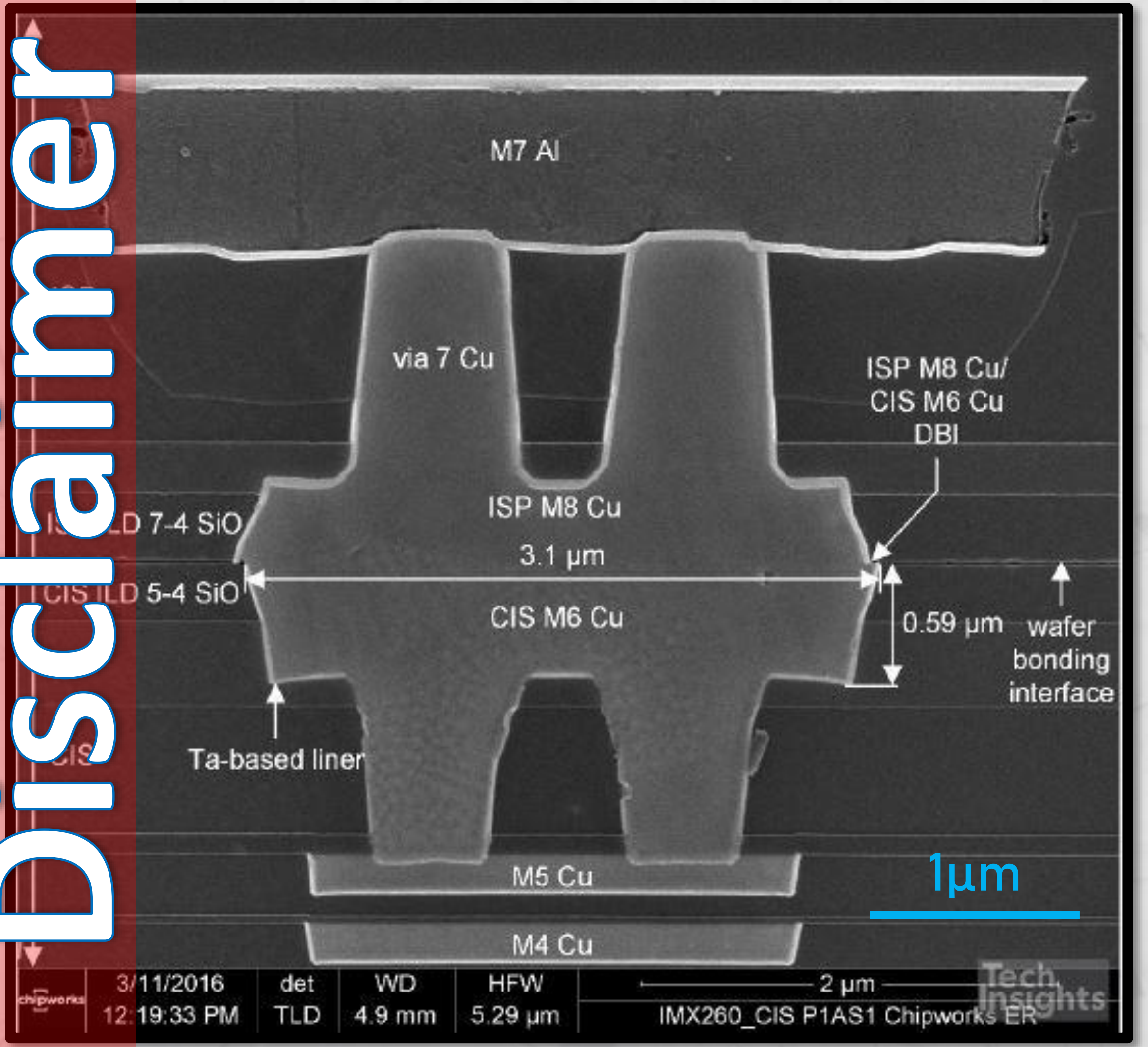
Sony direct bonding (IX260 – pixel array)

DOI: 10.1109/EDTM.2019.8731186

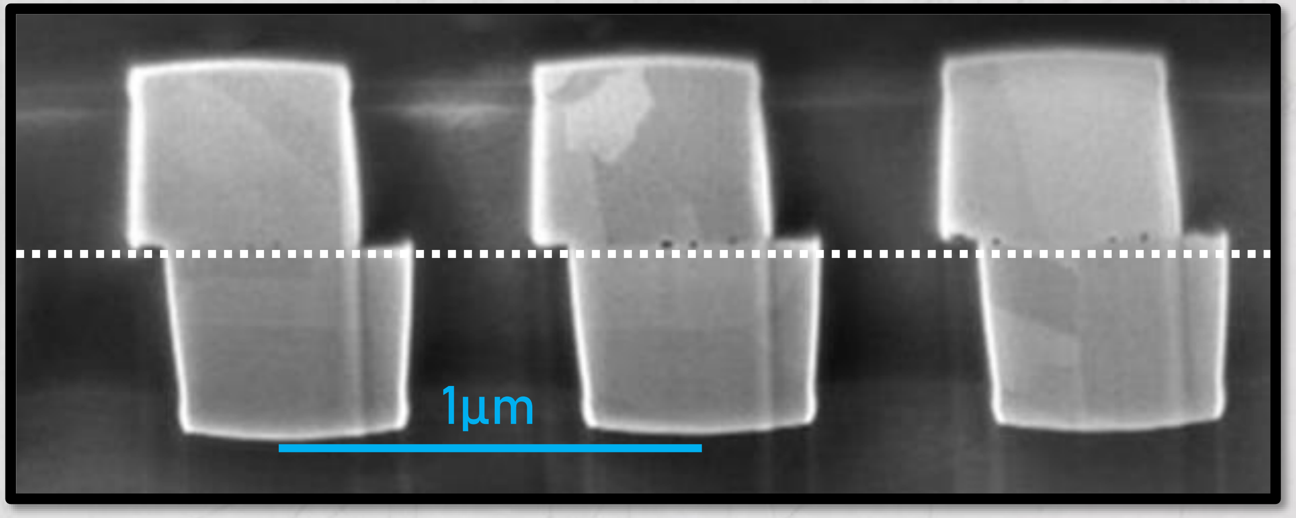
Difference is shrinking – 1 µm pitch possible

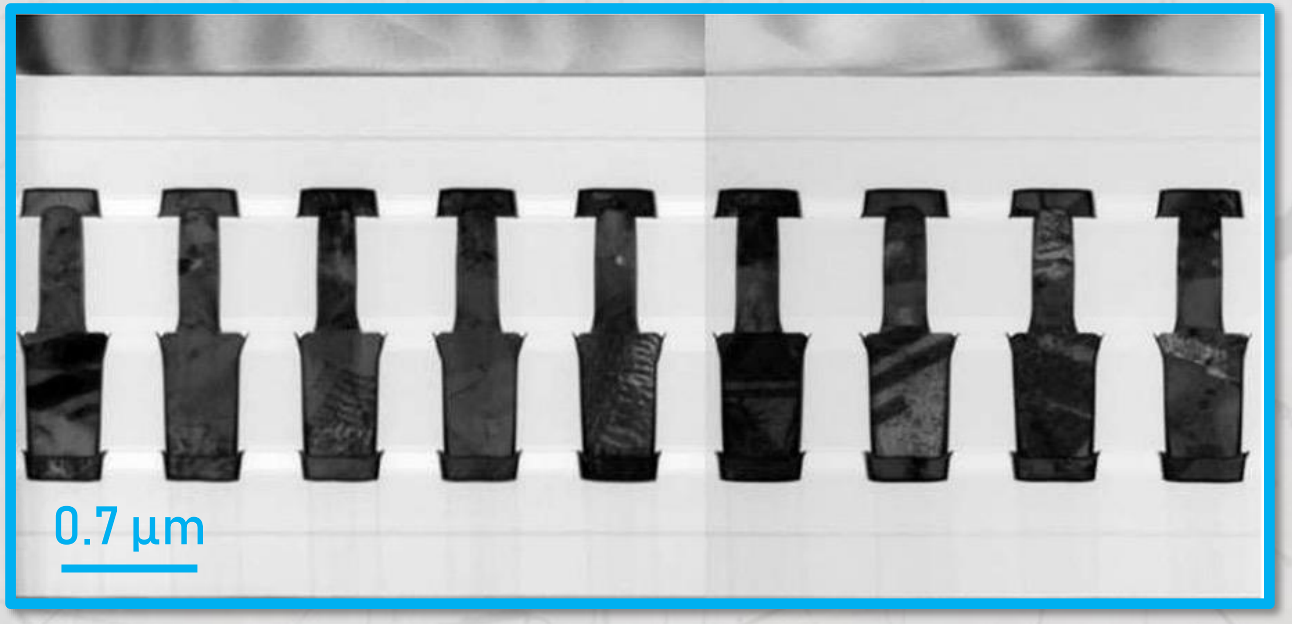
DOI: 10.1109/EDTM.2019.8731186.

Disclaimer



Sony direct bonding (Cu Cu) 1st gen

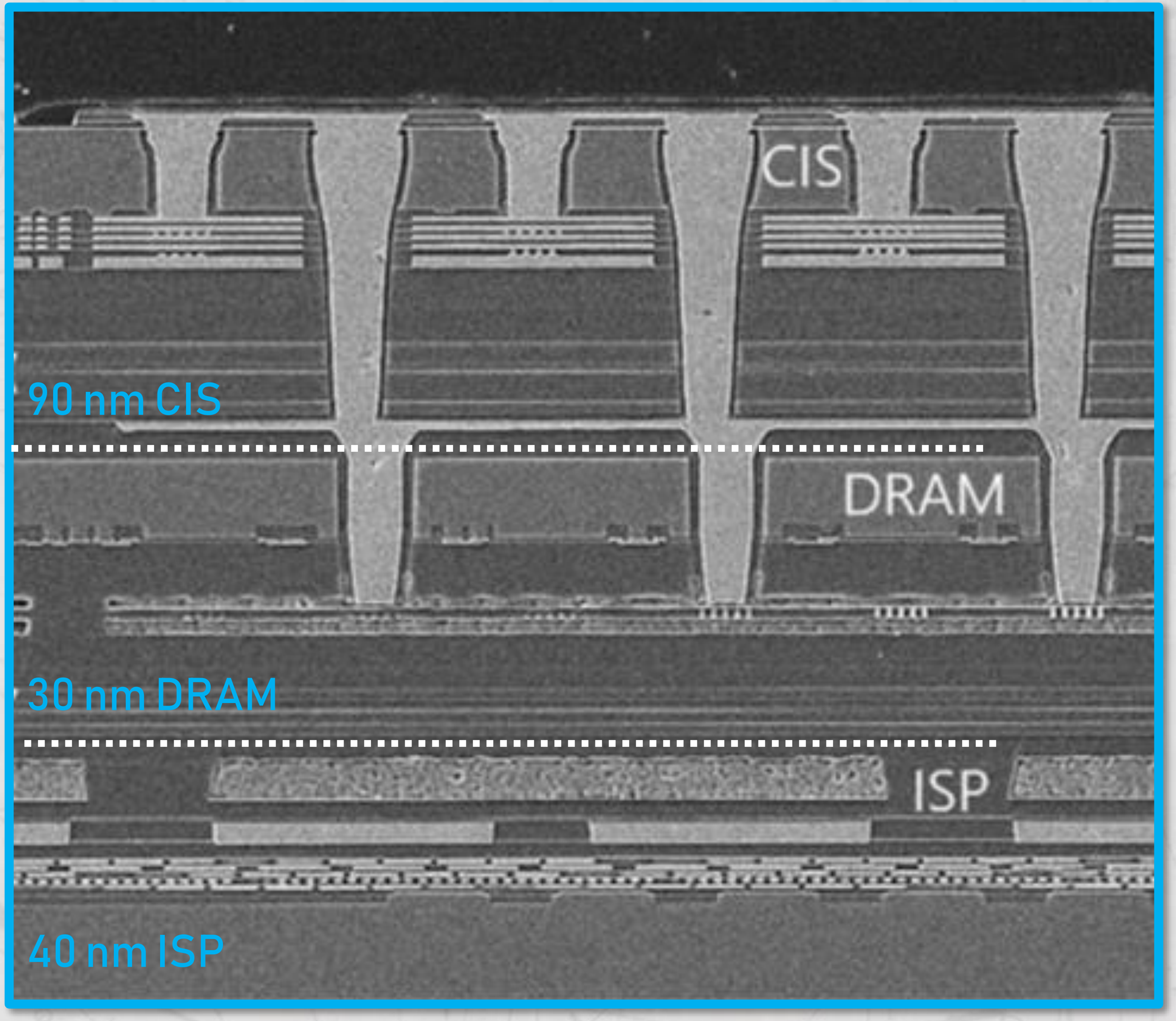




IMEC hybrid bonding

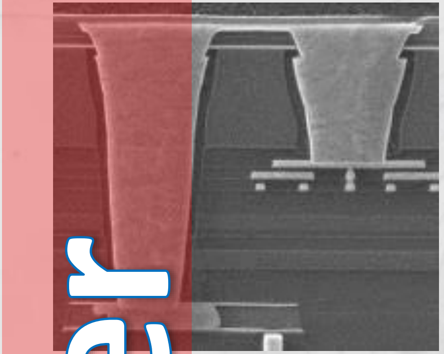
Disclaimer

And more can be added…

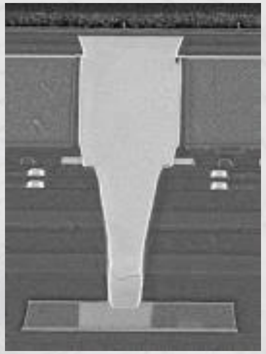


Sony 3-stacked imager (IX400, 2017)

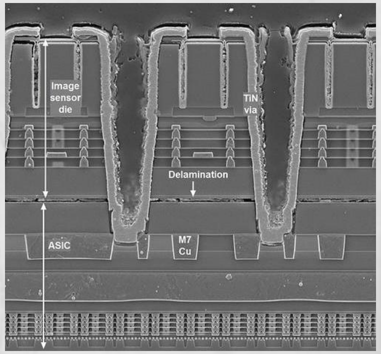
Disclaimer



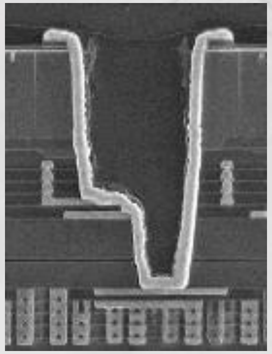
Sony 1st TSV (2013)



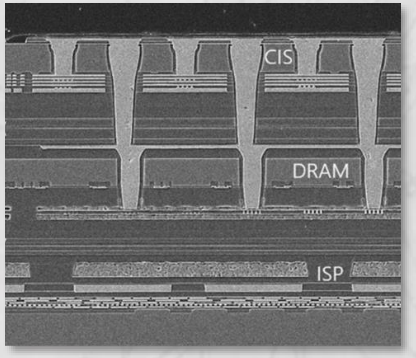
Sony 2nd TSV (2015)



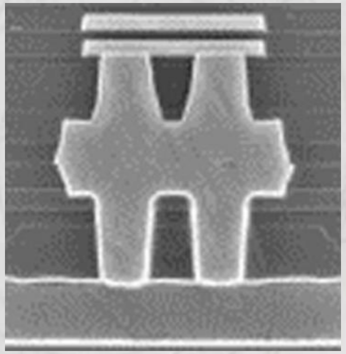
Samsung TSV (2016)



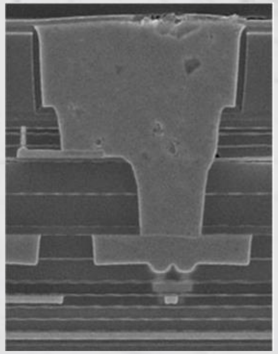
Samsung butted TSV



Sony 3 layer (2017)

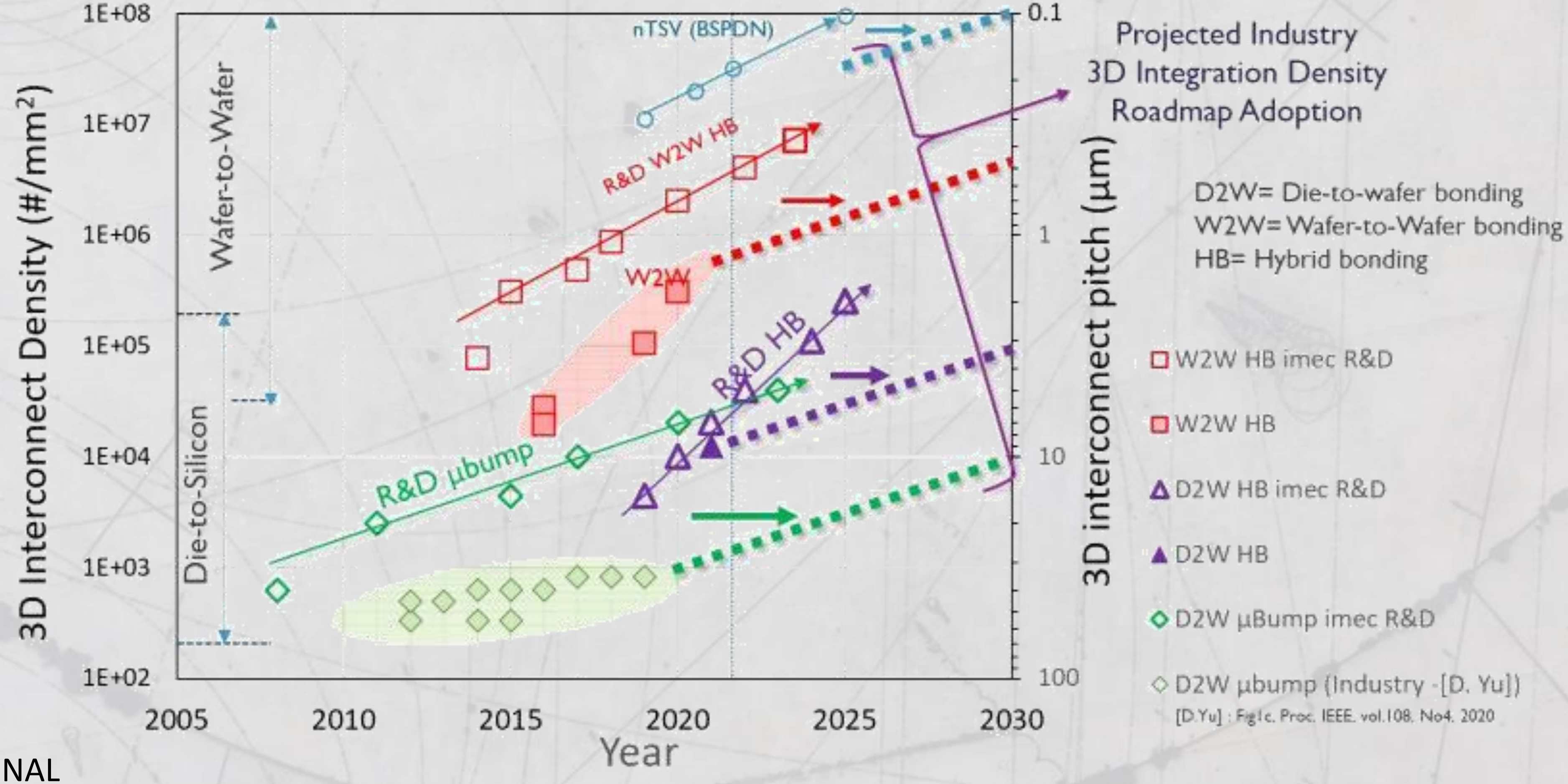


Sony 1st DBI (2018)



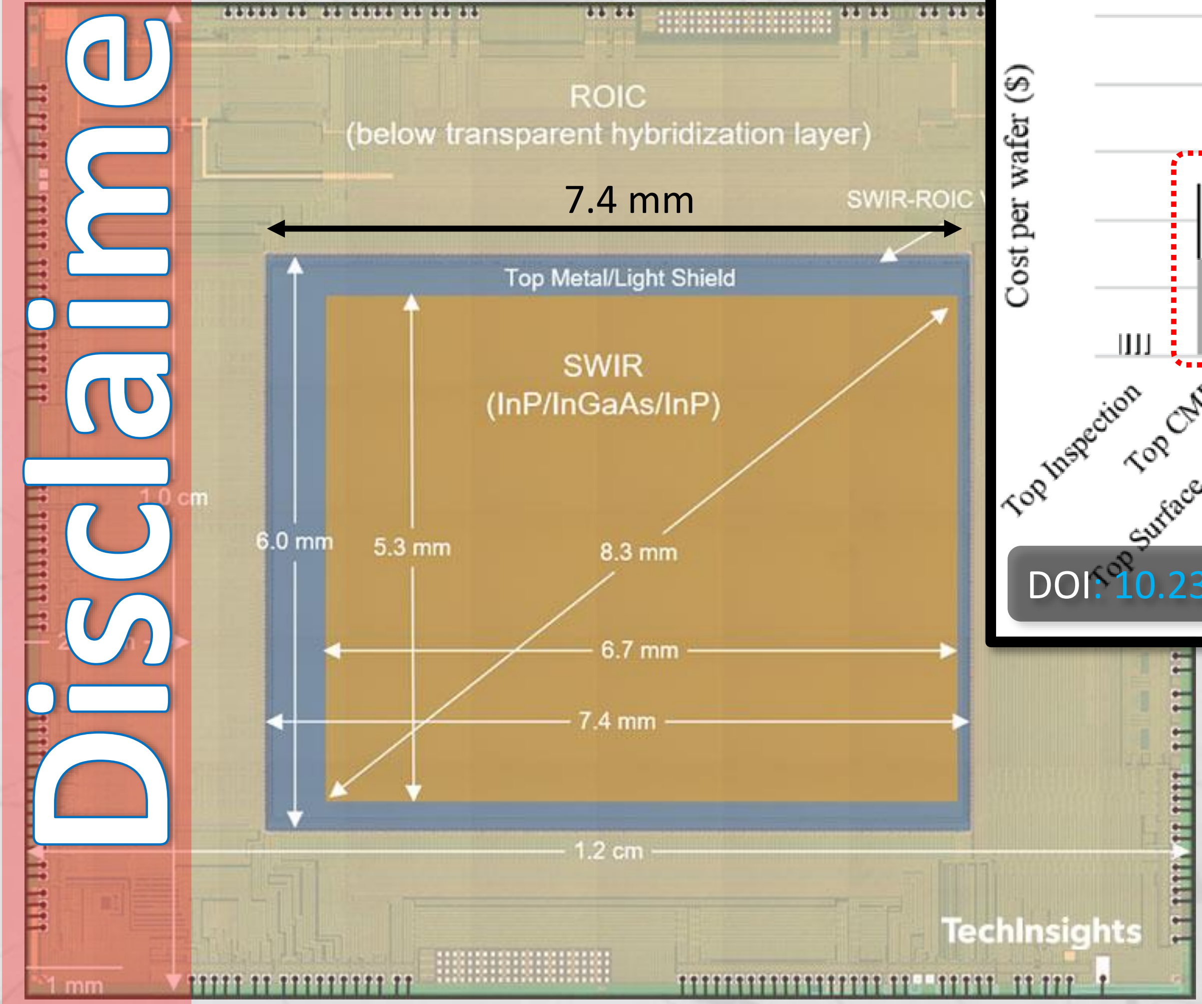
Omnivision 1st TSV (2013)

Omnivision 2nd TSV (2017)

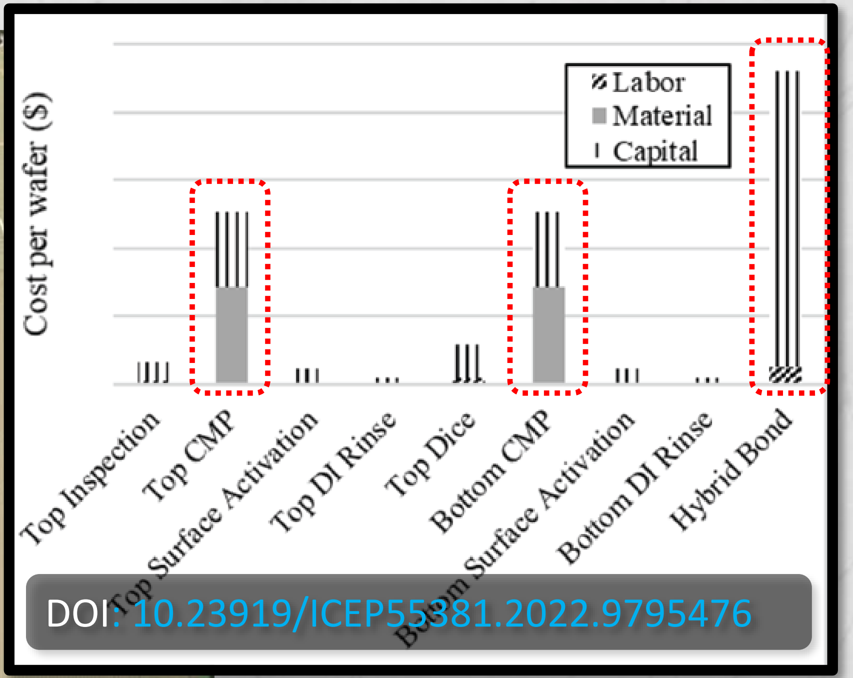


Unfortunately, not yet there for large area sensor

Disclaimer

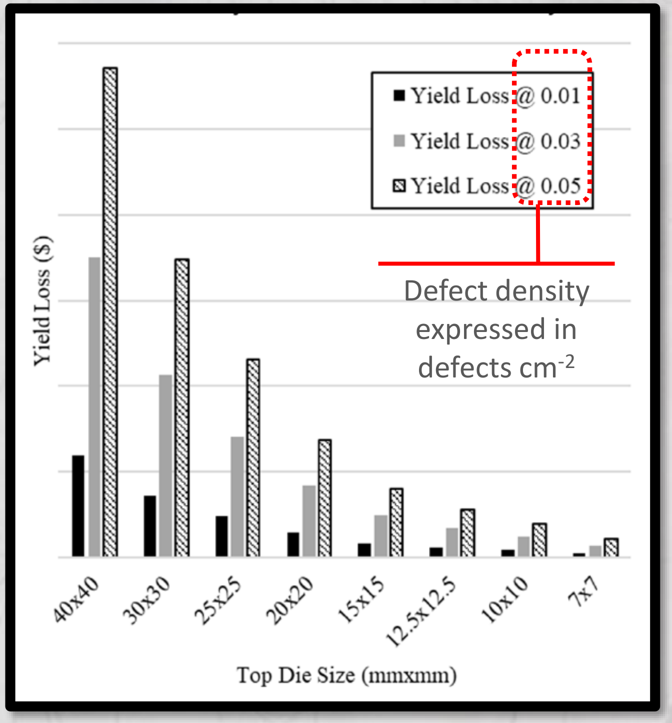


Processing costs breakdown for D2W Hybrid bonding



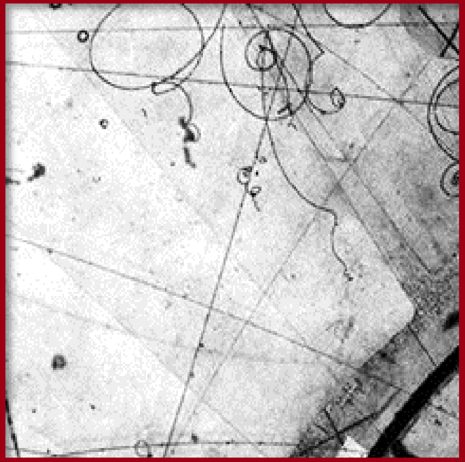
DOI: 10.23919/ICEP55381.2022.9795476

Yield Loss by Die Size and Defect Density



Practical limitation for (our) tracking application are

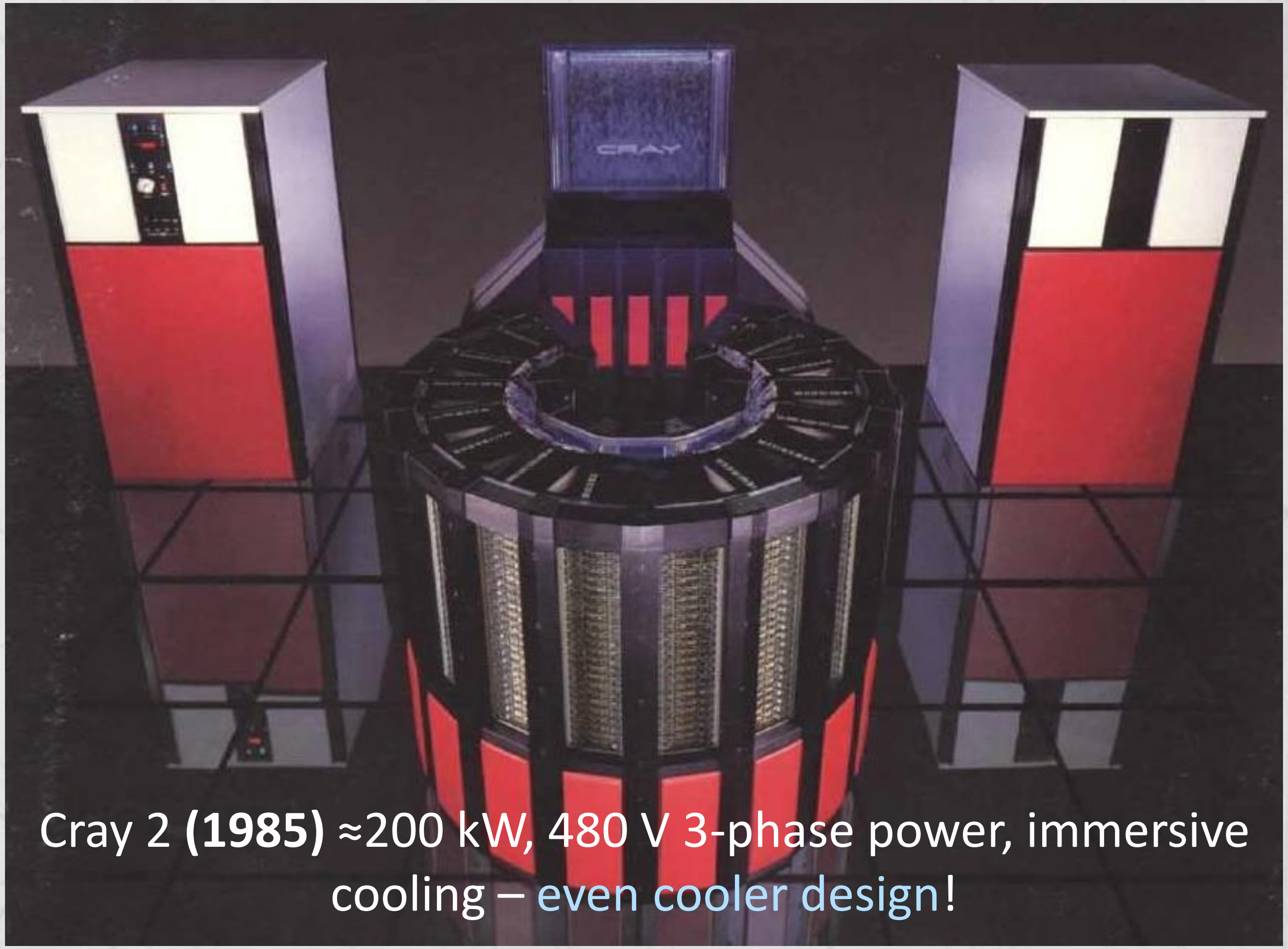
- accessibility: intended for 1000nds chips/hour
- yield/cost (for large area)
- maximum area: 40x40 mm^2 at present
- capacitance to be understood for low power



A different viewpoint

Computers as benchmark for information cost

Cray 1 **(1979)** – cool design dictated by cooling needs!

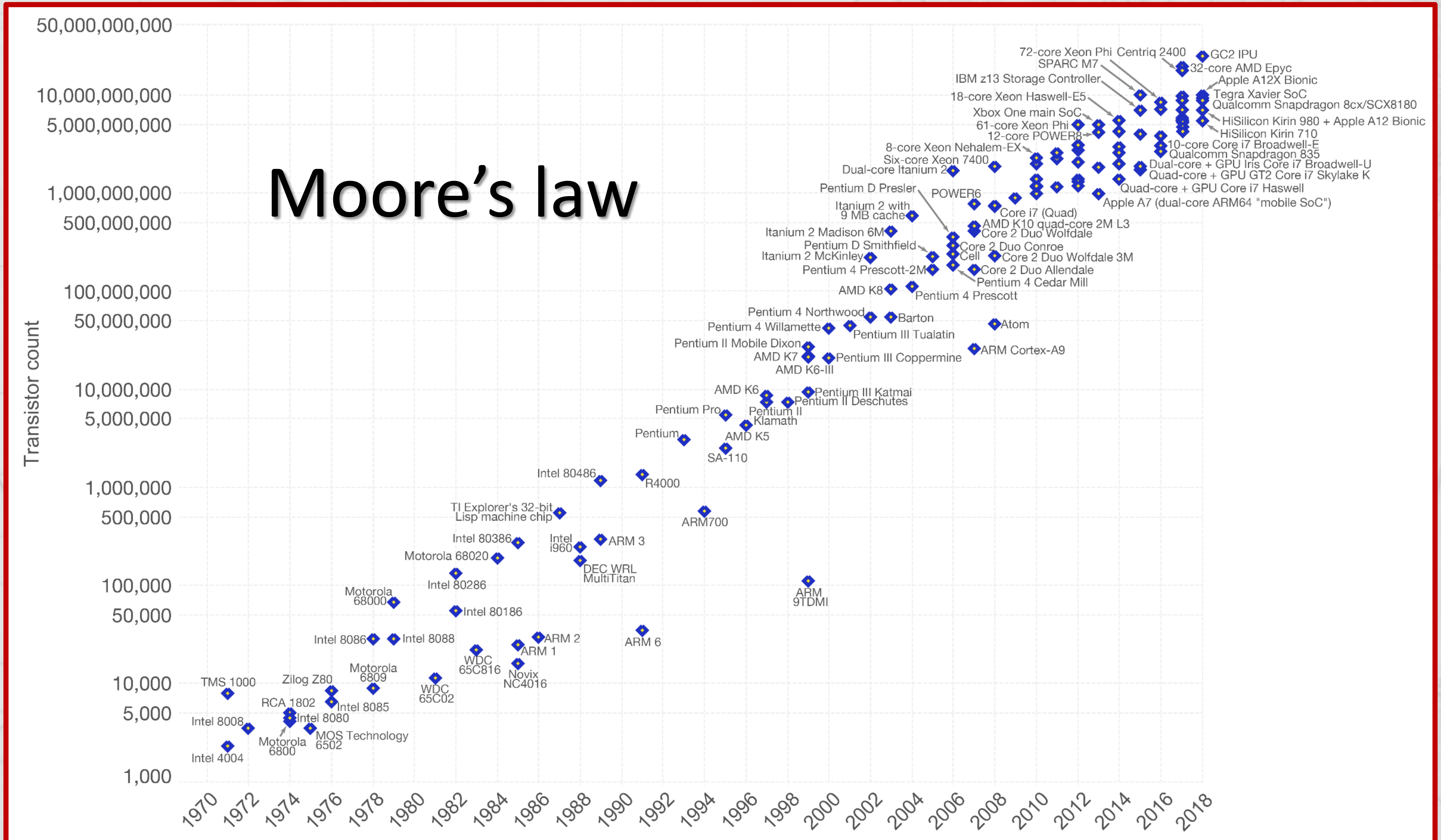


Cray 2 **(1985)** ≈200 kW, 480 V 3-phase power, immersive cooling – even cooler design!

Comparable computing power of Cray 2 on batteries!

The trend in the last 40+ years has been **decreasing the costs** (both energy and manufacturing) while **increasing the density** (stacking more transistors in the same volume). **What the consequences?**

Moore’s law



Transistor count
50,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
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1,000
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
2018
72-core Xeon Phi
Centriq 2400
GC2 IPU
SPARC M7
32-core AMD Epyc
IBM z13 Storage Controller
Apple A12X Bionic
18-core Xeon Haswell-E5
Tegra Xavier SoC
Qualcomm Snapdragon 8cx/SCX8180
Xbox One main SoC
61-core Xeon Phi
HiSilicon Kirin 980 + Apple A12 Bionic
12-core POWER8
HiSilicon Kirin 710
8-core Xeon Nehalem-EX
10-core Core i7 Broadwell-E
Six-core Xeon 7400
Qualcomm Snapdragon 835
Dual-core Itanium 2
Dual-core + GPU Iris Core i7 Broadwell-U
Quad-core + GPU GT2 Core i7 Skylake K
Pentium D Presler
POWER6
Quad-core + GPU Core i7 Haswell
Apple A7 (dual-core ARM64 "mobile SoC")
Itanium 2 with 9 MB cache
Core i7 (Quad)
AMD K10 quad-core 2M L3
Itanium 2 Madison 6M
Core 2 Duo Wolfdale
Pentium D Smithfield
Core 2 Duo Conroe
Itanium 2 McKinley
Cell
Core 2 Duo Wolfdale 3M
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Pentium 4 Cedar Mill
AMD K8
Pentium 4 Prescott
Pentium 4 Northwood
Barton
Pentium 4 Willamette
Pentium III Tualatin
Atom
Pentium II Mobile Dixon
AMD K7
Pentium III Coppermine
ARM Cortex-A9
AMD K6-III
AMD K6
Pentium III Katmai
Pentium II Deschutes
Pentium Pro
Pentium II Klamath
AMD K5
Pentium
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
ARM700
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
ARM 9TDMI
Motorola 68000
Intel 80186
Intel 8086
Intel 8088
ARM 2
ARM 6
WDC 65C816
ARM 1
Novix NC4016
Motorola 6809
TMS 1000
Zilog Z80
WDC 65C02
RCA 1802
Intel 8085
Intel 8080
Intel 8008
MOS Technology 6502
Motorola 6800
Intel 4004

The other side of the Moore’s law: complexity increases exponentially as well!

Apple I (1976)

1 (very good) electronic engineer (Steve Wozniak) who designed everything at night (was working at HP during the day).

Walkman (1979)

1 audio engineer who modified a pre-existent recorder to satisfy his CEO wish of listening music while on the plane.

Digital SLR (1999)

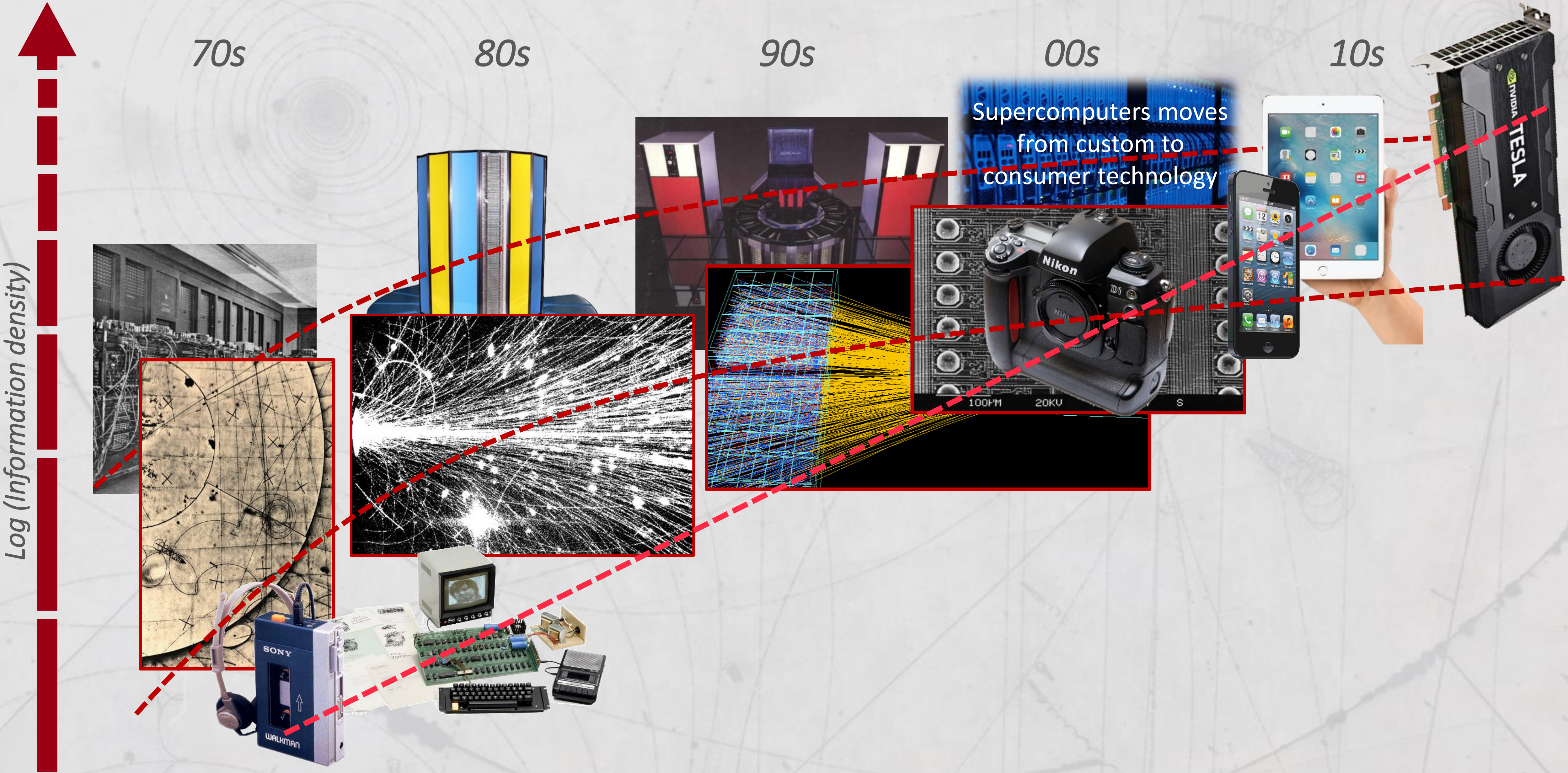
Small R&D team

Adapting available tech (3 M pixels out of 10M), outsourcing the sensor

iPhone 1 (2006)

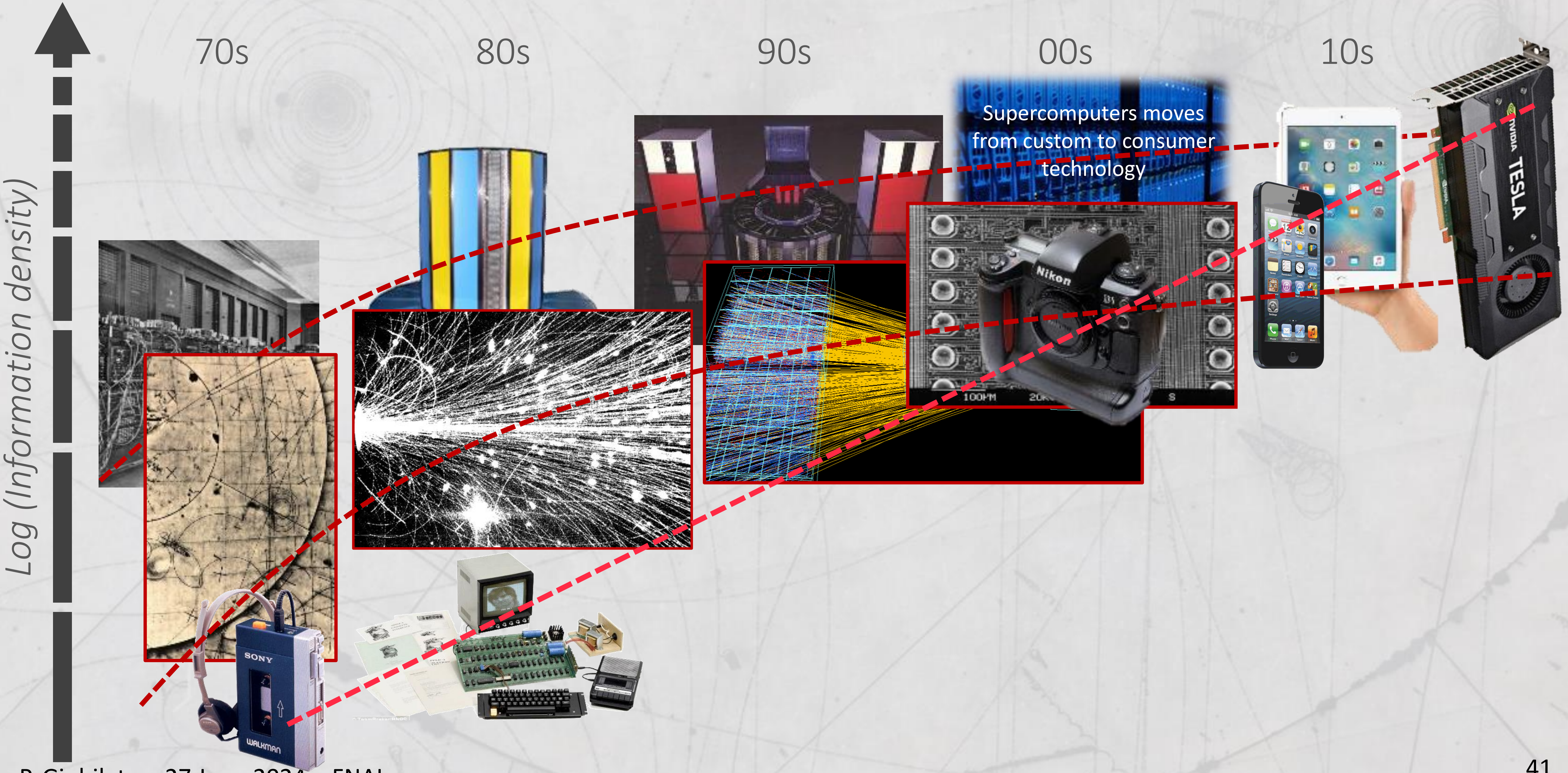
Team of 1000 employees working on "Project Purple“, 150 Million $ over 30 months, collaboration with AT&T.

Where do we physicists stand?

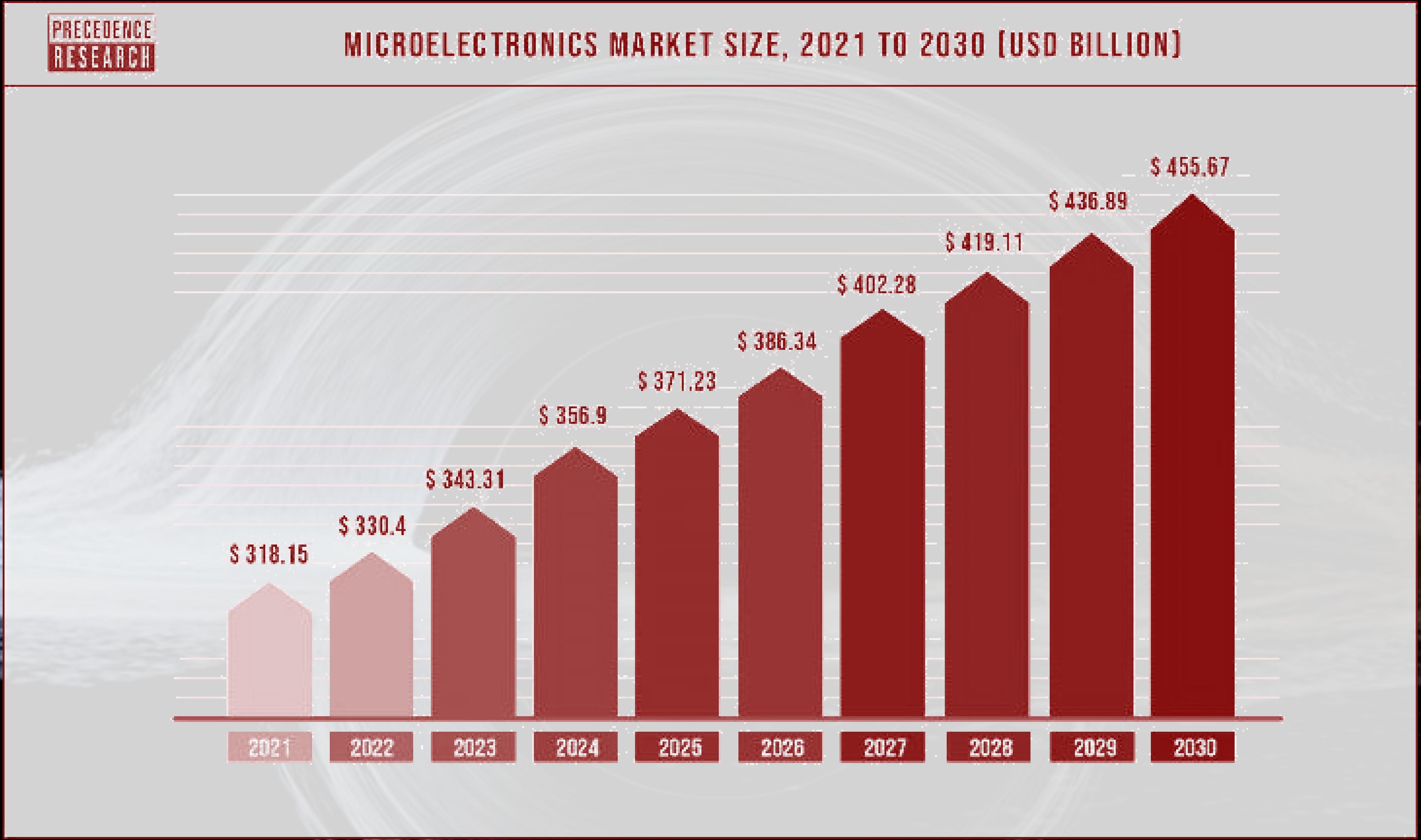


Supercomputers moves from custom to consumer technology

Where do we physicists stand?



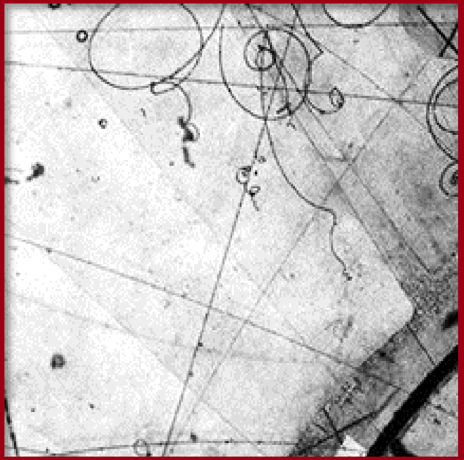
Supercomputers moves from custom to consumer technology



Interstellar's black hole "Gargantua" is not scientifically accurate (as shown in the movie) but the simulation produced 800 TByte of unprecedented quality data, which lead Kip Thorne (Nobel prize 2017) to investigate some unexpected effects (which you cannot see in the movie) about the lensing effect.

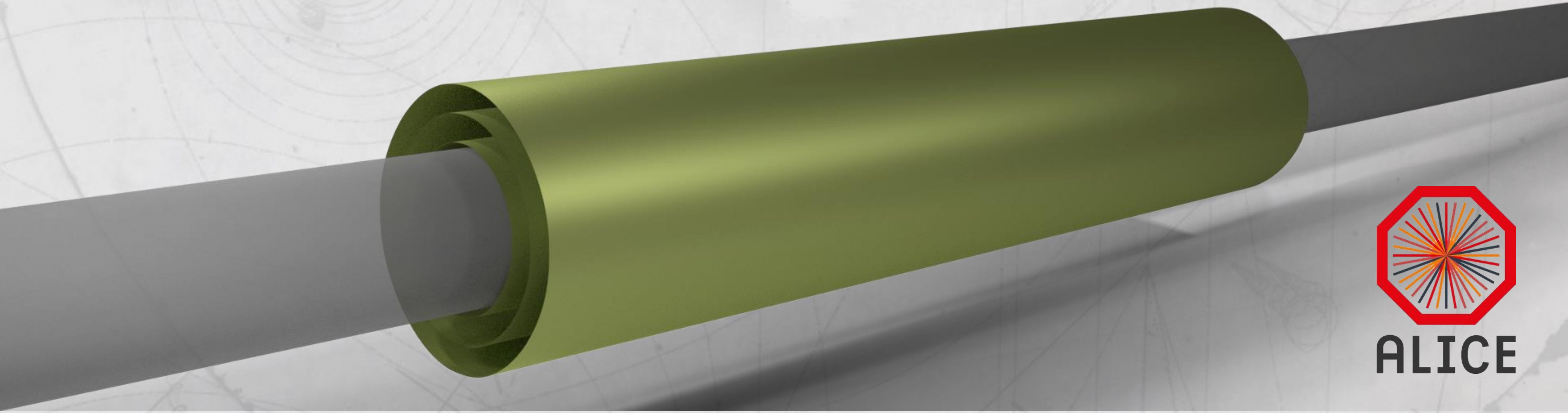
Class. Quantum Grav. **32** (2015) 065001

Thorne K S 2014 The Science of Interstellar



Trackers – ITS3

ALICE ITS3 vertex tracker (under construction)

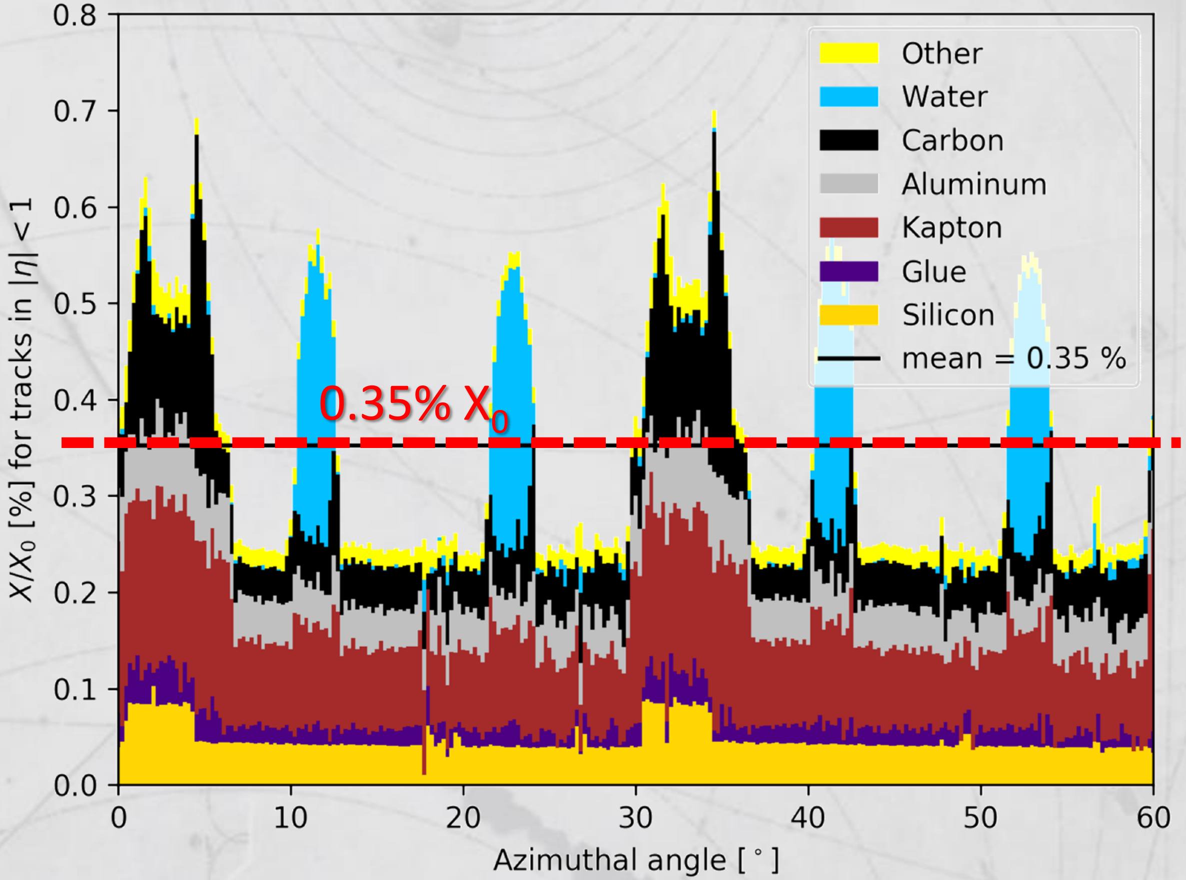


Simple idea: self-sustaining bent sensors, with no support

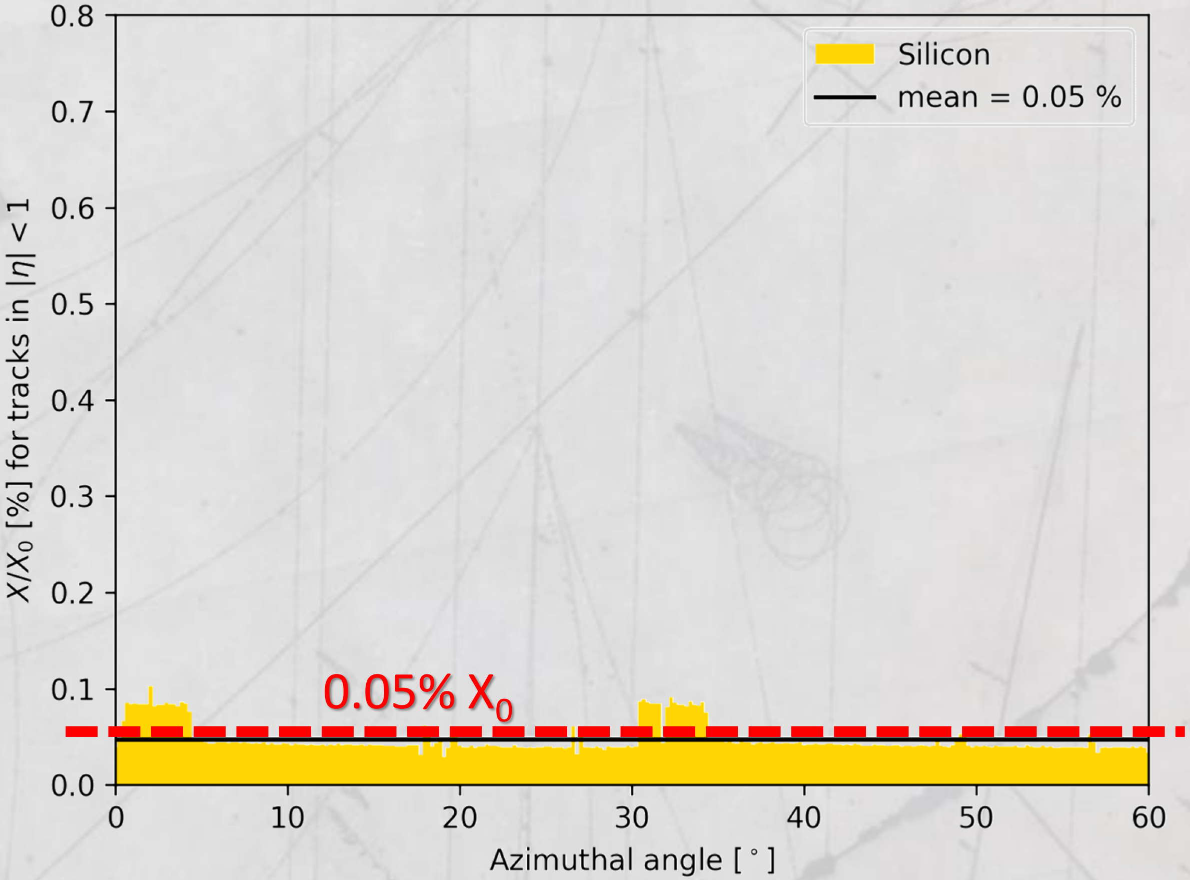
Possible when the sensor is thinned down to around 40 µm.

Vertexing – material budget advantage

Material budget – current ALICE ITS2



Material budget – foreseen ALICE ITS3



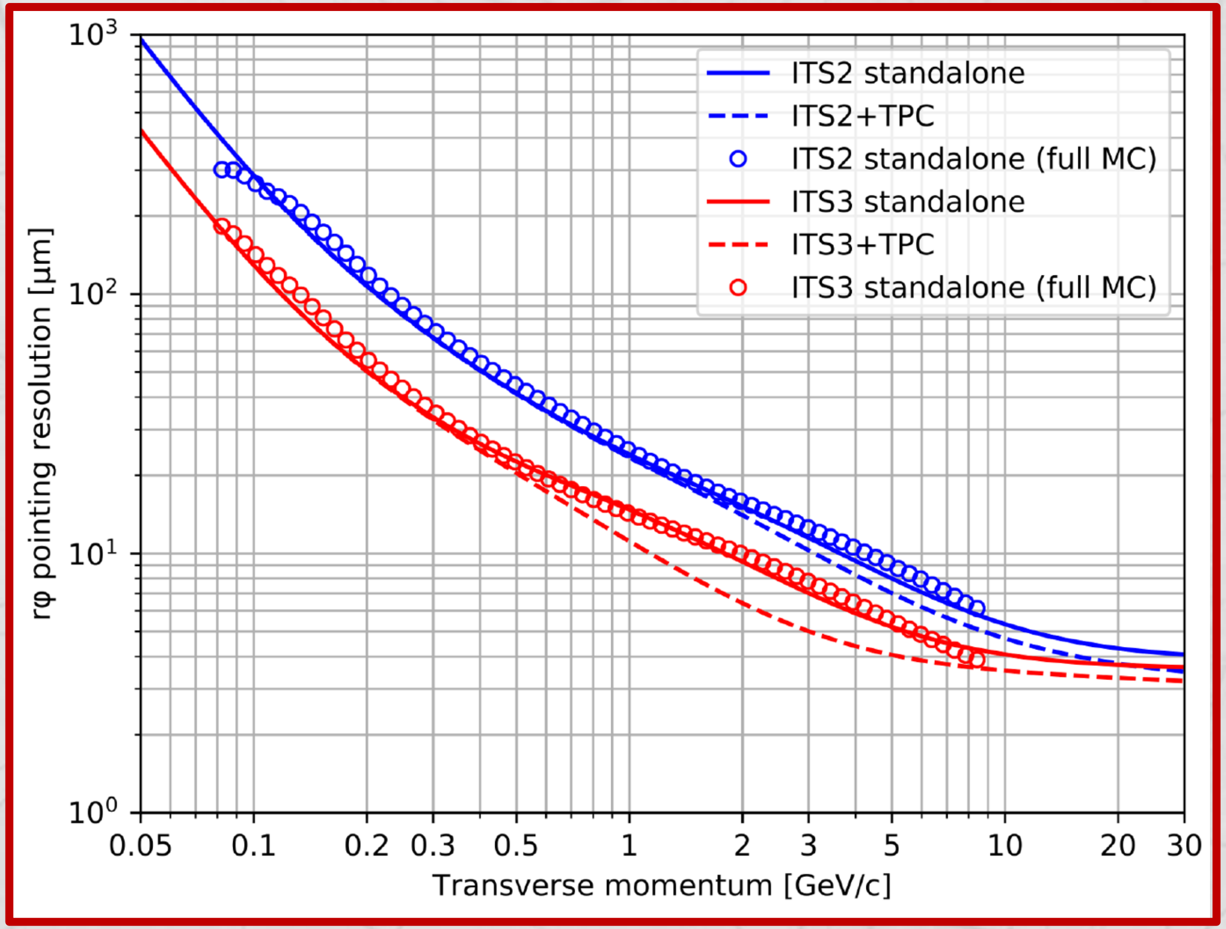
Vertexing – improved performance

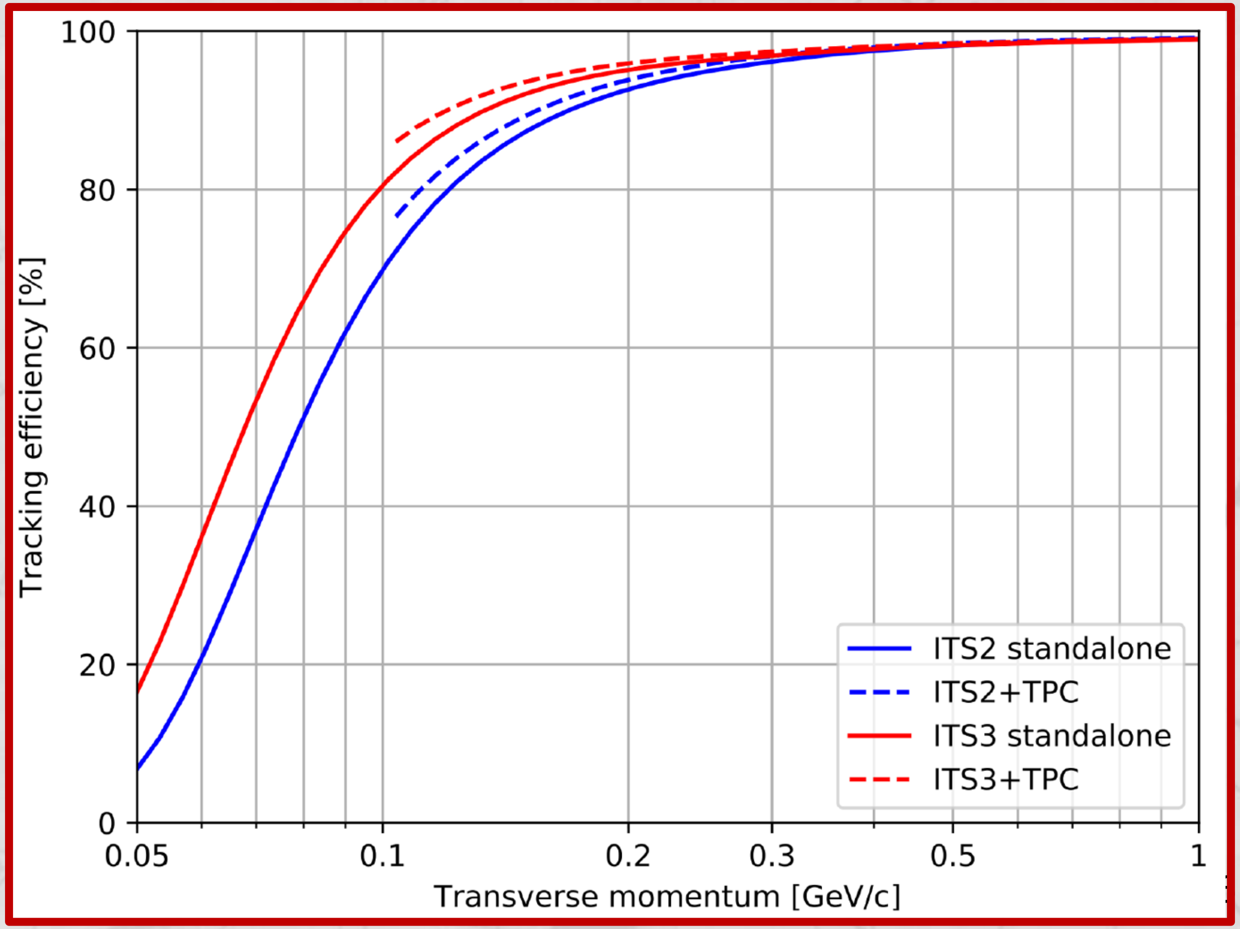
3 Cylindrical layers

- Made with 6 curved wafer-scale single-die
- Monolithic Active Pixel Sensors
- Radii 18/24/30 mm, length 27 cm
- Thinned down to <50 µm

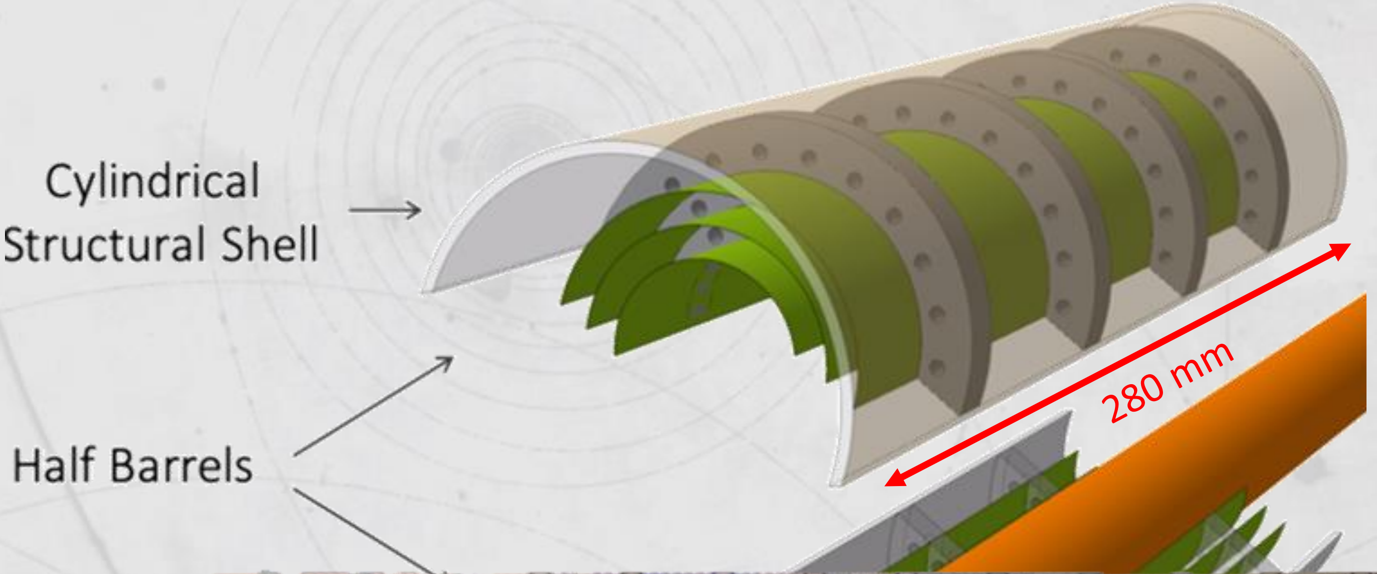
Position resolution ~5 µm

- Pixels Q(20 µm)
- No flexible circuits in the active area
- Distribute supply and transfer data on chip to the short edge





Vertexing – 280 mm long sensors, self sustaining

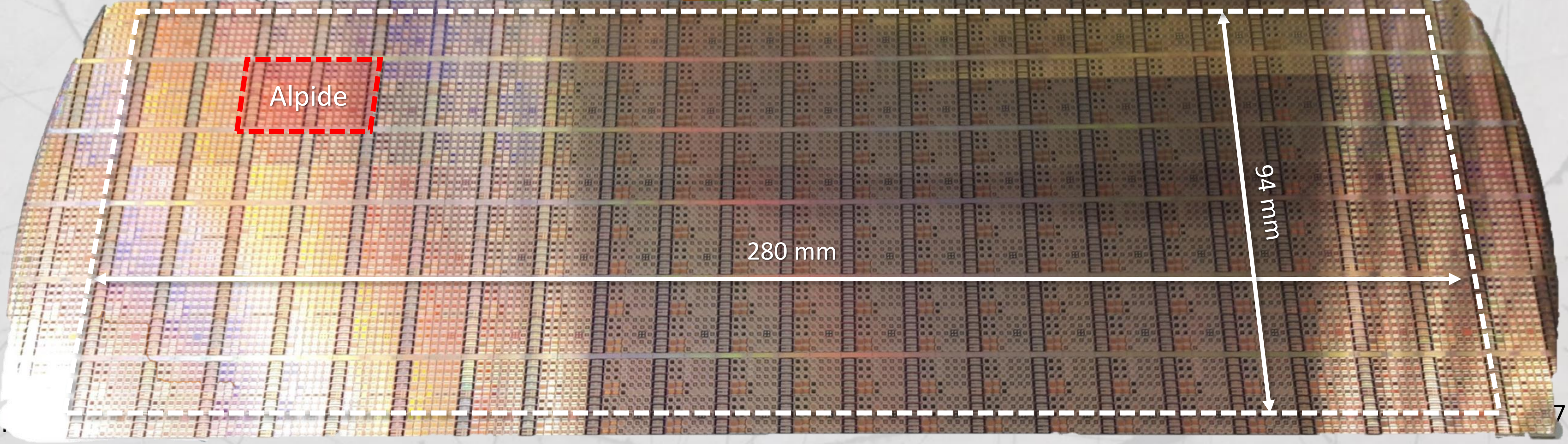


Tower Partner Semiconductor Ltd. Co.

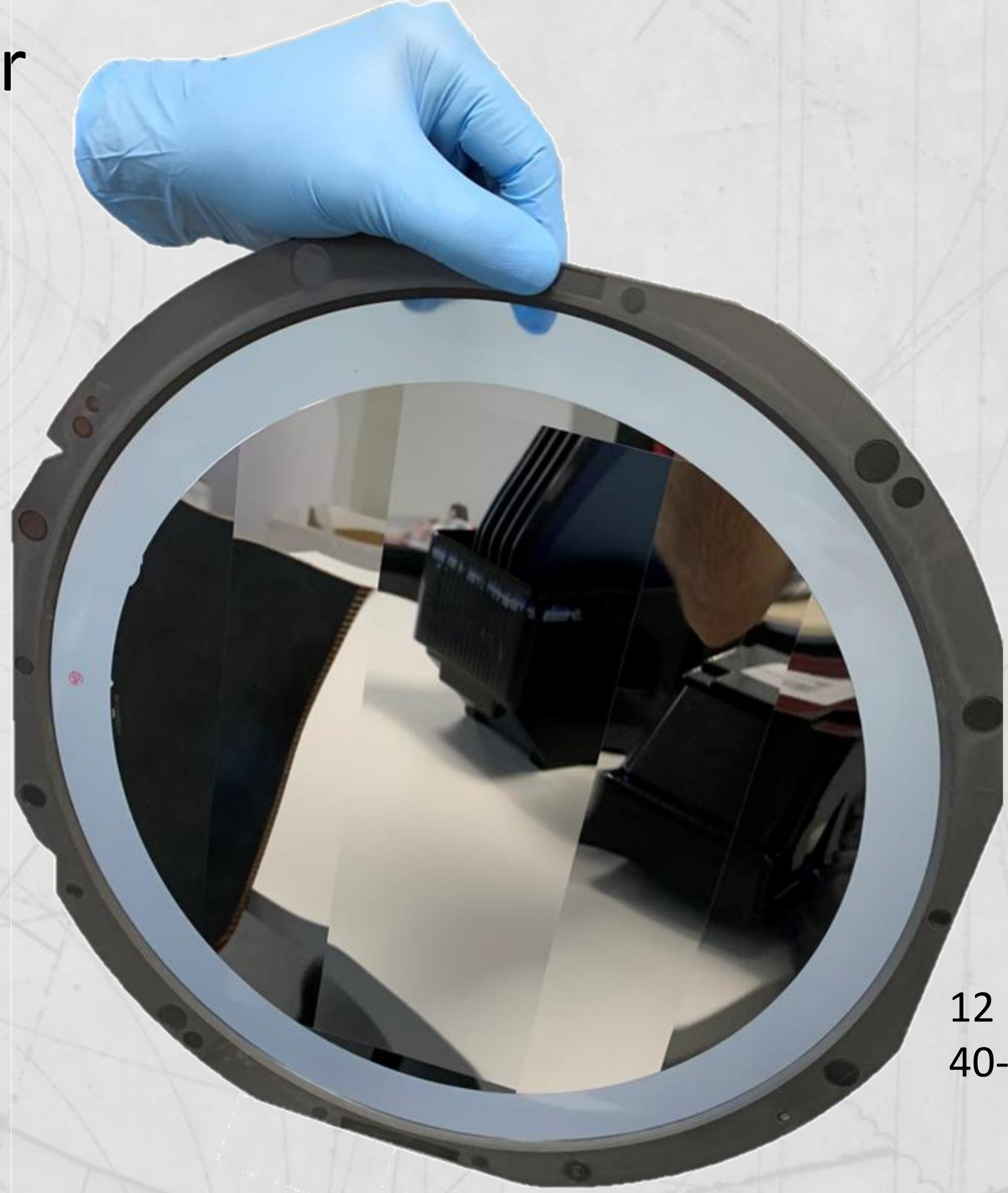
- 65 nm CMOS Imaging Sensor (CIS) process
- 300 mm wafer

Challenges

- Very large 280×94 mm² single silicon piece
- Thinned down to 30-50 µm
- **yield** is crucial: ways of dealing with imperfections need to be built in.



Wafer scale sensor



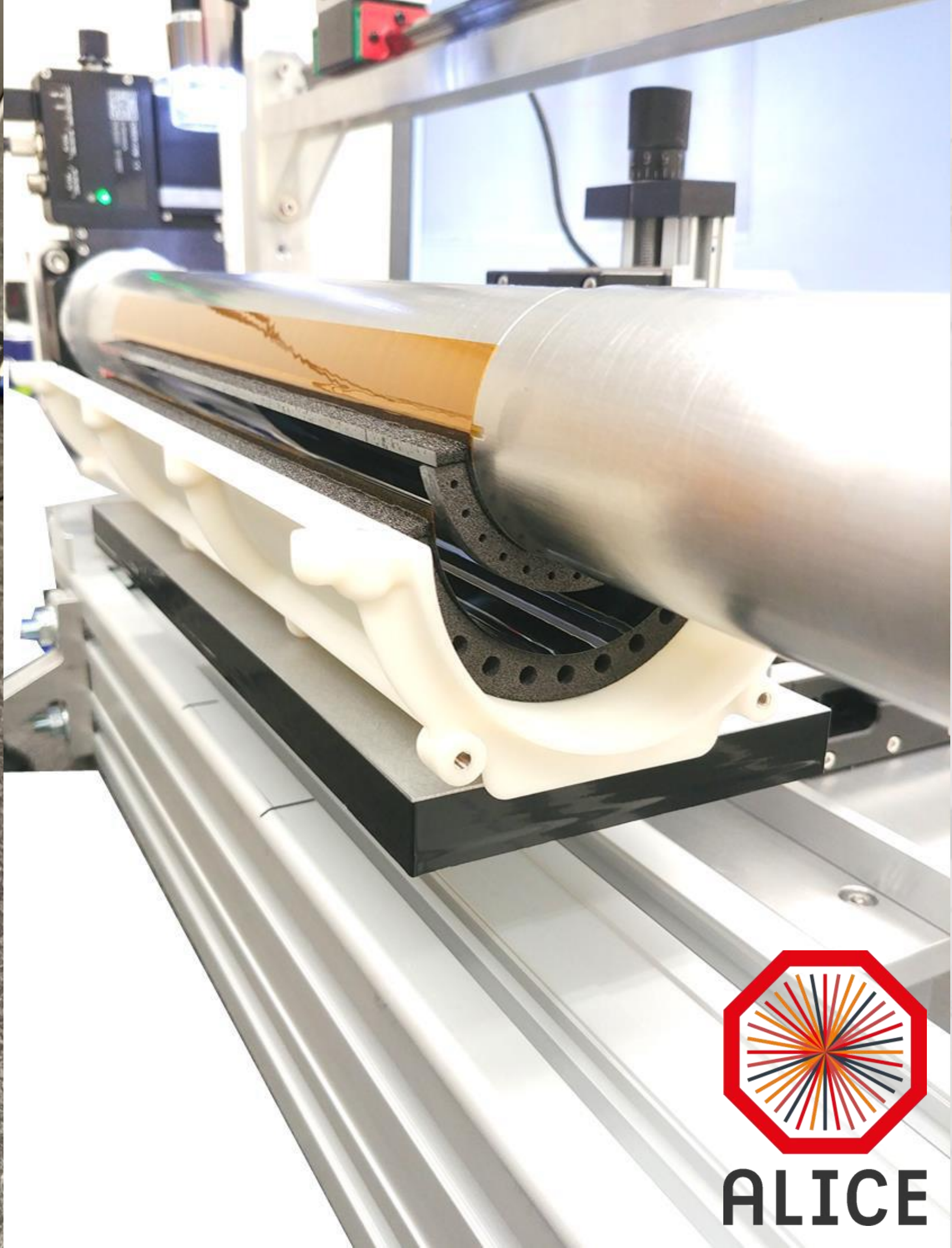
12 inches blank silicon wafer
40-50 micron thick

3-layer vertex prototypes

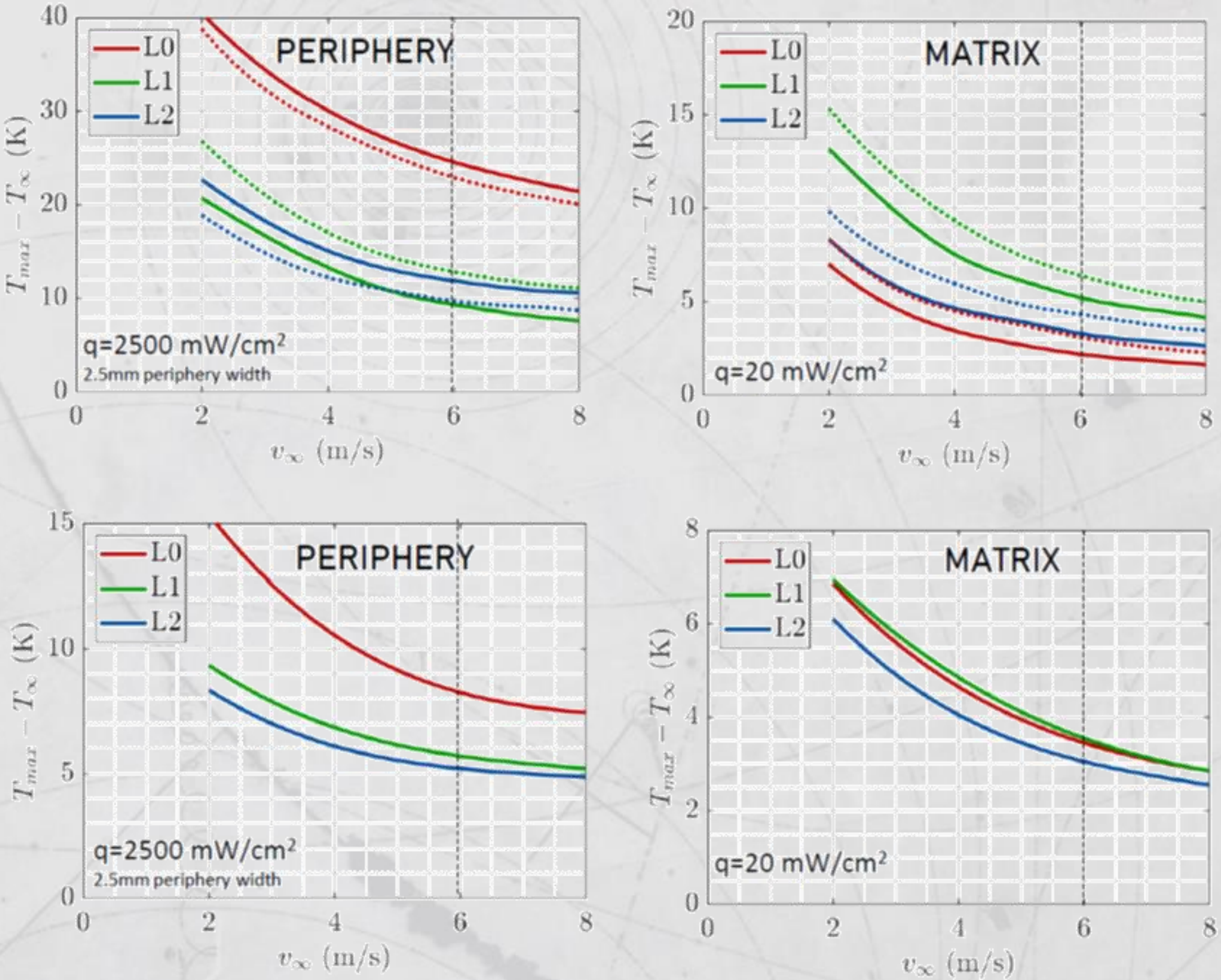
Old prototype

New improved version

ITS3 silicon bending

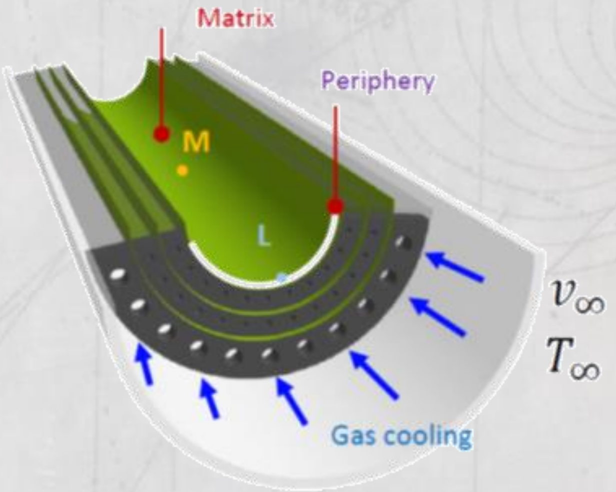


Cooling is critical



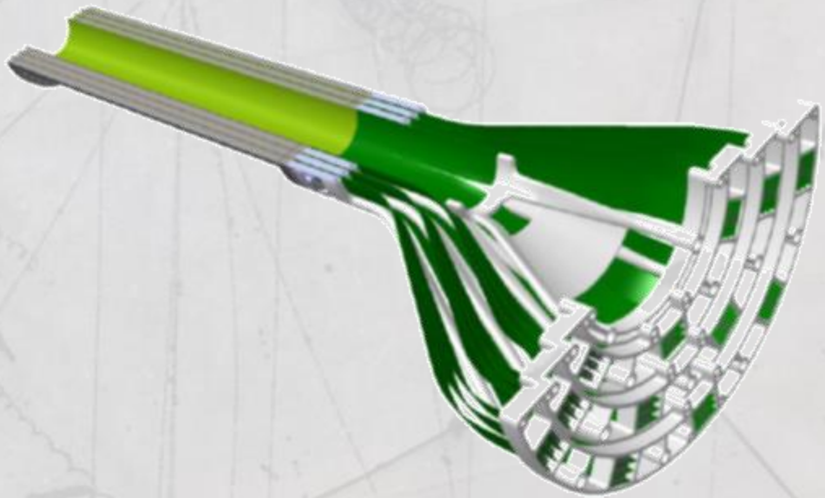
Maximum temperature variation in the Si layers. Experiments (continuous lines) and numerical simulations (dashed lines)

BBM2

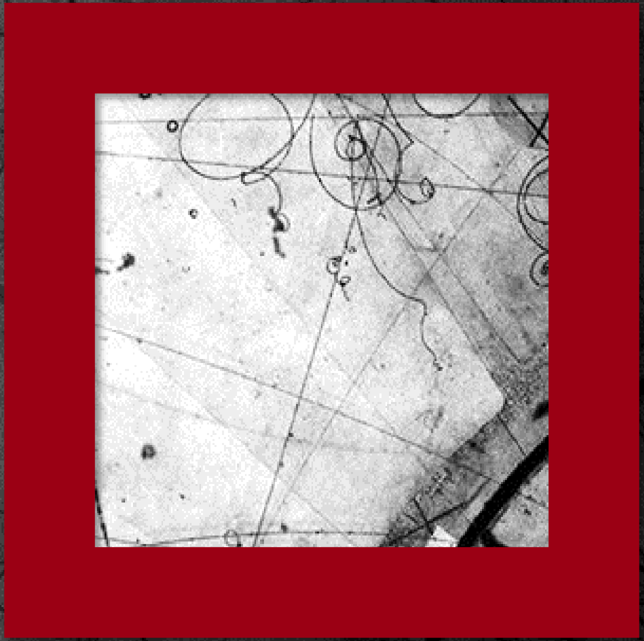


Updated air distribution

EM3

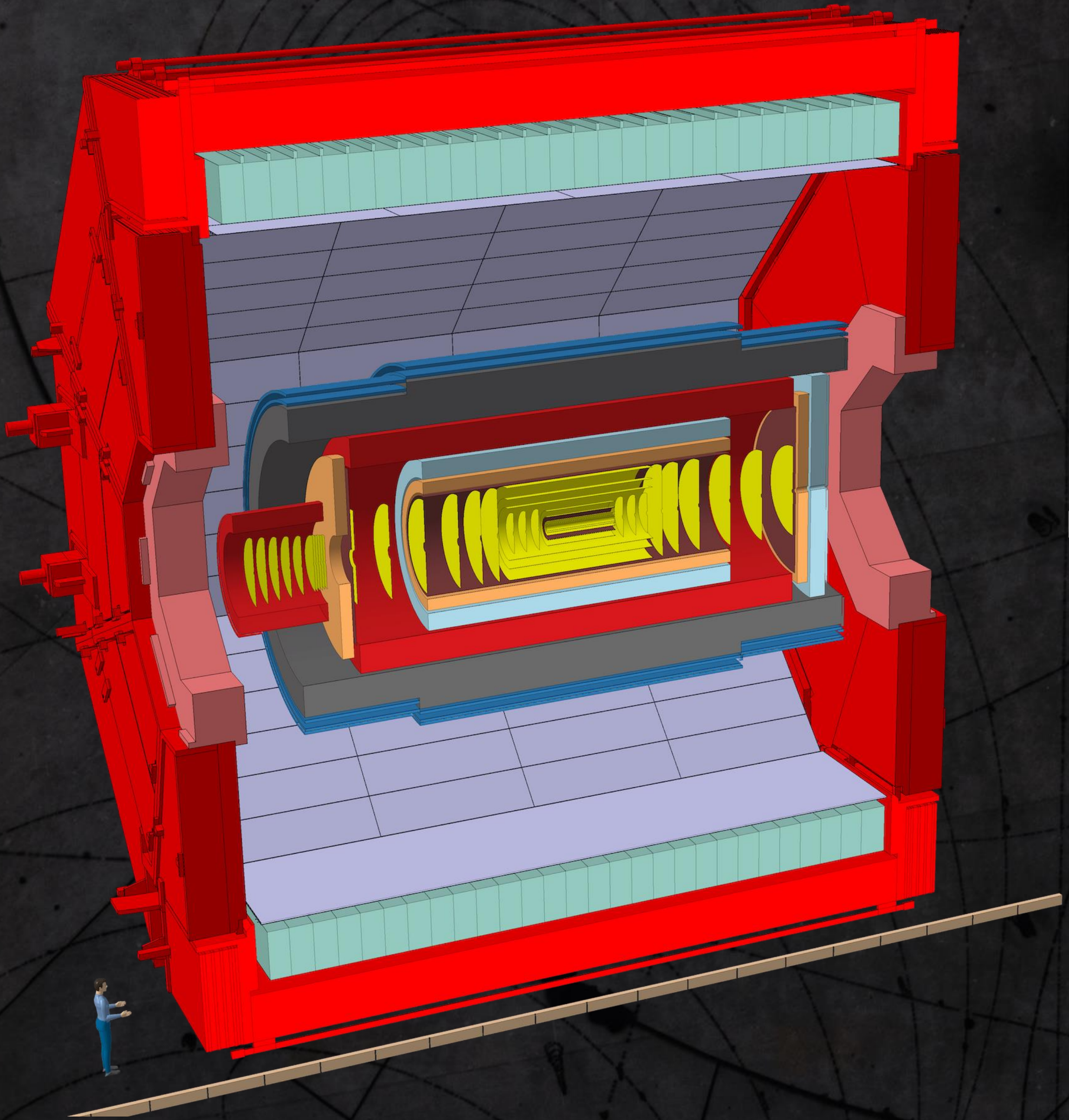


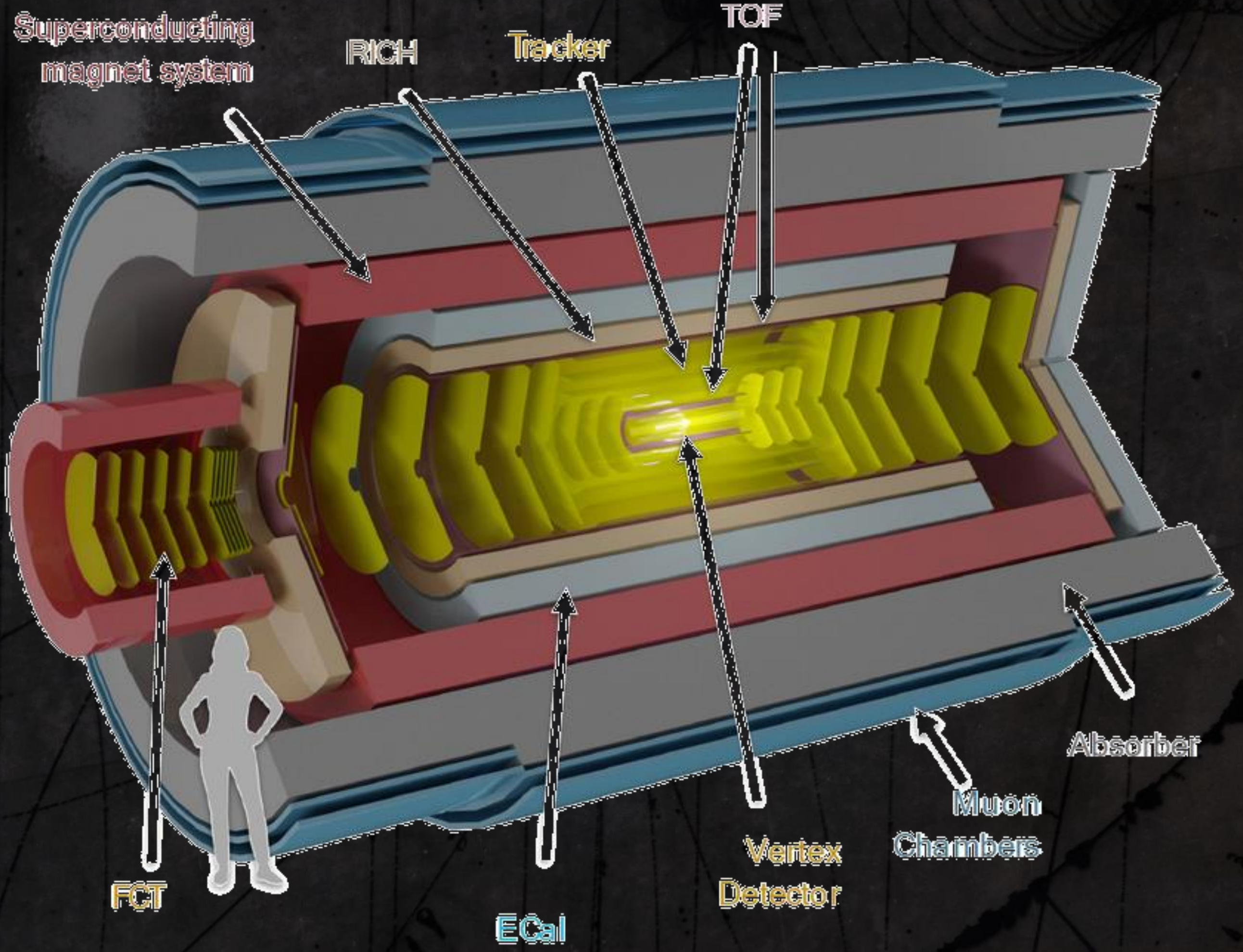
Possible improvement of L0 periphery under study



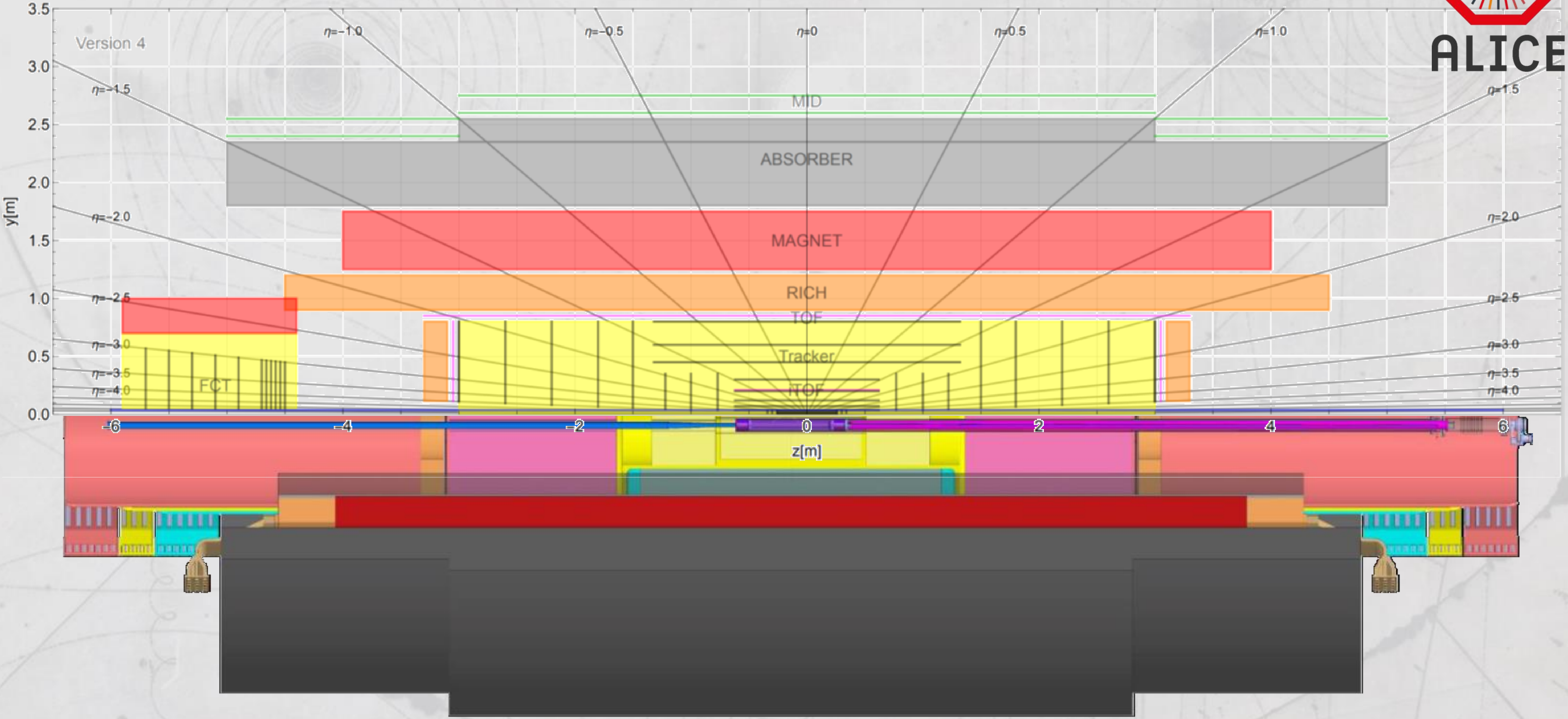
Trackers – ALICE3

From current ALICE to a VERY compact detector

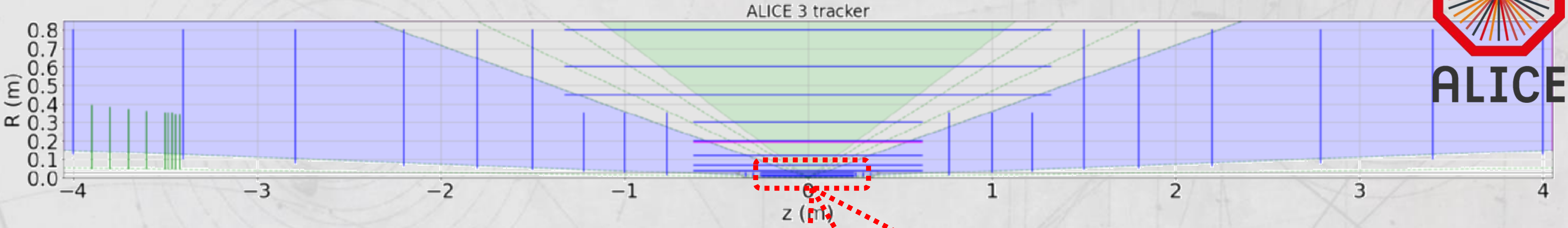




ALICE3 cutout (one of the several variants)



A large area tracker



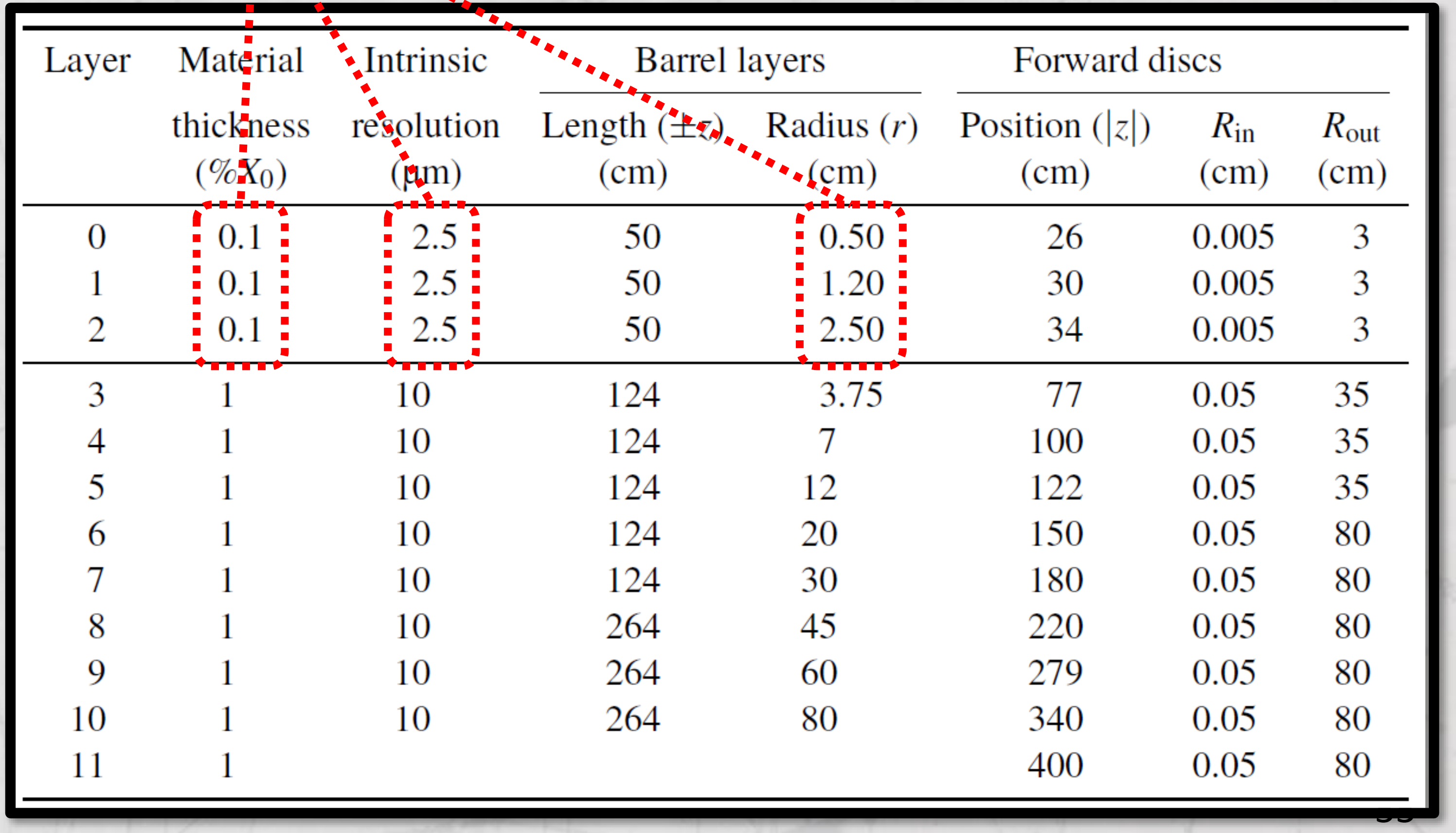
10 barrels, 11 discs

inner-most part within beam pipe

- large active area: ~60 m^2
- low material budget: 0.1% X0

for the inner layers – less than ITS2, while being larger

- high spatial resolution: 2.5 µm



Layer	Material thickness ($\%X_0$)	Intrinsic resolution (µm)	Barrel layers		Forward discs		
			Length ($\pm z$) (cm)	Radius (r) (cm)	Position ($\|z\|$) (cm)	R_{in} (cm)	R_{out} (cm)
0	0.1	2.5	50	0.50	26	0.005	3
1	0.1	2.5	50	1.20	30	0.005	3
2	0.1	2.5	50	2.50	34	0.005	3
3	1	10	124	3.75	77	0.05	35
4	1	10	124	7	100	0.05	35
5	1	10	124	12	122	0.05	35
6	1	10	124	20	150	0.05	80
7	1	10	124	30	180	0.05	80
8	1	10	264	45	220	0.05	80
9	1	10	264	60	279	0.05	80
10	1	10	264	80	340	0.05	80
11	1				400	0.05	80

Improving ITS3 5 µm vertex point resolution to 2.5 µm or better…

Pointing resolution (multiple scattering regime)

$$\sigma_p \propto r_0 \sqrt{\frac{x}{X_0}}$$

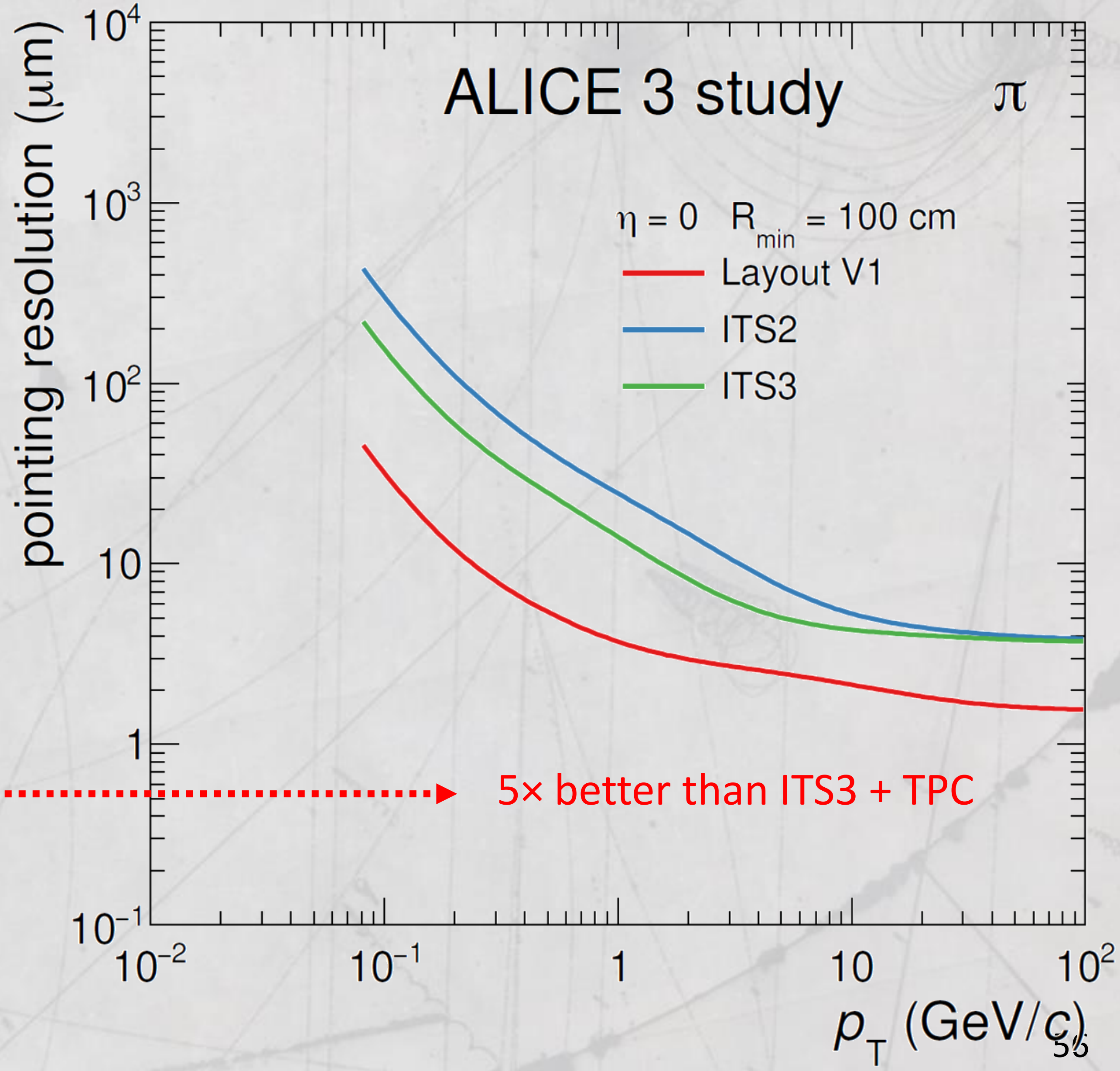
Impossible to improve upon ITS3 here

Necessary to get closer to the beam

to get to 10 µm @ pT = 200 MeV/*c* radius and material of first layer become crucial.

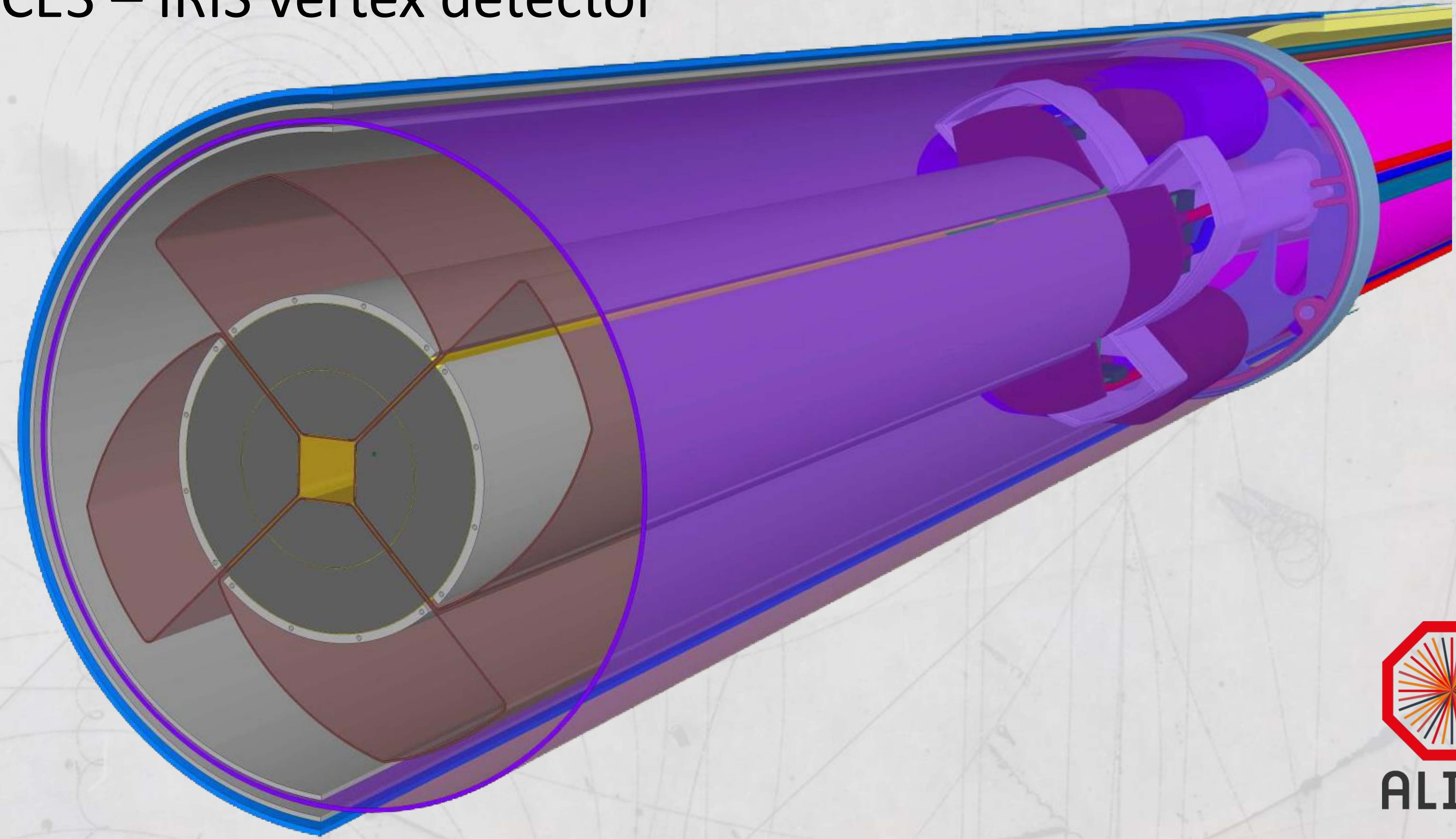
Minimal radius given by required aperture

- R ≈ 5 mm at top energy
- R ≈ 15 mm at injection energy



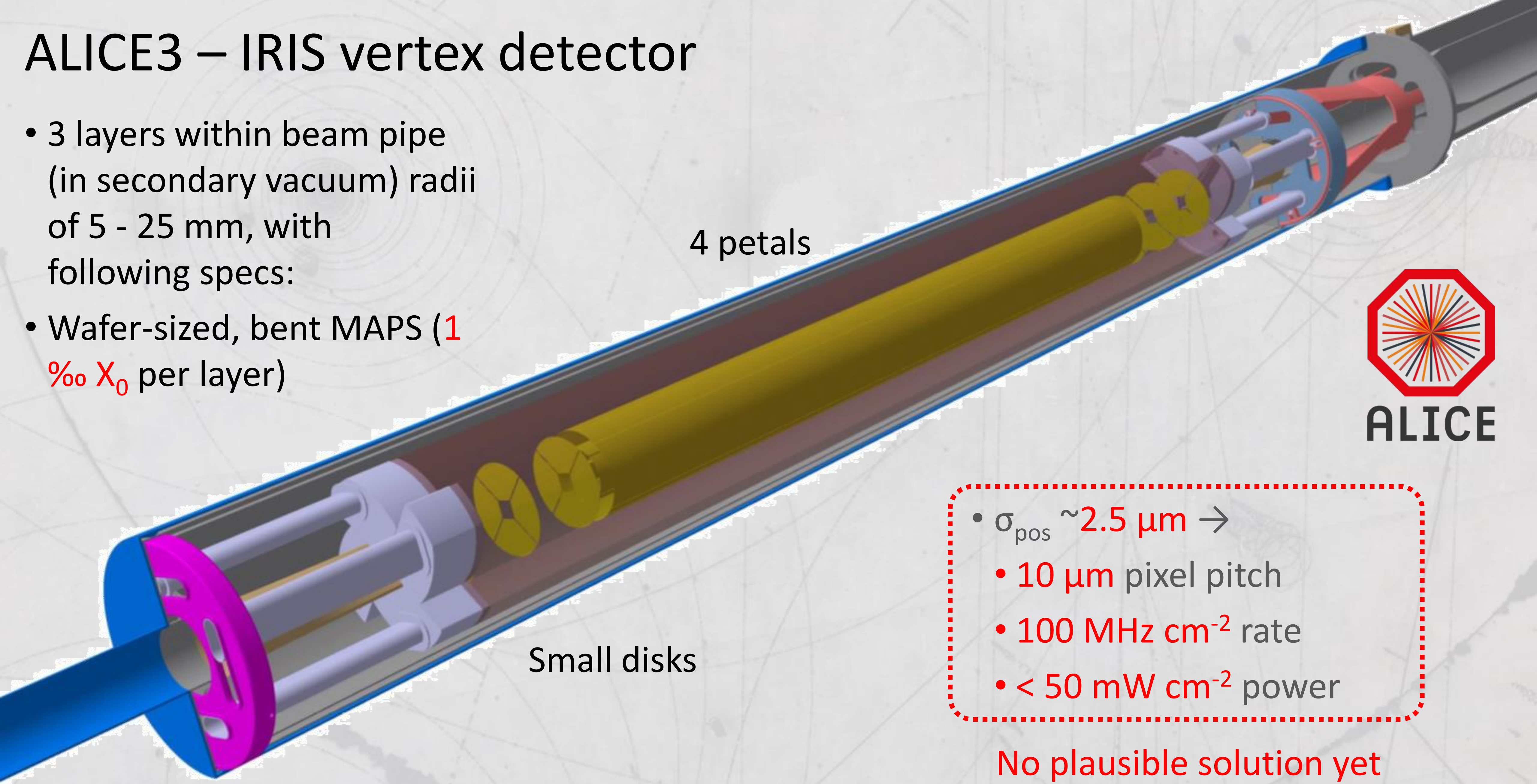
5× better than ITS3 + TPC

ALICE3 – IRIS vertex detector



ALICE3 – IRIS vertex detector

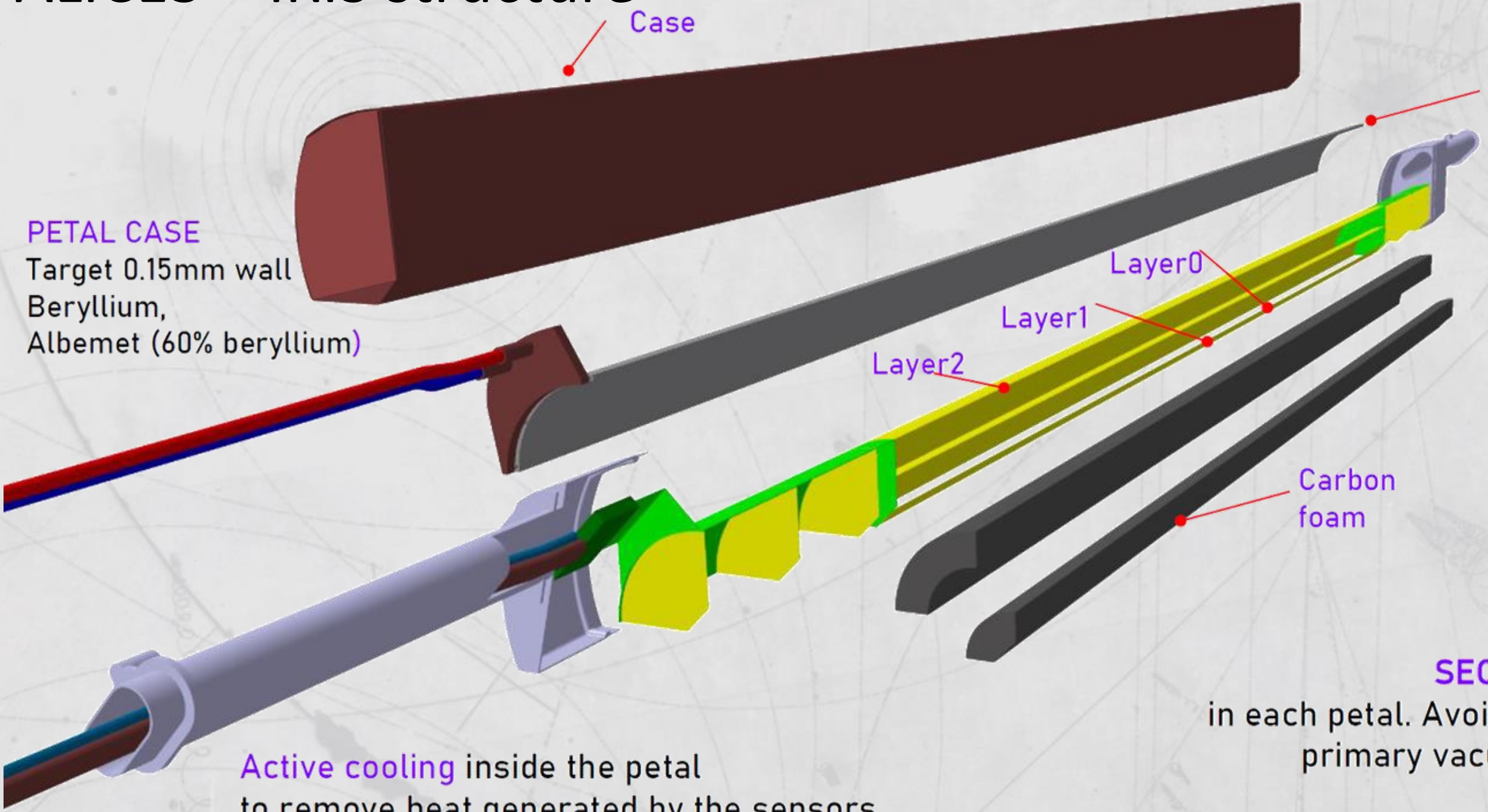
- 3 layers within beam pipe (in secondary vacuum) radii of 5 - 25 mm, with following specs:
- Wafer-sized, bent MAPS (1 ‰ X_0 per layer)



- σ_{pos} ~2.5 µm →
  - 10 µm pixel pitch
  - 100 MHz cm^{-2} rate
  - < 50 mW cm^{-2} power

No plausible solution yet

ALICE3 – IRIS structure

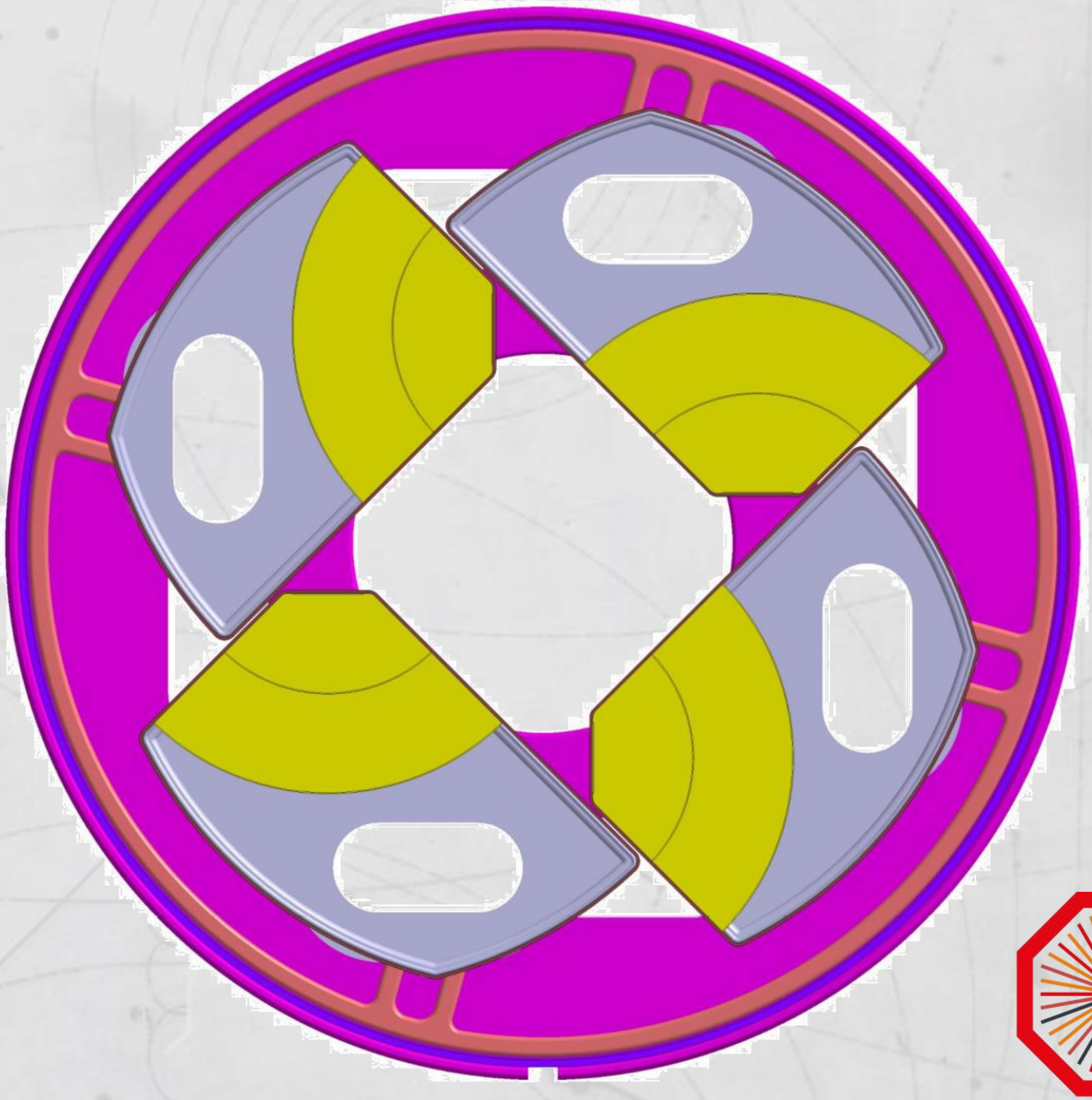


PETAL CASE
Target 0.15mm wall
Beryllium,
Albemet (60% beryllium)

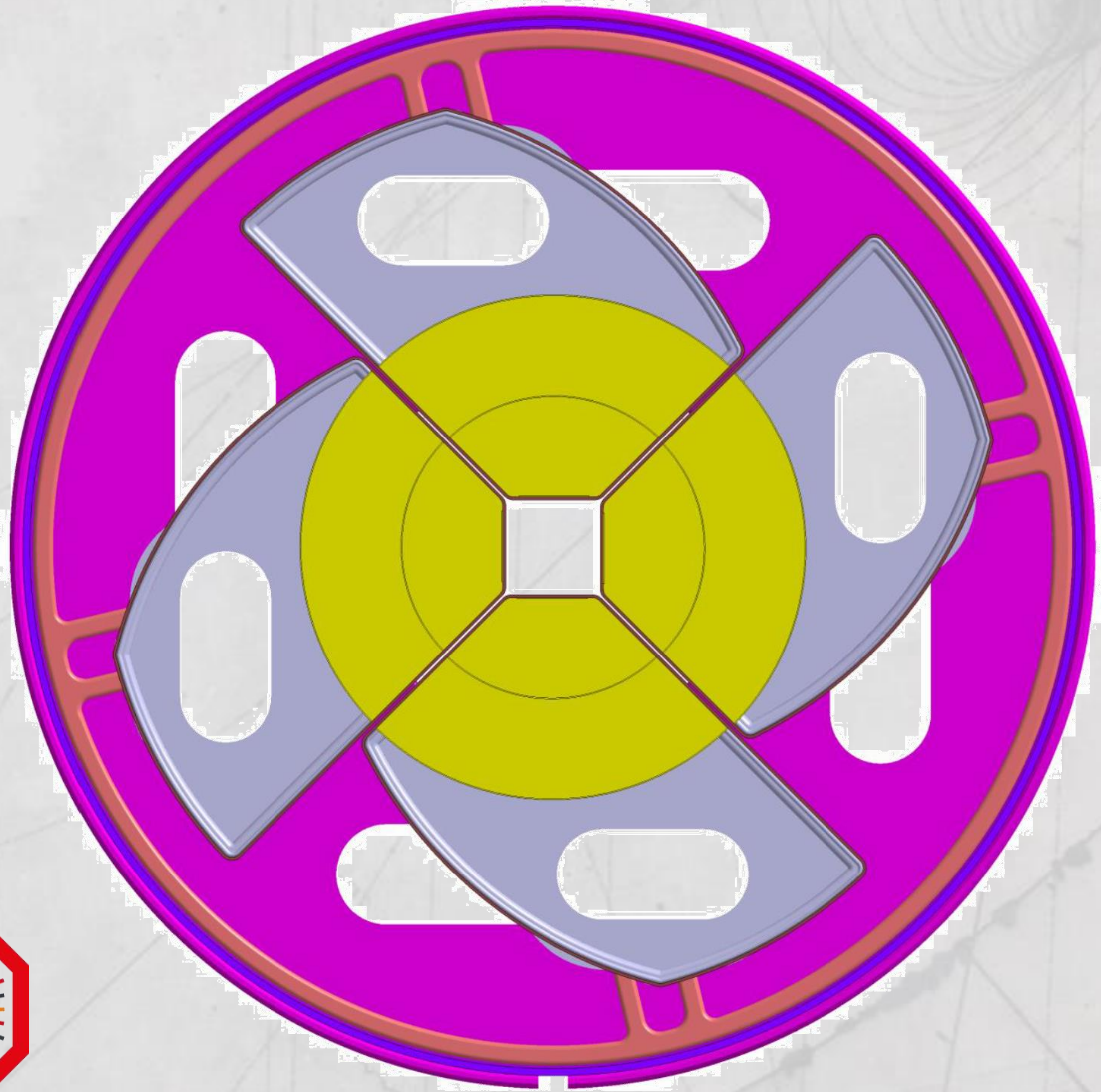
SECONDARY VACUUM
in each petal. Avoid contamination of
primary vacuum from detector
outgassing

Active cooling inside the petal
to remove heat generated by the sensors.
A coldplate is in thermal contact through
Carbon paper/ foam to the sensors

At injection



Data taking



Requires a radical design of the first 3 layers

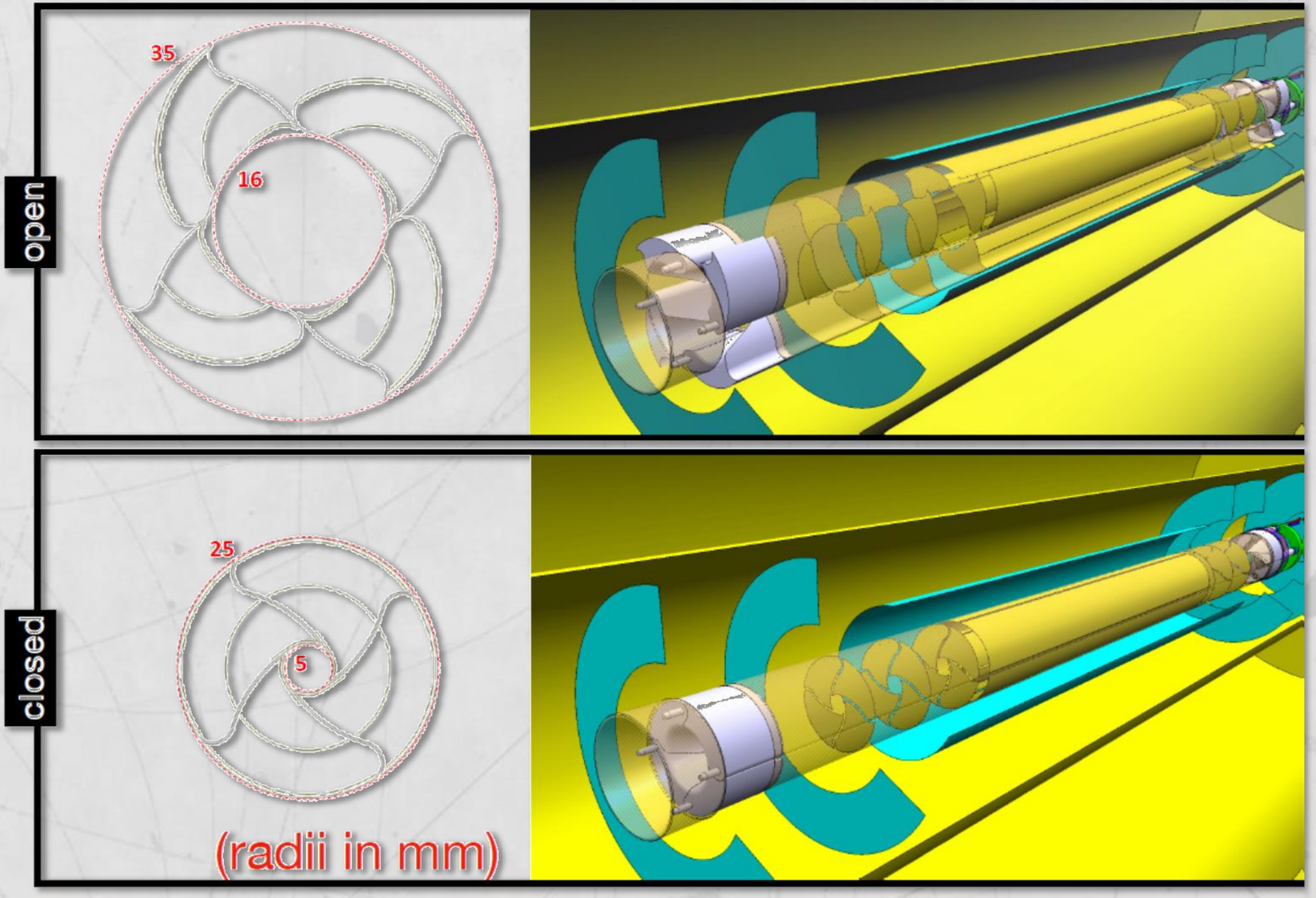
- 3 layers within beam pipe (in secondary vacuum) radii of 5 - 25 mm, with following specs:

- wafer-sized, bent MAPS
- 1 ‰ X_0 per layer

ITS3 tech

- σ_{pos} ~2.5 µm →
  - 10 µm pixel pitch
  - 100 MHz cm^{-2} rate
  - < 50 mW cm^{-2} power

No answer



Foreseen operational figures*

Layer	Radii	Area	Flux		Bandwidth [Gb s^{-1}]				Power		Radiation	
	Cm		[MHz cm^{-2}]	[GHz lyr^{-1}]	Hits	Noise	Total	[Tb m^{-2} s^{-2}]	[W]	[W/m^2]	NIEL [1 Mev n$_{eq}$cm^{-2}]	TID [Mrad]
0	0.5	0.016	96	17	274	1.0	275	17.2	13	812	9×10^{15}	288
1	1.2	0.038	16	7.3	117	2.4	119	3.13	32	840	1.6×10^{15}	50
2	2.5	0.075	3.8	3.6	57	5.0	62	0.82	66	880	3.6×10^{14}	12
3	3.8	0.29	1,7	1.8	28	0.7	79	0.6	175	603	1.6×10^{14}	5
4	7	0.55	0.48	1.2	18	1.4	43	0.27	131	238	4.6×10^{13}	1.5
5	12	0.94	0.16	0.8	13	2.4	27	0.07	224	238	1.6×10^{13}	0.5
6	20	1.6	0.058	0.6	9.9	4.0	19	0.011	374	233	5.6×10^{12}	0.2
7	30	2.3	0.026	0.5	7.9	6.0	16	0.006	561	243	2.5×10^{12}	0.08
8	45	7.5	0.012	0.6	9.6	19.1	33	0.004	1792	238	1.1×10^{12}	0.04
9	60	10.0	6.5×10^{-3}	0.5	8.2	25.5	36	0.003	2389	238	6.3×10^{11}	0.02
10	80	13.0	3.7×10^{-3}	0.4	6.8	34.0	42	0.003	3185	245	3.5×10^{11}	0.01

*
- bandwidth: 16 bit/hit, single pixel clusters
- radiation load: 50 months of 24 MHz pp interactions
- Fake-hit rate: 10^{-8} px^{-1} event^{-1} @ 40 MHz readout rate

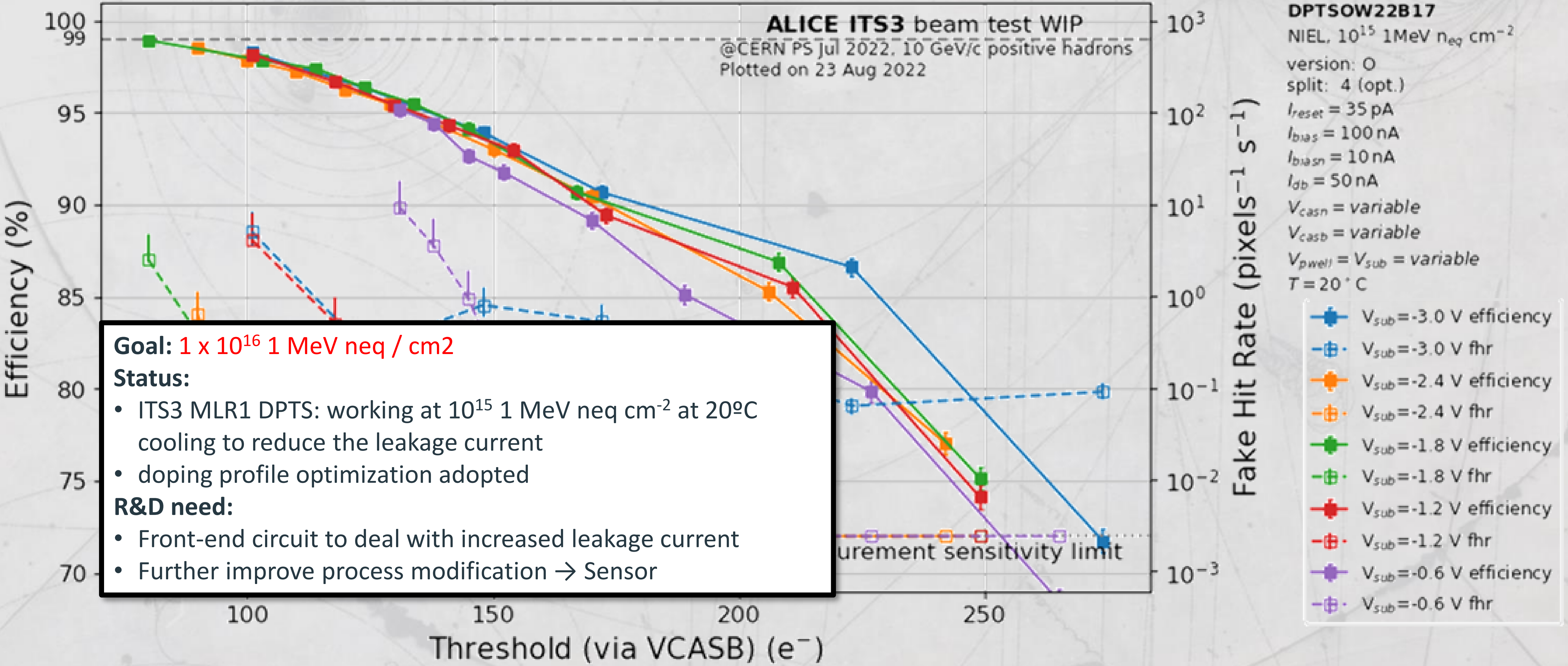
Foreseen operational figures*

Item	Unit	Next ITS		ITS3	ITS2
	Cm	Vertex	Tracker		
Pixel pitch [µm]	[µm]	9 ÷ O(10×10)	28 ÷ O(50×50)	O(20×20)	28
Spatial resolution [µm]	[µm]	2 ÷ 2.5	2 ÷ 10	5	5
Time resolution [ns]	[ns]	10 ÷ 100	10 ÷ 100	100 ÷ O(1000)	O(1000)
Shaping time [ns]	[ns]	25 ÷ 200	25 ÷ 200	200 ÷ O(5000)	O(5000)
Fake hit rate	[px^{-1} event^{-1}]	< 10^{-8}	< 10^{-8}	< 10^{-7}	<< 10^{-6}
Power consumption	[mW cm^{-2}]	70 (+75%)	20	20 (matrix)	30 ÷ 40
Hit flux	[MHz cm^{-2}]	20 ÷ 94		8.5	5
NIEL	[1 MeV n_{eq} cm^{-2}]	1×10^{16}		3×10^{12}	3×10^{12}
TID	[Mrad]	300 ÷ 1000	5	0.3	0.3

- In red: likely not achievable (no idea at the moment)
- In yellow: not strictly necessary, more a goal
- In blue: more realistic, expected goal

65 nm proven technology – 10^{15} 1 MeV n_{eq} cm^{-2} measurements

- Proven by R&D53 (ATLAS – CMS)
- Comparable results in Tower-Jazz 65 nm



Goal: 1 x 10^{16} 1 MeV neq / cm2

Status:

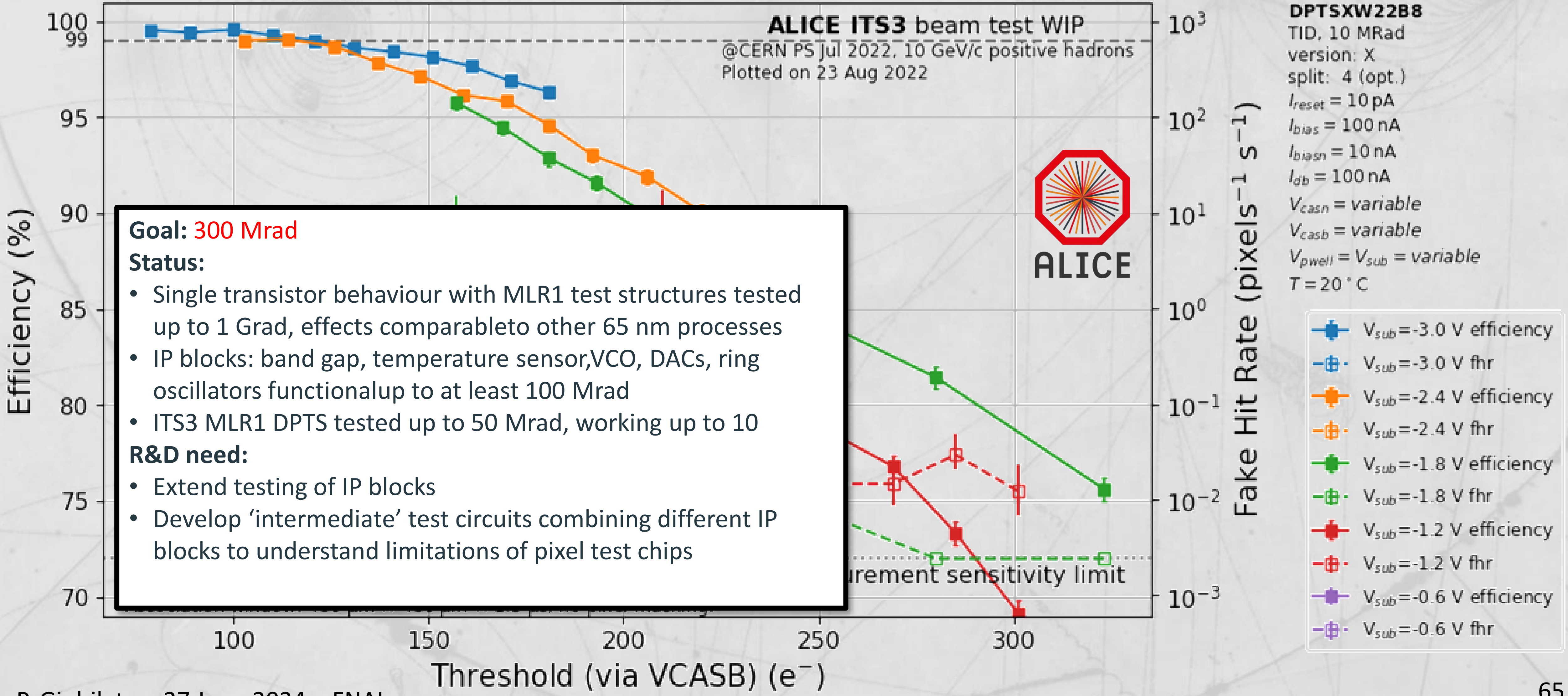
- ITS3 MLR1 DPTS: working at 10^{15} 1 MeV neq cm^{-2} at 20ºC cooling to reduce the leakage current
- doping profile optimization adopted

R&D need:

- Front-end circuit to deal with increased leakage current
- Further improve process modification → Sensor

65 nm proven technology – 10 Mrad measurements

- Proven by R&D53 (ATLAS – CMS)
- Comparable results in Tower-Jazz 65 nm



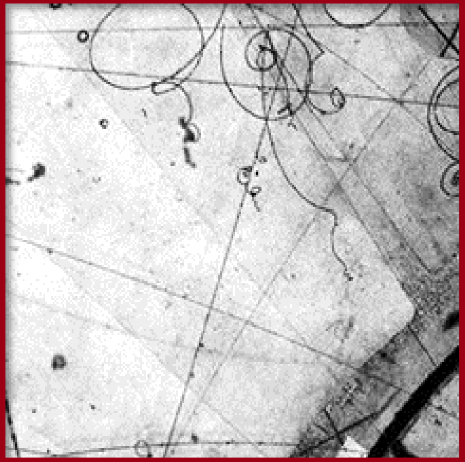
Goal: 300 Mrad

Status:

- Single transistor behaviour with MLR1 test structures tested up to 1 Grad, effects comparableto other 65 nm processes
- IP blocks: band gap, temperature sensor,VCO, DACs, ring oscillators functionalup to at least 100 Mrad
- ITS3 MLR1 DPTS tested up to 50 Mrad, working up to 10

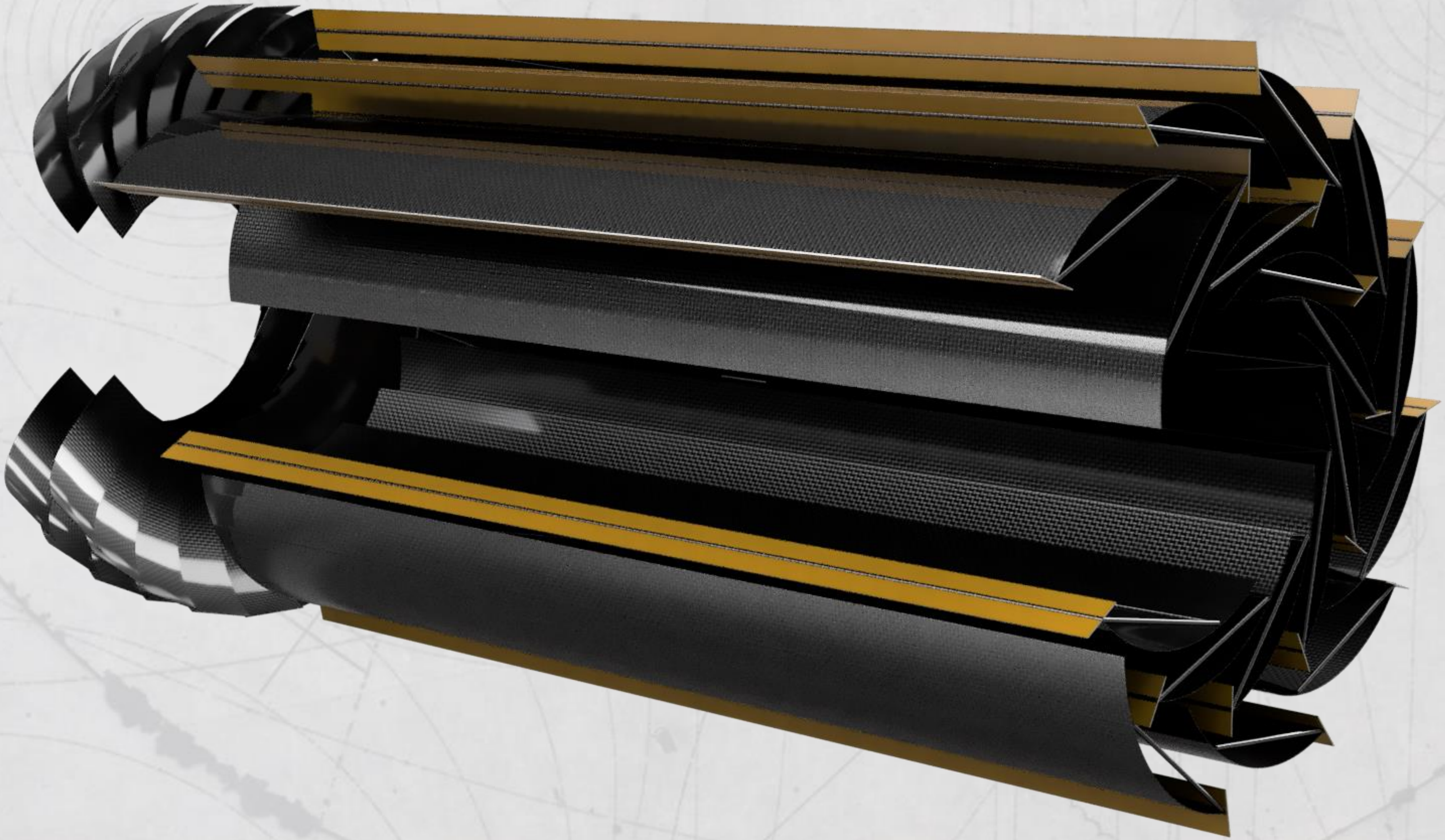
R&D need:

- Extend testing of IP blocks
- Develop 'intermediate' test circuits combining different IP blocks to understand limitations of pixel test chips

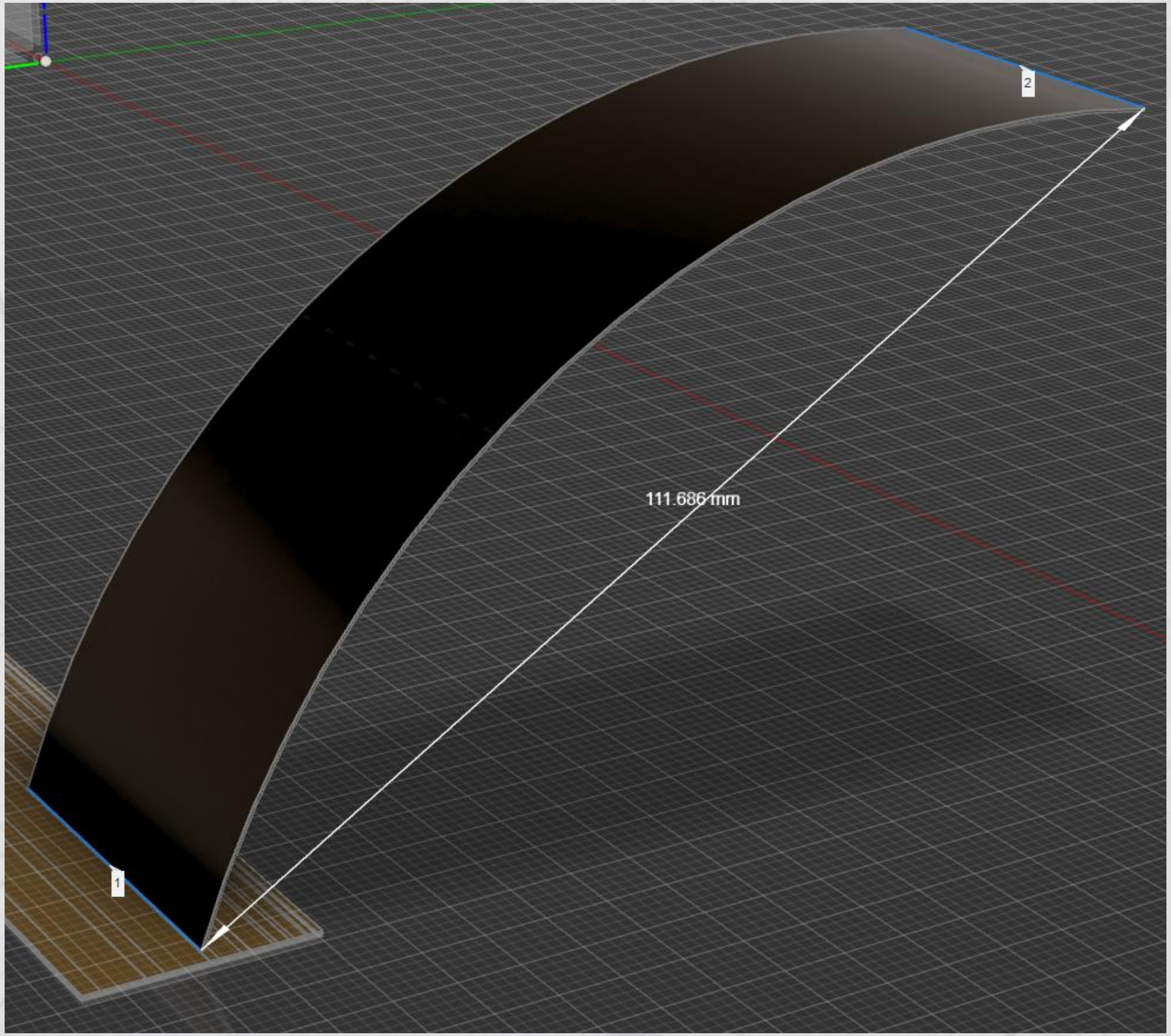


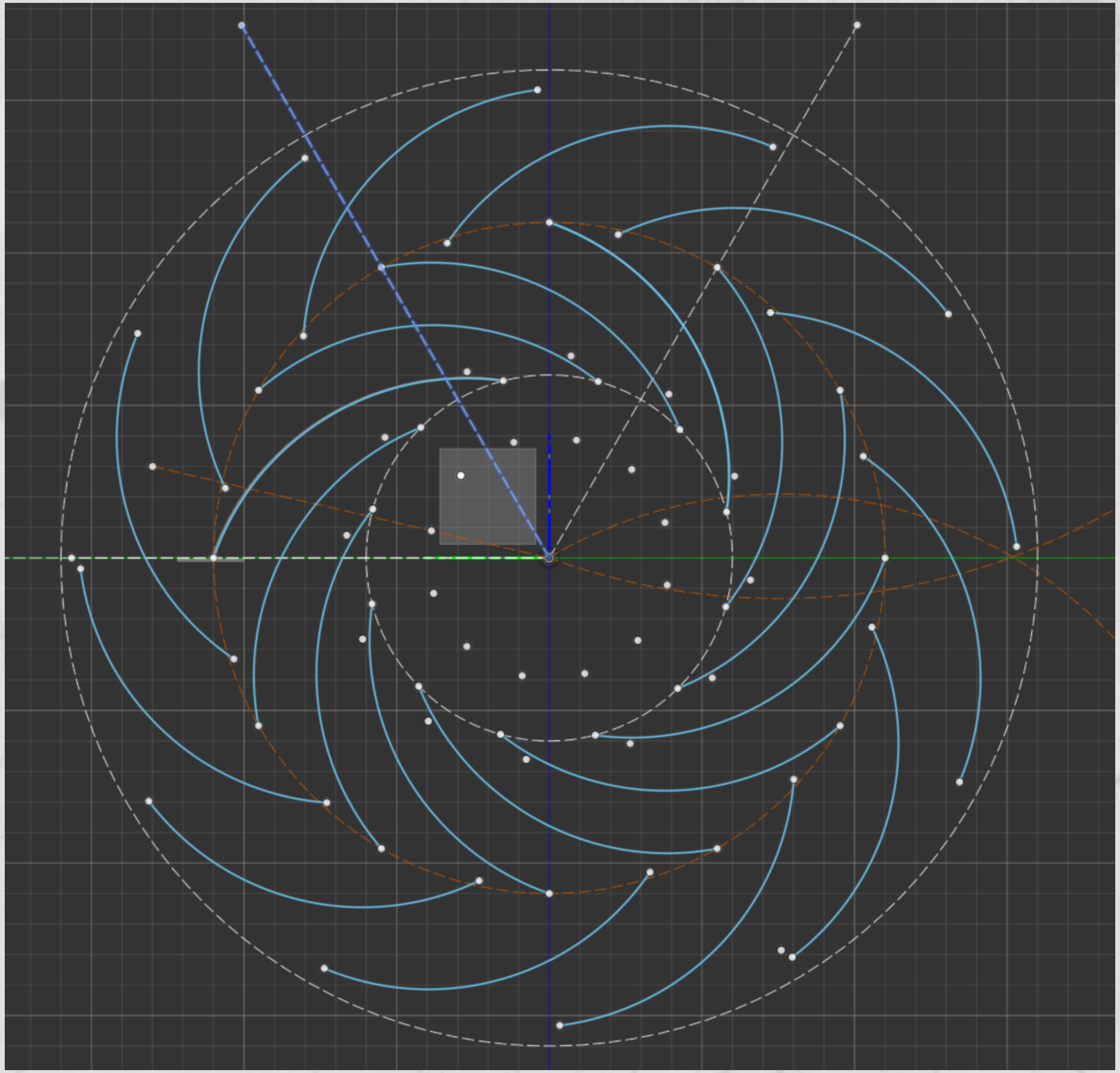
Trackers – NEXT

Ultralight middle layers concept (6 – 16 cm)

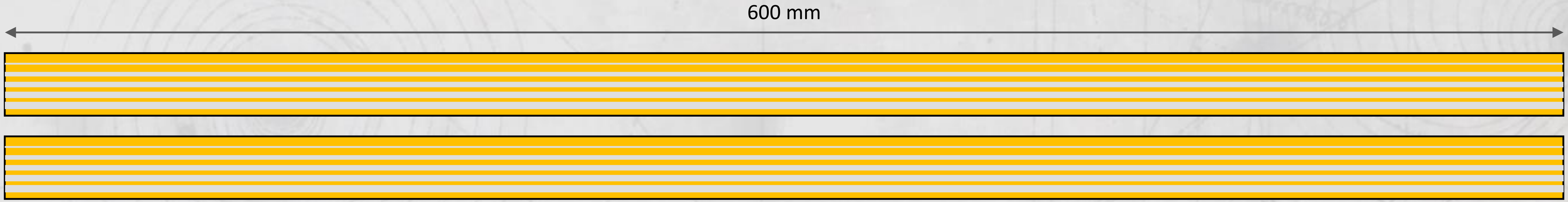


ALICE3 middle layers concept (6 – 16 cm radius)

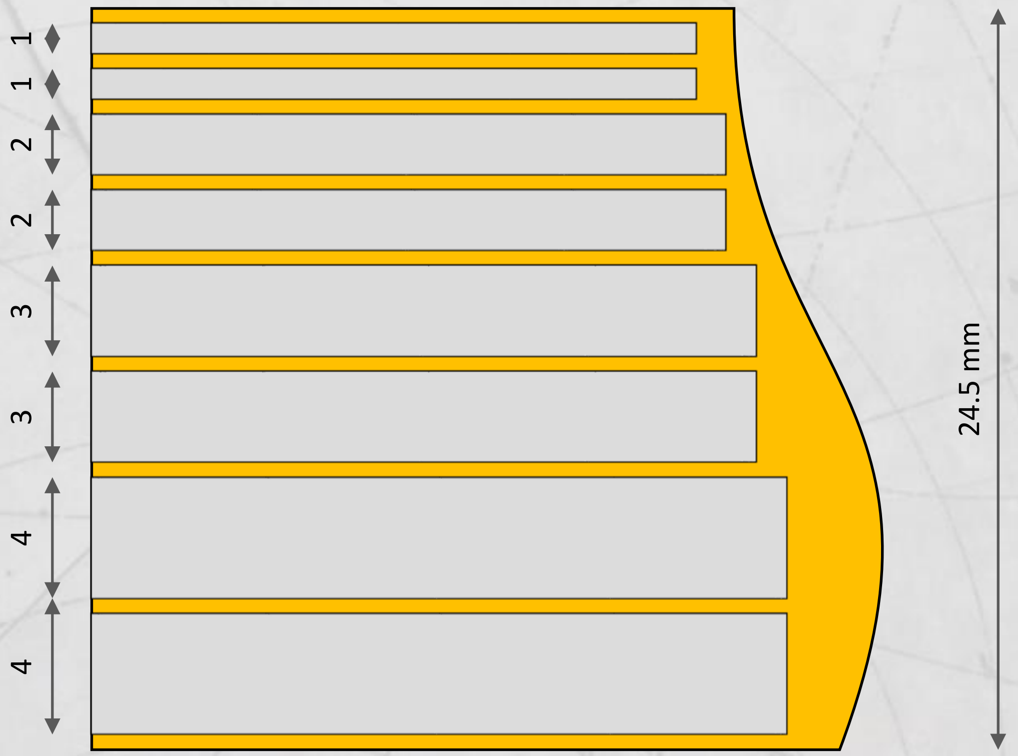




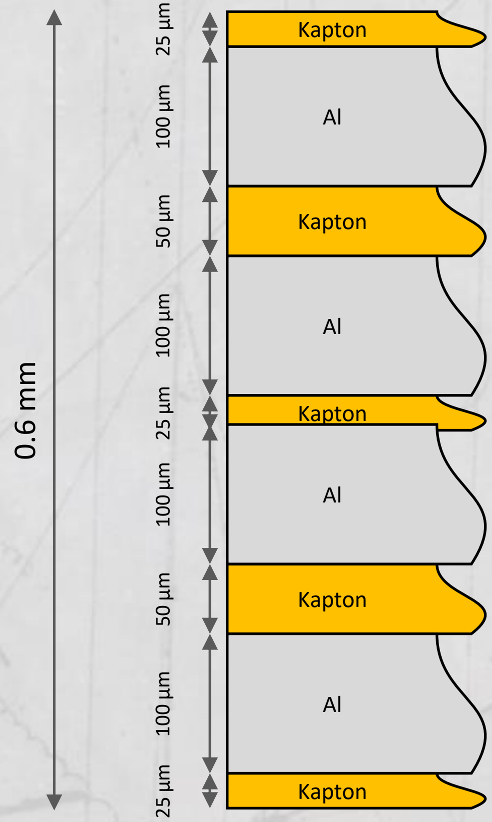
Power bus – short barrel – 2 layered buses – 10 mW cm^{-2}



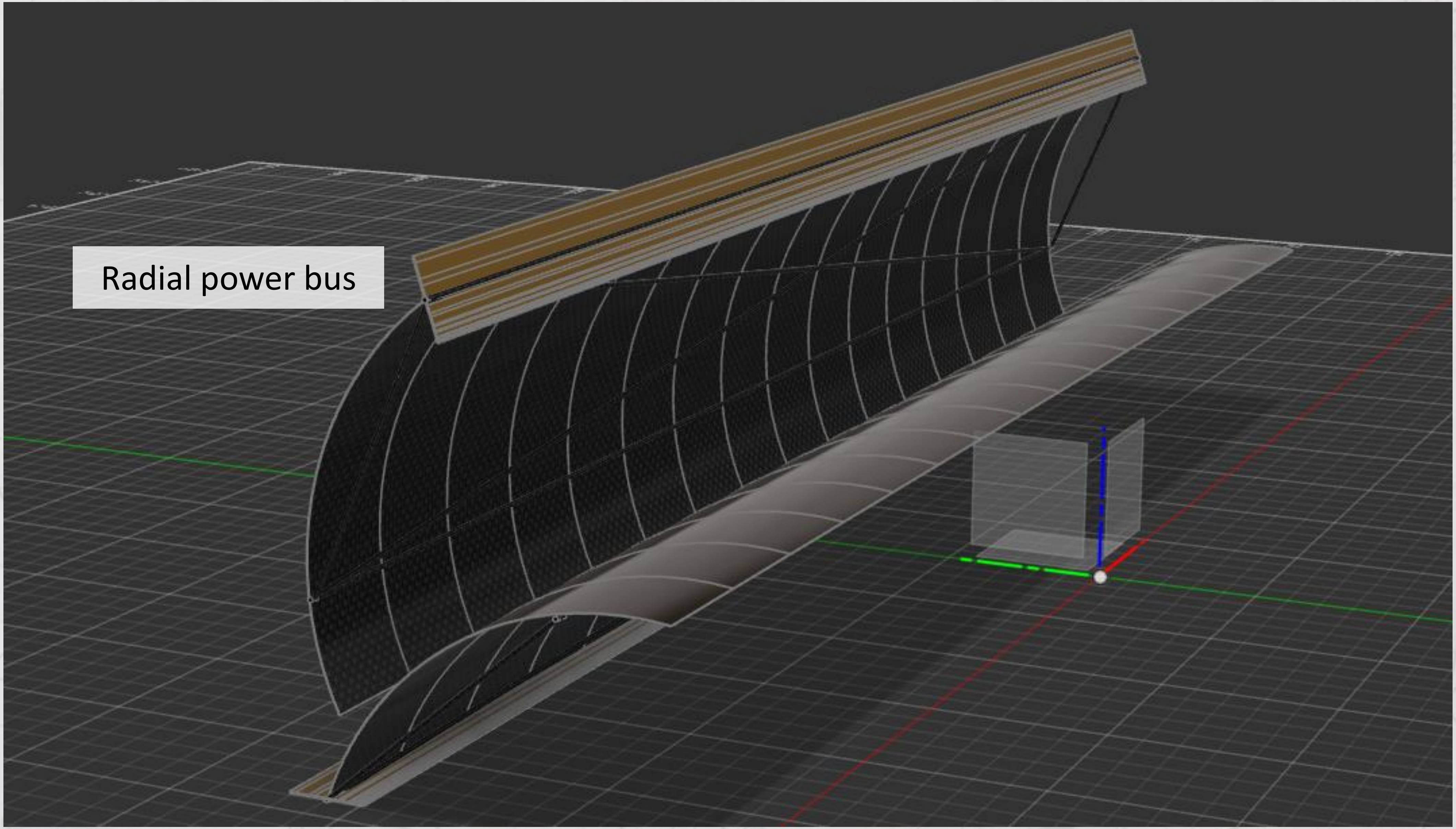
Power bus lane top view



Power bus stack up

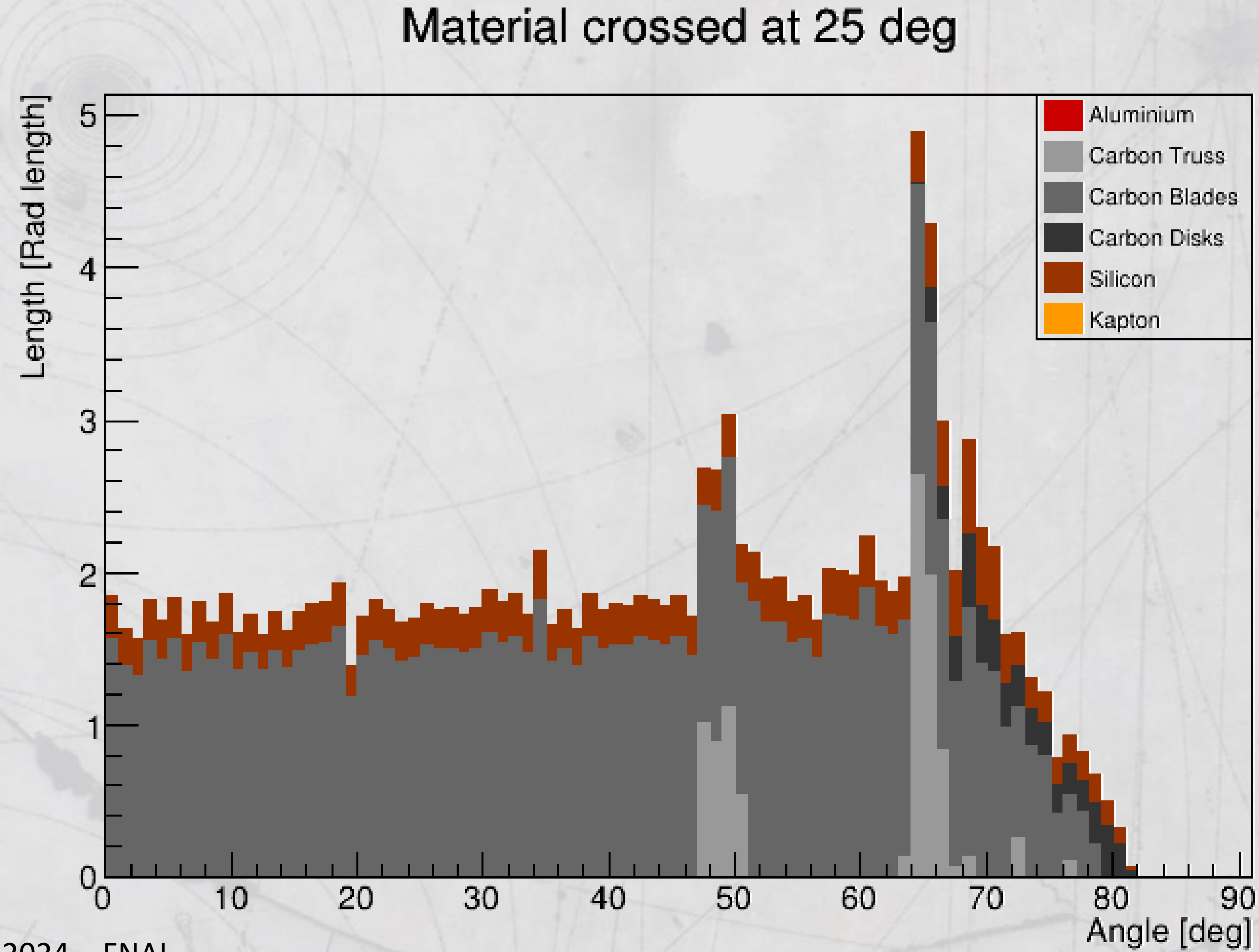


Chevron layout: 4 tracking points with 2 staves

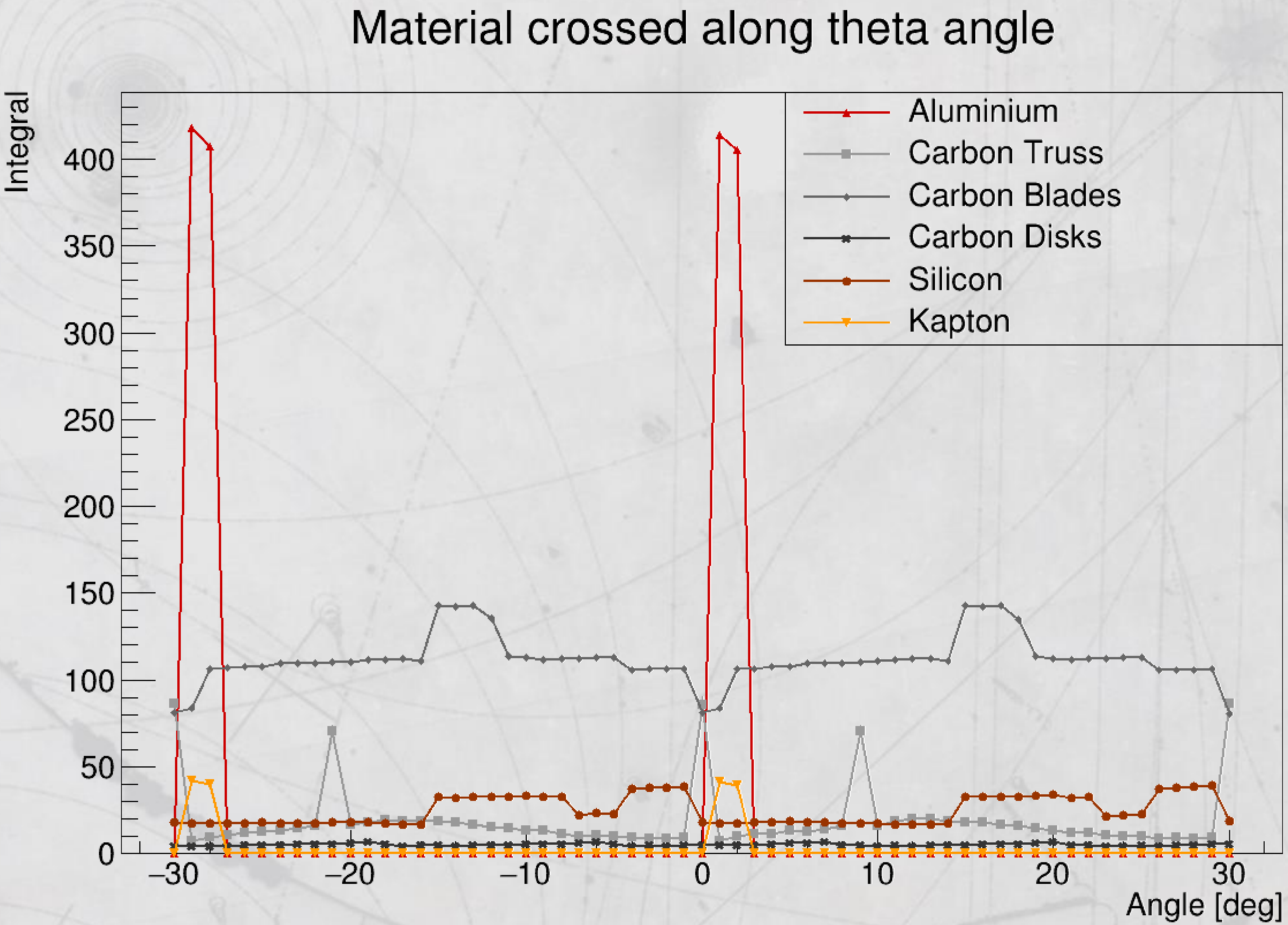


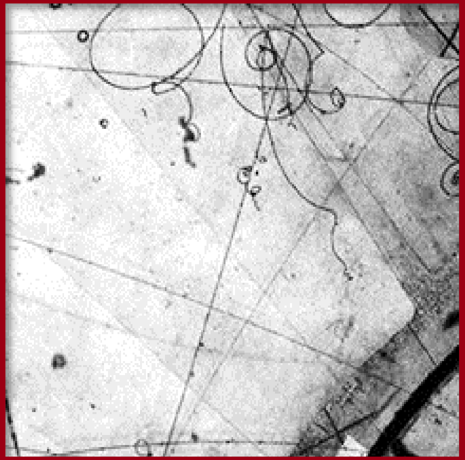
Radial power bus

Extremely reduced material budget



Spikes of clustered metal (power bus) to supply the sensors

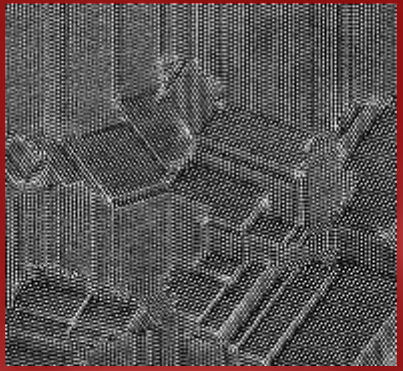




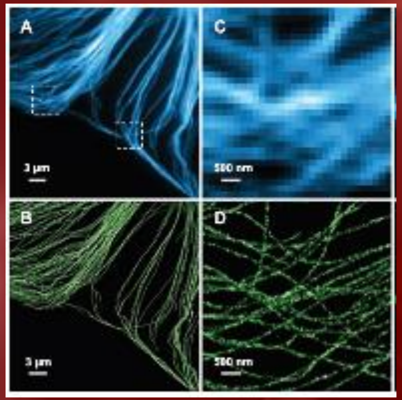
Outreach (mandatory!)

Tracking is <u>NOT</u> limited to particle physics

Nanometer (e^-)

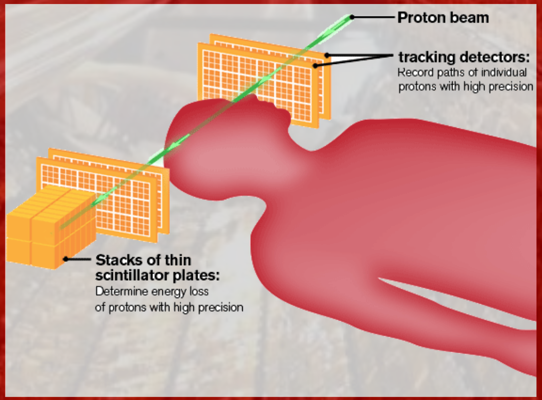


Micron (γ)



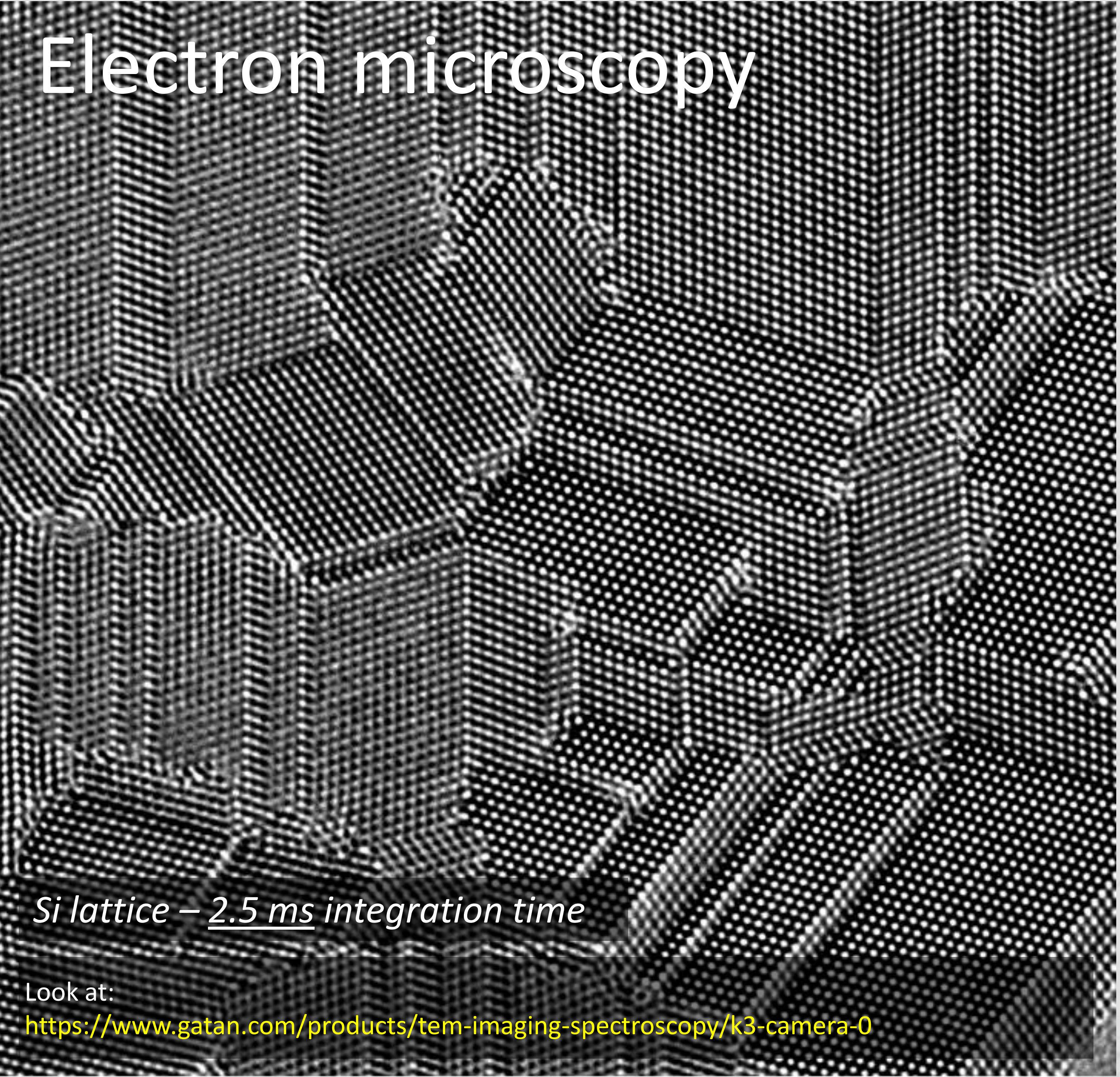
Millimetes (χ)

Meter (p)



and beyond

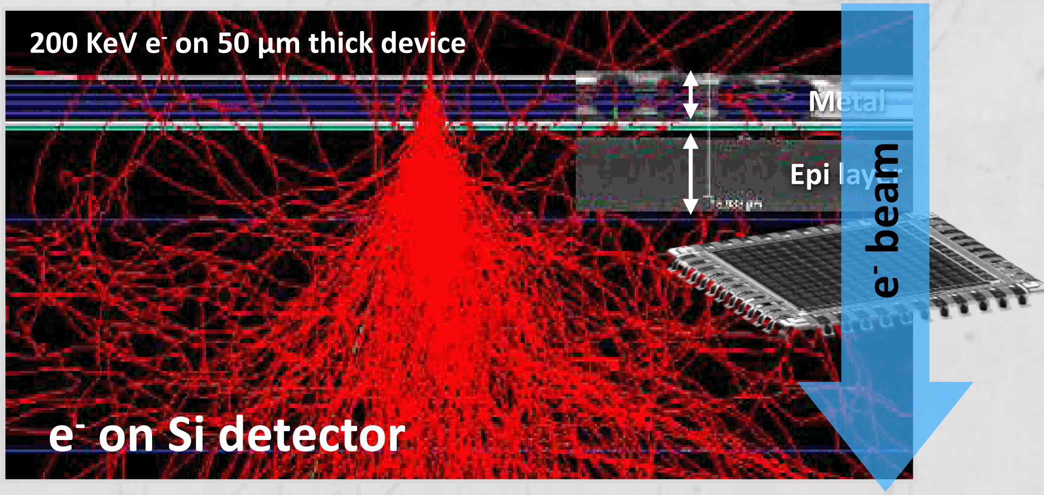
Electron microscopy



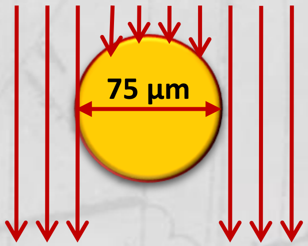
Si lattice – 2.5 ms integration time

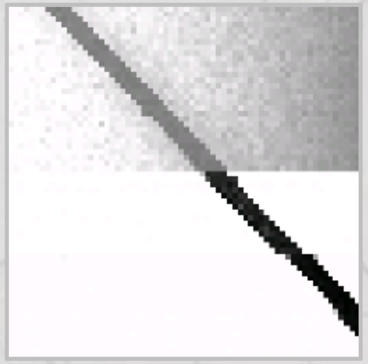
Look at:
https://www.gatan.com/products/tem-imaging-spectroscopy/k3-camera-0

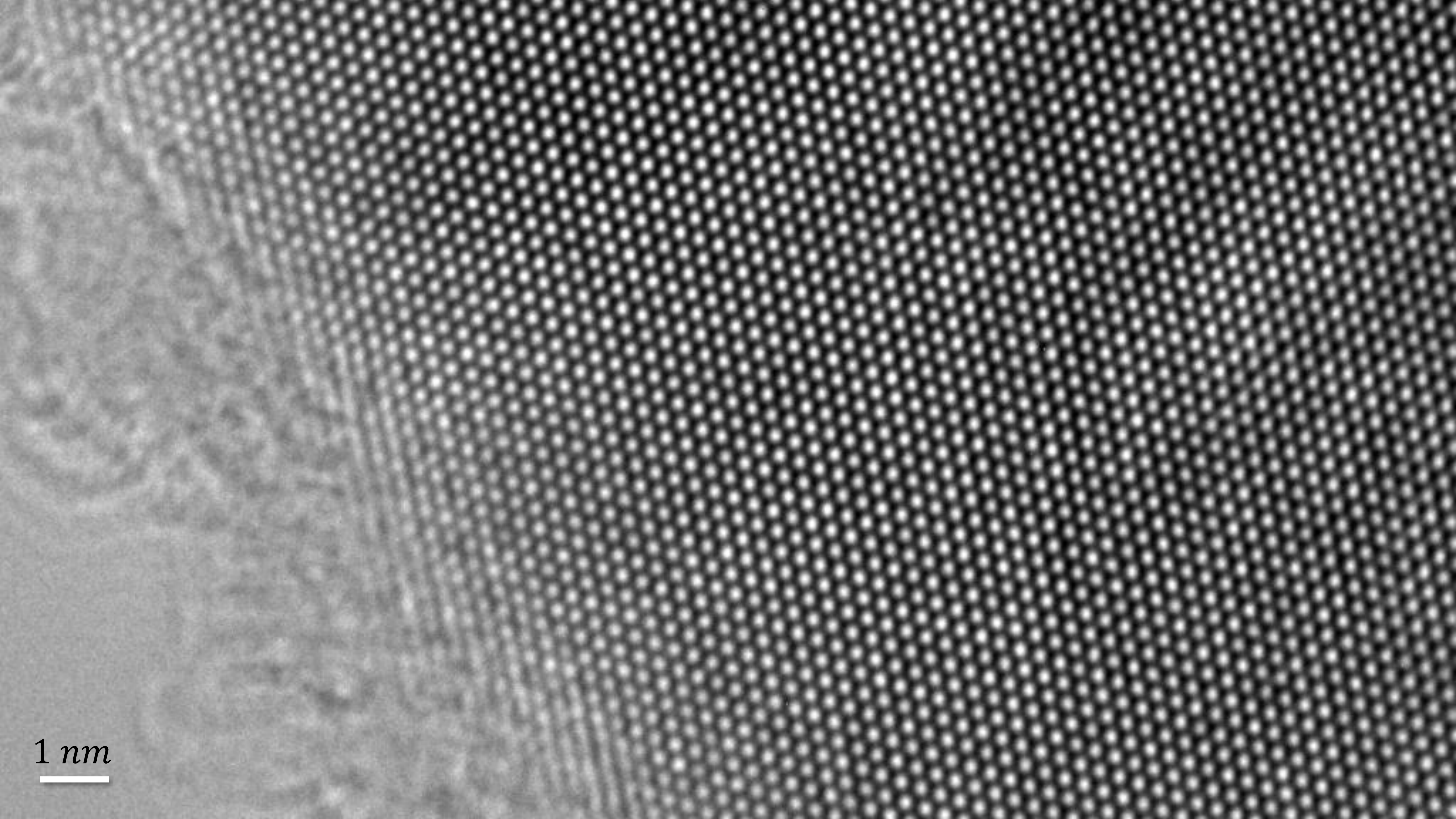
- MAPS in Electron Microscpy (**300 KeV e^-**)
- High resolution (**10 µm** pixel pitch)
- Need to be rad-hard (**1 Mrad**) to withstand the beam.



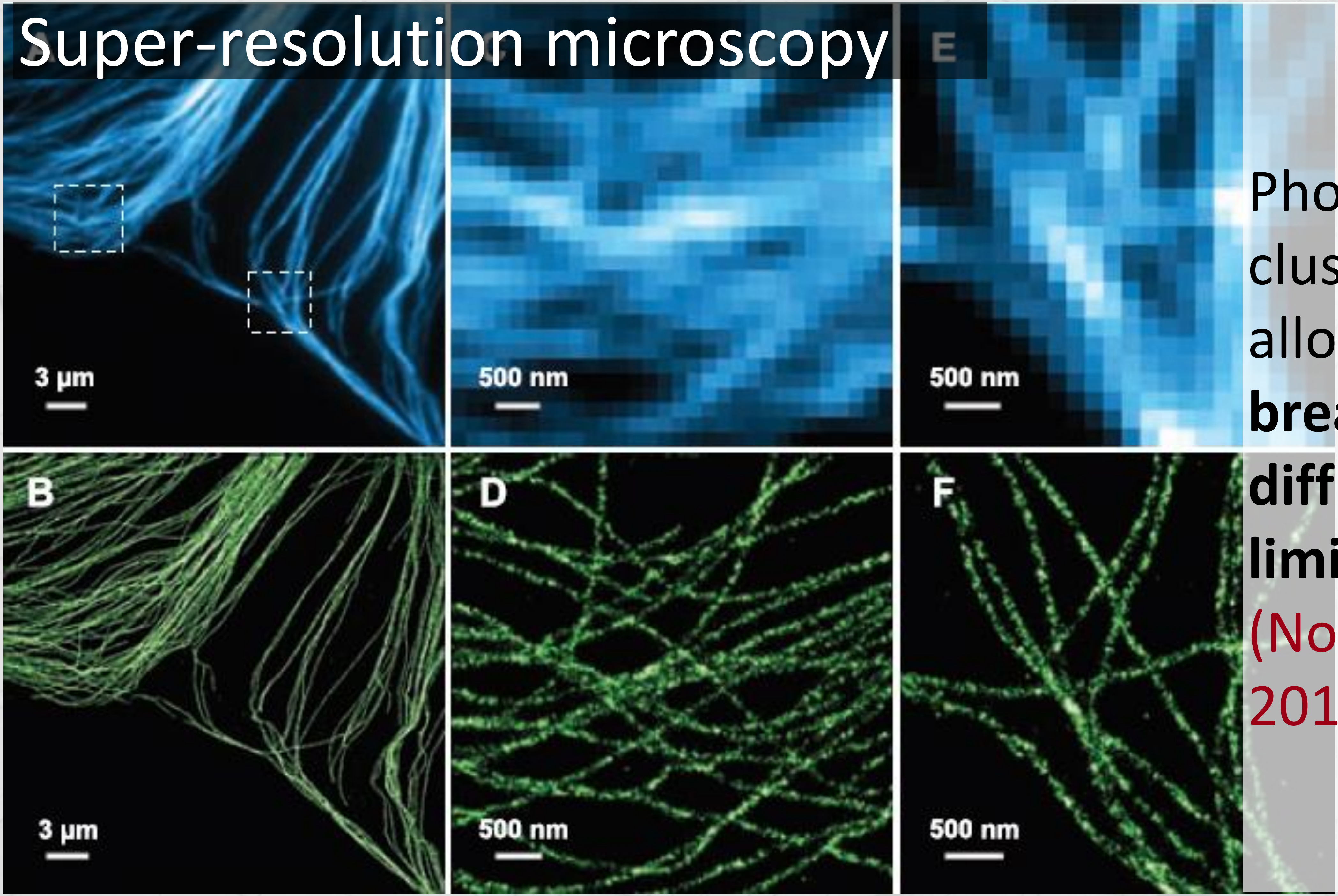
- Resolution is limited by the spread of e^- charge collected by the pixels.
- By running a real-time clustering algorithm is possible to vastly improve image resolution.






1 nm

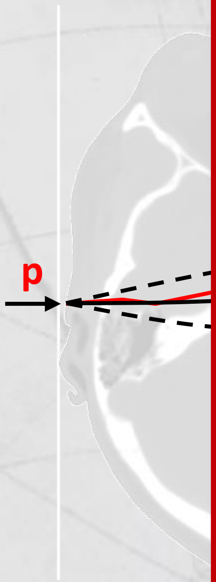
Super-resolution microscopy



Photon clustering allows **breaking the diffraction limit** (Nobel Prize 2014)

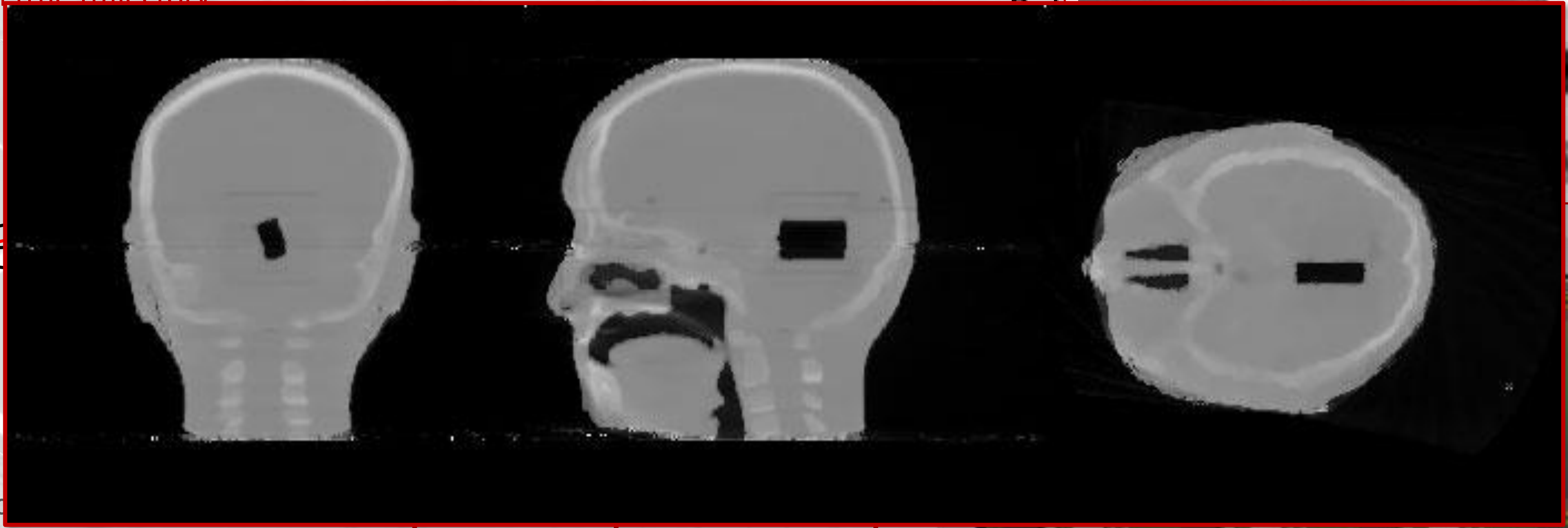
Body low-dose (proton) tomography

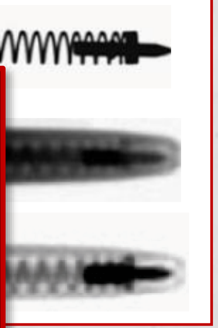
Advancing state-of-the-art in medical imaging using **protons** instead of photons to get **better tissues resolution and less dose to the patient.**



Entry and

Most Likely Path calculation





With at least 10^8 tracks (energy loss, exit point & angle, entry point) recorded, we can reconstruct a complete 3D image.

Industrial applications

X-ray **Computed Tomography** and imaging help verifying production and food quality

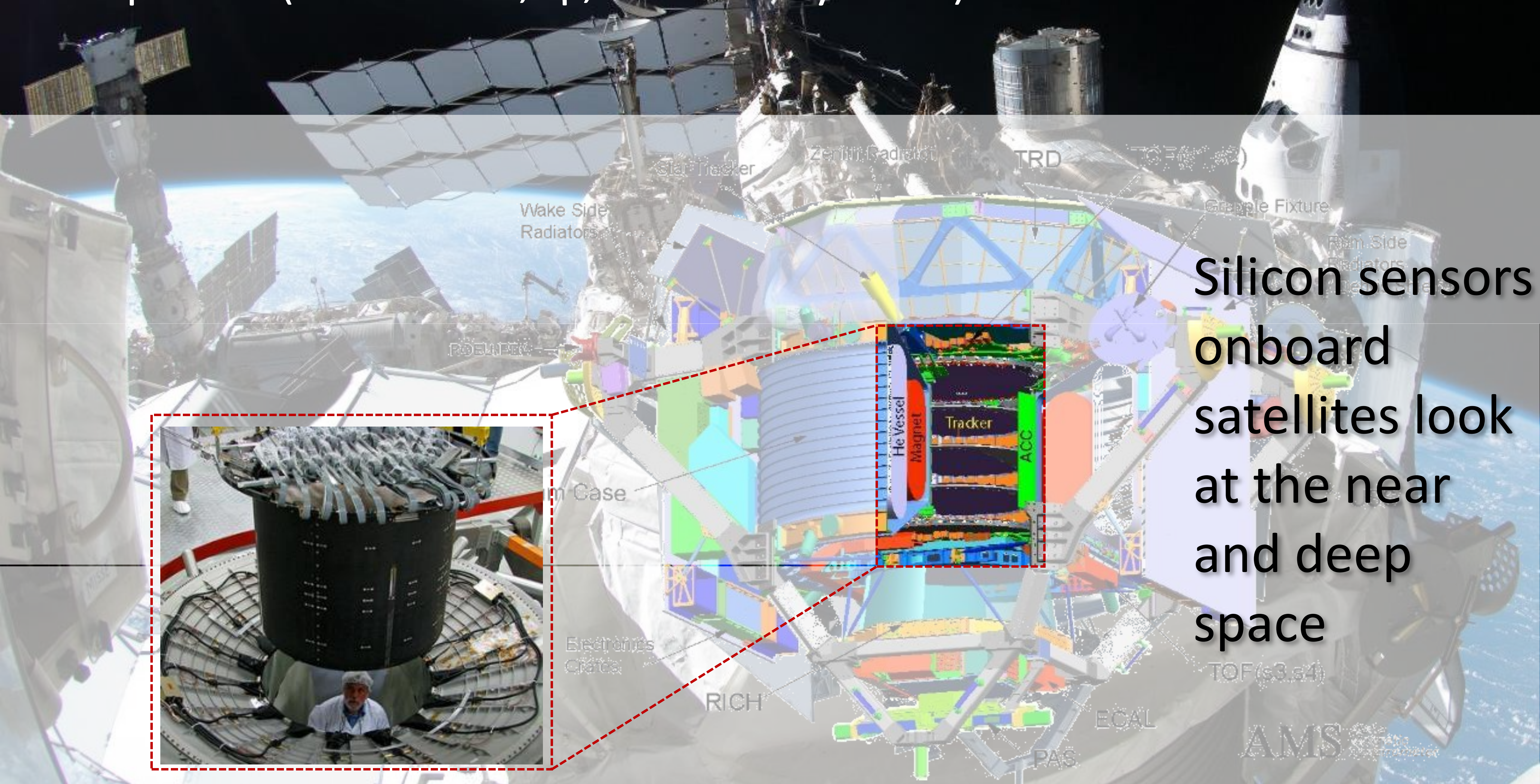
✔ Compliant

Uniform distribution of jam inside the croissant

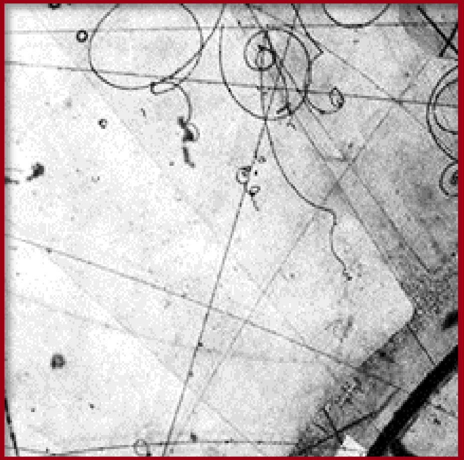
✖ Non-compliant

Incorrect filling quantity and irregular filling distribution

In space (cosmics, γ, and beyond)



Silicon sensors onboard satellites look at the near and deep space



Backup

Power consumption and distribution likely the BIGGEST issues

Consumption

Biggest contributors:

- Front-end circuits: use maximum possible pixel size (enters quadratically)
  - optimise the charge collection carefully
  - optimisation of the time resolution
- On-chip data transmission (see dedicated slide)

- **Status:** – No comparable chip available, differ in terms of pixel size, hit rate capabilities, time resolution,…

Distribution

Vertex Detector

- Stitched chip of 25 cm length (chip split in *z*-direction) and 1 cm width*
- 70 mW cm^{-2} power consumption
- On-chip metal layers for power distribution
- Aluminium, O(1µm) thick
- 20% / 2 mm width used for supply 0.5 Ω/cm * 25 cm = 13 Ω
- Chip operating at 1 V – Average current along a 1 cm wide, 25 cm long chip: 0.9 A
- 3 V voltage drop

Power consumption multiplied!

Outer Tracker

- Parallel powering of chips low voltages, high currents
- sub-optimal in terms of material budget and space

Power distribution alternatives

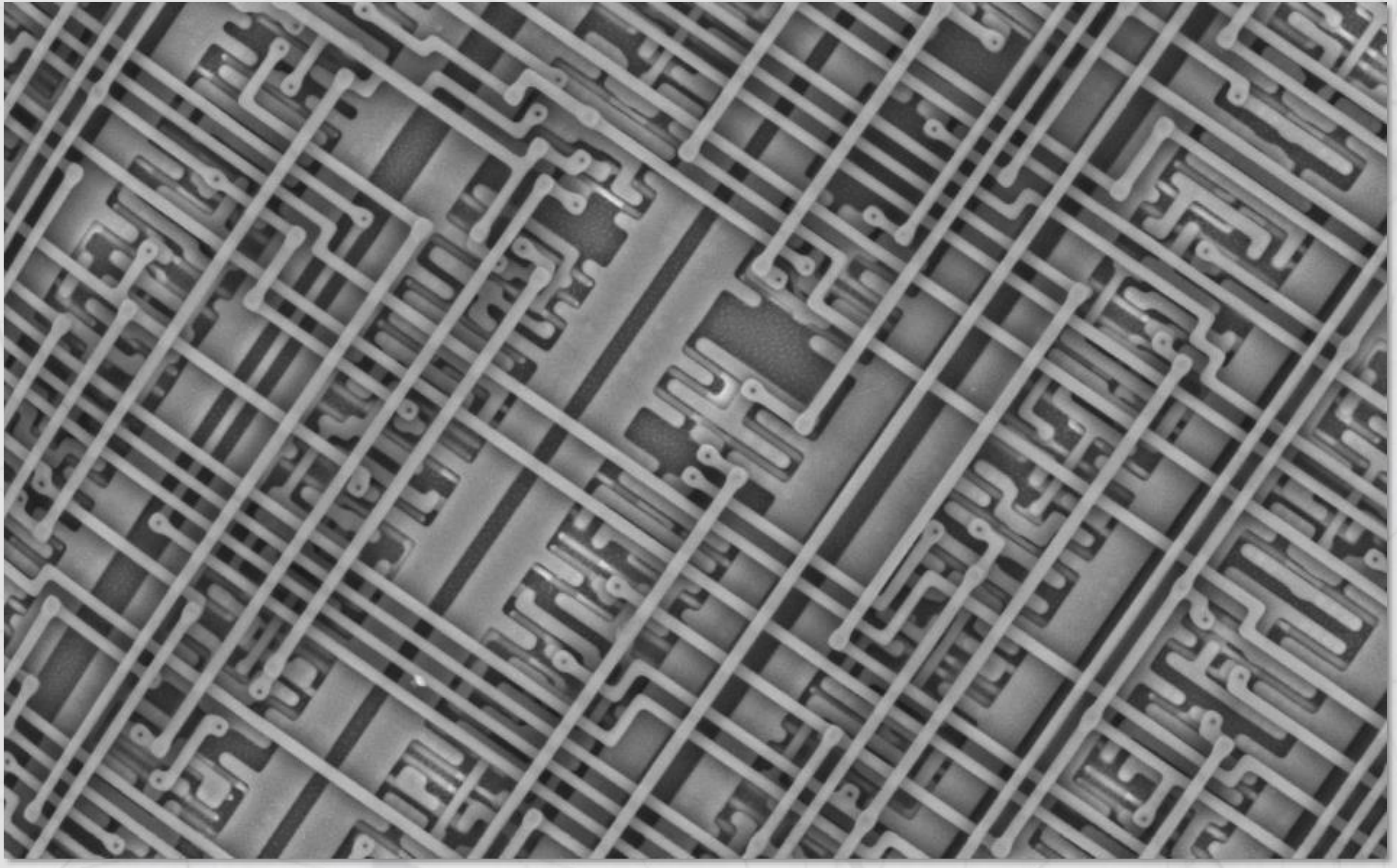
Serial powering
- Current reduction of roughly a factor of 10
- Complicated to realize with stitching: substrate is acting as common reference (unless depletion zones separate the domains)
- safer option use separate chips instead of stitching

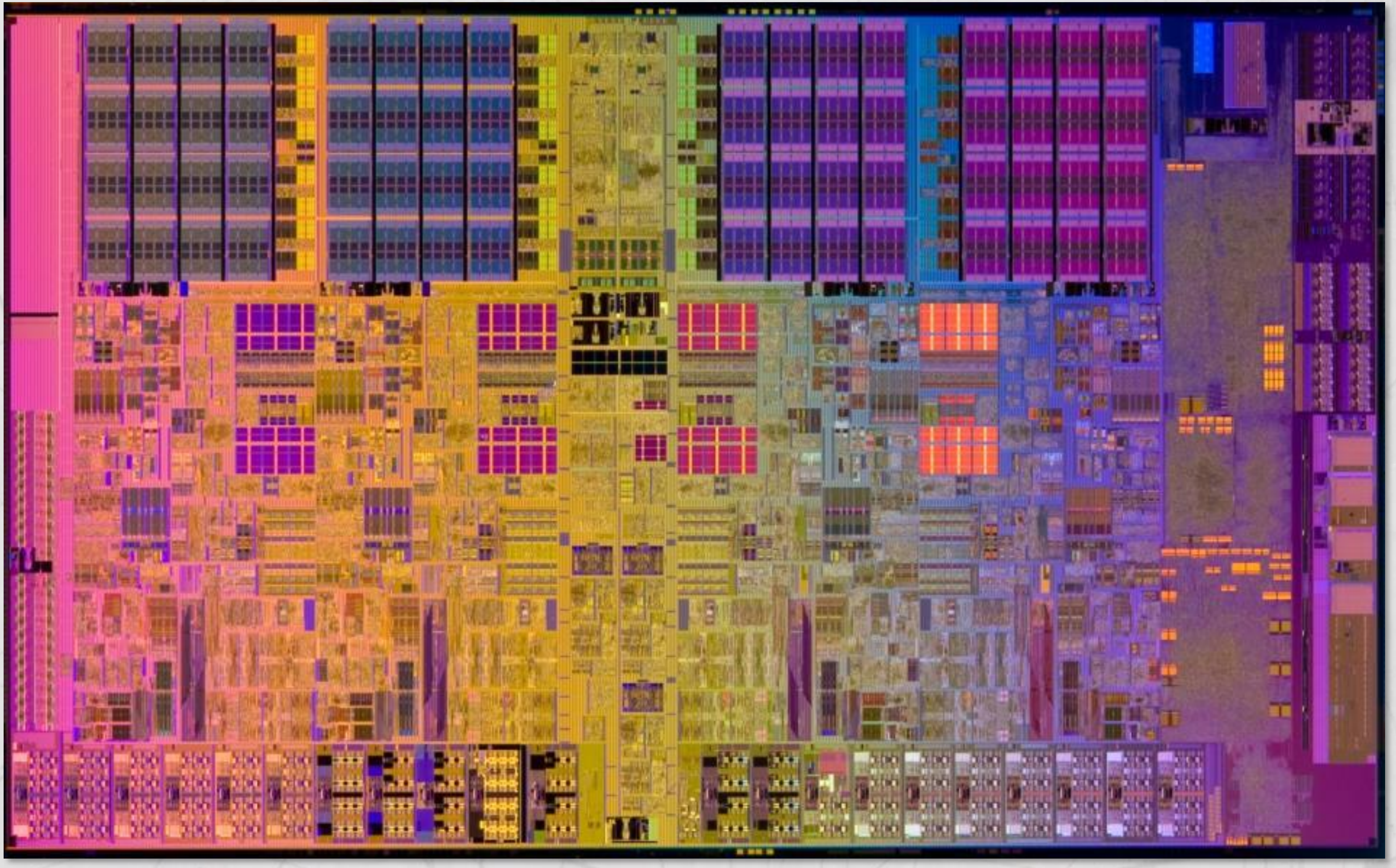
Status:
- in use for ATLAS and CMS LS3 tracker upgrades

R&D need:
- LDO shunt regulator
- Prototyping of a module using existing MAPS

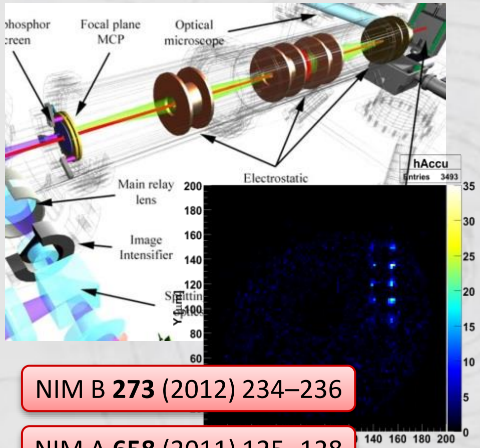
Redistribution Layer (RDL)
- Additional copper and polyamide layer(s) added to the wafer
- Trade off between resistance and material budget
- Impacts the flexibility

R&D need:
- Prototyping of RDL assemblies
- Study of the mechanical properties (i.e. bending and thermal cycles) of RDL assemblies





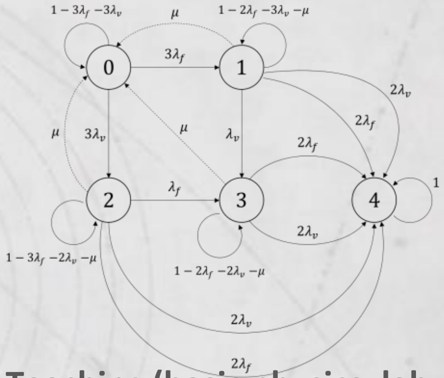
Where do I come from



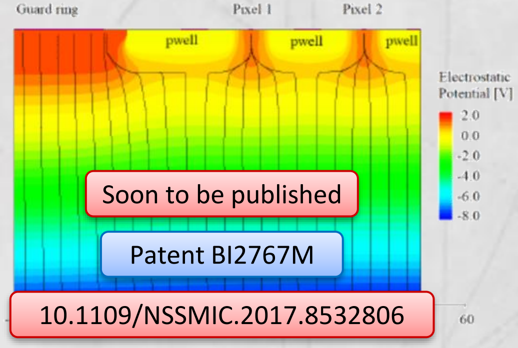
NIM B **273** (2012) 234–236

NIM A **658** (2011) 125–128

First SEU nuclear microscope – **INFN**



Teaching (basic physics, lab, detectors and electronics) **UniPD**

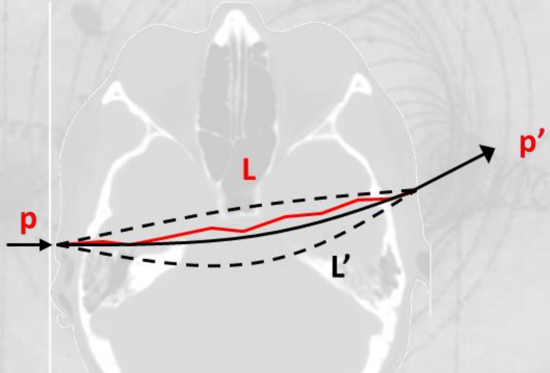


Soon to be published

Patent BI2767M

10.1109/NSSMIC.2017.8532806

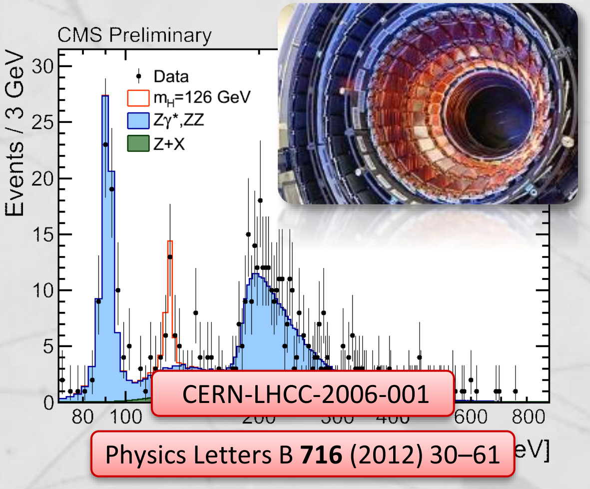
Innovative pixel sensors and architectures – **INFN**



10.1109/TRPMS.2018.2825499

https://doi.org/10.1016/j.nima.2018.10.155

Medical physics **ERC** & **UniPD** & **INFN**

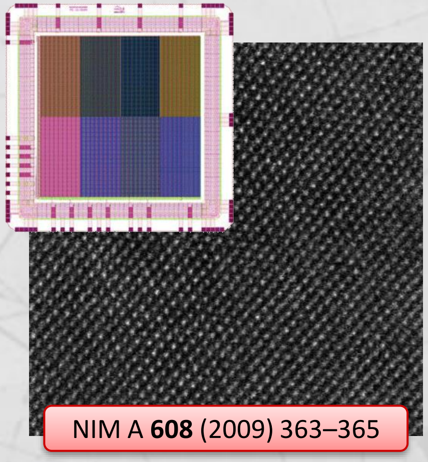


CERN-LHCC-2006-001

Physics Letters B **716** (2012) 30–61

Science **21** (2012) 1569 – 1575

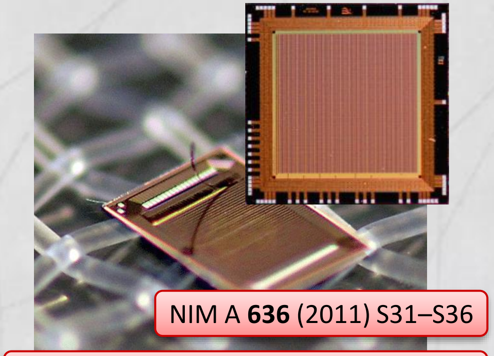
Tracker and vertex detectors **INFN** & **CERN**



NIM A **608** (2009) 363–365

NIM A **622** (2010) 669–677

ILC & TEAM 0.5 Å microscope – **Berkeley**



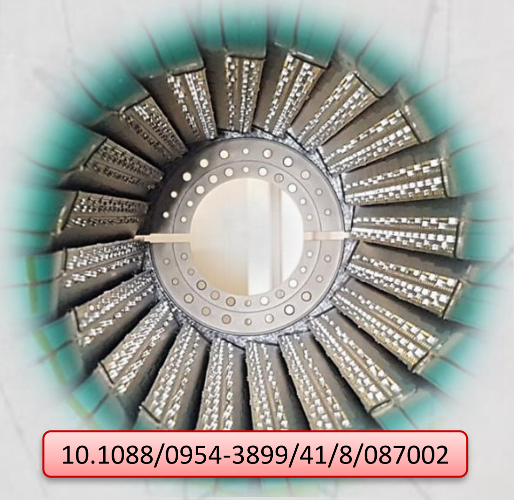
NIM A **636** (2011) S31–S36

dx.doi.org/10.1016/j.nima.2012.10.098

dx.doi.org/10.1016/j.nima.2013.04.042

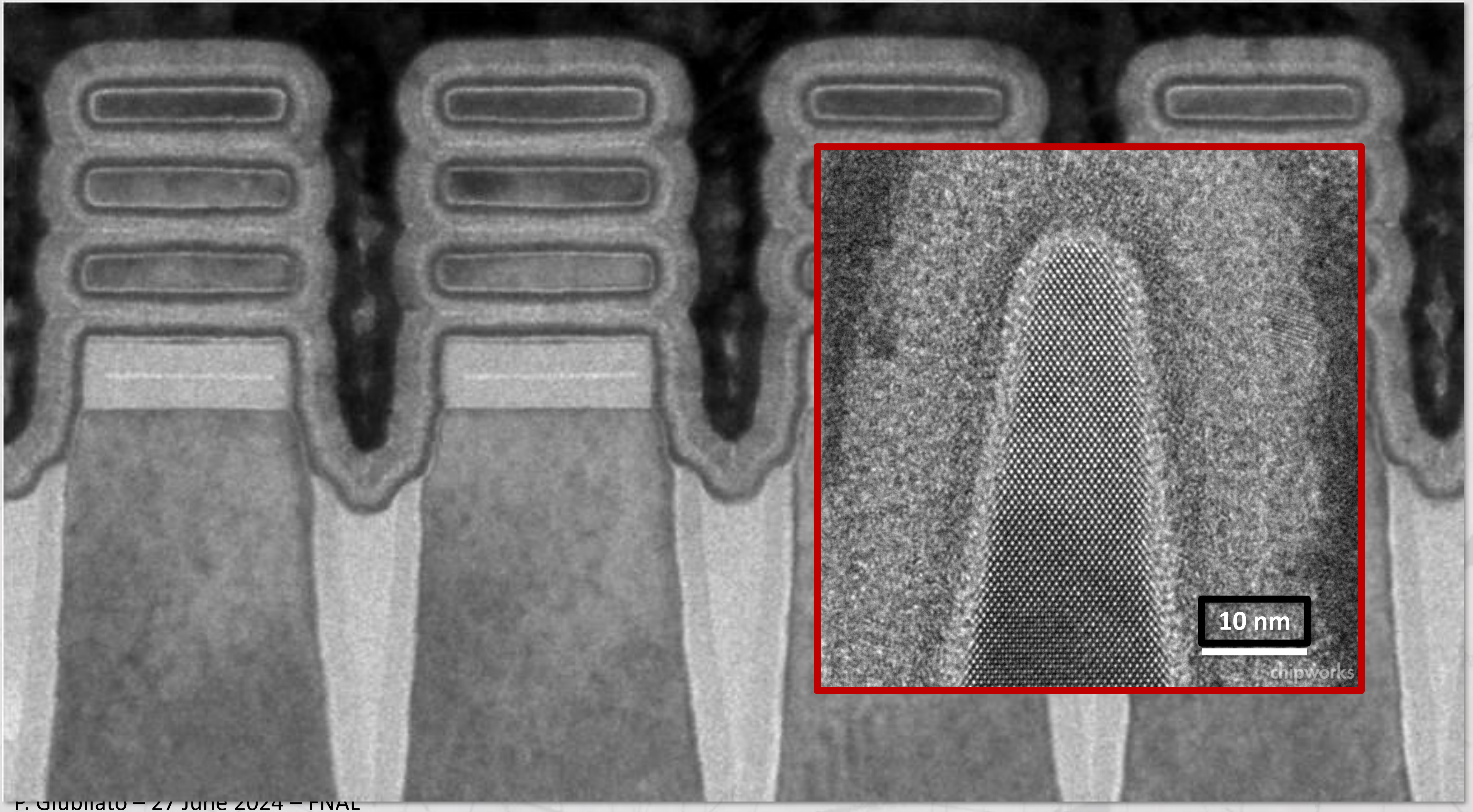
Patent WO 2013075728

LePix & OrthoPix R&D **INFN** & **CERN**



10.1088/0954-3899/41/8/087002

ALICE ITS upgrade **INFN** & **CERN**


10 nm
chipworks