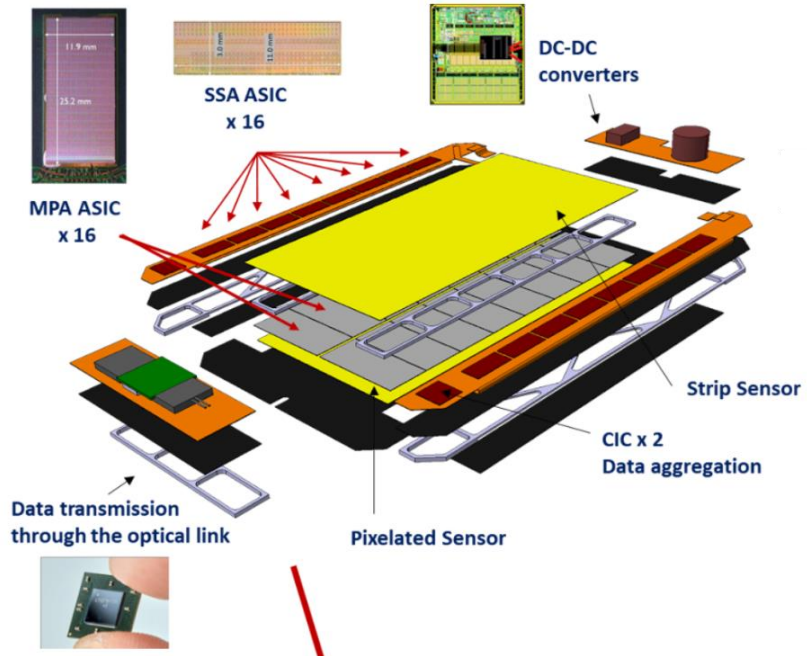
"Embedded software application for a RISC-V based system-on-chip (SoC) for LHCb Velo detector"

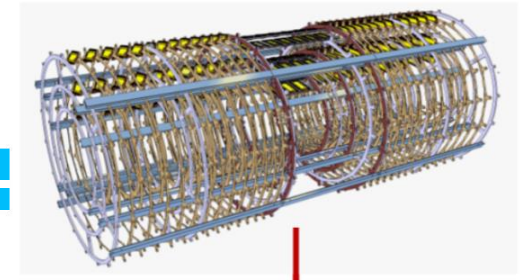
Mentors: Alessandro Caratelli
Marco Andorno

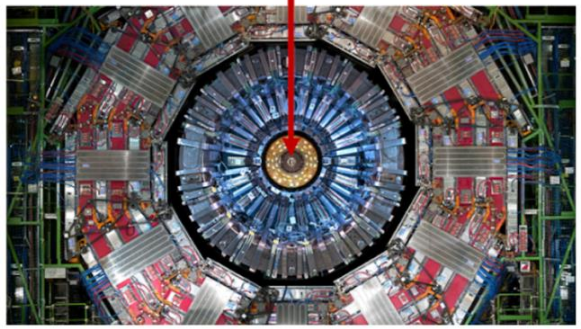
CERN Microelectronics

Project description



❖ Example of ASICs that have been designed by the team, and how those chips are installed in the CMS detector, one of the 4 experimental on the Large Hadron Collider (LHC) at CERN.





Scale of ASIC design continue to grow

Our current focus is on integrating System-on-Chip (SoC) techniques to efficiently consolidate multiple functions onto a single chip while enabling programmability on-detector ASICs.

Advancing SoC Automation

Interconnect the C++ code with the Hardware Abstraction Layer (HAL)

Minimize the user effort in hardware/software code design

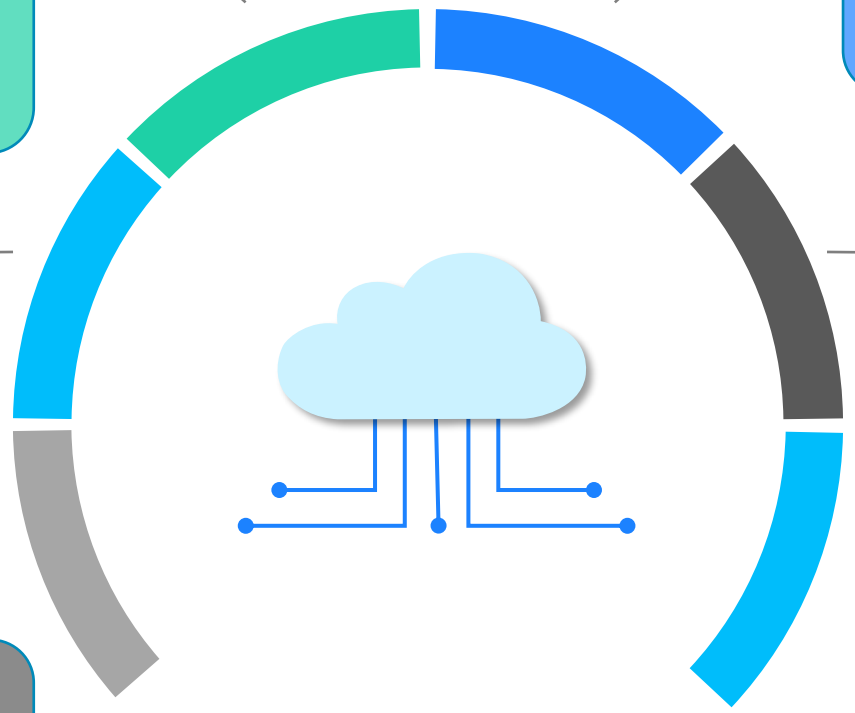
Fast prototype reducing chances of hardware/software bugs

Execute the C++ code on the simulated RISC-V based SoC

Project stages

Create a simple C++ code to read/write parameters

Design the prototype



Setup C++ environment to communicate with the HAL

Verify the conceptual model

Understand basics of the SOCRATES (HAL) platform

Thanks for your attention!

Author: Tarasenko Viktoriia