Beam Synchronous Timing over White Rabbit

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Beam Synchronous Timing (BST)

- Distribute beam synchronous clocks to **beam instrumentation** around the LHC and SPS rings (and transfer lines)
  - 40.0789 MHz “bunch clock”
  - 11.245 kHz “turn clock” (n.b. also called “F_{rev}” by RF and “orbit” by exp.)

- Distribute a small number of “messages” containing machine status and triggers (coming from the GMT) on every turn
  - LHC: https://wikis.cern.ch/display/BEBI/LHC+BST+Message
  - SPS: https://wikis.cern.ch/display/BEBI/SPS+BST+Message

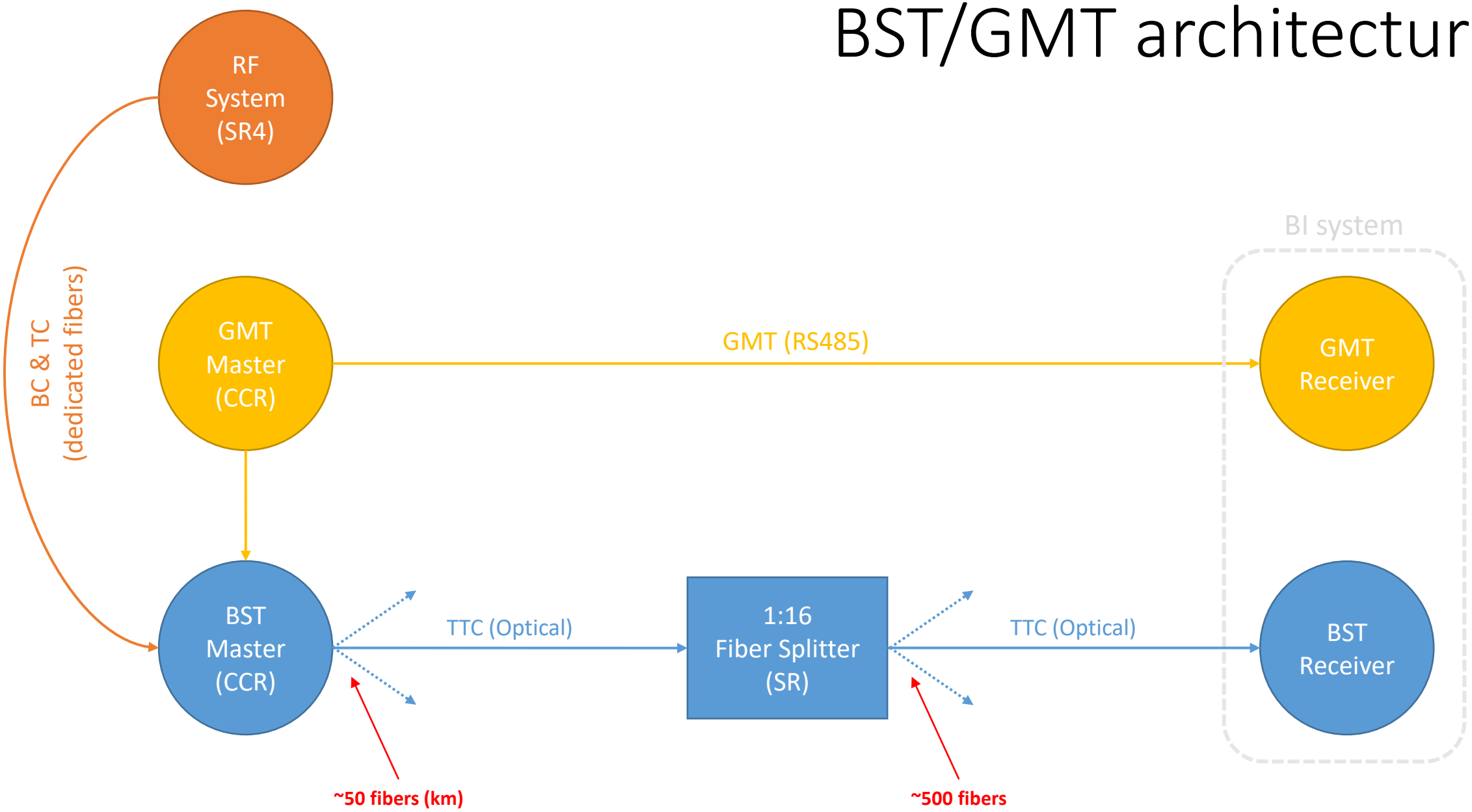
- Optical transmission based on TTC technology (developed by EP)

- A more complete introduction to the current BST was given at the previous workshop

BST issues

- Complex architecture based on many old and obsolete components reaching end of life
  - BOBR, TTC components, CTG-BST
- Limited possibility for expansion without a major reworking
  - No free tasks in the LHC masters
  - Limited number of bytes can be sent per turn in SPS
- BOBR clock recovery (jitter) performance is not fantastic (~300ps rms)
  - A few instruments require higher precision clocks
- No automatic compensation of delay drifts and beam time of flight
- For SPS ion operation: can only follow “average” frequency of the FSK RF which is not bunch synchronous
  - Limitation for FBCTs and other bunch-by-bunch diagnostics

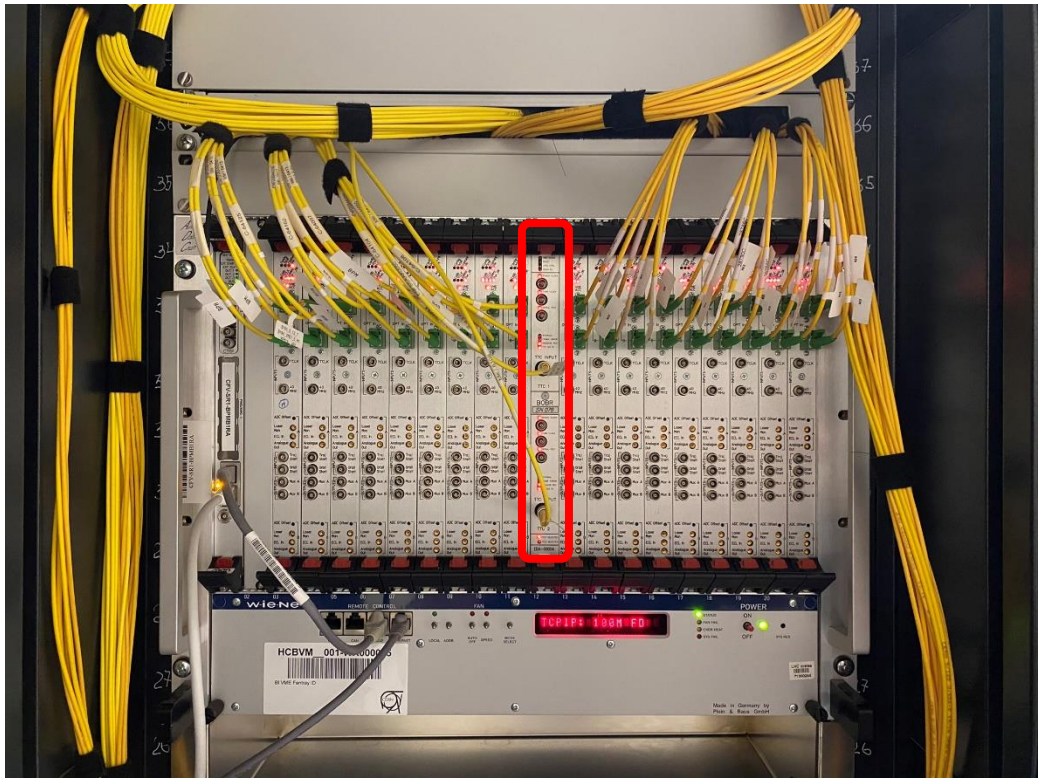
BST/GMT architecture



BST receivers

Systems based on “BI” VME crates

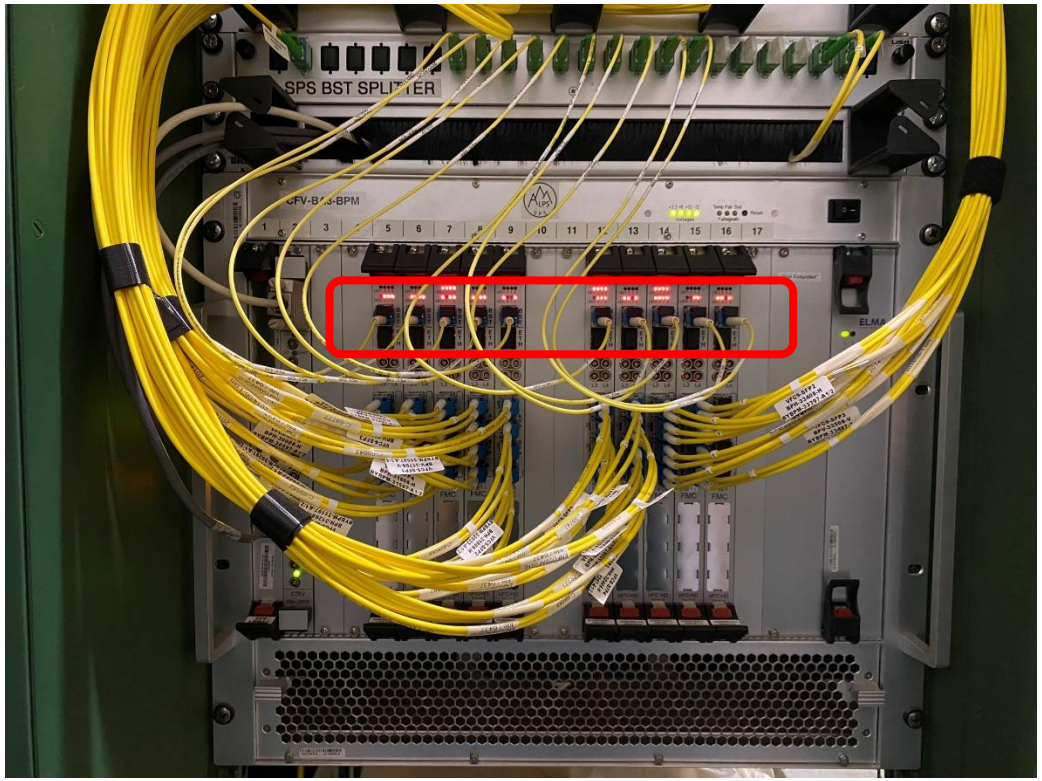
Small number of signals distributed on custom backplane P0 connector from BOBR card in slot 12



Note the trend is to have fewer systems like this…

Systems based on standard VME crates

Each acquisition card (VFC) has its own BST link on a front panel SFP connector, decoding in FPGA

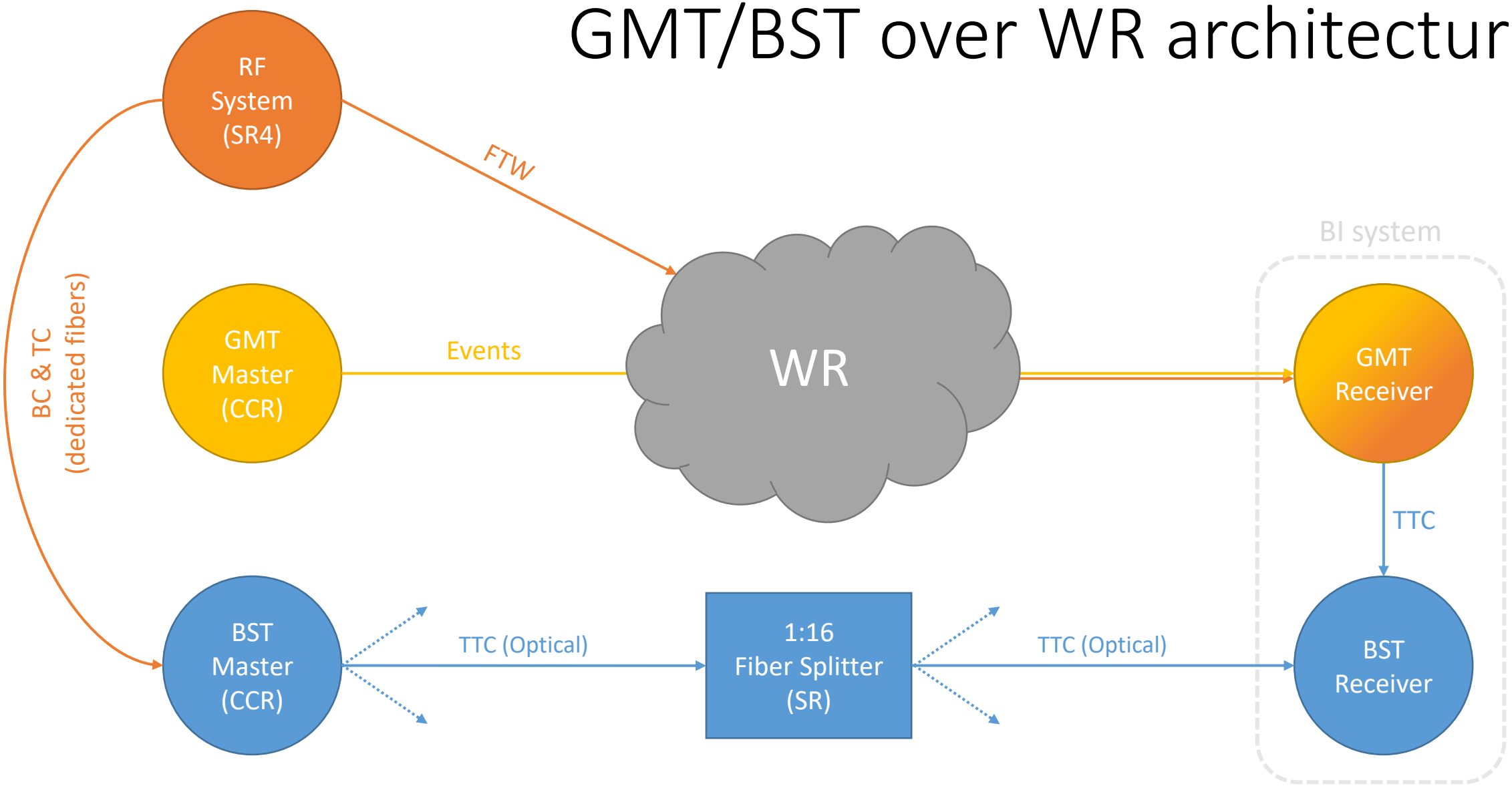


…and more like this!

BST over White Rabbit?

- Migration to White Rabbit (WR) for the General Machine Timing (GMT) in LHC/SPS is planned for LS3
- RF are already using WR to distribute FTW in SPS and plan LHC in LS3
- So, both the timing events and RF will be on the same WR network
- So, we can think about a **single** network for both GMT and BST
- But we must support the existing TTC-based BST receivers for the lifetime of (HL-)LHC!
  - The majority of our operational systems rely on it, even those which will only be deployed during/after LS3!
  - Would be a MASSIVE investment if we wanted to redesign/replace them
- Aim: 100% compatibility for existing BI systems

GMT/BST over WR architecture



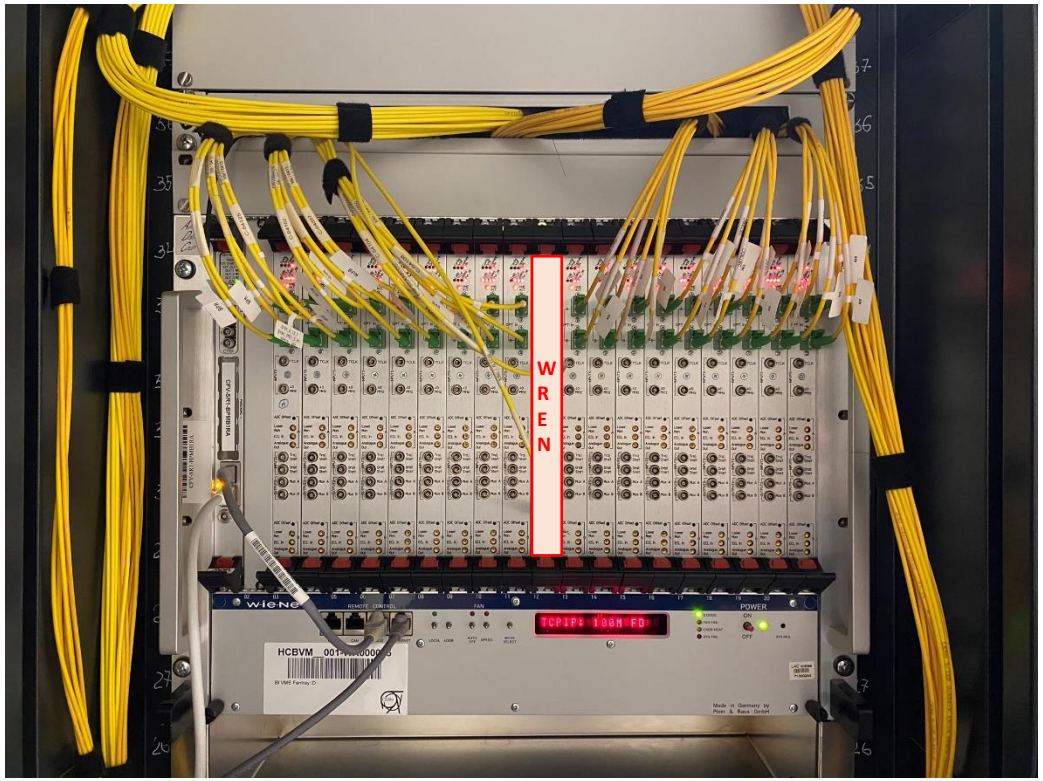
BST over White Rabbit – the idea

- Each WR timing receiver (WREN) will be able generate a TTC-format output stream encoding a BST message
  - Therefore, each VME crate will have a local “BST Master”
  - Aiming for clock performance comparable to today (300ps rms)
- This architecture offers several advantages
  - A single timing receiver design for both GMT & BST
    - No need to design a new BOBR or dedicated BSToWR receiver
  - CCR BST Masters are no longer required
    - No need to design a new BST Masters to replace obsolete components
  - No more global TTC optical fiber network to maintain
  - WR allows fiber-delay compensation
    - Automatic correction of seasonal drifts/etc up the crate level

BST receivers – future

Systems based on “BI” VME crates

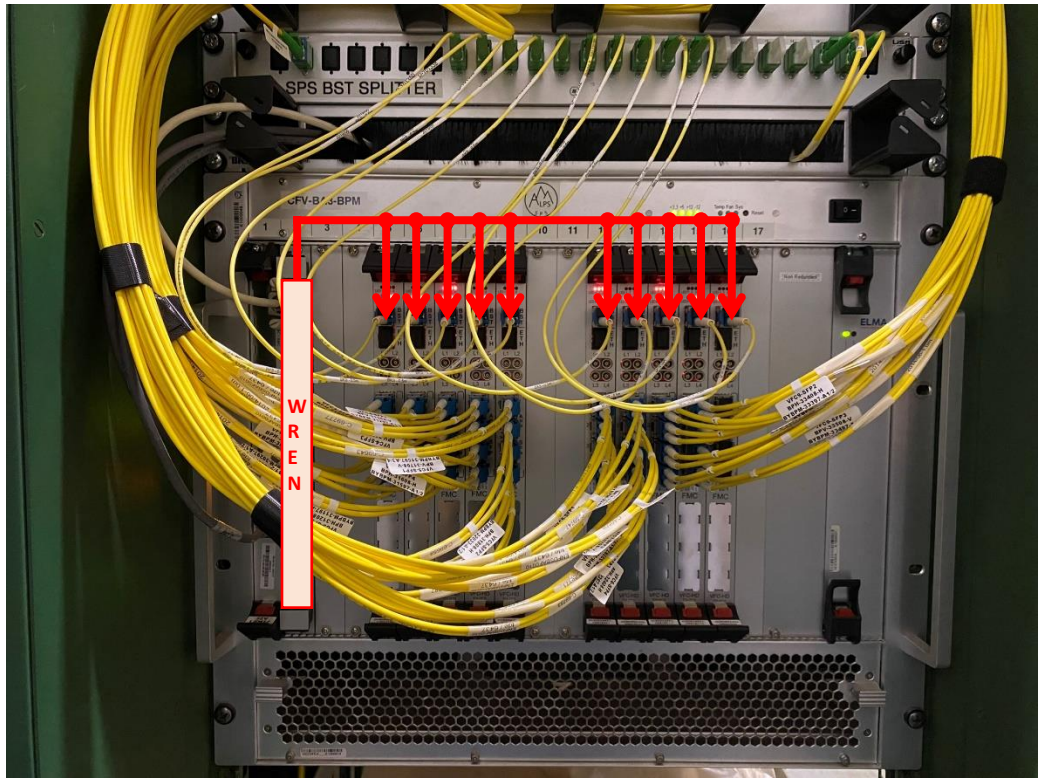
A WREN will replace the BOBR and directly drive the backplane P0 connector with the existing signals



Note, likely only for the LHC BPMs and BLMs after LS3!

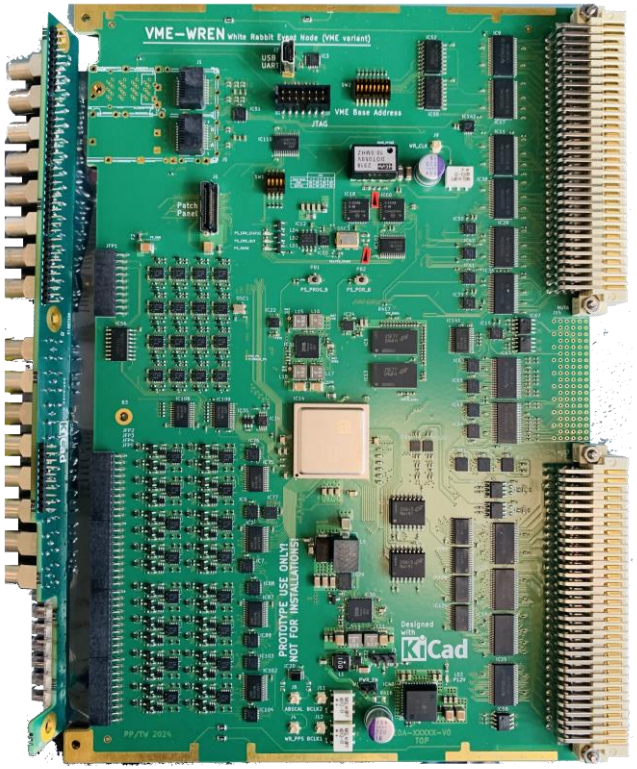
Systems based on standard VME crates

A WREN will replace the CTRV and generate a TTC signal via SFPs on an RTM to connect to the VFCs



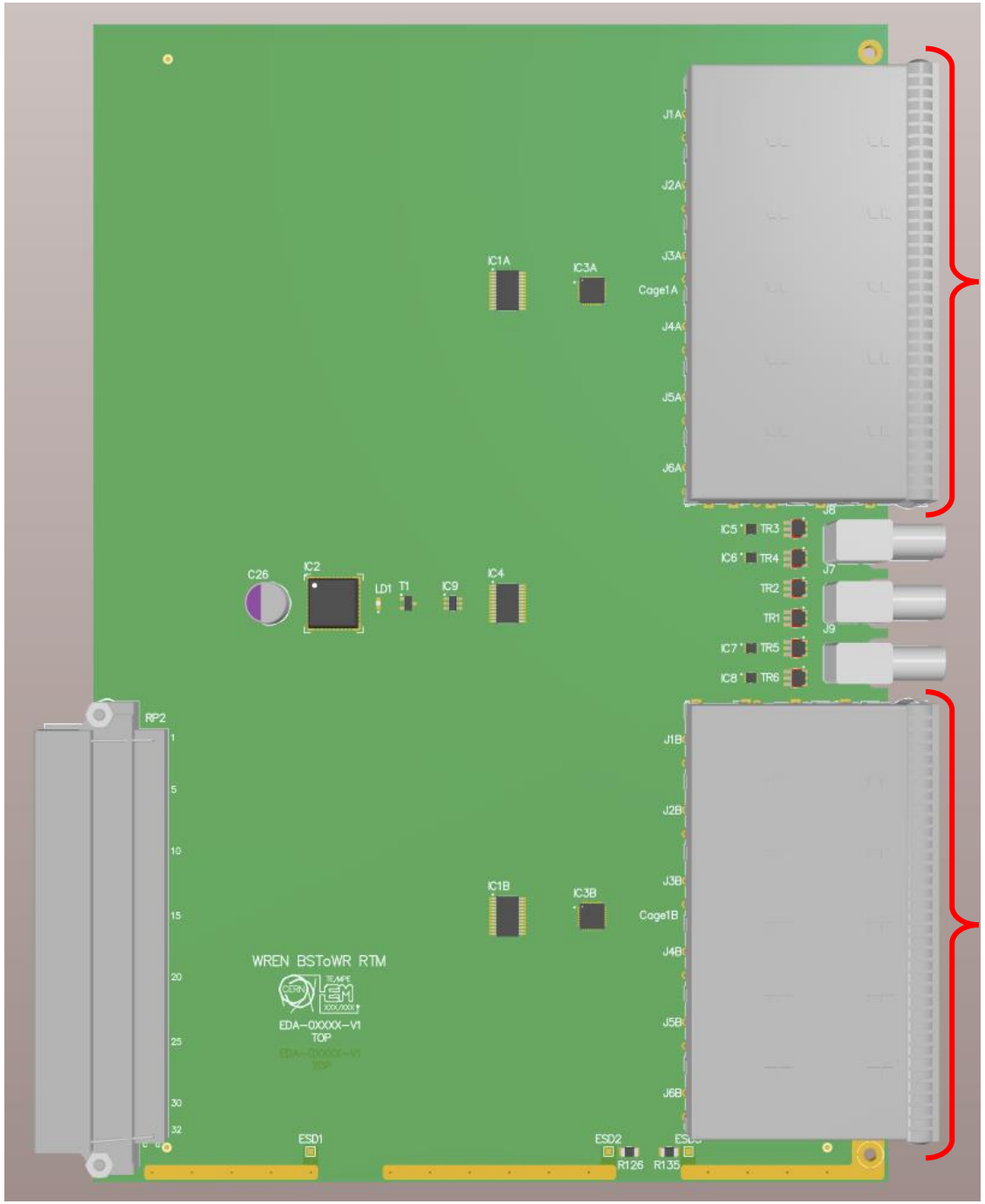
WREN – White Rabbit Event Node

- New timing receiver replacing the existing CTRs
- Three form factors: VME, PCIe, PXIe
  - **Note:** no more PMC version, so will require an additional free slot in the VME crate!
- All form factors will feature 32 counters (4 or 8 today)
  - So, one WREN can replace 4 CTRV
- Single/double width VME cards with different number of LEMO outputs
  - Additionally: all 32 outputs available on a 1U passive patch panel mounted outside the crate (also for PCIe)
- It will be possible to output the bunch/turn clocks on one of the FP LEMO outputs (also for PCIe)



WREN RTM for BST

- Will sit behind VME-WREN and provide TTC/BST outputs on SFP
  - Note, only compatible with ELMA VME crates!
- 6x SFP for BST1, 6x SFP for BST2
  - Option to output BST for LHC1/LHC2/SPS on either or both
  - SFP gives a direct connection to a single VFC or multiple via optical splitters (with high power SFPs)
- LEMO test points for TTC, BC, TC
  - ECL levels (800mVpp)
- Preliminary schematics (CERNbox)



WREN RTM Limitations

- The RTM will **ONLY** work in ELMA VME crates as it is not mechanically compatible with the Wiener “BI” type
- This means that any systems using VFC with BST/SFP in BI-type crates will need to either:
  1. Replace the crates by ELMA type **(preferred)**
  2. Take the BST connection from another crate
- Based on the feedback gathered about the BST the only impacted system in BI is the BRA
  - All other BI systems using VFC+BST/SFP are also using ELMA crates
  - Propose that the simplest solution is to replace the BRA crates by ELMA ones (and recuperate the BI crates as spares!)

Deployment plan

- CEM will have WRENs available in late 2024 (for lab) and more in early 2025
- Aim is to have a demonstrator of BST over WR in the SPS during 2025 on a few pilot (non-critical) systems
- LHC depends on availability of FTW distribution from RF (not before LS3?)
- Initial deployment plan:
  - Complete deployment in SPS during LS3 replacing existing BST
  - Pilot systems in LHC after LS3 with full deployment during a subsequent YETS
- But this plan will be revised based on the experience gained in 2025
  - LHC BST *should* be simpler than SPS (lower F_{rev} & F_{rf} frequency swing)
  - Strong desire to renovate LHC completely in LS3, if possible, to avoid the need for extra recommissioning time after subsequent YETS
- Legacy BST Masters will be maintained until all systems are migrated

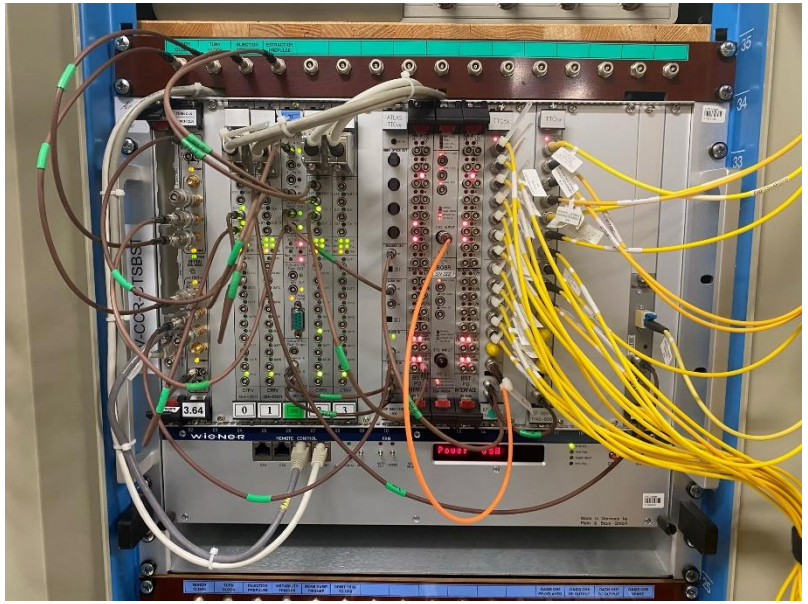
Conclusion

- The migration to GMT over WR combined with the fact that RF FTW are distributed over the same WR network gives us an opportunity to replace the existing BST based on TTC technology
- Aim of the BST renovation is to be 100% compatible with all existing BI systems:
  - **Systems using P0:** WREN will replace BOBR and drive directly the P0
  - **Systems using VFC:** WREN RTM will provide possibility of driving directly 12 VFCs in the same crate
- Aim to have a first test deployment in SPS during 2025

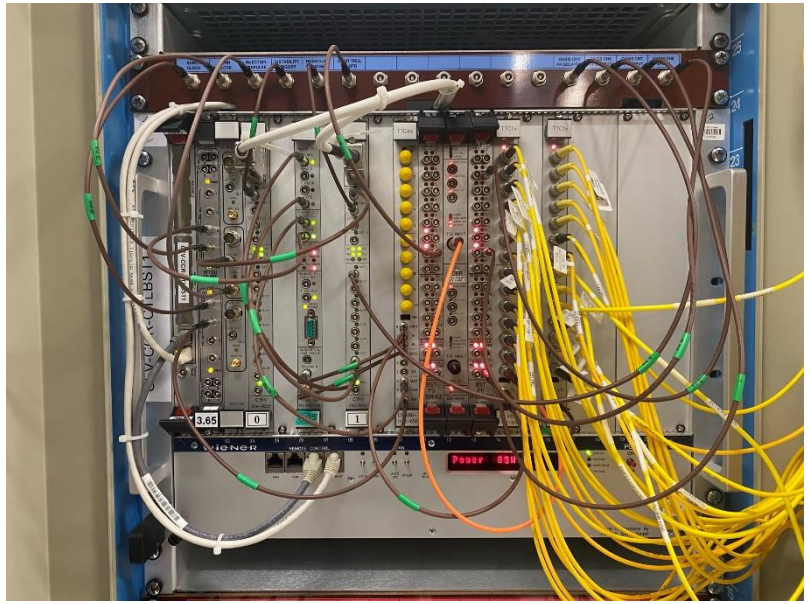
Backup

BST architecture – masters

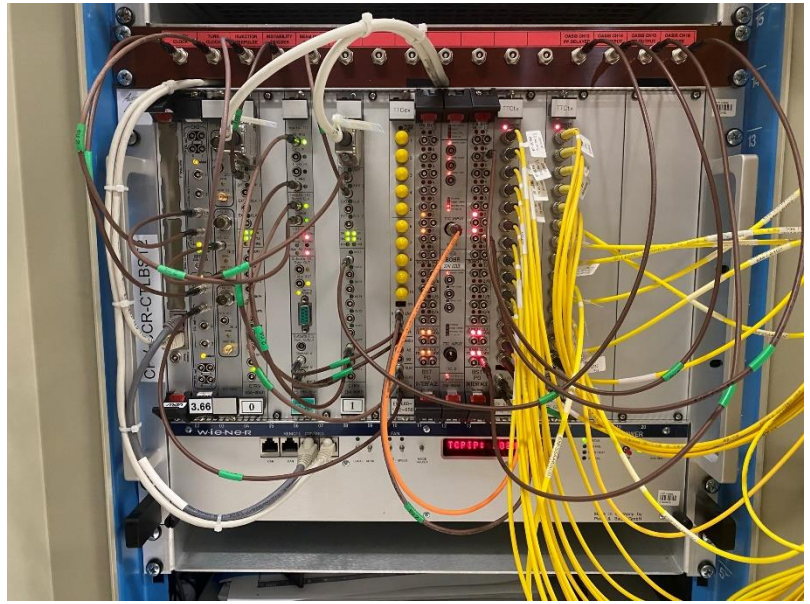
- Three BST masters located in CCR (Prevessin) RA0907
- Mix of components from BE/CEM, EP/ESE, SY/BI + SY/RF



SPS



LHC Beam 1

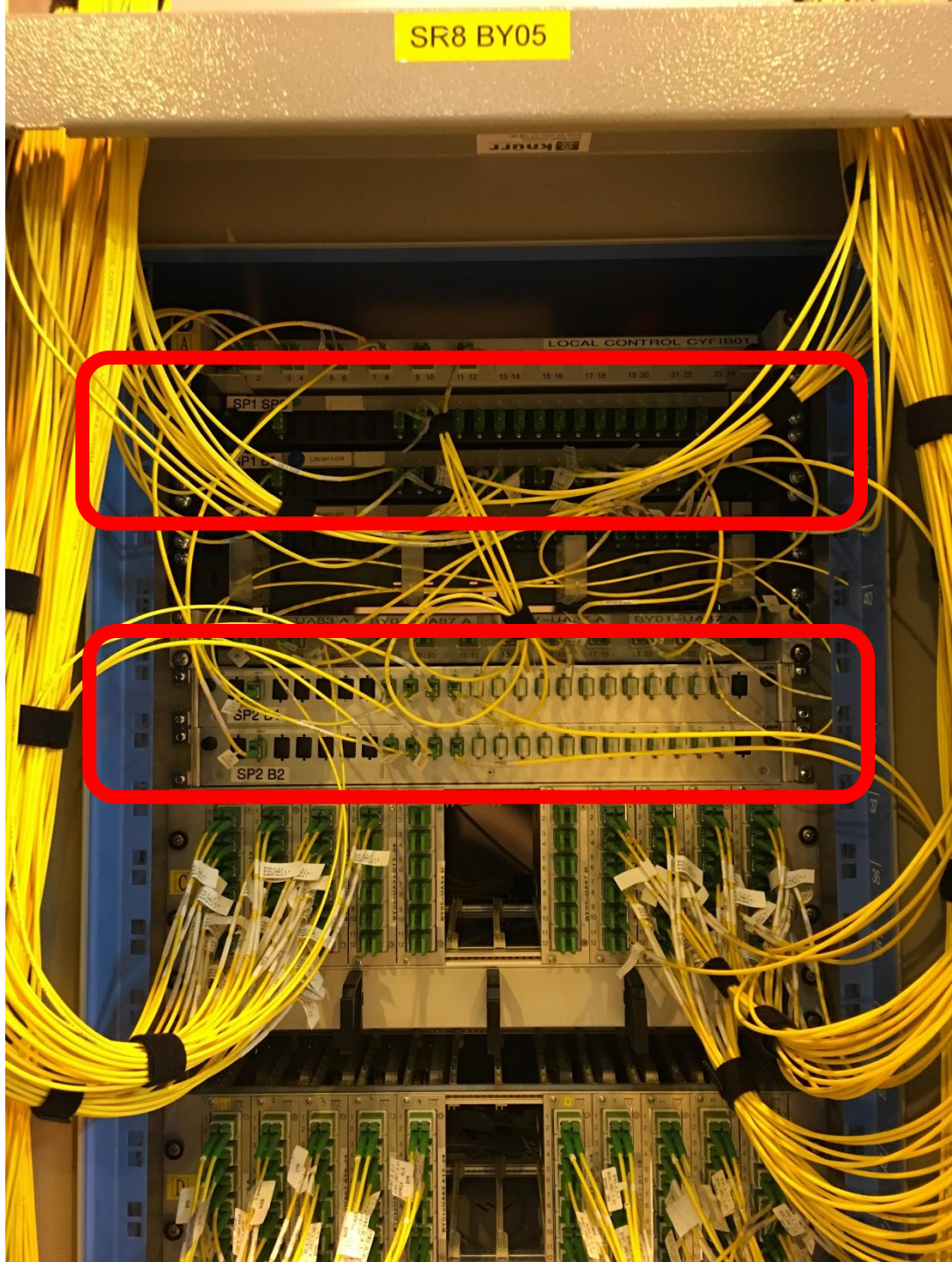


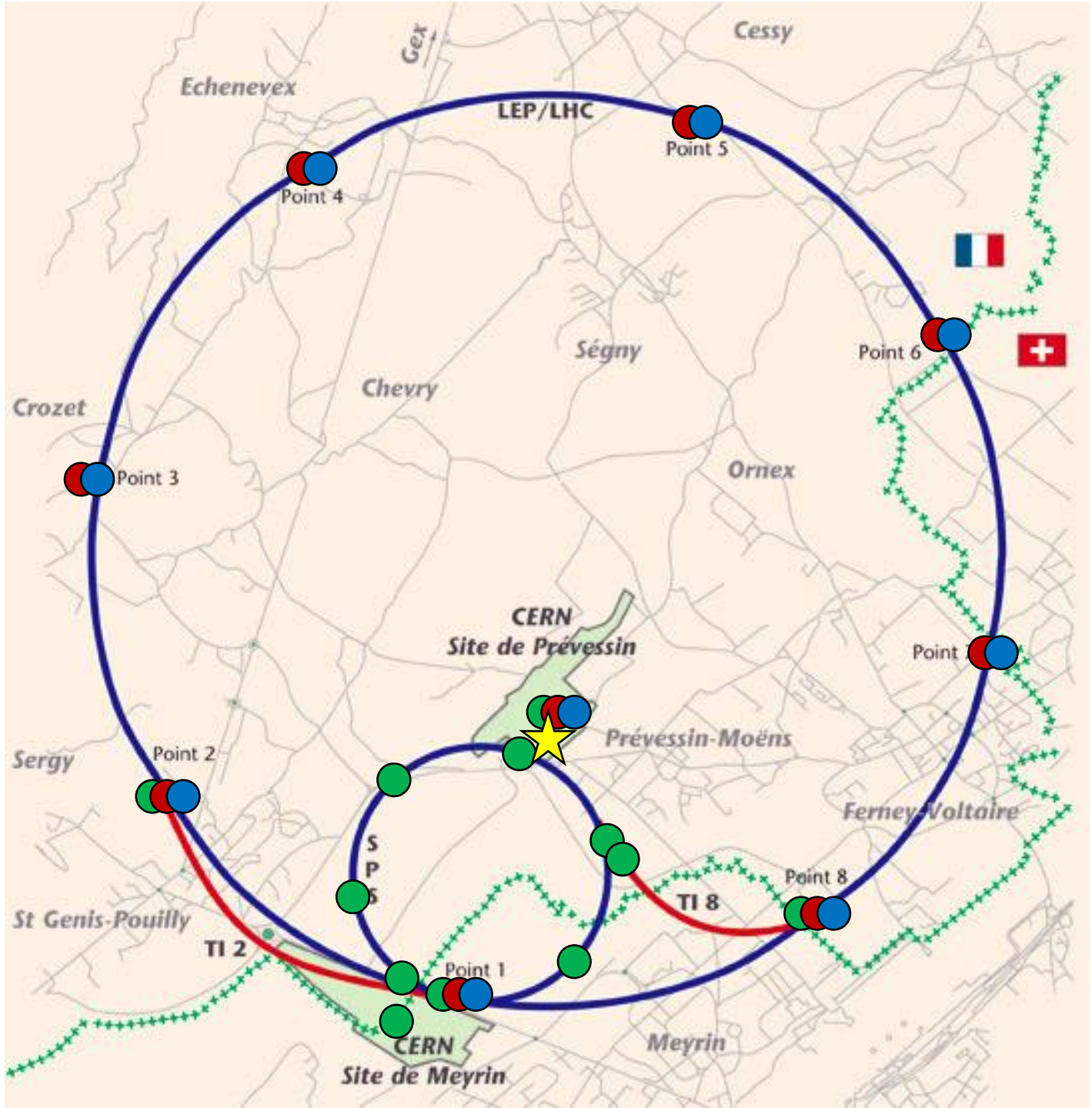
LHC Beam 2

LHC beams are entirely independent! 2x the infrastructure!

BST architecture

- Distribution on (1-6x) fibers from CCR to each LHC/SPS surface building and labs
  - **SPS:** BA1, BA2, BA3, BA4, BA5, BA6, BA7, HCA4, SR2, SR8, 865, 866, 867
  - **LHC:** SR1, SR2, SR3, SX4, SR5, SR6, SR7, SR8, 865, 866, 867
- 1:16 passive optical splitters in the surface building
  - Fiber patch cords for surface racks
  - Long fibers to underground racks
- **~500 receivers!**
  - **Mostly BI**
  - **A few in the experiments**





CCR

LHC B1

LHC B2

SPS

BST message

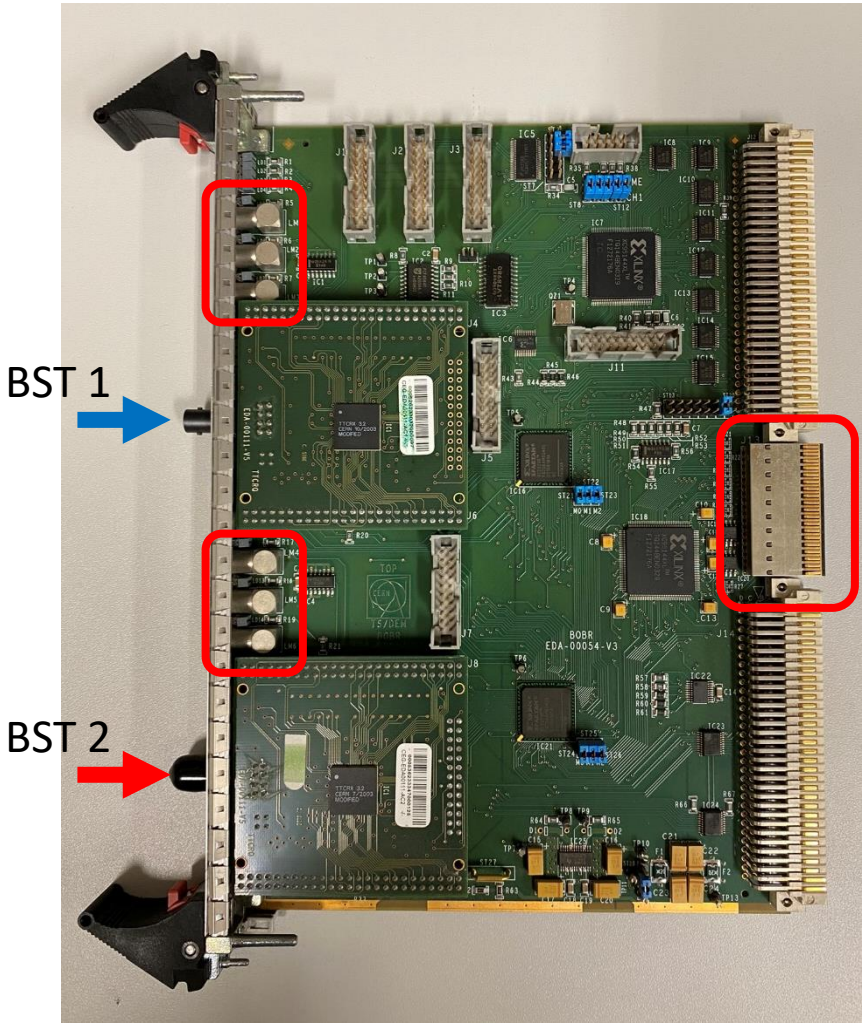
- 58 bytes of information sent every turn in LHC
  - Automatically populated
  - Static information
  - Taken directly from the GMT telegram (update at 1Hz by a FESA class)
  - UTC clocks and replication of GMT timing events
  - System specific triggers generated in the BST master code
- SPS only sends a subset (17b)

BST message layout

Position	Content	Comment
0 → 7	GPS absolute time	Automatically sent by the CTG
8 → 12	Acquisition triggers	See separate table below
13 → 15		
16	Diagnostics byte	Sent by the "diagnostics" task
17	BST master status	Sent by the "values" task
18 → 21	Turn count	Automatically sent by the CTG
22 → 25	LHC fill number	Sent by the "values" task
26 → 27	Machine mode	Sent by the "values" task
28 → 29		
30 → 31	Beam momentum (120MeV)	Sent by the "values" task
32 → 35	Intensity beam 1 (1E10)	Sent by the "values" task
36 → 39	Intensity beam 2 (1E10)	Sent by the "values" task
40 → 55		
56 → 58	External triggers	Automatically sent by the CTG

BST receiver – BOBR

- Dual channel BST receiver in VME form factor
  - Design from 2002-2005
- Distributes signals on P0 (in specific “BI” crates)
  - Bunch/turn clocks
  - Two selectable message bytes
  - Eight “bunch selector” signals (not used)
- Bunch/turn clocks available on front-panel
  - LEMO 00 with “TTL” levels
- Generates interrupts for CPU
- **A single BOBR serves an entire crate (up to 18 VME cards) via P0 distribution and backplane fanout**



BST receiver – VFC/others

- Today, most BI developments are based on the VFC-HD or other standalone FPGA boards
  http://www.ohwr.org/projects/vfc-hd/wiki
- BST IP core is available for integration in FPGA
  https://gitlab.cern.ch/bi/HDL_Cores/BST_FPGA
- Provides beam synchronous clocks (160.32MHz, BC & TC) and all message bytes to FPGA for user logic
- **Each board has its own optical receiver → requires many more optical splitter outputs**