Addressing interface between HGTD and the BIS system

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A-22 (review panel of the HGTD HV FDR): The interaction of the HGTD DCS and HGTD power supplies with the BIS must be specified in more detail. **In particular, it needs to be clarified whether switching between different HV levels will be needed as a function of the LHC state and if yes, how the interface with the BIS will be implemented.** Current detector systems use the “stable beams” hardware signal for switching between HV levels (“standby” = off or reduced, “ready” = on). Furthermore, it should be clarified if and how the injection permit hardware signal from the HGTD should be provided to the BIS.

How HGTD will manage BIS is under discussion:

- **Pure hardware solution**, using HVP, HVP Master and BIS cards in MIC, cannot be possible because HGTD HV power supplies do not support it;

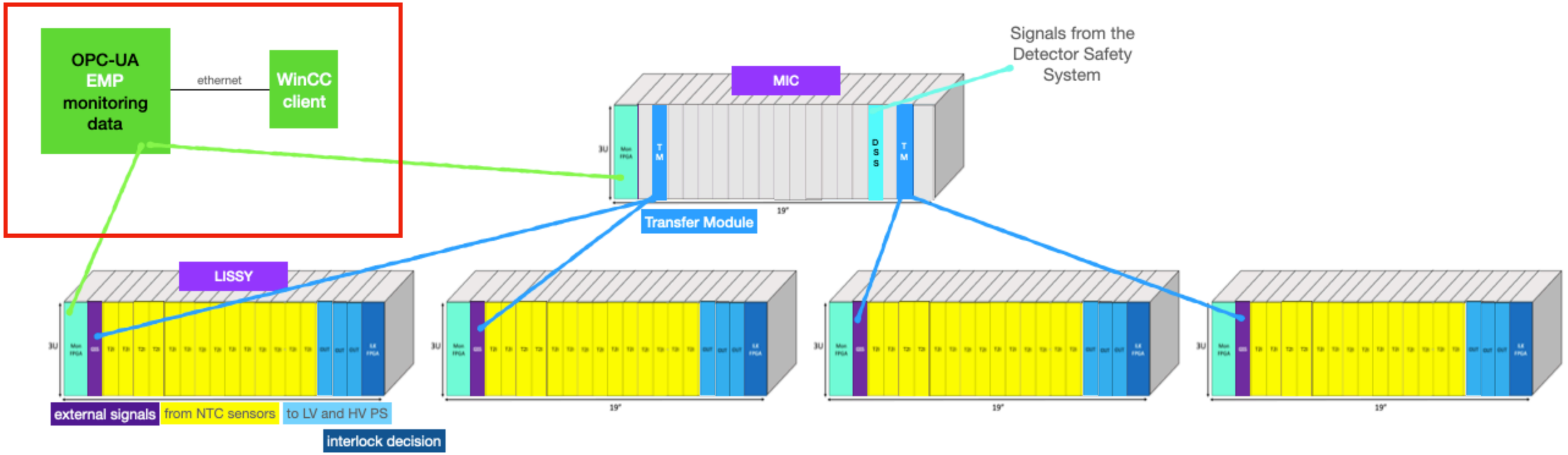
- **Pure software solution** - this must be evaluated, bearing in mind that it is network dependent, PC machine dependent, so it is vulnerable. In case of problems with these systems, how to ensure the protection of the detector in case of urgent power off?

- **Mixed solution** - DCS manages BIS system but interlock remains as the last line of defense.
  This is the focus of our discussion today.

Important to keep in mind - HGTD HV PS need certain (reduced) HV value to fulfil the HGTD lumi program

Mixed solution - DCS manages BIS system but interlock remains as the last line of defense.

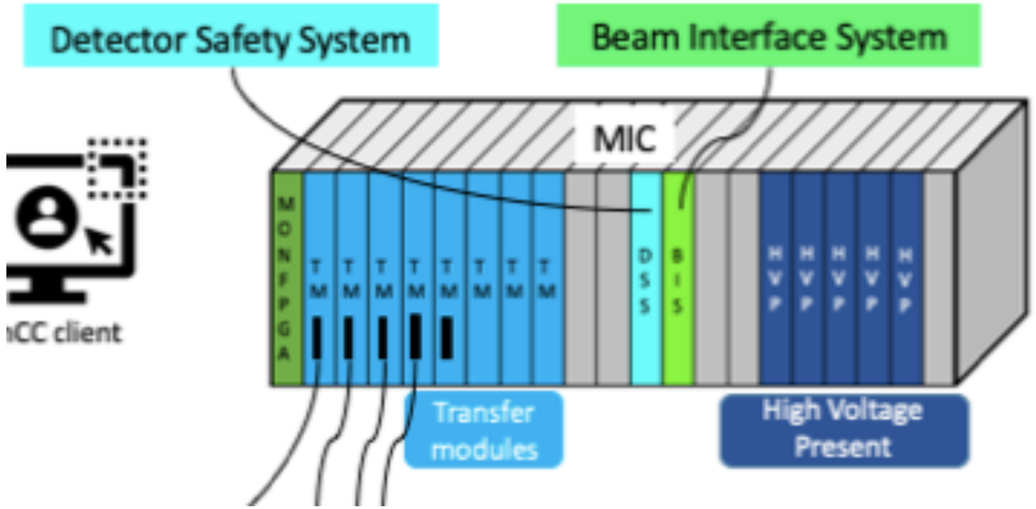
Could a flag “DCS READY” be communicated to Interlock?



Could it be through EMP/OPC/Mon-FPGA? In case of not-READY shutdown compulsively the HV power supplies through LISSY/llk-FPGA/OUT modules?

If “DCS READY”, DCS is able to manage the IP (Injection Permit) and the SB (Stable Beam) flags.

Could DCS propagate IP, either directly or through ELMB, to HVP Master?



Or Spare-in/out cards in MIC would be needed?

9.4. SPARE-IN

The SPARE-IN module

- Can receive up to three signals from external sources,
- These signals are routed to all TM modules in parallel.
- It has 3 test signals,
- Monitoring of the signals
- this module won't be built, just the lines on the backplane should be foreseen

9.5. SPARE-OUT

The SPARE-OUT module

- Can send out two signals
- Collects two signals per LISSY and combines the signals logically
- Monitoring of the signals
- This module won't be built, just the lines on the backplane should be foreseen

9.2. BIS module

The Beam Interface System module

- Receives one signal from BIS.
- The signal from BIS is a differential RS485 signal.
- The BIS module translates the differential RS485 signal into an standard interlock signal
- The interlock signal is distributed hardwired to the TM modules via the backplane. The signal can be distributed to all TM in parallel.
- The signal is monitored by the MON-FPGA.
- There is a test signal, which is set and monitored by the MON-FPGA.

Does this description mean that BIS card does not send any signal to LHC BIS?

- BIS card in MIC receives signals from LHC

- HVP Master card sends signals to LHC

If this is true, we could use BIS card propagate the non-SB via TM/GSS/Ilk-FPGA/OUT module. This would be a pure hardware solution with no intervention from DCS. But if I understand correctly it does not allow to reduce the HV to a certain value, just shutdown to 0.

Backup

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3.3.4 Beam Interface System (BIS) ITk Interlock System Strategy - AT2-IE-ES-0005

The BIS will send one signal to the ITk interlock system to enable or disable application of high voltage to the Pixel and Strip sensors according to beam conditions. This will be treated within the local interlock crate in the same manner as any other DSS signal (apart from the Emergency Stop), although it shall only affect HV channels. By return each HV crate sends a signal which indicates if High Voltage is present back to the central interlock crate, which combines these signals to generate the injection permit sent back to BIS. A cross check is provided by the DCS software based upon the monitored output of the Pixel and Strip High Voltage power supplies. Taken together, this replicates the functionality of the current Pixel and SCT systems. For Strips there is some flexibility in the actual HV state via the commercial crate controller in software. In the case that a standby HV state is required by strips, then the BIS signal to the interlock would be handled in software.

This is though HVP Master, right? Does it mean that BIS card only receives signals from LHC? Does not send any signal?