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M2Or1A-04: FEM and Modelica Modelling of Current Sharing in Tape Stack Cables; Influence of ICR, ITR, Defect Number, Defect Patterns, and Thermal Boundary Conditions

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Previous simulations have shown that the current sharing level decreases with increasing defect density in the middle layer of a three-layer stack cable. Earlier studies focused on a five-layer YBCO tape structure composed of copper, silver, YBCO, Hastelloy, and copper. However, in real-world applications, the buffer layer exists between YBCO and Hastelloy, which has not been accounted for in previous models.

Simulations were performed using Comsol for three-layer cable models with single-layer defects, and Modelica to address the complexity and computational inefficiency of Comsol for modeling five-layer cables with three-layer defects. Defect patterns such as column and tic-tac-toe configurations were tested. A buffer layer was added to the Comsol simulation, modeled as an insulating layer, to see the impact of the buffer layer on a single-side YBCO tape current sharing level. Also, the simulation will be run to see the performance of a double-sided YBCO tape structure under the same conditions.

The analysis revealed that the current sharing level varied significantly with defect patterns, with the column defect pattern demonstrating the worst performance. The simulation showed the buffer layer decreased the current sharing level. Additionally, the double-sided tape configuration exhibited a higher current sharing level compared to the single-sided tape.

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