

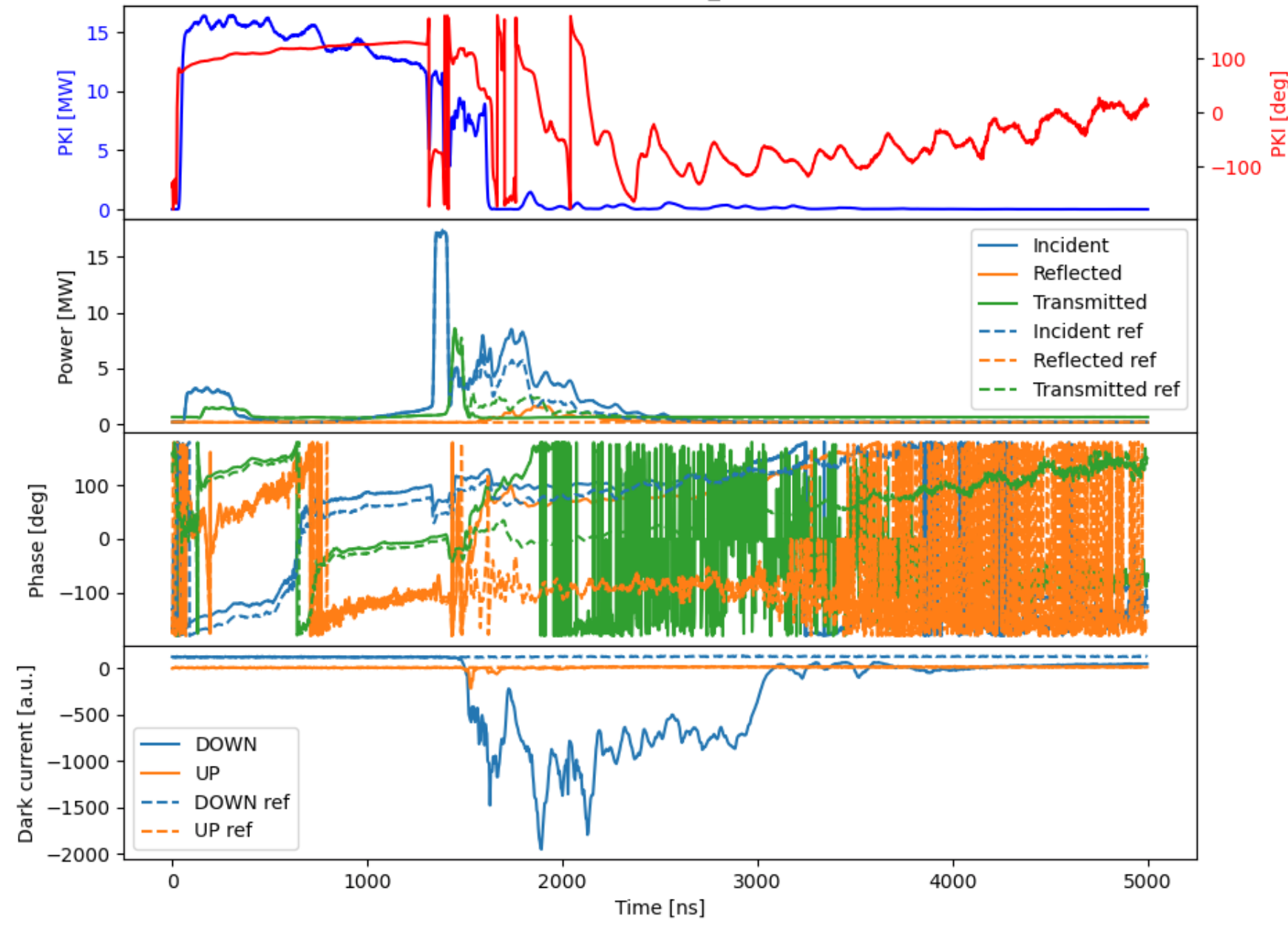
TD31 N3N4

October 2024

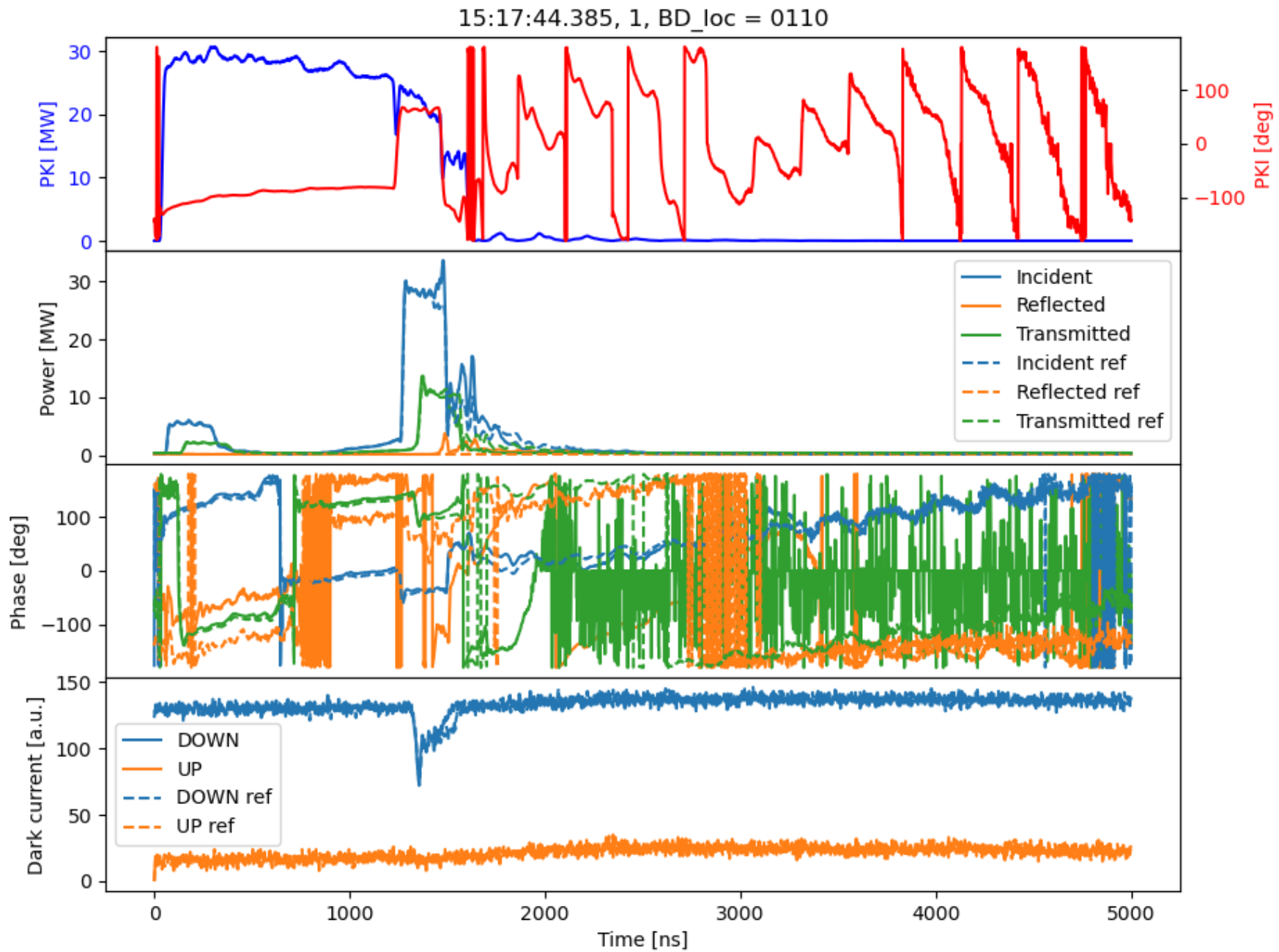
MARTINEZ REVIRIEGO, Pablo; ALONSO ARIAS, Paz

pablo.martinez.reviriego@cern.ch, paz.alonso.arias@cern.ch

Some pulses

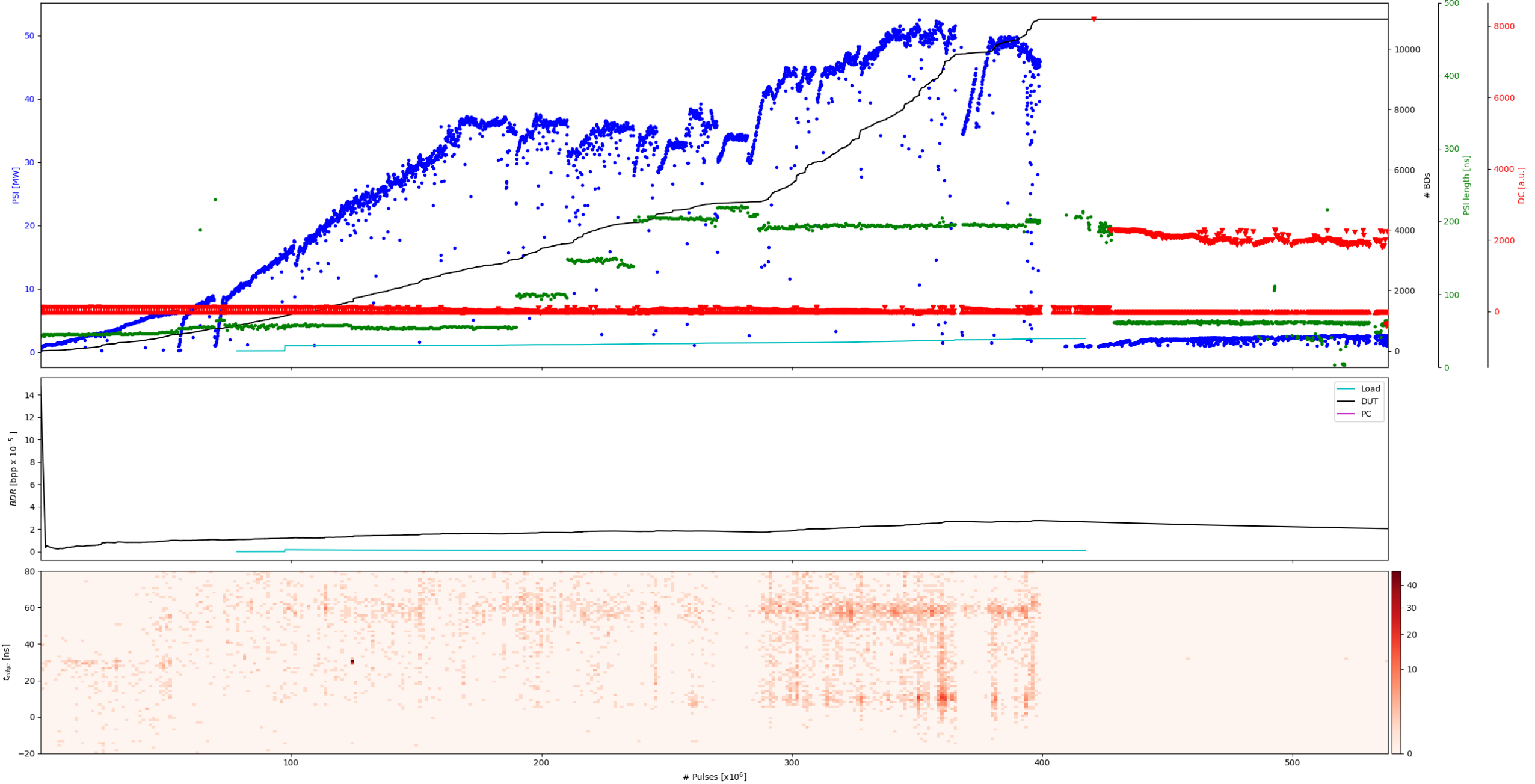


Some pulses

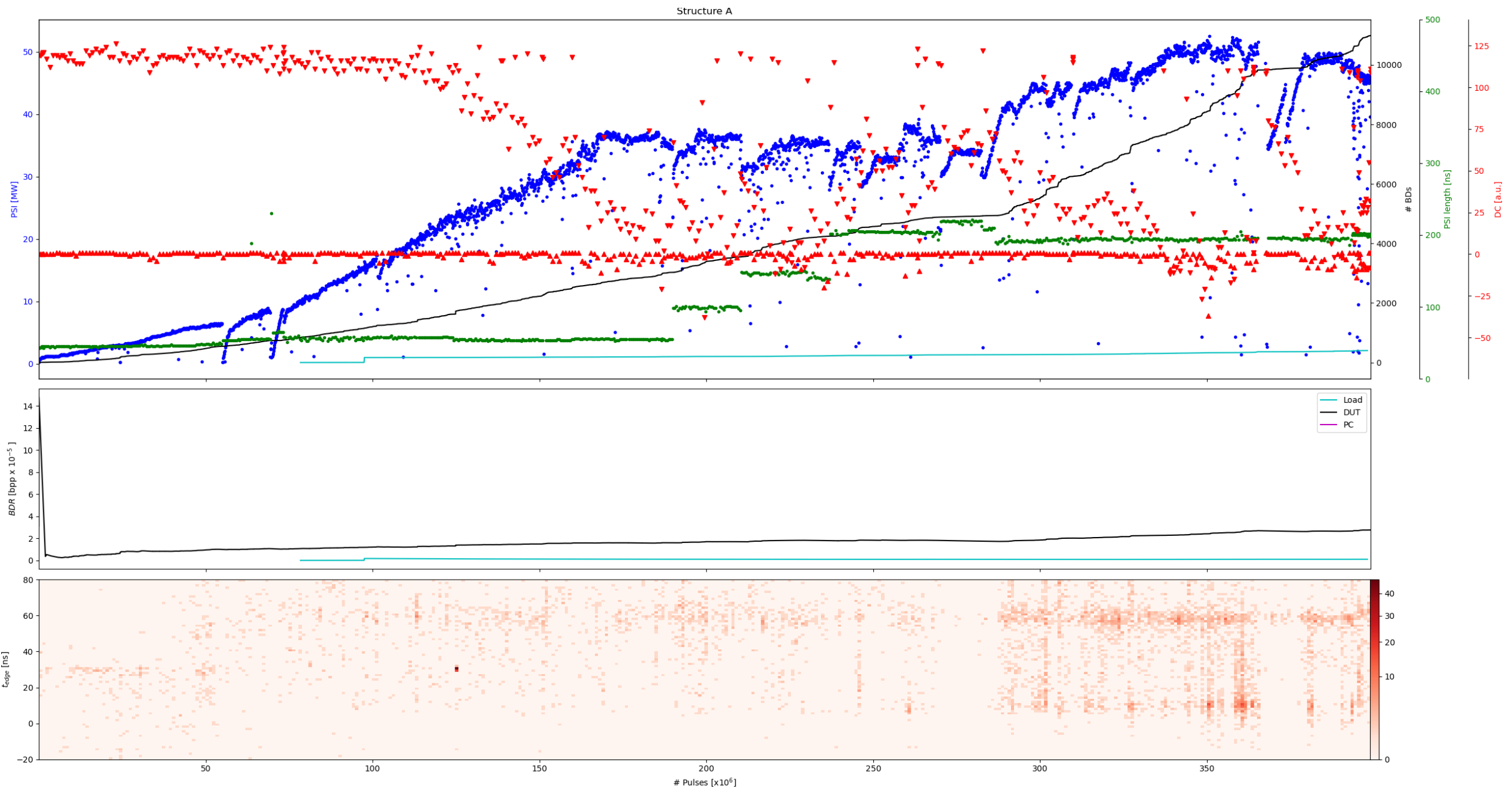


History plot A

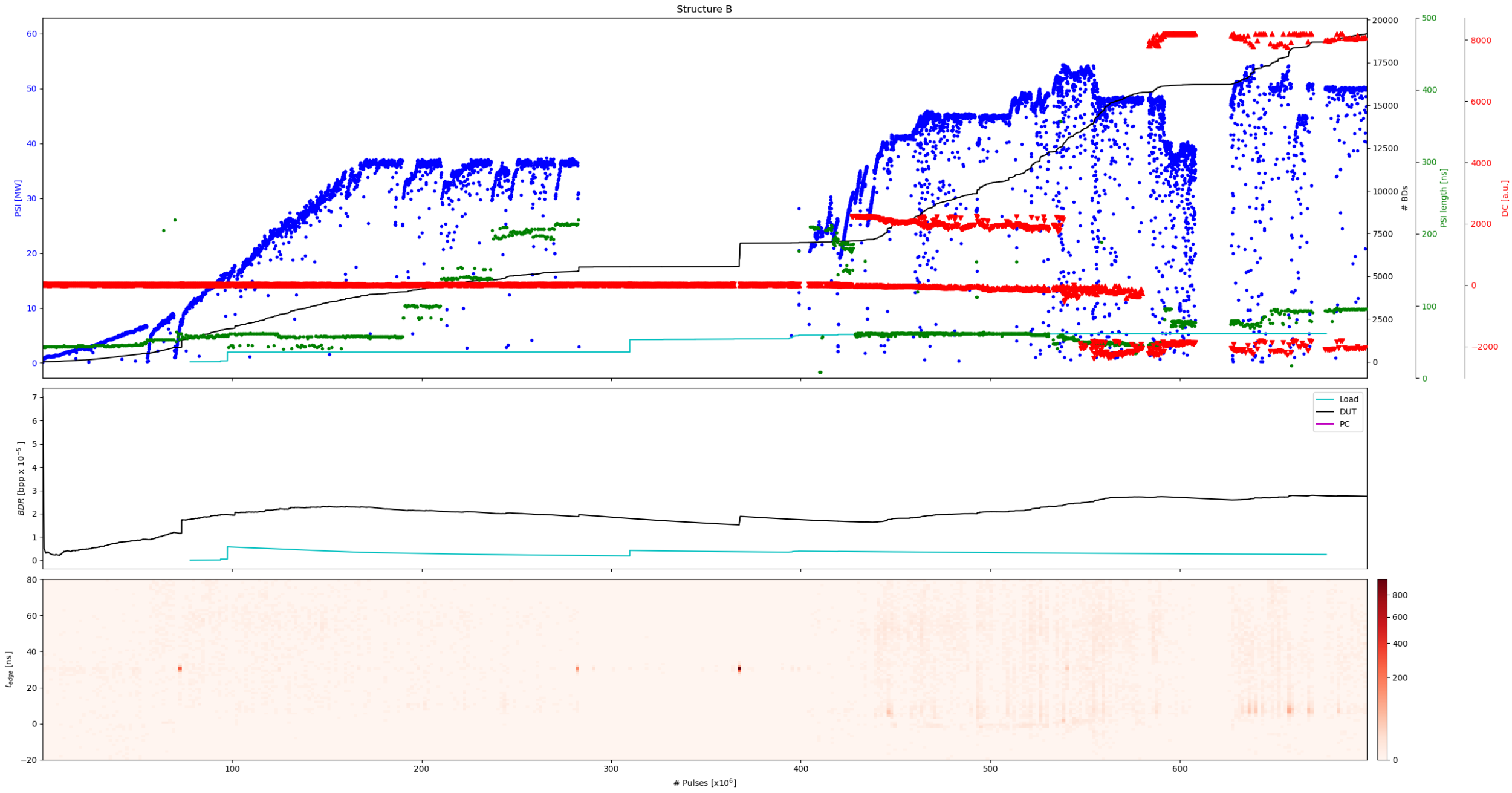
Structure A



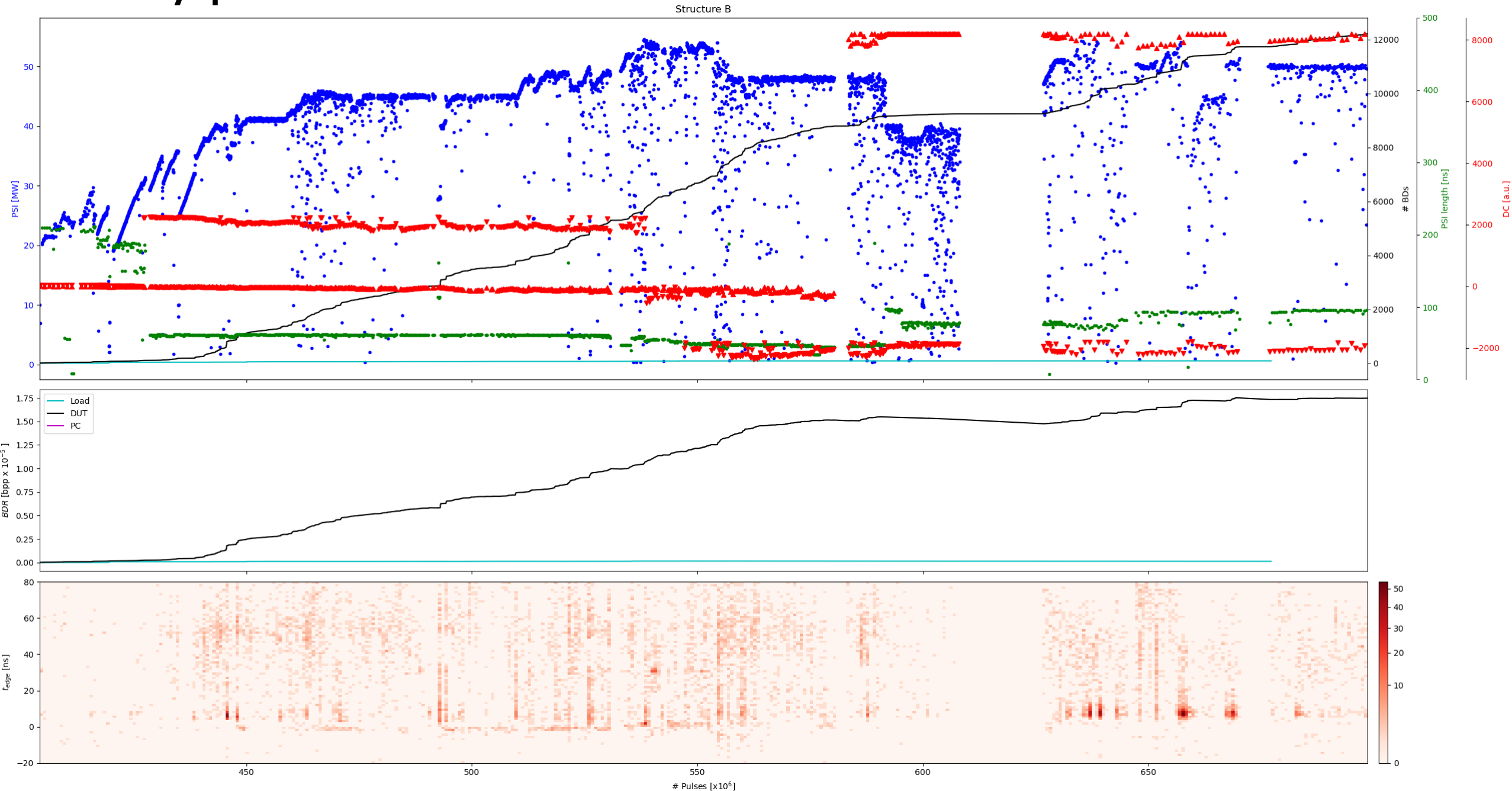
History plot A



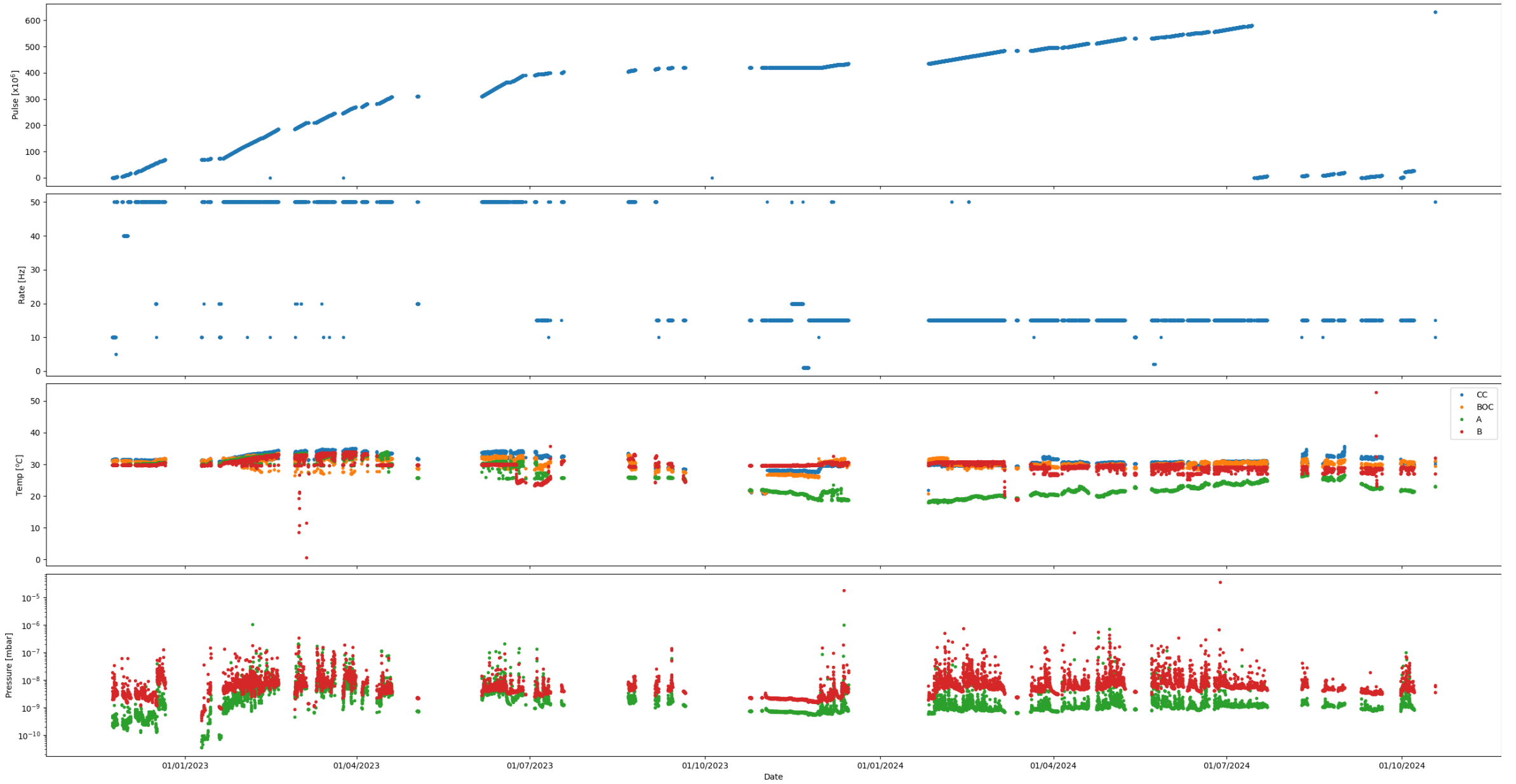
History plot B



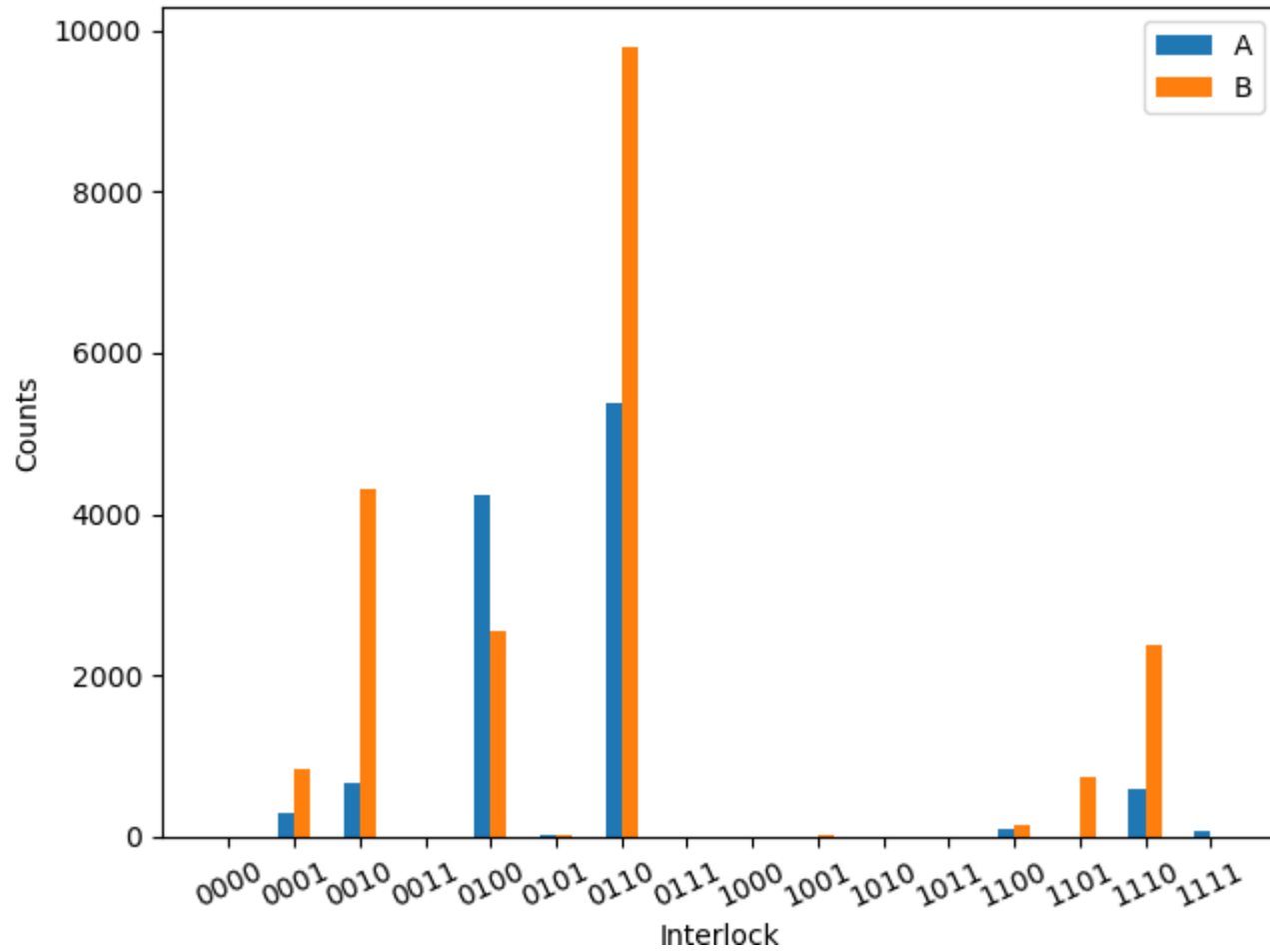
History plot B



History settings

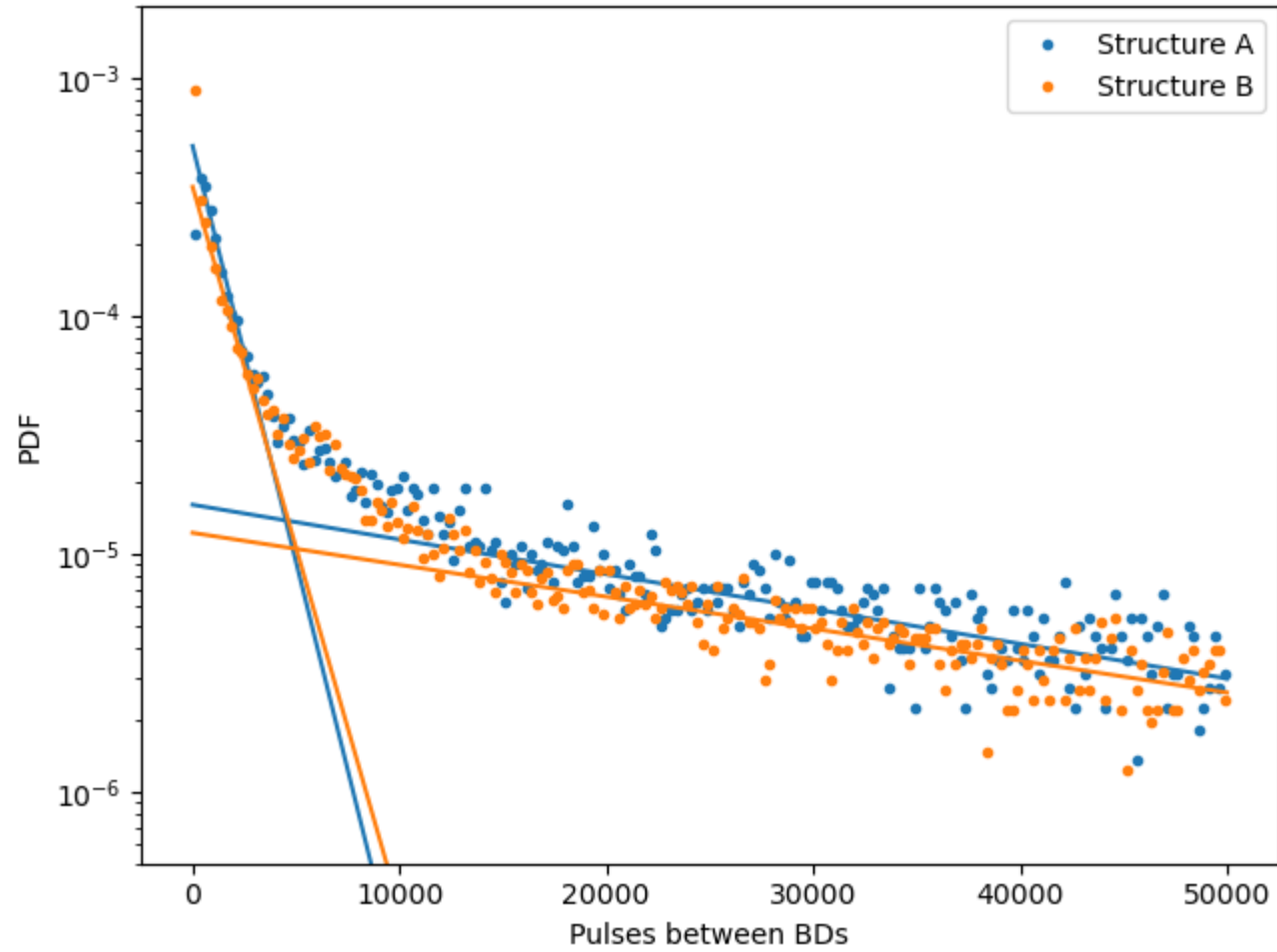


Interlocks



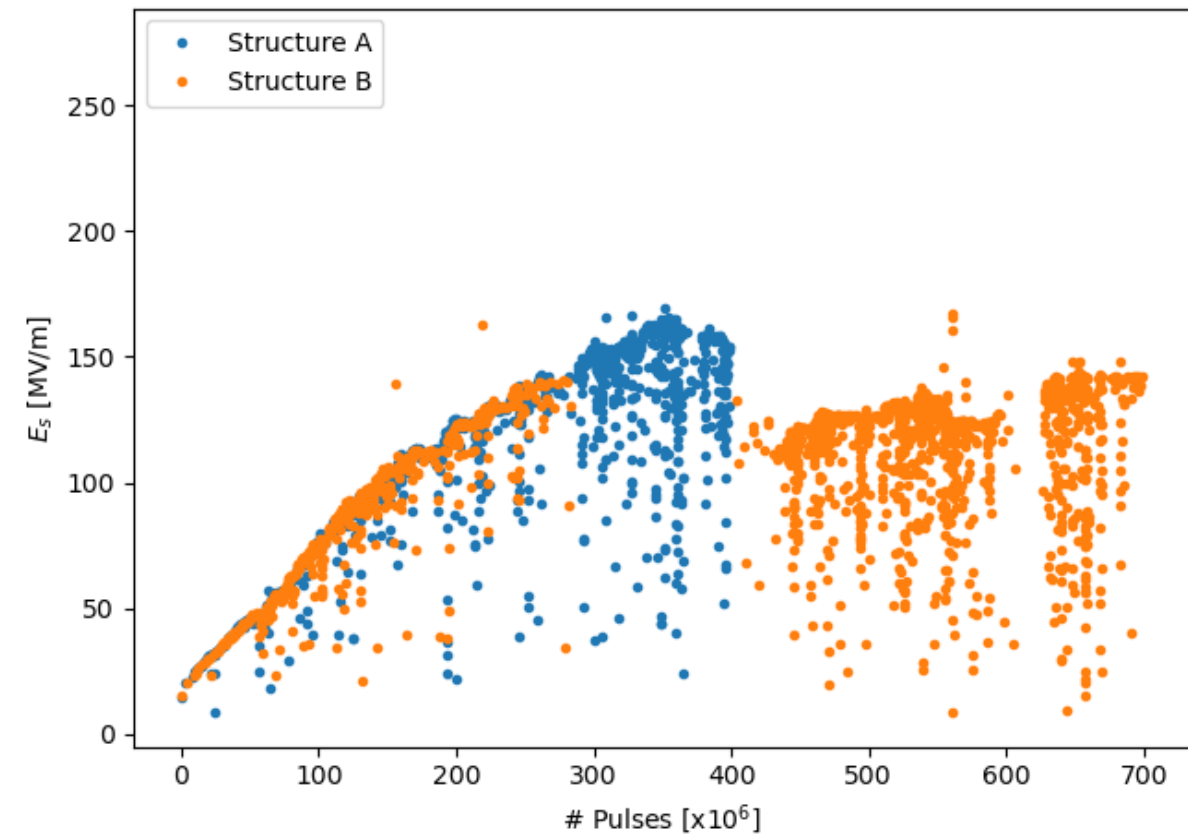
Bit	Interlock
0	PER
1	DC
2	PSR
3	PKR

Pulses between BDs

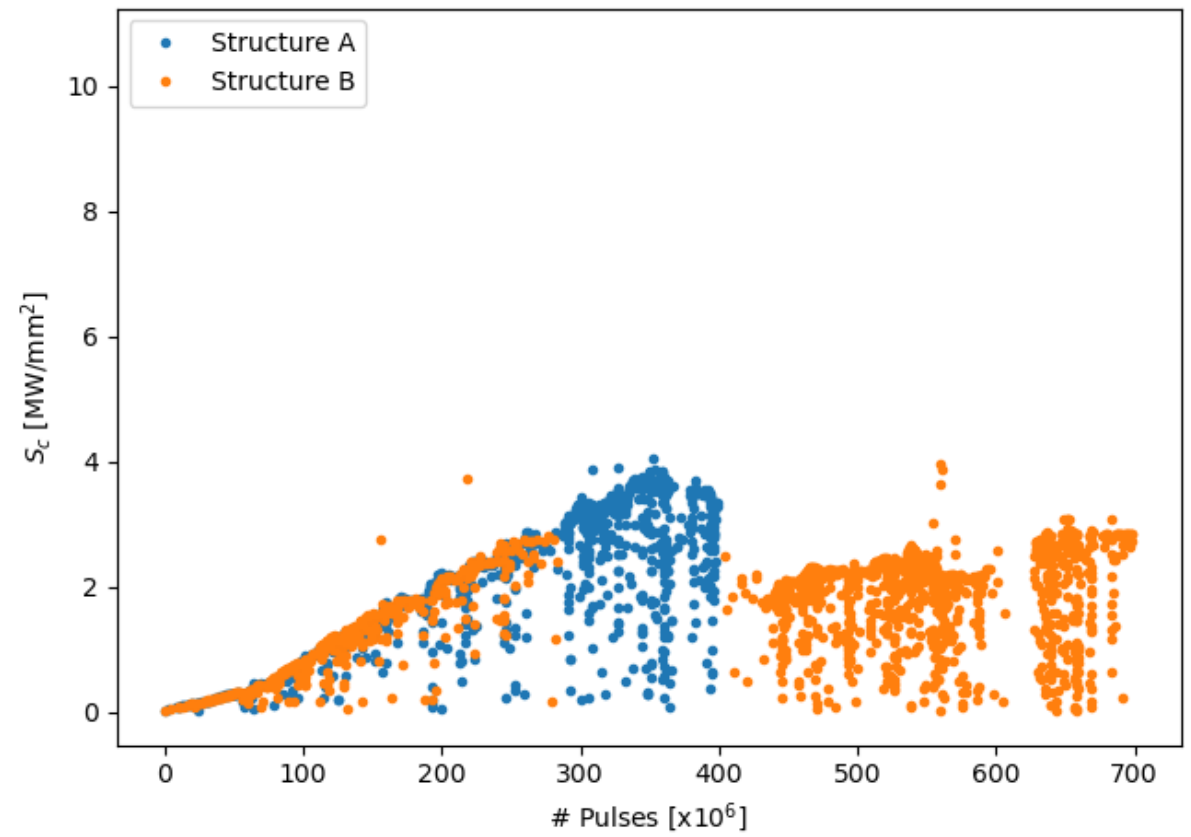


Conditioning history

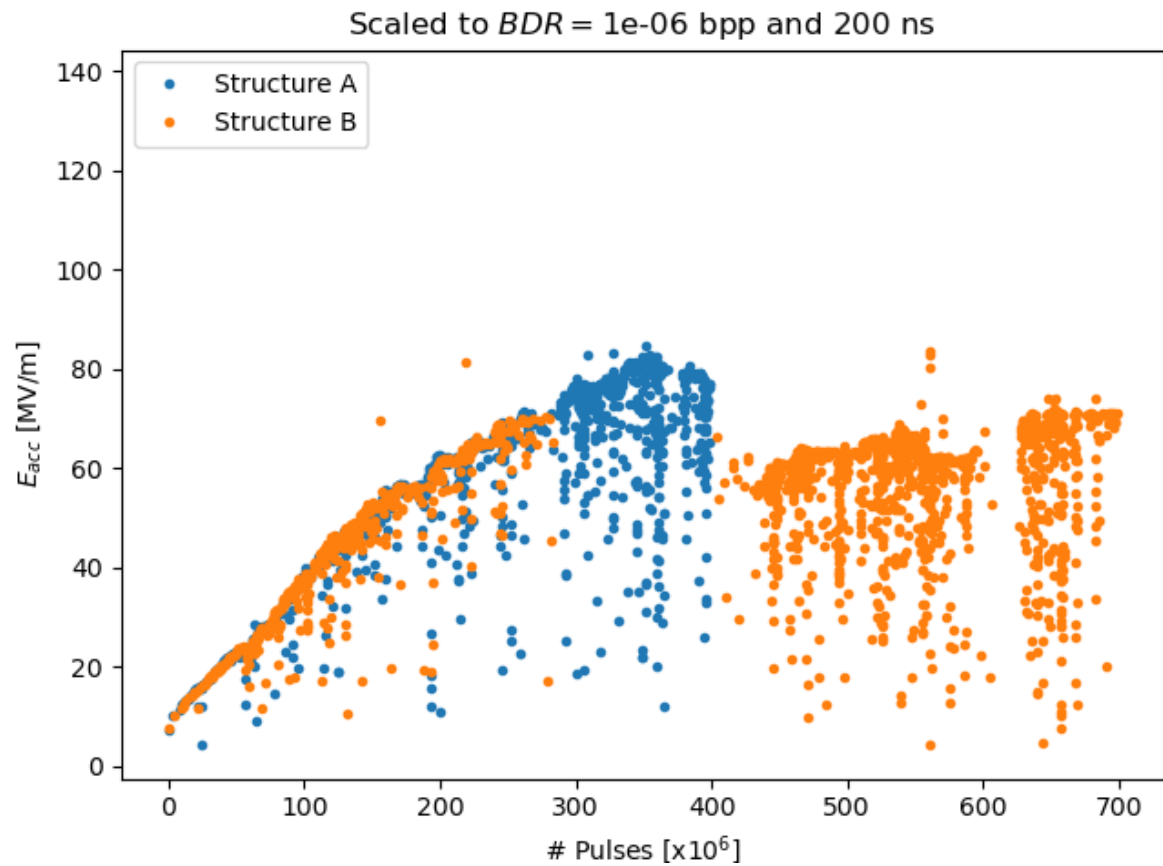
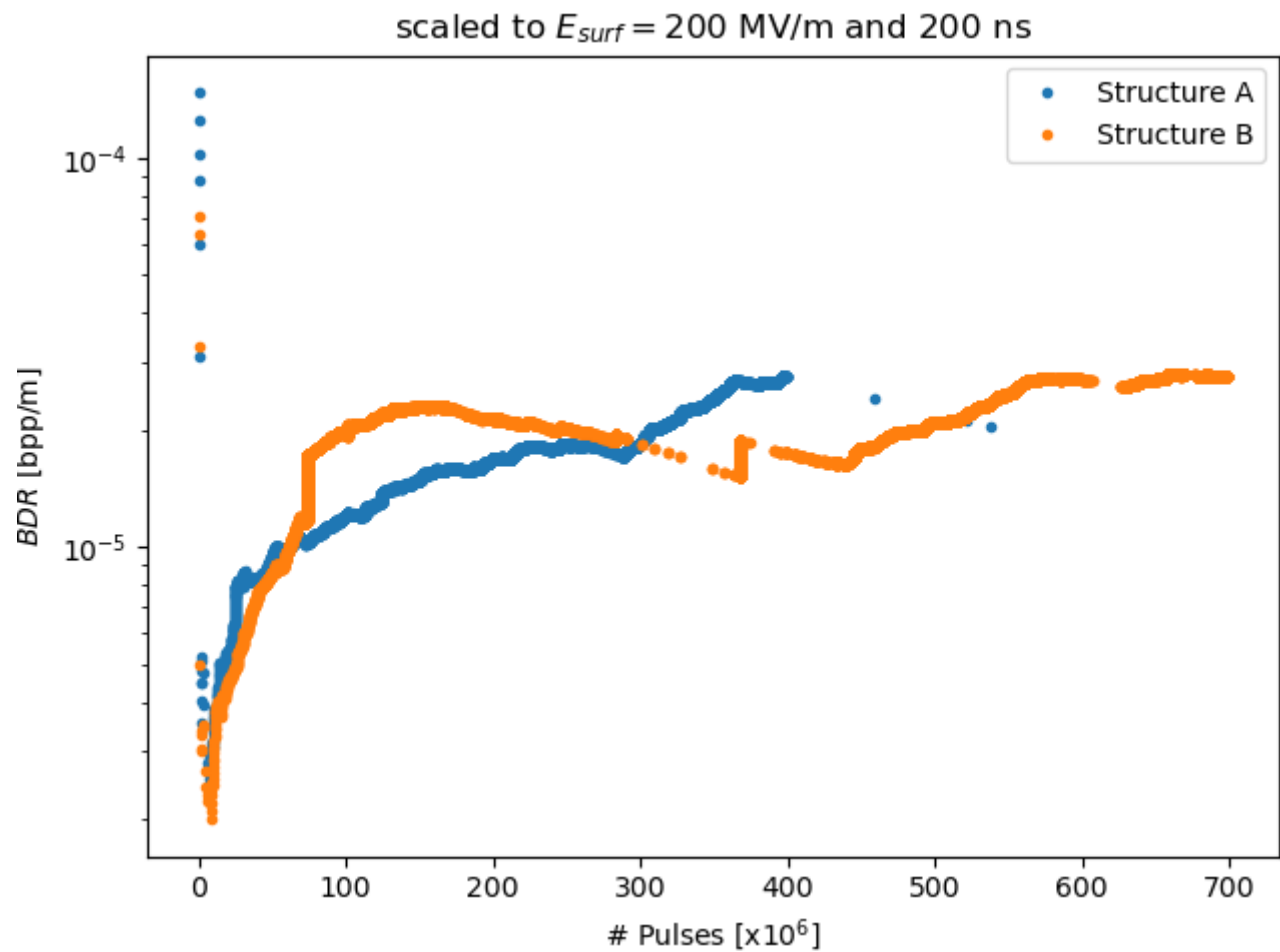
Scaled to $BDR = 1e-06$ bpp and 200 ns



Scaled to $BDR = 1e-06$ bpp and 200 ns



BDR evolution



Final performance

