LHC & SPS NANOSECOND TIME RESOLUTION BLM SYSTEM
CONSOLIDATION STRATEGIES

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Outline

- Current status
- Consolidation objectives
- Discussion about possible strategies
- Summary

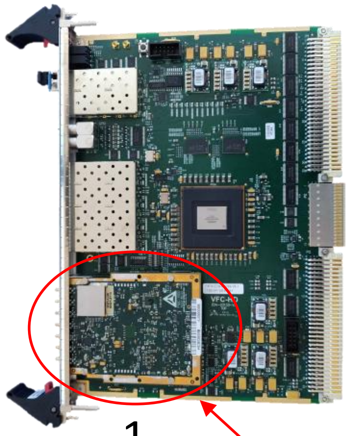
CURRENT STATUS

Current BI diamond BLM installations and platforms

Machine	#detectors	Readout	Photo
LHC	11	FMC-1000 650MSPS 14-bits 2-ch digitiser on VME VFC card	1
TI2 & TI8	2	FMC-1000 650MSPS 14-bits 2-ch digitiser on VME VFC card	1
SPS	4	FMC-1000 650MSPS 14-bits 2-ch digitiser on VME VFC card	1,3
TT20	1	FMC-1000 650MSPS 14-bits 2-ch digitiser on VME VFC card	3
PS	17	Oasis (PCI Digitiser U1071A/DP1400-002, 8-bit 2-ch)	2
PSB	8	Oasis (PCI Digitiser U1071A/DP1400-002, 8-bit 2-ch)	2
F61	1	Picoscope (8-12 bits, 4-ch, 1GHz BW, 5GS/s)	3
In development [1]		IAM FMC 500MSPS 4-ch 14-bits digitiser on VME VFC card	4

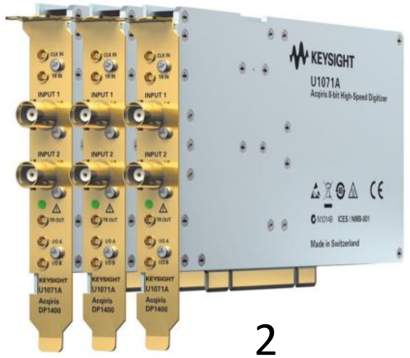
44 detectors, 4 readout types

Notes :
[1] 500MSPS 4-ch proposed replacement for PSB detectors



1

FMC-1000
650 MSPS, 2ch



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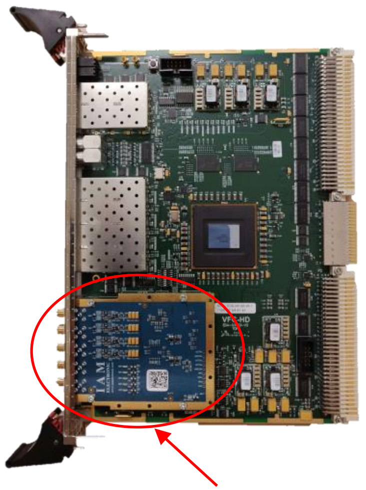
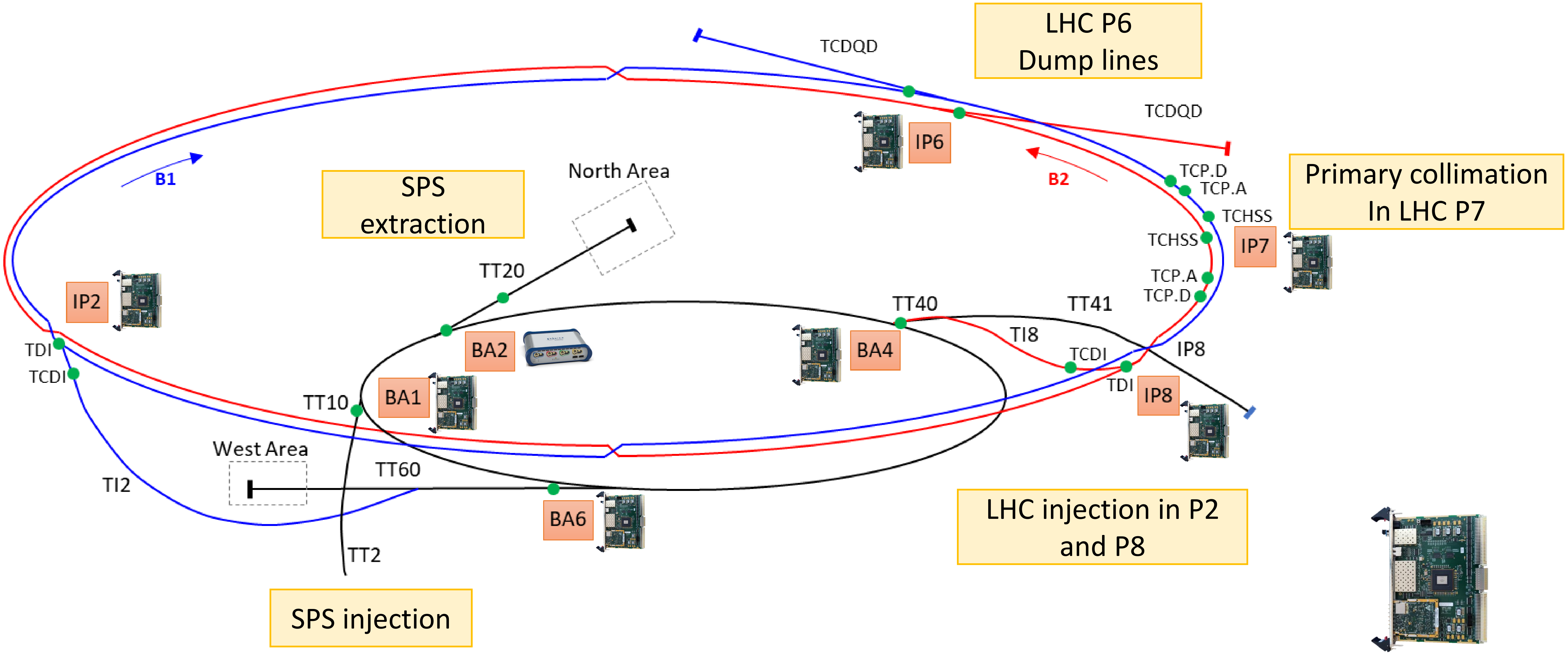
3



4

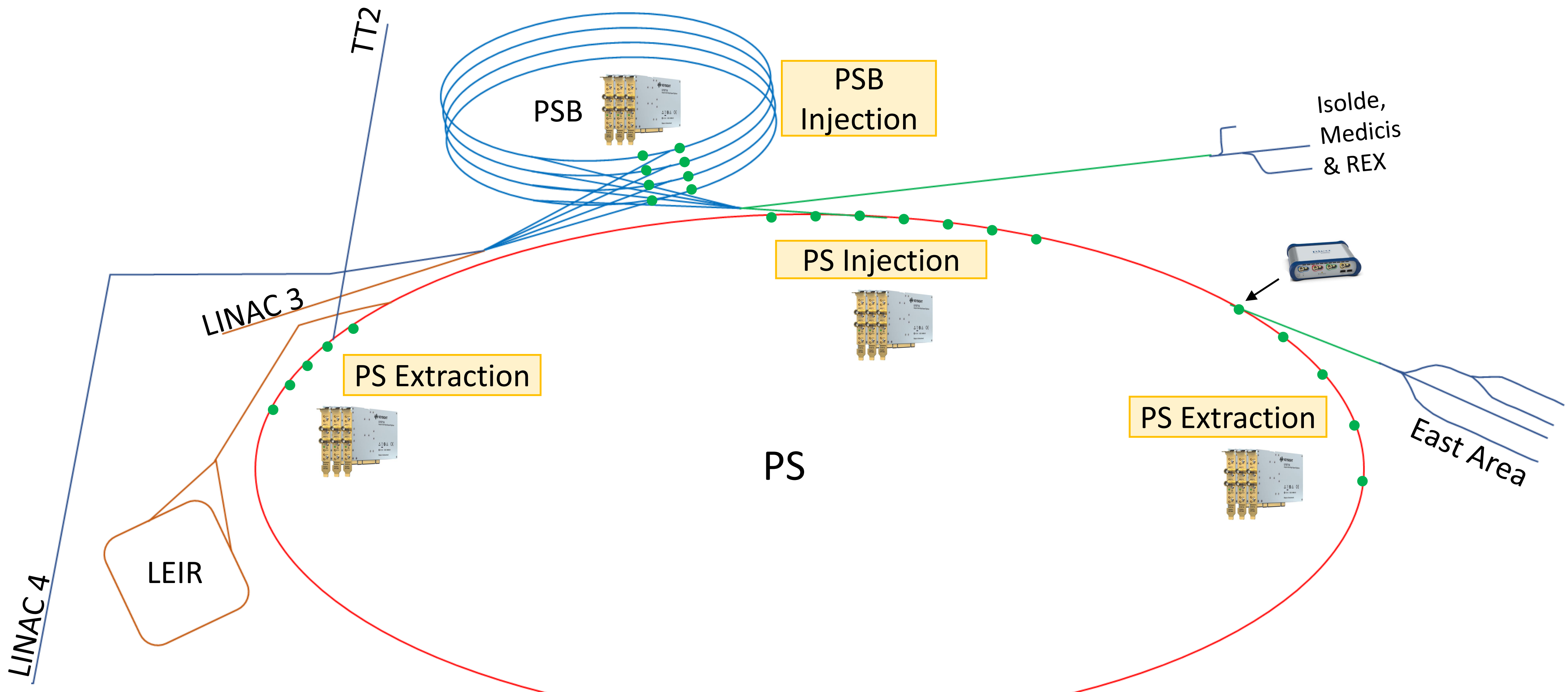
IAM FMC
500 MSPS, 4ch

LHC and SPS systems



FMC-1000 650MSPS 14-bits 2-ch digitiser on VME VFC card

PS and PSB systems



Consolidation objectives

Critical
Priority #1

1) Old power supplies can not be monitored or controlled remotely

⇒ Plan to use of FMC-2ch HV module (production on-going, thus out of the scope of current discussion)

Critical
Priority #1

2) Solve lack of spares for maintenance, new installations or testing (16 operational FMC card, 1 in the TB, 0 spares)[1]

⇒ Need of new/additional digitizers

Critical
Priority #1

3) Refactoring the firmware (hidden bugs and non-synchronicities) + WR

⇒ Resources to rewrite the FW and produce set of TB

Moderate
Priority #2

4) Solve noise and coupled interferences in some locations

⇒ Possible strategies: Consider optical transmission between Front-End and Back-End

Moderate
Priority #2

5) Get some dynamic range adaptability to different beam scenarios

⇒ Possible strategies: remote control of variable gains, additional channels, etc

Moderate
Priority #2

6) Increase VME readout BW

⇒ Possible strategies: Move away of VME for DDR readout, for example using UDP on optical links towards a concentrator

Wish-to-have
Priority #3

7) Remote calibration or testing

⇒ Redesign of the front-end to allow the injection of a calibration signal

[1] Already reported on TB 9/02/2023

POSSIBLE STRATEGIES

Possible strategies

1) Purchase additional FMC-1000 digitisers

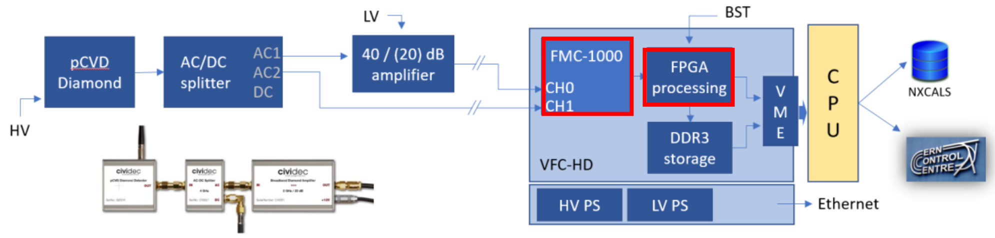
2) Buy/build new FMC digitiser based on same/similar ADC

3) Use Timepix4 BLM

4) Use BCMF23 CMS readouts ASIC (& LpGbt & VTRx+)

5) Replace readout platform based on VFC+FMC by a RFSoC SoM

1.- Purchase additional FMC-1000 digitisers



⇒ Smallest research investment, thus smallest risk

⇒ Benefits: Tackles

- the spare issue (L1)
- (readout BW limitation (L2), FW issues (L1))

⇒ Estimated consolidation cost with this strategy:

HW	MOQ = 10pc & ~12kCHF/pc	~120 kCHF
Persons/year	1 Quest for refactoring the FW: 105kCHF/y * 2y	~210 kCHF

⇒ Time planning: ~1y

⇒ Other criteria:

- Technical perspective:
  - Does not tackle front-end issues: Saturation and dynamic range adaptability, noise immunity, remote calibration or testing
- Strategically:
  - Will continue with VFC platform, so same than other BI-BL systems ⇒ reduces know-how risk at the section/group level, lower R&D and maintenance effort, etc

2.- Build/Buy new FMC digitisers

⇒ Similar strategy to previous. Tackles the same priorities.

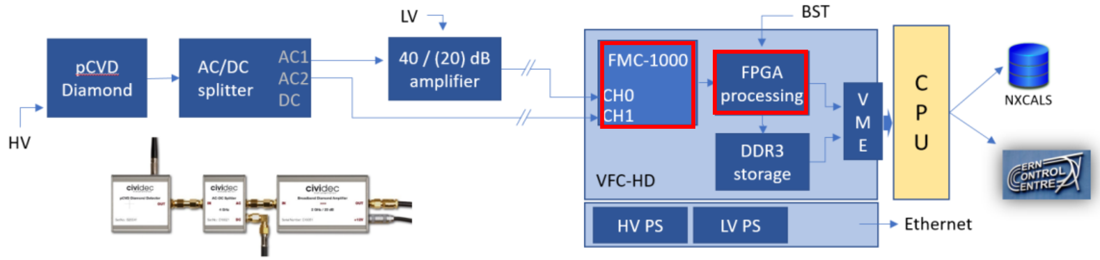
⇒ Alternative plan if we are not allowed to buy additional FMC-1000 cards

⇒ We could make a new design based on same ADC to prevent vendor lock-in and minimize FW re-design, even if still quite some refactoring is necessary.

⇒ Estimated cost with this strategy:

HW	Option A) Build	FMC Digitiser (components + PCB) : ~2 kCHF/pc [1] ▪ if only LHC & SPS + spares: ~20pc ⇒ 40 kCHF ▪ if also PS & PSB + spares : ~50pc [2] ⇒ 100 kCHF + design cost (~10kCHF)	~110 kCHF
	Option B) Buy	COTS FMC Digitiser : ~8-10 kCHF/pc ▪ if only LHC & SPS + spares: 20pc ⇒ 160k – 200k CHF ▪ if we migrate PS & PSB : 50pc ⇒ 400k - 500k CHF	~200k - 500k CHF
Person/year		1 Quest for FW development: 105 kCHF/y * 2y	210 kCHF

⇒ Time: ~2y or more



Notes:
[1] Very rough estimation: 500 CHF/ADC + 800 CHF (PCB) + other components and margin
[2] Assuming 2ch / digitizer card

2.- Build/Buy new FMC digitisers

⇒ Other criteria:

- Technical perspective:
  - It does not tackle issues related to the detector side : noise or interferences on the cables, dynamic range adaptability, remote testing, etc.
  - No change on the data type provided to the users
- Strategically:
  - IMHO, better to build than to buy to prevent the vendor lock-in and foster the know-how within the group instead of losing it in favour of providers
    - High speed complex PCB, but there are schematics and layouts available (EVAL-FMCDAQ3-EBZ), and other groups may eventually be interested.
  - This path will continue using the VFC platform, so same platform than other BI-BL systems (minimizes know-how risk and effort at the section/group level).

3.- Use Timepix4 BLM development

⇒ This strategy tackles:

All!

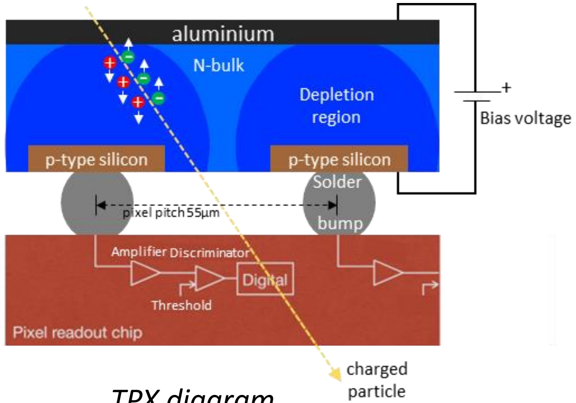
- the spare issue (L1), FW issues (L1), BW readout (L2), noise immunity (L2)
- remote calibration (L2), and potentially dynamic range adaptability (L2)

⇒ Estimated cost with this strategy:

HW	Detectors: ~2k CHF/pc * 20 pc[2] detectors (if only LHC+SPS) ⇒ 40kCHF Back-End + FEC : ~7k CHF/pc * 10pc[3] ⇒ ~70kCHF + Pulling of fibres (not accounted here)	~110 kCHF
Person/year	1 Origin (for dBLM vs Timepix BLM comparison): 85kCHF/y * 1y [1] 1 Quest for FW development: 105kCHF/y * 2y	~300 kCHF

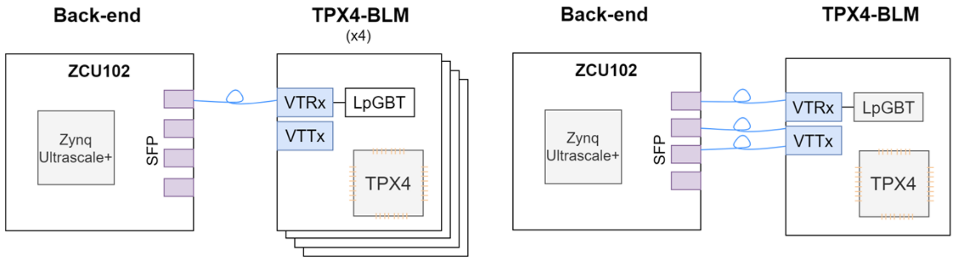
⇒ Time : ~2y or more

[1] Already requested at beginning of 2024
[2] 6@LHC-P7+2@LHC-P2+2@LHC-P8+3LHC-P6+2@SPS ~ 15pc +spares
[3] 3@SPS+3@LHC(P2,P6,P8)+2@LHC(P7) ~ 7 pc+3 spares



TPX diagram

TPX3-BLM prototype



Design architectures for TPX4-BLM: a) Standard version (up to ~58 Mevents/s) b) Fast version (up to ~155 MEvents/s)

3.- Use Timepix4 BLM development (cont.)

⇒ Long term agreement between XEI and BL to develop a fast-deploying fast BLM system. Specs EDMS 2802519

⇒ FW will need to be re-written to provide typical fast BLM data (bunch loss integrals, turn loss integrals, time of arrival histogram, capture) from ToT and ToA.

⇒ Some uncertainties at the detector level need to be studied: Can we cover the required dynamic range at the different dBLM locations and scenarios ? ⇒ Test at Charm foreseen in 2024

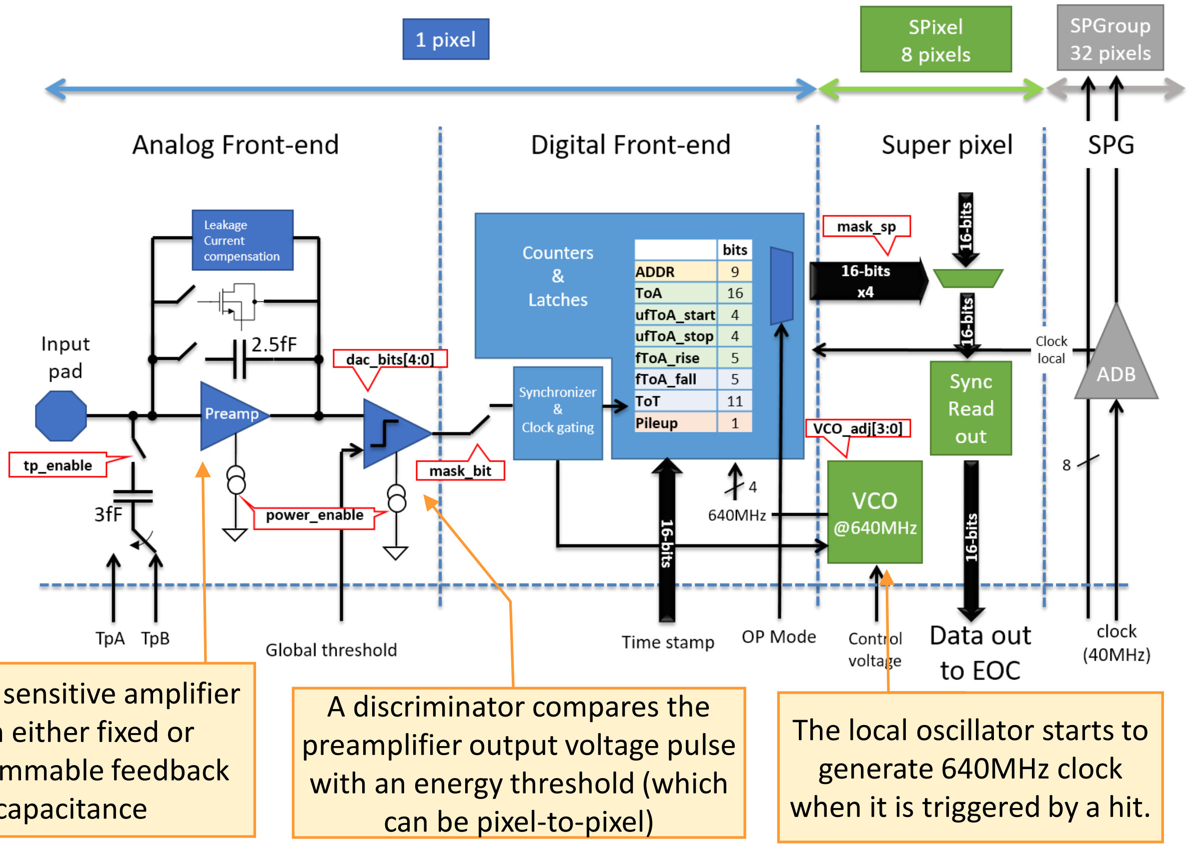
⇒ Seems a good solution for slow extraction locations

⇒ Other criteria

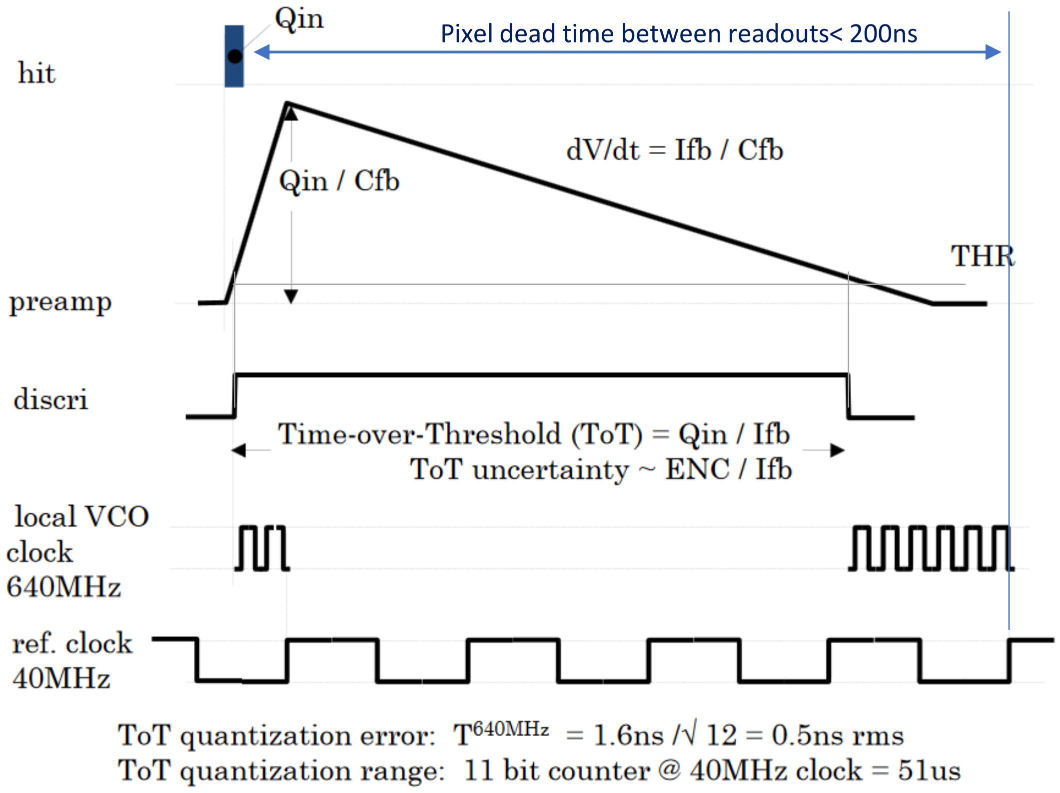
- Strategically:
  - Complete change of paradigm w.r.t. what is being done now within BI-BL ⇒ different sensor, different platform (SoC), different measurement principle (discriminator after analogue integration in quantified space instead of direct digitalization and digital integration).
  - Higher level of testing and adjustments features at the cost of a relatively higher complexity.
    - Pixel equalization, space quantification will be used only for the dynamic range adaptability, calibration w.r.t. number of pixels enabled

Timepix4 BLM additional information

Size : 24.7 x 30.0 mm^2 (6.94 cm^2 sensitive area > 1 cm^2 pCVD diamond) ⇒ Larger signal expected
Number of pixels : 448 x 512 pixels ⇒ Which can be individually enabled and calibrated
When a pixel has a hit above a pre-defined and programmable threshold, it sends Time of Arrival (ToA with time resolutions <200ps), Time over Threshold (ToT with a resolution of 1.56ns) + hit coordinates



Timepix4 pixel schematic

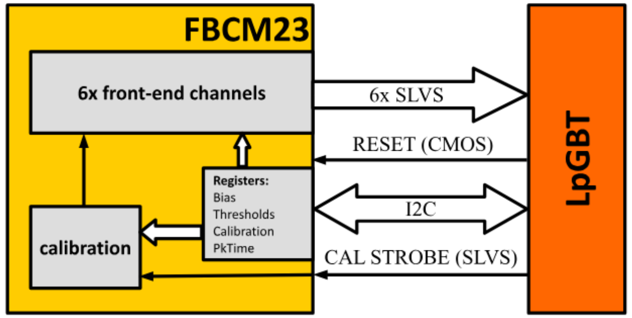


ToT measurement principle

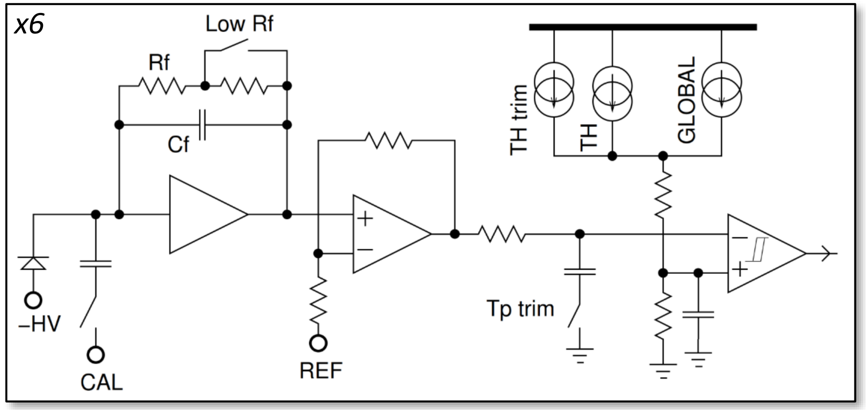
3.- Use BCMF23 CMS readouts ASICs

⇒ New ASIC developed for the phase-2 upgrade of the CMS Fast Beam Condition Monitoring (BRIL project).

- During Run2, previous ASIC version, BCM1F was used as a luminometer with sub-bunch crossing precision. Connected detectors were a mixture of sCVD, pCVD and Silicon sensors.
- Upgraded during LS2. Now use only AC coupled cooled silicon diodes
- Future upgrade for HL-LHC plans to use the new version: BCMF23 ASIC.
- It consists of an integrator pre-amplifier and a discriminator. The ASIC produces an analogue pulse, where the rising edge defines de ToA, and the duration defines the ToT (∝ Q ∝ Ex/dx).
- This signal is routed towards an LpGBT which continuously samples it (32 Samples/bunch, 0.78ns time resolution) and transmits it to the back-end over an optical link via VTRx+.
- ASIC was designed to withstand 2 MGy and $2x10^{15}$ 1Mev eq. n/cm^2, ENC <900 e$^-$.
- Pre-amplifier characterised by fast rise time, narrow pulses, and fast return to baseline after multiple MIPs.
- Adjustable feedback resistor (25 or 50 kOhm), 69 dB open loop gain
- Prototype received by Q3-2023, and it is being qualified. Report will be soon available.



FBCM23 block diagram



FBCM23 schematic

3.- Use BCMF23 CMS readouts ASICs (cont.)

⇒ This strategy would tackle:

- the spare issue (L1), FW issues (L1), BW readout (L2), noise immunity (L2)
- remote calibration (L2), dynamic range adaptability (L2)

⇒ Cost:

HW	Unknown for the moment. Mask + 100 chips ~33 kCHF	50 kCHF - 100 kCHF ?
Person/year	1 Quest for FW development: 105kCHF/y * 2y 1 Quest/staff for HW development	>> 210 kCHF

⇒ Time: 2y or more

⇒ Strategically:

- The front-end card will have many similarities to the current BLM ASIC card used to readout ICs (ASIC + LpGBT + VTRx). The backend could also stay on the VFC platform. No FMC digitiser needed.
- It will require new PCB development, and characterisation of ASIC for its use as BLM
- Similar incertitude than for TPX4-BLM: dynamic range and saturation at dBLM locations ?
- Complex integration into the PCB since the ASIC requires bonding
- It will require development of FW to get from the ToT & ToA data, the bunch loss integrals, turn loss integrals, ToA histogram and capture.

4.- Replace readout platform to RFSoC

⇒ This strategy would tackle:

- the spare issue (L1), FW issues (L1), readout BW (L2)
- Might deal with dynamic range adaptability if RFSoC version selected has attenuators.

⇒ Cost:

HW	Estimated to be comparable to FMC-1000 + Design and production of Anal. front-end card ~10pc (for LHC & SPS)	< 150 kCHF ?
Persons/year	1 Quest for FW develoment: 105 kCHF/y * 2y 1 Quest/staff for HW development	>210 kCHF

Region	# Detectors	# channels
LHC P7	6	12
LHC P2	2	3
LHC P8	2	3
LHC P6	3	3

Region	# Detectors	# channels
SPS BA2	2	2
SPS BA4	1	2
SPS BA6	1	2
SPS BA1	1	2

Due to the detector distribution:

- Current system (FMC-1000): 16 digitiser cards and no growth capacity
- RFSoC based system : (Assuming 8x ADC/SoM) : 9 digitiser cards and growth capacity

4.- Replace readout platform to RFSoC (cont.)

⇒ Profit of developments from other instruments (HL-LHC BPMs, Head-Tail, etc.) and reuse as much as possible

- Same SoM (with RFSoC) solution than the HL-LHC BPMs
  - Required dBLM BW[1] << HL-LHC BPM BW ⇒ But this improves the Noise Spectral Density
  - IMHO, interesting solution only if a SoM BI standard platform is developed (similar to what was done with VFC-HD)

⇒ It could potentially become a common BI platform if some modularity is added, for example the capability to adapt different detector signals to the RFSoC module by means of some daughter board

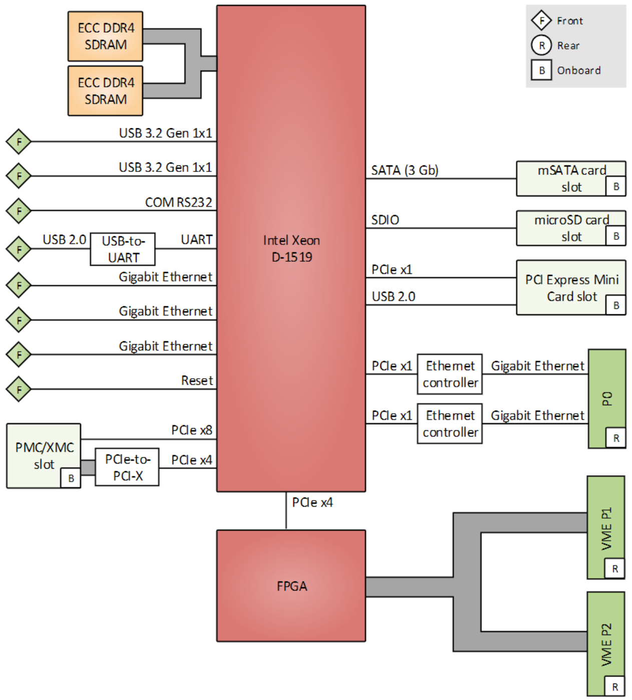
⇒ The SoC potentially opens the door to more powerful UFO or beam loss anomalies search algorithms, using SW based or ML algorithms

[1] Signal rise time ~4ns. 2-3 samples at 650MSp/s

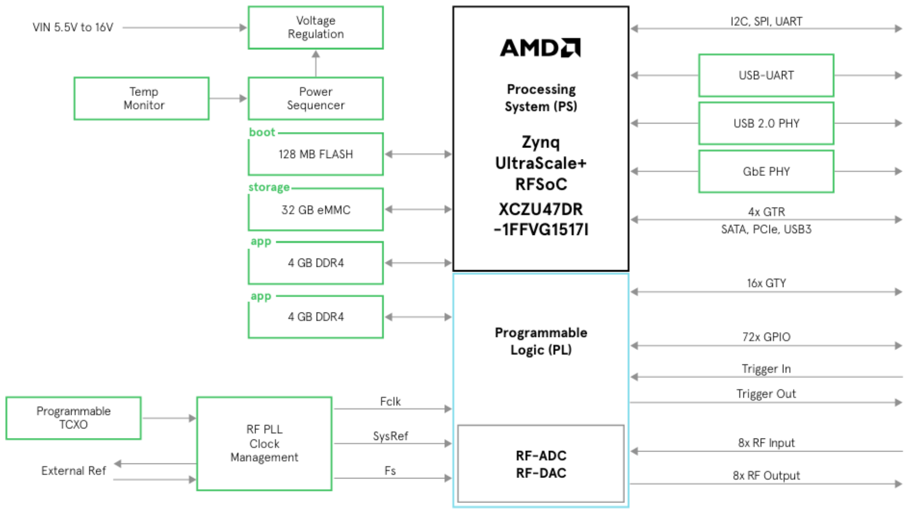
4.-RFSoC path: Processor comparison (Men A25 vs Arm 56)

VMEbus CPU board based on Intel's Xeon D-1519 server CPU (4 cores, 1.5GHz)
Caches: cache (32K data + 32K instruction), L2 (256 K), LLC (1.5MB)
VMEbus interface is implemented as an open-source, FPGA-based solution (MBLT, theor. max ~40MB/s)
2x USB 3.2 ports, 1x Gb Ethernet ports and 2x RS232 COMs at the Front panel
8 GB DDR4 SDRAM (2.1GHz) with ECC and Flash
Slots for mSATA and microSD cards (?)
1x XMC slot or 1x PMC slot (typicall CTRP module as GMT timing Rx)
MTBF ~70000 h

Figure 2. Functional diagram

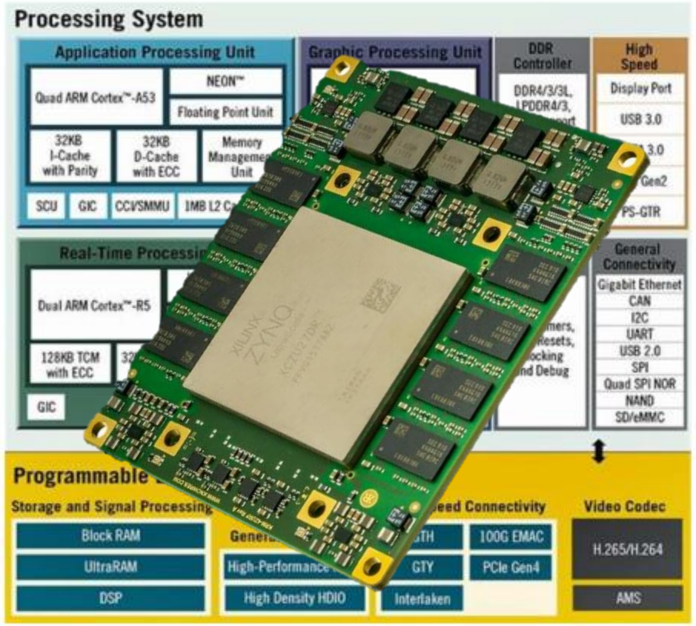


Block diagram



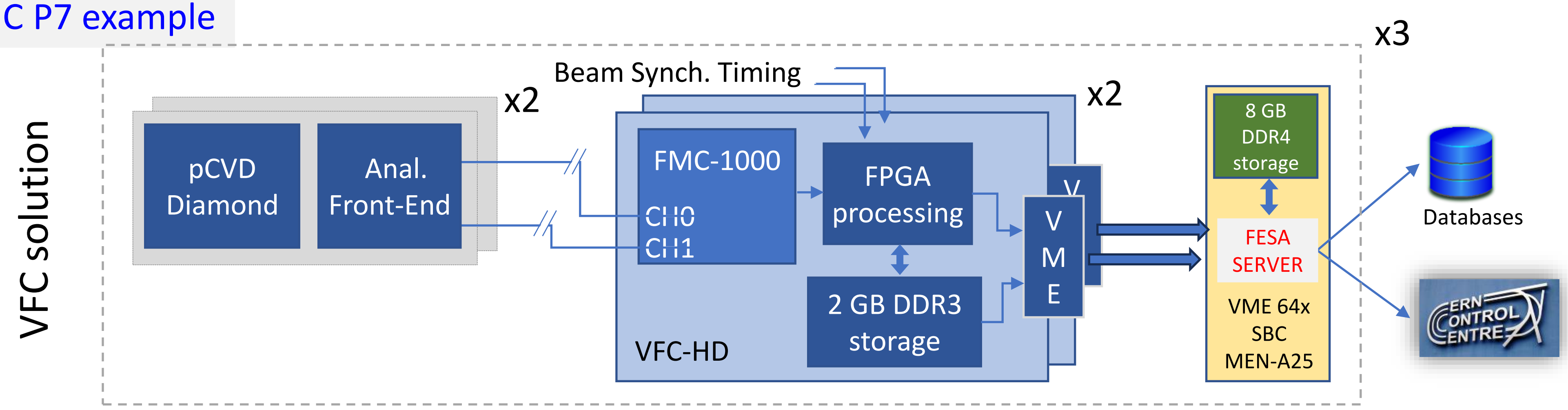
KRM4ZU47DR SoM just as an example:
UltraScale+ Gen3 ZU47DR RFSoC
- Arm Cortex-A53 (4 cores, 1.33GHz)
- Arm Cortex-R5F (2 cores, 533MHz)
- Arm Mali-400 MP GPU (667MHz)

2-8 GB DDR4 (as PS RAM), 2-8GB DDR4 (as PL RAM) working @ 2.4GT/s
64GB eMMC & 1GB QSPI
16+4 GTY/GTR transceivers @32Gb/s and 6.6Gbps
90 x 75 mm
Carrier board needed:
Connectors, Timing Rx, powering

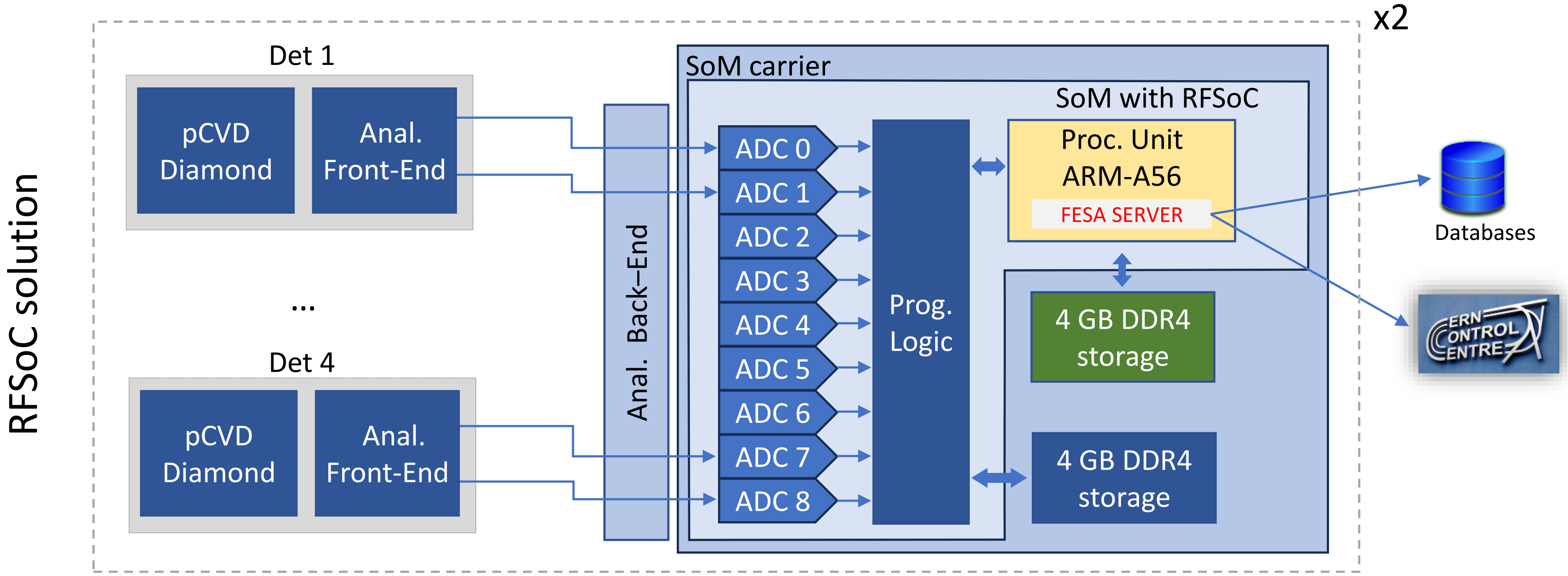


4.-RFSoC path : FECs on SoC vs FECs on dedicated SBC

LHC P7 example



- 4 channels processed in a more performant Proc. Unit + more (PS) mem.
- 1 GB/channel for capture acq. (@PL)



- 8 channels processed in a smaller Proc. Unit with less (PS) memory
- 0.5 GB/channel for capture acq. ⇒ Shorter acq. window
- FPGA will require ~x4 more memory blocks

4.-RFSoC path additional data: ADC comparison

	FMC-1000
# ADCs	2
Fs_{max}	1.25 GS/s
# bits/ADC	14
ENOB	~10
Coupling	DC
BW	1 GHz
Input range	±0.42V
SNR	65 dB
SFDR	79 dB
THD	-78 dBc
NSD	-152 dBFS/Hz
Crosstalk	-95 dB
# DACs	2 (@1.23GS/s)
# bits/DAC	16
From factor	FMC, VITA 57.1

Notes:
- Use AD9680-BCPZ-1250 as ADC + LMK4828 as Clk jitter cleaner
- Analog Devices provides schematic & layout of Eval. Board : EVAL-FMCDAQ3-EBZ

	RFSoC ZU47DR Gen 3
# ADCs	8
Fs_{max}	2.5GS/s / 5.0 GS/s ☺
# bits/ADC	14
ENOB	
Coupling	
BW	6 GHz
Input range ☺	1 Vpp | 4.8 Vpp (with attenuation)
Digital Atten.	0..27dB (1 dB step) ☺
SNR	
SFDR	84 dB ☺
THD	
NSD	-150 dBFS/Hz
Crosstalk	-75 dB
# DACs	8 (@ 6.5GS/s)
# bits/DAC	14

SUMMARY


Deep learning
Artificial Inteligence
ML
Big data
machine learning
Data mining
Processing
Algorithms
Underfitting
Regression
Forest
IA
mc
Reinforcement learning
Convolutional Neural Networks
Recurrent Neural Networks
Hyperparameter
Analysis
Dimensionality Reduction
Backpropagation
Training data set
Automation
Supervised learning
Large language model
Pattern recognition
neural networks

Summary

	Buy FMC-1000	other FMC digitisers	TimePix4 BLM	BCMF23 ASIC	RFSoC
Spares availab.	✔	✔	✔	✔	✔
Noise & interferences	✗	✗	✔ Optical tx	✔ Optical tx	✗
Adaptative DR	✗ Req. additional HW	✗ Req. additional HW	To be studied	To be studied	✔ Some models contain var. atten.
DDR readout BW limitation	With FW change + concentrator	With FW change + concentrator	✔ High speed tcvrs between front-end and back end	✔ High speed tcvrs between front-end and back end	✔ if FESA in SoC fast and direct reading from the DDR.
HW effort	None	None / Medium	✔ Work already in progress	High	High
FW effort	Refactoring	New design	New design (Synergies with BI-XEI)	New design (Synergies with BI-BL)	New design (Synergies with BI-BP)
SW effort	Low	Medium	Medium	Relatively high	Relatively high
Complexity / Risk	Low	Medium	Medium	Relatively high	Relatively high
Cost HW | p·y	120k | 210k	50k..200k | 210k	110k | 300k	<100k | >210 kCHF	150k | 210k
Development Time	1y	2y	2y	2y	2y
Other		Generic solution, eventually also valid for oBLM, or other devices	✔ Work already in progress		Generic solution, eventually also valid for oBLM, or other devices

Conclusions

- It has been presented the number, locations and types of dBLM systems in the different machines
- It has been listed the aspects where consolidation is needed
- It has been listed 5 different possible strategies that could improve some of these consolidation points
- It has been described the main characteristics, pros, cons and estimated cost of the different strategies
- Next steps?
  - Testing the TPX4-BLM could provide useful insights about its suitability as fast BLM system.
  - BI's RFSoC could become a standard platform for more systems if some modularity is added. For example, add the ability to attach analogue daughterboards needed for other systems.

Thank you for your attention

Time for questions and comments

Decision making steps