



Contribution ID: 168

Type: poster

Optimisation of Multi-Qubit Chip Topology

The poster titled “Optimisation of Multi-Qubit Chip Topology” focuses on designing scalable and efficient architectures for multi-qubit quantum processors. The research highlights superconducting qubits, known for their controllability and role as fundamental units of quantum information in quantum computing. This study emphasises the importance of parameters such as entanglement, quantum error correction, and scalability in multi-qubit chip design. The team proposes a 2D architecture with three qubits arranged in an equilateral triangle and a 3D architecture with four qubits in a tetrahedral structure. These configurations can serve as modular units for larger quantum systems. Future directions include optimising resonator lengths, energy participation ratios, and scaling up the architecture for larger multi-qubit arrays and systems. In high-energy physics, qubit systems are used for quantum simulations complex particle interactions. Thus, an easily scalable multi-qubit chip will definitely be the way forward to complex calculations and simulations of particle collisions at high energies, thus paving the way for its usage in high energy physics in the near future for newer and more exciting discoveries.

Email Address of submitter

rajatava.m@gmail.com

Short summary

Authors: Prof. DEV, B N; Mr CHATTERJEE, Priyangshu (IIT Kharagpur); MUKHOPADHYAY, Rajatava (TCG Crest); Dr MANDAL, Snehal (TCG Crest)

Presenters: Mr CHATTERJEE, Priyangshu (IIT Kharagpur); MUKHOPADHYAY, Rajatava (TCG Crest)

Session Classification: Networking cocktail and Poster Session